PRELIMINARY

Integrated Circuit Systems, Inc.

ICS848004I

FEMTOCLOCKS™ CRYSTAL-TO-SSTL_2 FREQUENCY SYNTHESIZER

GENERAL DESCRIPTION

The ICS848004I is a 4 output SSTL_2 Synthesizer optimized to generate Fibre Channel reference clock frequencies and is a member of the HiPerClocks™ family of high performance clock solutions from ICS. Using a 26.5625MHz 18pF parallel resonant crystal, the following frequencies can be generated based on the 2 frequency select pins (F_SEL[1:0]): 212.5MHz, 187.5MHz, 159.375MHz, 156.25MHz, 106.25MHz and 53.125MHz. The ICS848004I uses ICS' 3rd generation low phase noise VCO technology and can achieve 1ps or lower typical rms phase jitter, easily meeting Fibre Channel jitter requirements. The ICS848004I is packaged in a small 24-pin TSSOP package.

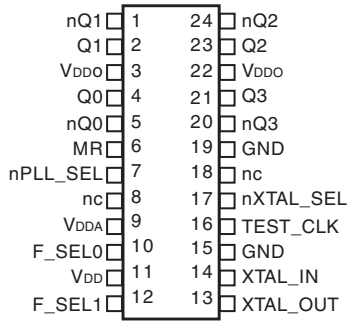
FEATURES

- Four SSTL_2 differential clock output pairs
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input
- Supports the following output frequencies: 212.5MHz, 187.5MHz, 159.375MHz, 156.25MHz, 106.25MHz, 53.125MHz
- VCO range: 560MHz - 680MHz
- RMS phase jitter @ 212.5MHz, using a 26.5625MHz crystal (637kHz - 10MHz): 0.80ps (typical)
- SSTL operating voltage supply ranges:
  V_{DD} = 3.0V to 3.6V, V_{DDO} = 3.0V to 3.6V
  V_{DD} = 2.3V to 3.6V, V_{DDO} = 2.3V to 2.7V
  V_{DD} = 2.3V to 3.6V, V_{DDO} = 1.7V to 1.9V
- -40°C to 85°C ambient operating temperature

FREQUENCY SELECT FUNCTION TABLE

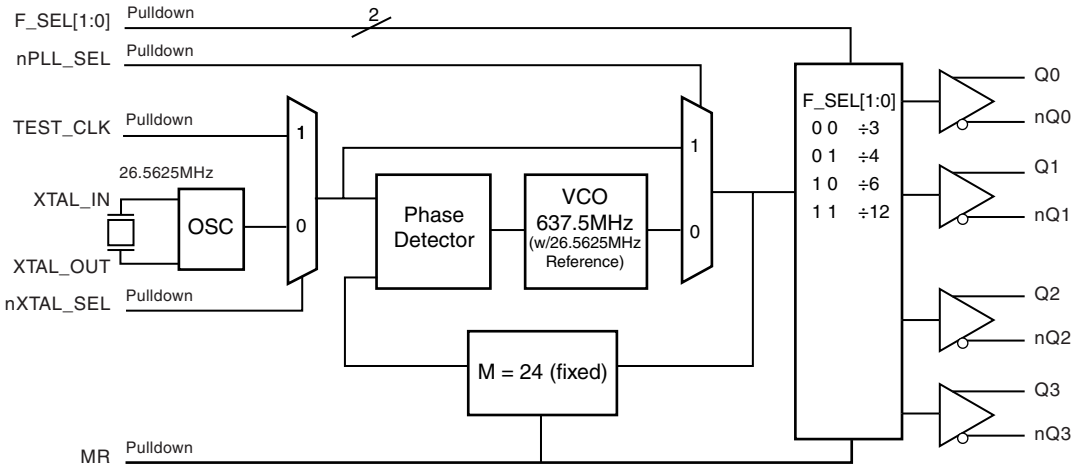
Inputs						Output Frequency (MHz)
Input Frequency (MHz)	F_SEL1	F_SEL0	M Divider Value	N Divider Value	M/N Divider Value	
26.5625	0	0	24	3	8	212.5
26.5625	0	1	24	4	6	159.375
26.5625	1	0	24	6	4	106.25
26.5625	1	1	24	12	2	53.125
26.04166	0	1	24	4	6	156.25
23.4375	0	0	24	3	8	187.5

PIN ASSIGNMENT



ICS848004I
24-Lead TSSOP
4.40mm x 7.8mm x 0.92mm
package body
G Package
Top View

BLOCK DIAGRAM



The Advance Information presented herein represents a product currently in design or being considered for design. The noted characteristics are design targets. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	nQ1, Q1	Output		Differential output pair. SSTL_2 interface levels.
3, 22	V_{DDO}	Power		Output supply pins.
4, 5	Q0, nQ0	Ouput		Differential output pair. SSTL_2 interface levels.
6	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
7	nPLL_SEL	Input	Pulldown	Selects between the PLL and TEST_CLK as input to the dividers. When LOW, selects PLL (PLL Enable). When HIGH, deselects the reference clock (PLL Bypass). LVCMOS/LVTTL interface levels.
8, 18	nc	Unused		No connect.
9	V_{DDA}	Power		Analog supply pin.
10, 12	F_SEL0, F_SEL1	Input	Pulldown	Frequency select pins. LVCMOS/LVTTL interface levels.
11	V_{DD}	Power		Core supply pin.
13, 14	XTAL_OUT, XTAL_IN	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.
15, 19	GND	Power		Power supply ground.
16	TEST_CLK	Input	Pulldown	LVCMOS/LVTTL clock input.
17	nXTAL_SEL	Input	Pulldown	Selects between crystal or TEST_CLK inputs as the the PLL Reference source. Selects XTAL inputs when LOW. Selects TEST_CLK when HIGH. LVCMOS/LVTTL interface levels.
20, 21	nQ3, Q3	Output		Differential output pair. SSTL_2 interface levels.
23, 24	Q2, nQ2	Output		Differential output pair. SSTL_2 interface levels.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	58.3°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO}$ = 3.3V±10%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.0	3.3	3.6	V
V_{DDA}	Analog Supply Voltage		3.0	3.3	3.6	V
V_{DDO}	Output Supply Voltage		3.0	3.3	3.6	V
I_{DD}	Power Supply Current			TBD		mA
I_{DDA}	Analog Supply Current			TBD		mA
I_{DDO}	Output Supply Current			TBD		mA

TABLE 3B. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA}$ = 3.3V±10% OR 2.5V±10%, V_{DDO} = 2.5V±10%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.3	3.0	3.6	V
V_{DDA}	Analog Supply Voltage		2.3	3.0	3.6	V
V_{DDO}	Output Supply Voltage		2.3	2.5	2.7	V
I_{DD}	Power Supply Current			TBD		mA
I_{DDA}	Analog Supply Current			TBD		mA
I_{DDO}	Output Supply Current			TBD		mA

TABLE 3C. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA}$ = 3.3V±10% OR 2.5V±10%, V_{DDO} = 1.8V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.3	3.0	3.6	V
V_{DDA}	Analog Supply Voltage		2.3	3.0	3.6	V
V_{DDO}	Output Supply Voltage		1.7	1.8	1.9	V
I_{DD}	Power Supply Current			TBD		mA
I_{DDA}	Analog Supply Current			TBD		mA
I_{DDO}	Output Supply Current			TBD		mA

TABLE 3D. LVCMOS / LVTTL DC CHARACTERISTICS, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V	-0.3		0.8	V
			V_{DD} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	TEST_CLK, MR, F_SEL0, F_SEL1, nPLL_SEL, nXTAL_SEL,	V_{DD} = V_{IN} = 3.6 or 2.7V			150	µA
I_{IL}	Input Low Current	TEST_CLK, MR, F_SEL0, F_SEL1, nPLL_SEL, nXTAL_SEL,	V_{DD} = 3.6V or 2.7V, V_{IN} = 0V	-150			µA

TABLE 3E. DIFFERENTIAL DC CHARACTERISTICS, V_{DD} = V_{DDA} = V_{DDO} = 3.3V±10%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Output Differential Voltage		0.7			V
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1		0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1		0.5		V_{DDO} - 0.85	V
V_{OH}	Output High Voltage; NOTE 2			>2.1		V
V_{OL}	Output Low Voltage; NOTE 2			<0.9		V

NOTE 1: V_{CMR}, V_{PP} defined for driving TEST_CLK input with differential levels other than SSTL_2.
NOTE 2: Outputs terminated with 50Ω to ground.

TABLE 3F. DIFFERENTIAL DC CHARACTERISTICS, V_{DD} = V_{DDA} = 3.3V±10% OR 2.5V±10%, V_{DDO} = 2.5V±10%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Output Differential Voltage		0.7			V
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1		0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1		0.5		V_{DDO} - 0.85	V
V_{OH}	Output High Voltage; NOTE 2			>1.77		V
V_{OL}	Output Low Voltage; NOTE 2			<0.73		V

NOTE 1: V_{CMR}, V_{PP} defined for driving TEST_CLK input with differential levels other than SSTL_2.
NOTE 2: Outputs terminated with 50Ω to ground.

TABLE 3G. DIFFERENTIAL DC CHARACTERISTICS, V_{DD} = V_{DDA} = 3.3V±10% OR 2.5V±10%, V_{DDO} = 1.8V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Output Differential Voltage		0.7			V
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1		0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1		0.5		V_{DDO} - 0.85	V
V_{OH}	Output High Voltage; NOTE 2			>1.19		V
V_{OL}	Output Low Voltage; NOTE 2			<0.615		V

NOTE 1: V_{CMR}, V_{PP} defined for driving TEST_CLK input with differential levels other than SSTL_2.
NOTE 2: Outputs terminated with 50Ω to ground.

TABLE 4. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency		23.33	26.5625	28.33	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

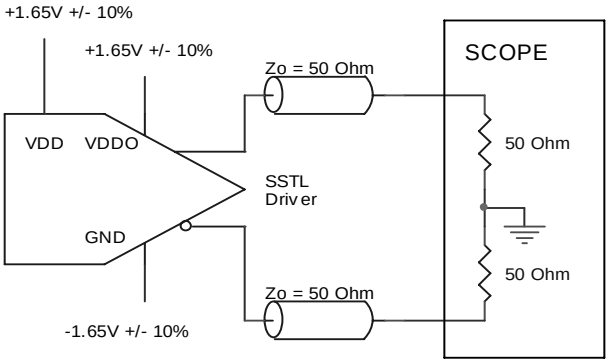
NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 5. AC CHARACTERISTICS, TA = -40°C TO 85°C

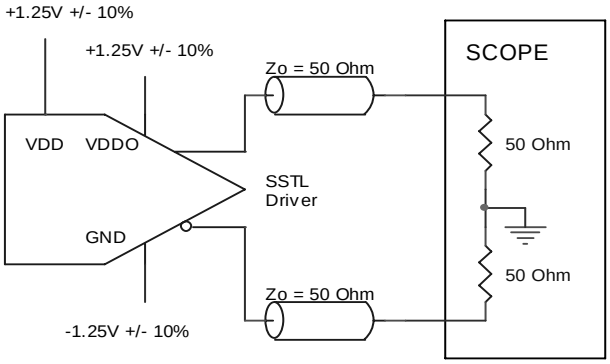
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	F_SEL[1:0] = 00	186.67		226.66	MHz
		F_SEL[1:0] = 01	140		170	MHz
		F_SEL[1:0] = 10	93.33		113.33	MHz
		F_SEL[1:0] = 11	46.67		56.66	MHz
*t*sk(o)	Output Skew; NOTE 1, 2			TBD		ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 3	212.5MHz, (637kHz - 10MHz)		0.80		ps
		159.375MHz, (637kHz - 10MHz)		0.78		ps
		156.25MHz, (1.875MHz - 20MHz)		0.50		ps
		106.25MHz, (637kHz - 10MHz)		0.81		ps
		53.125MHz, (637kHz - 10MHz)		0.79		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		650		ps
odc	Output Duty Cycle			50		%

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at V_{DDO}/2.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Please refer to the Phase Noise Plot.

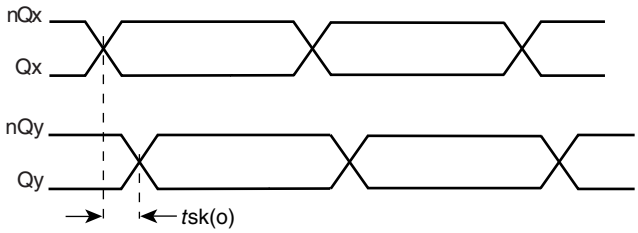
PARAMETER MEASUREMENT INFORMATION



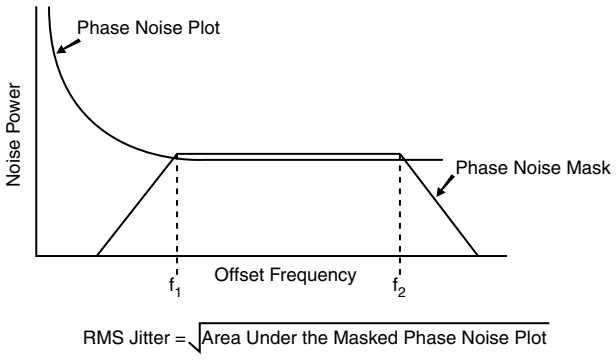
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



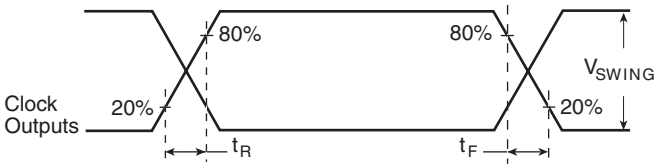
2.5V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



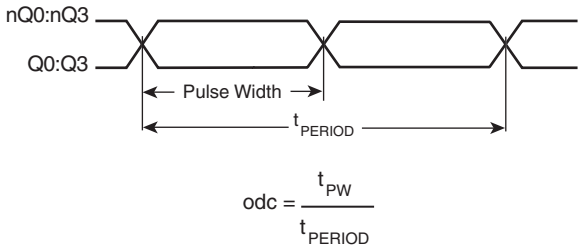
OUTPUT SKEW



RMS PHASE JITTER



OUTPUT RISE/FALL TIME



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS848004I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA}.

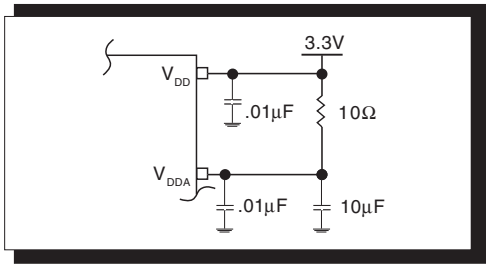


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS848004I has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 26.5625MHz 18pF parallel resonant crystal and were chosen to minimize the ppm error.

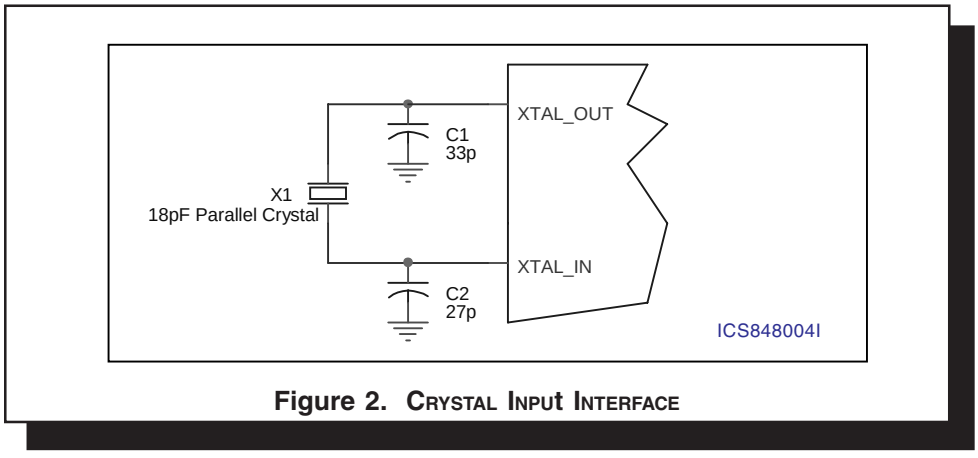


Figure 2. CRYSTAL INPUT INTERFACE

SSTL INTERFACE

Figures 3A to 3C show interface example of ICS848004I SOCKET/nSOCKET input driven by an SSTL driver. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. The SSTL termination shown in these examples are also suitable for ICS48004I SSTL output drivers.

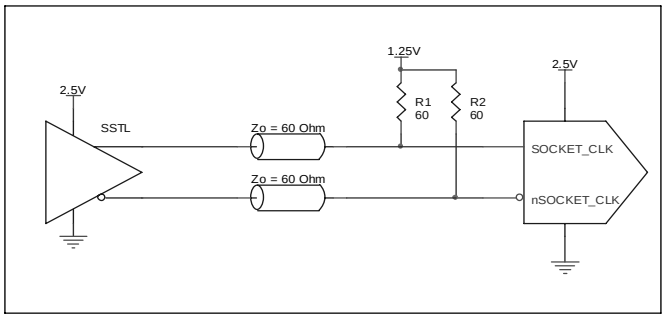


FIGURE 3A. TYPICAL SSTL INTERFACE FOR $V_{DD}/2$ = 1.25V BEING AVAILABLE

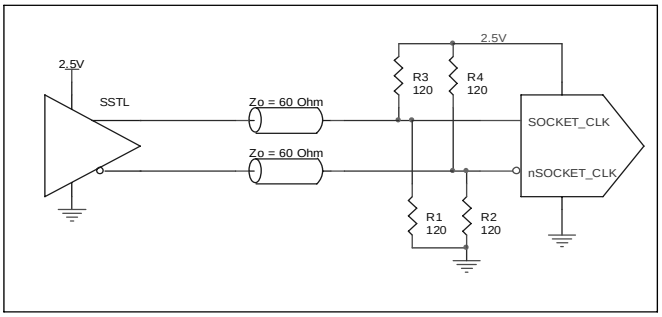


FIGURE 3B. SSTL INTERFACE FOR $V_{DD}/2$ = 1.25V WITH NO AVAILABLE

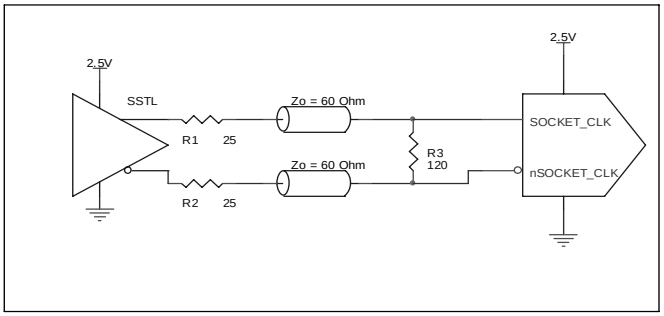


FIGURE 3C. DIFFERENTIAL SSTL INTERFACE

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 24 LEAD TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

TRANSISTOR COUNT

The transistor count for ICS848004I is: 2951

PACKAGE OUTLINE - G SUFFIX FOR 24 LEAD TSSOP

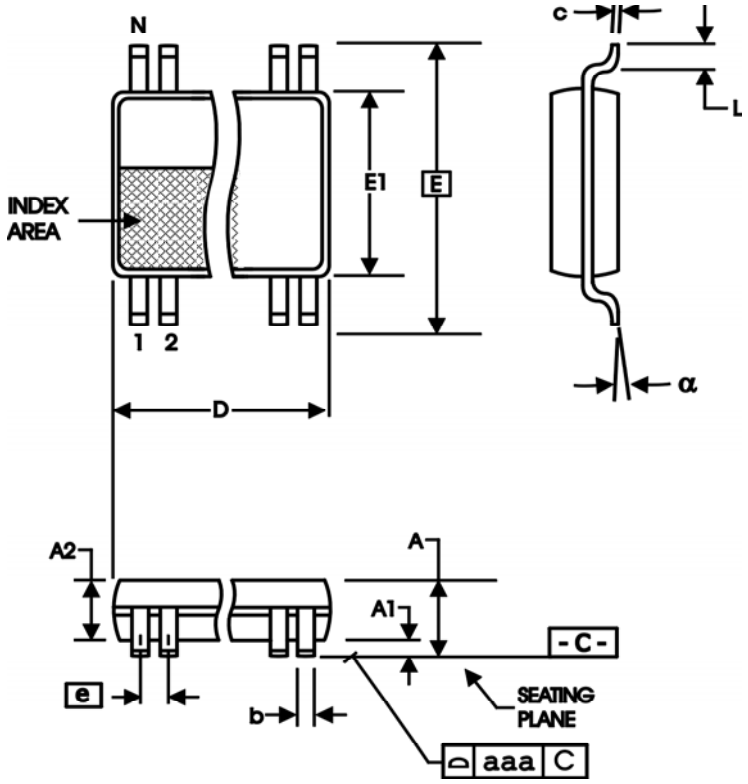


TABLE 7. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS848004AGI	ICS848004AGI	24 Lead TSSOP	tube	-40°C to 85°C
ICS848004AGIT	ICS848004AGI	24 Lead TSSOP	2500 tape & reel	-40°C to 85°C