



Integrated  
Circuit  
Systems, Inc.

**PRELIMINARY**

**ICS86004**  
15.625MHz TO 62.5MHz, 1:4 LVCMOS/LVTTL  
ZERO DELAY CLOCK BUFFER

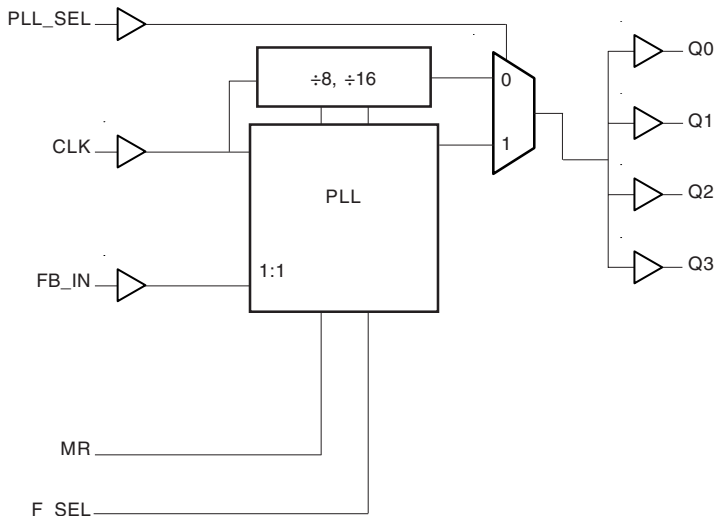
## GENERAL DESCRIPTION

The ICS86004 is a high performance 1:4 LVCMOS/LVTTL Clock Buffer and a member of the HiPerClock<sup>SM</sup> family of High Performance Clock Solutions from ICS. The ICS86004 has a fully integrated PLL and can be configured as zero delay buffer and has an input and output frequency range of 15.625MHz to 62.5MHz. The VCO operates at a frequency range of 250MHz to 500MHz. The external feedback allows the device to achieve “zero delay” between the input clock and the output clocks. The PLL\_SEL pin can be used to bypass the PLL for system test and debug purposes. In bypass mode, the reference clock is routed around the PLL and into the internal output divider.

## FEATURES

- 4 LVCMOS/LVTTL outputs, 7Ω typical output impedance
- Single LVCMOS/LVTTL clock input
- CLK accepts the following input levels: LVCMOS or LVTTL
- Output frequency range: 15.625MHz to 62.5MHz
- Input frequency range: 15.625MHz to 62.5MHz
- VCO range: 250MHz to 500MHz
- External feedback for “zero delay” clock regeneration with configurable frequencies
- Fully integrated PLL
- Cycle-to-cycle jitter: 50ps (typical)
- Output skew: 40ps (typical)
- Static Phase Offset: TBD
- Full 3.3V or 2.5V, or 3.3V core/2.5V output operating supply
- Industrial temperature information available upon request

## BLOCK DIAGRAM



## PIN ASSIGNMENT

Q1	1	16	VDDO
GND	2	15	Q2
Q0	3	14	GND
F_SEL	4	13	Q3
VDD	5	12	VDDO
CLK	6	11	MR
GND	7	10	FB_IN
VDDA	8	9	PLL_SEL

**ICS86004**  
**16-Lead TSSOP**  
4.4mm x 3.0mm x 0.92mm package body  
**G Package**  
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.



**TABLE 1. PIN DESCRIPTIONS**

Number	Name	Type		Description
1, 3, 13, 15	Q1, Q0, Q3, Q2	Output		Clock outputs. 7Ω typical output impedance. LVCMOS/LVTTL interface levels.
2, 7, 14	GND	Power		Power supply ground.
4	F_SEL	Input	Pulldown	Frequency range select input. LVCMOS/LVTTL interface levels.
5	V <sub>DD</sub>	Power		Core supply pin.
6	CLK	Input	Pulldown	LVCMOS/LVTTL clock input.
8	V <sub>DDA</sub>	Power		Analog supply pin.
9	PLL_SEL	Input	Pullup	Selects between the PLL and reference clock as input to the dividers. When LOW, selects the reference clock (PLL Bypass). When HIGH, selects PLL (PLL Enabled). LVCMOS/LVTTL interface levels.
10	FB_IN	Input	Pulldown	Feedback input to phase detector for regenerating clocks with "zero delay". Connect to one of the outputs. LVCMOS/LVTTL interface levels.
11	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the outputs to go low. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
12, 16	V <sub>DDO</sub>	Power		Output supply pins.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		KΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		KΩ
C <sub>PD</sub>	Power Dissipation Capacitance (per output)	V <sub>DD</sub> , V <sub>DDA</sub> , V <sub>DDO</sub> = 3.465V		TBD		pF
		V <sub>DD</sub> , V <sub>DDA</sub> = 3.465V, V <sub>DDO</sub> = 2.625V		TBD		pF
		V <sub>DD</sub> , V <sub>DDA</sub> , V <sub>DDO</sub> = 2.625V		TBD		pF
R <sub>OUT</sub>	Output Impedance		5	7	12	Ω

**TABLE 3A. CONTROL INPUT FUNCTION TABLE, PLL\_SEL = 1**

Input	Input/Output Frequency Range (MHz)	
	Minimum	Maximum
F_SEL = 0	31.25	62.5
F_SEL = 1	15.625	31.25

**TABLE 3B. CONTROL INPUT FUNCTION TABLE, PLL\_SEL = 0**

Input	Output
F_SEL	
0	Ref ÷8
1	Ref ÷16



**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_i$	-0.5V to $V_{DD} + 0.5V$
Outputs, $V_o$	-0.5V to $V_{DDO} + 0.5V$
Package Thermal Impedance, $\theta_{JA}$	89°C/W (0 lfpm)
Storage Temperature, $T_{STG}$	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{DDA}$	Analog Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		3.135	3.3	3.465	V
$I_{DD}$	Power Supply Current			85		mA
$I_{DDA}$	Analog Supply Current			15		mA
$I_{DDO}$	Output Supply Current			5		mA

**TABLE 4B. LVCMOS / LVTTL DC CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$  OR  $2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	FB_IN, MR, PLL_SEL, F_SEL	2		$V_{DD} + 0.3$	V
		CLK	2		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage	FB_IN, MR, PLL_SEL, F_SEL	-0.3		0.8	V
		CLK	-0.3		1.3	V
$I_{IH}$	Input High Current	CLK, MR, FB_IN, F_SEL	$V_{DD} = V_{IN} = 3.465V$		150	$\mu A$
		PLL_SEL	$V_{DD} = V_{IN} = 3.465V$		5	$\mu A$
$I_{IL}$	Input Low Current	CLK, MR, FB_IN, F_SEL	$V_{DD} = 3.465V, V_{IN} = 0V$	-5		$\mu A$
		PLL_SEL	$V_{DD} = 3.465V, V_{IN} = 0V$	-150		$\mu A$
$V_{OH}$	Output High Voltage; NOTE 1		$V_{DDO} = 3.465V$	2.6		V
			$V_{DDO} = 2.625V$	1.8		V
$V_{OL}$	Output Low Voltage; NOTE 1		$V_{DDO} = 3.465V$ or $2.625V$		0.5	V

NOTE 1: Outputs terminated with 50 $\Omega$  to  $V_{DDO}/2$ . See Parameter Measurement Information Section, *Output Load Test Circuit diagrams*.



**TABLE 4C. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = V_{DDA} = 3.3V \pm 5\%$ ,  $V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{DDA}$	Analog Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		2.375	2.5	2.625	V
$I_{DD}$	Power Supply Current			TBD		mA
$I_{DDA}$	Analog Supply Current			TBD		mA
$I_{DDO}$	Output Supply Current			TBD		mA

**TABLE 4D. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Core Supply Voltage		2.375	2.5	2.625	V
$V_{DDA}$	Analog Supply Voltage		2.375	2.5	2.625	V
$V_{DDO}$	Output Supply Voltage		2.375	2.5	2.625	V
$I_{DD}$	Power Supply Current			TBD		mA
$I_{DDA}$	Analog Supply Current			TBD		mA
$I_{DDO}$	Output Supply Current			TBD		mA

**TABLE 5A. AC CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency	F_SEL = 0	31.25		62.5	MHz
		F_SEL = 1	15.625		31.25	MHz
$tp_{LH}$	Propagation Delay, Low-to-High; NOTE 1	PLL_SEL = 0V, $f \leq 250MHz$		TBD		ns
$t(\emptyset)$	Static Phase Offset; NOTE 2, 4	PLL_SEL = 3.3V		TBD		ps
$t_{sk(o)}$	Output Skew; NOTE 3, 4	PLL_SEL = 0V		40		ps
$f_{jit(cc)}$	Cycle-to-Cycle Jitter; NOTE 4			50		ps
$t_L$	PLL Lock Time			1		mS
$t_R / t_F$	Output Rise/Fall Time			600		ps
odc	Output Duty Cycle			50		%

All parameters measured at  $f_{MAX}$  unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the output at  $V_{DDO}/2$ .

NOTE 2: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable.

NOTE 3: Defined as skew between outputs at the same supply voltages and with equal load conditions.

Measured at  $V_{DDO}/2$ .

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.



**TABLE 5B. AC CHARACTERISTICS,  $V_{DD} = V_{DDA} = 3.3V \pm 5\%$ ,  $V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency	F_SEL = 0	31.25		62.5	MHz
		F_SEL = 1	15.625		31.25	MHz
$t_{p_{LH}}$	Propagation Delay, Low-to-High; NOTE 1	PLL_SEL = 0V, $f \leq 250MHz$		TBD		ns
$t(\emptyset)$	Static Phase Offset; NOTE 2, 4	PLL_SEL = 2.5V		TBD		ps
$t_{sk(o)}$	Output Skew; NOTE 3, 4	PLL_SEL = 0V		TBD		ps
$f_{jit(cc)}$	Cycle-to-Cycle Jitter; NOTE 4			TBD		ps
$t_L$	PLL Lock Time			TBD		mS
$t_R / t_F$	Output Rise/Fall Time			TBD		ps
odc	Output Duty Cycle			TBD		%

All parameters measured at  $f_{MAX}$  unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the output at  $V_{DDO}/2$ .

NOTE 2: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable.

NOTE 3: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at  $V_{DDO}/2$ .

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

**TABLE 5C. AC CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency	F_SEL = 0	31.25		62.5	MHz
		F_SEL = 1	15.625		31.25	MHz
$t_{p_{LH}}$	Propagation Delay, Low-to-High; NOTE 1	PLL_SEL = 0V, $f \leq 250MHz$		TBD		ns
$t(\emptyset)$	Static Phase Offset; NOTE 2, 4	PLL_SEL = 2.5V		TBD		ps
$t_{sk(o)}$	Output Skew; NOTE 3, 4	PLL_SEL = 0V		TBD		ps
$f_{jit(cc)}$	Cycle-to-Cycle Jitter; NOTE 4			TBD		ps
$t_L$	PLL Lock Time			TBD		mS
$t_R / t_F$	Output Rise/Fall Time			TBD		ps
odc	Output Duty Cycle			TBD		%

All parameters measured at  $f_{MAX}$  unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the output at  $V_{DDO}/2$ .

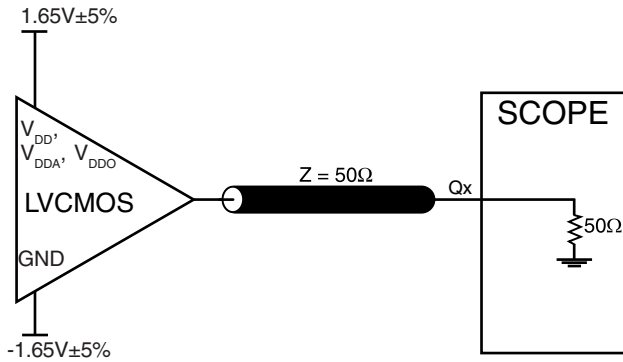
NOTE 2: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable.

NOTE 3: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at  $V_{DDO}/2$ .

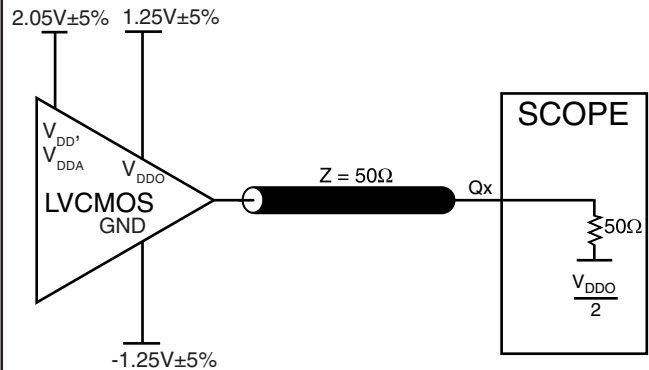
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.



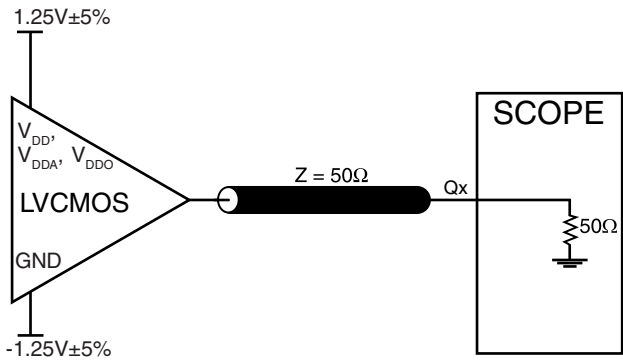
**PARAMETER MEASUREMENT INFORMATION**



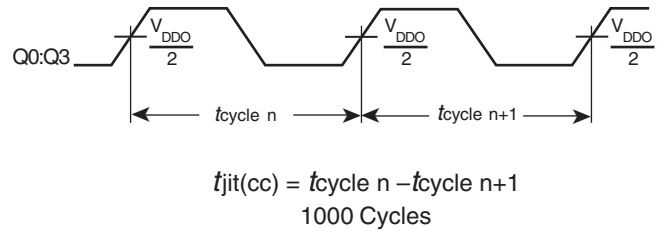
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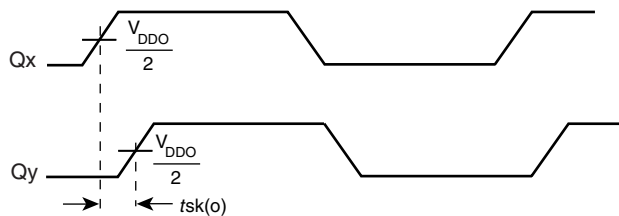
**3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT**



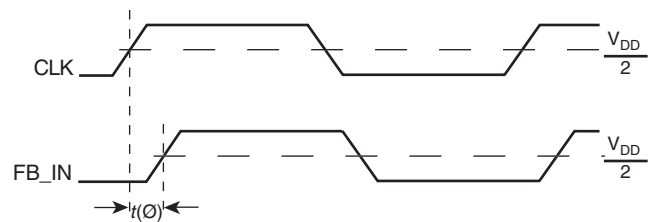
**2.5V CORE/ 2.5V OUTPUT LOAD AC TEST CIRCUIT**



**CYCLE-TO-CYCLE JITTER**



**OUTPUT SKEW**



$t(\emptyset)_{mean}$  = Static Phase Offset  
(where  $t(\emptyset)$  is any random sample, and  $t(\emptyset)_{mean}$  is the average of the sampled cycles measured on controlled edges)

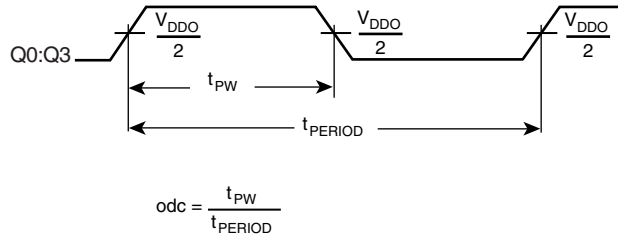
**STATIC PHASE OFFSET**



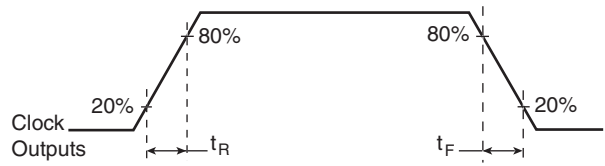
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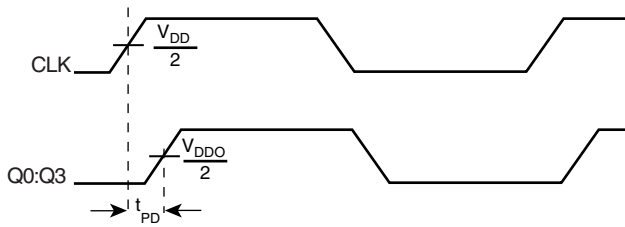
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**OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD**



**OUTPUT RISE/FALL TIME**



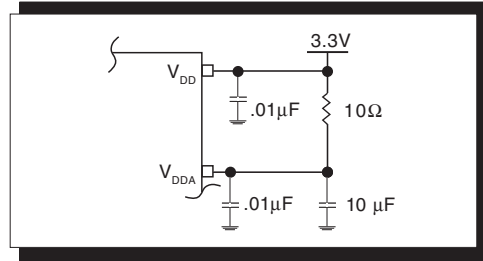
**PROPAGATION DELAY**



**APPLICATION INFORMATION**

**POWER SUPPLY FILTERING TECHNIQUES**

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS86004 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{DD}$ ,  $V_{DDA}$ , and  $V_{DDO}$  should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a  $10\Omega$  resistor along with a  $10\mu F$  and a  $.01\mu F$  bypass capacitor should be connected to each  $V_{DDA}$ .

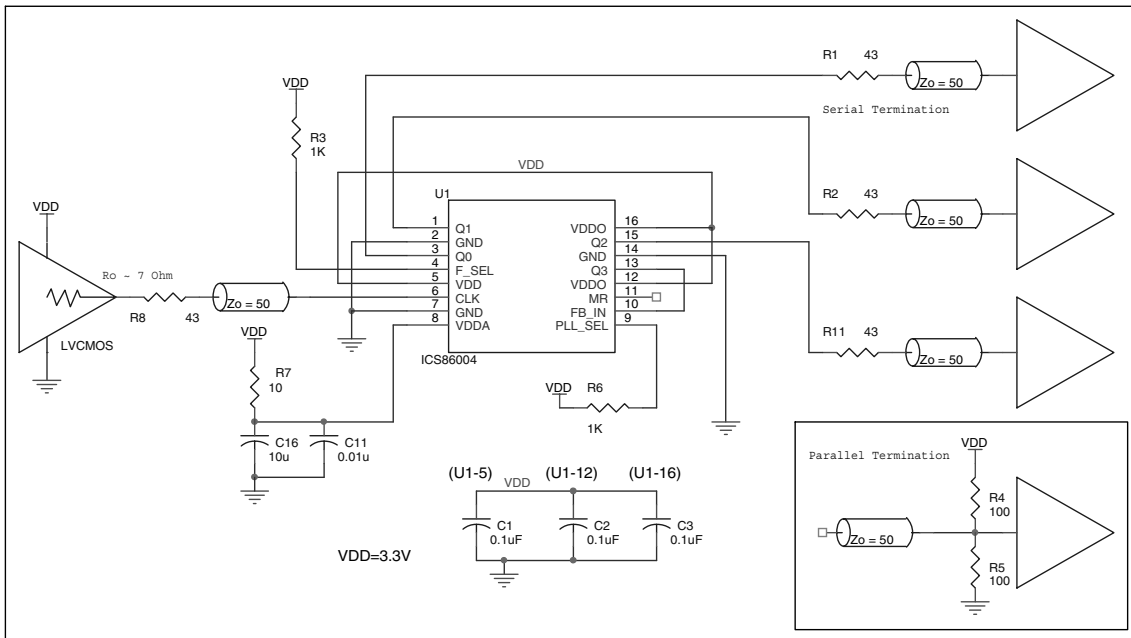


**FIGURE 1. POWER SUPPLY FILTERING**

**SCHEMATIC EXAMPLE**

*Figure 2* shows a schematic example of using an ICS86004. It is recommended to have one decouple capacitor per power pin. Each decoupling capacitor should be located as close as possible

to the power pin. The low pass filter R7, C11 and C16 for clean analog supply should also be located as close to the  $V_{DDA}$  pin as possible.



**FIGURE 2. ICS86004 SCHEMATIC EXAMPLE**





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### RELIABILITY INFORMATION

TABLE 5.  $\theta_{JA}$  VS. AIR FLOW TABLE FOR 16 LEAD TSSOP

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	137.1°C/W	118.2°C/W	106.8°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	89.0°C/W	81.8°C/W	78.1°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

#### TRANSISTOR COUNT

The transistor count for ICS86004 is: 2496

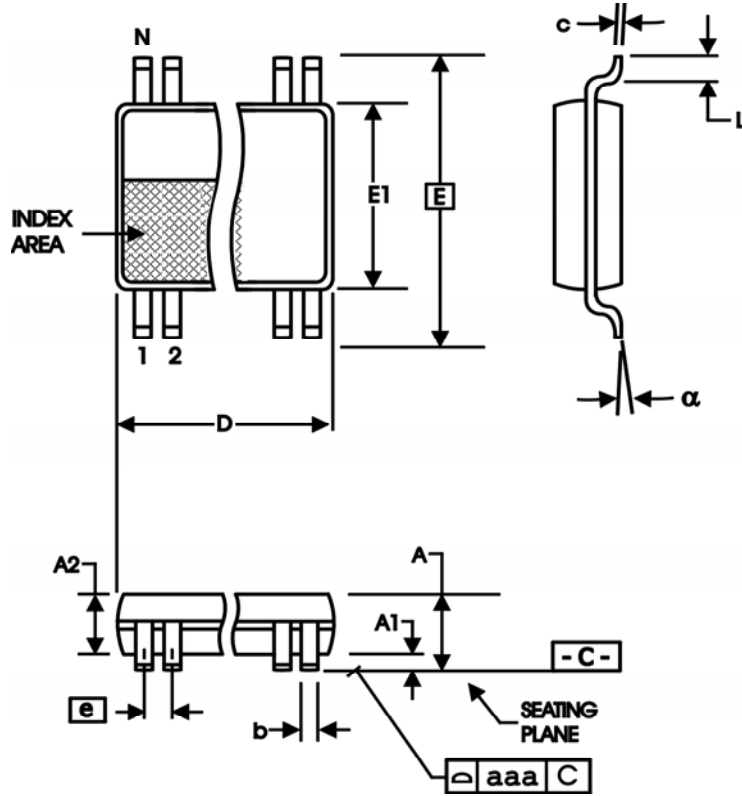


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**PACKAGE OUTLINE - G SUFFIX 16 LEAD TSSOP**



**TABLE 6. PACKAGE DIMENSIONS**

SYMBOL	Millimeters	
	Minimum	Maximum
N	16	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
alpha	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153



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**TABLE 7. ORDERING INFORMATION**

<b>Part/Order Number</b>	<b>Marking</b>	<b>Package</b>	<b>Count</b>	<b>Temperature</b>
ICS86004BG	ICS86004BG	16 Lead TSSOP	94 per tube	0°C to 70°C
ICS86004BGT	ICS86004BG	16 Lead TSSOP on Tape and Reel	2500	0°C to 70°C

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