# MOTOROLA SEMICONDUCTOR TECHNICAL DATA

# Advance Information Dual Video Amplifiers CMOS

Each of these devices contains two amplifiers realized in CMOS. Each amp also employs two lateral NPN bipolar transistors.

The MC14576A contains two internally-compensated operational amplifiers. On-chip gain-setting resistors result in a noninverting voltage gain of  $6.0 \text{ dB} \pm 1.0 \text{ dB}$  at 4.43 MHz for each amp. Each noninverting input of the MC14576A appears as a mostly-capacitive load of about 10 pF.

The MC14577A also contains two internally-compensated operational amplifiers. However, the gain for each amp is adjustable with external components. (The value of the closed-loop voltage gain with a 150  $\Omega$  load should not exceed 10 dB at 5 MHz and 6 dB at 10 MHz.) All inputs of the MC14577A appear as mostly-capacitive loads of about 10 pF.

- Direct Drive of 150  $\Omega$  Loads
- · Maximum Supply Current: 40 mA per Package
- Operating Voltage Range P Suffix: 5.0 to 12 V Relative to VSS F Suffix: 5.0 to 10 V Relative to VSS
- · May be used with Single or Dual Supplies
- Operating Temperature Range P Suffix: –20 to 70°C

F Suffix: -20 to 50°C

- Excellent Differential Gain: 3% Maximum @ 4.43 MHz
- Excellent Differential Phase: 3° Maximum @ 4.43 MHz
- Guaranteed Bandwidth: 10 MHz
- · Minimal External Components Required

# MC14576A MC14577A

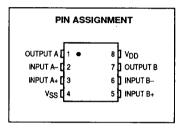


P SUFFIX PLASTIC DIP CASE 626

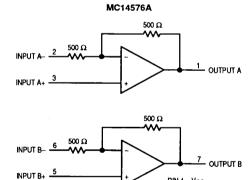
F SUFFIX SOG PACKAGE CASE TBD

## ORDERING INFORMATION

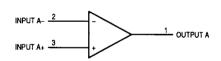
MC14576AP, MC14577AP Plastic DIP MC14576AF, MC14577AF SOG Package

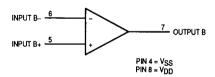


#### SYMBOLIC REPRESENTATIONS



#### MC14577A





NOTE: Resistors are shown above with nominal values.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

PIN 4 = VSS

PIN 8 = VDD

#### MAXIMUM RATINGS\*.

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage (Referenced to VSS)	-0.5 to +14	٧
Vin	DC Input Voltage	V <sub>SS</sub> -0.5 to V <sub>DD</sub> +0.5	٧
Vout	DC Output Voltage	V <sub>SS</sub> -0.5 to V <sub>DD</sub> +0.5	٧
T <sub>stg</sub>	Storage Temperature -65 to +150		°C
TL	Lead Temperature (10-Second Soldering)	260	°C

<sup>\*</sup> Maximum Ratings are those values beyond which damage to the device may occur.

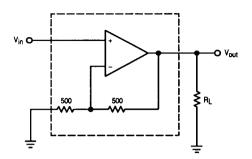
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range VSSS4(Vin or Vout)SVDD.

Unused inputs must always be tied to an appropriate voltage level (e.g., either VSS or VDD). Unused outputs must be left open.

### ELECTRICAL CHARACTERISTICS ( $T_A=25^{\circ}C$ , Reference Figures 1 and 2, $R_L=150~\Omega$ Unless Otherwise Indicated)

Symbol	Parameter	Test Condition	V <sub>DD</sub> V	V <sub>SS</sub>	Guaranteed Limit	Unit
VDD	Power Supply Voltage Range (Referenced to VSS) P Suffix F Suffix		_		5.0 to 12 5.0 to 10	٧
IDD	Maximum Power Supply Current (Per Package)	V <sub>in</sub> = 0 V, R <sub>L</sub> = ∞ (open)	+5.0	-5.0	40	mA
N	Maximum Output Noise	V <sub>in</sub> = 0 V, BW = 30 Hz to 25 MHz	+5.0	-5.0	250	μV RMS
Av	Closed-Loop Voltage Gain	V <sub>in</sub> = 2.0 V p-p, f = 4.43 MHz	+5.0	-5.0	5.0 to 7.0	dB
BW	Bandwidth	V <sub>in</sub> = 2.0 V p-p, A <sub>V</sub> within ±3.0 dB of the gain at 4.43 MHz	+5.0	-5.0	10	MHz
V <sub>out</sub>	Minimum Output Voltage Swing	V <sub>in</sub> = 4.0 V p-p, f = 10 MHz	+5.0	<b>-5.0</b>	3.5	V p-p
		V <sub>in</sub> = 1.5 V p-p, f = 5.0 MHz	+2.5	-2.5	2.0	
_	Maximum Differential Gain	V <sub>in</sub> = 300 mV p-p biased from -0.5 to +0.5 V, f = 4.43 MHz	+5.0	<b>−5.0</b>	3.0	%
	Maximum Differential Phase	V <sub>in</sub> = 300 mV p-p biased from -0.5 to +0.5 V, f = 4.43 MHz	+5.0	5.0	3.0	Degrees
PSRR	Minimum Power Supply Rejection Ratio, VDD or VSS pins	V <sub>in</sub> = 0 V, ΔV <sub>DD</sub> or ΔV <sub>SS</sub> = 400 mV p-p @ 100 kHz	+5.0	-5.0	43	dB
_	Minimum Channel Separation	V <sub>in</sub> = 1.0 V p-p, f = 4.43 MHz	+5.0	-5.0	40	dB
C <sub>in</sub>	Maximum Input Capacitance	V <sub>in</sub> = 1.0 V p-p, f = 4.43 MHz	+5.0	-5.0	TBD	pF
Rin	Minimum Input Resistance, all Inputs except Input A– and Input B– of the MC14576A		+5.0	5.0	107**	Ω

<sup>\*\*</sup>Typical value only; not guaranteed.



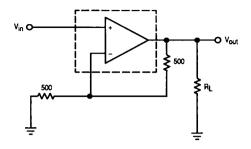


Figure 1. MC14576A Test Circuit

Figure 2. MC14577A Test Circuit

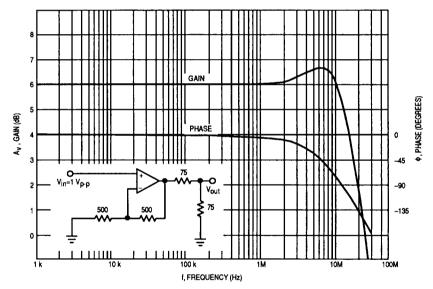


Figure 3. Typical Gain/Phase-Frequency Response (Not Guaranteed)

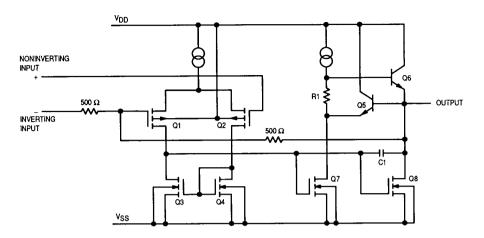


Figure 4. MC14576A Schematic

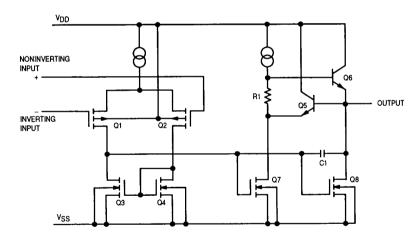


Figure 5. MC14577A Schematic

#### APPLICATIONS

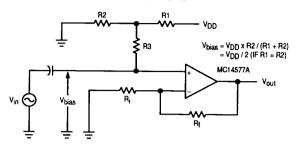


Figure 6. AC-Coupled Noninverting Amplifier with Single-Supply Operation

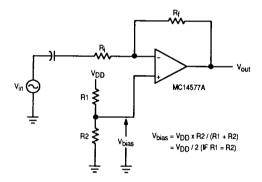


Figure 7. AC-Coupled Inverting Amplifier with Single-Supply Operation

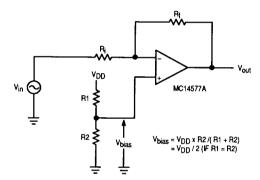


Figure 8. DC-Coupled Inverting Amplifier with Single-Supply Operation

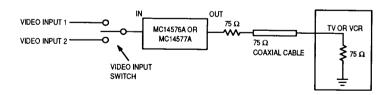


Figure 9. Typical Application of MC14576/77A

MOTOROLA CMOS APPLICATION-SPECIFIC DIGITAL-ANALOG INTEGRATED CIRCUITS

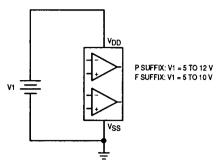


Figure 10. Single-Supply Operation

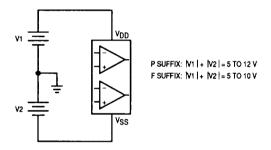


Figure 11. Dual- or Split-Supply Operation