OKI Semiconductor

This version: Jun. 1999

Preliminary

ML9052

132-Channel LCD Driver with Built-in RAM for LCD Dot Matrix Displays

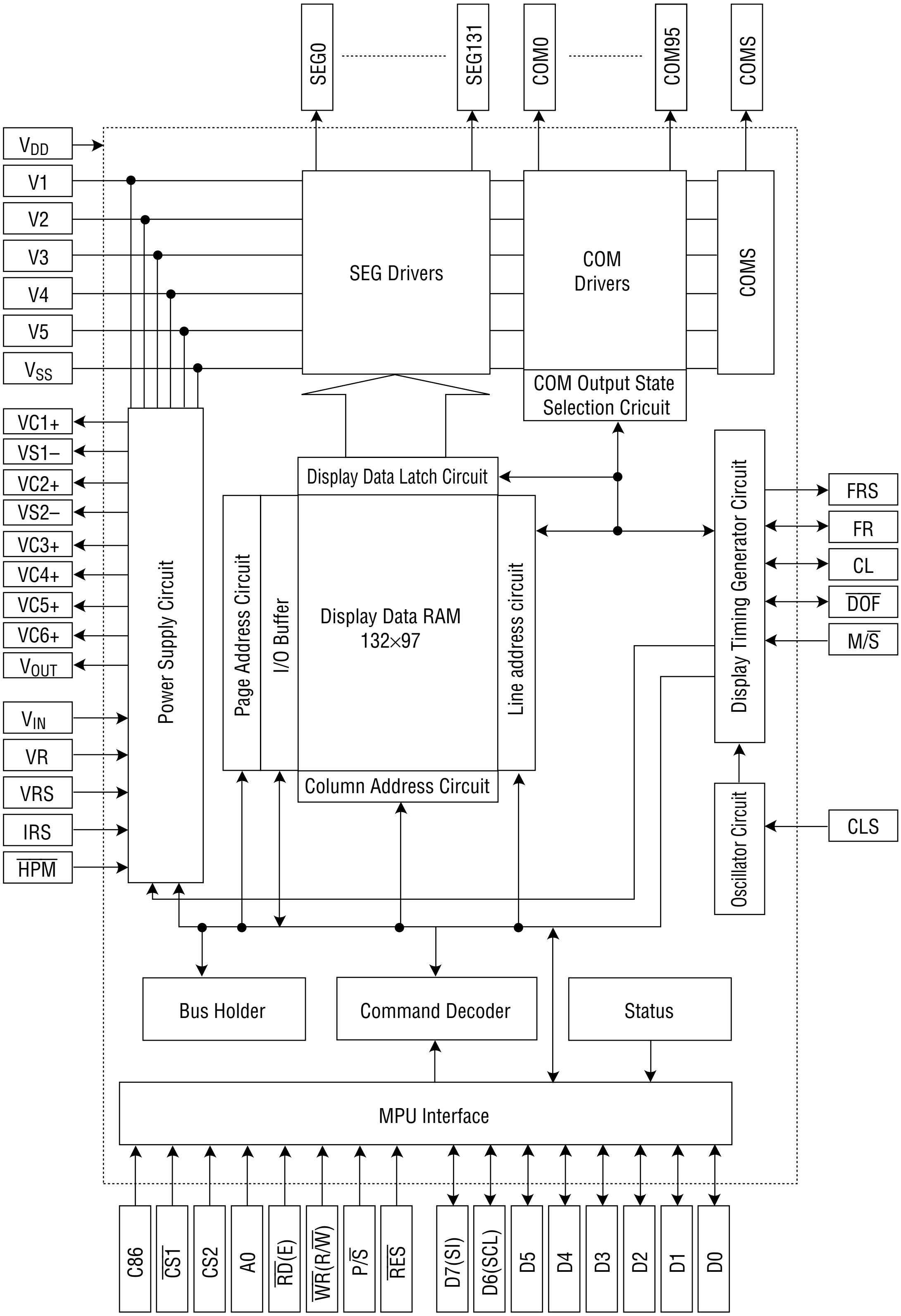
GENERAL DESCRIPTION

The ML9052 is an IC for dot matrix graphic LCD devices carrying out bit map display. This IC can drive a dot matrix graphic LCD panel under the control of an 8-bit microcontroller. Since all the functions necessary for driving a bit map type LCD device are incorporated in a single chip, using the ML9052 makes it possible to implement a bit map type dot matrix graphic LCD system with only a few chips.
Since the bit map method, in which one bit of display RAM data turns ON or OFF one dot in the display panel, is employed, it is possible to carry out displays with a high degree of freedom such as Chinese character displays, etc. With a single device, it is possible to construct a graphic display system with a maximum of 132×97 dots. The display can be expanded further using two devices.
The ML9052 with a built-in RAM, which is fabricated using the CMOS process, achieves low-power operation and is ideally suitable for displays in battery-operated portable equipment.
The ML9052 has 97 common signal outputs and 132 segment signal outputs and a single device can drive a display of up to 97 × 132 dots.
This device is not resistant to radiation or to light.

FEATURES

- Direct display of the RAM data using the bit map method
  Display RAM data "1" ... Dot is displayed
  Display RAM data "0" ... Dot is not displayed
- Display RAM capacity
  97 × 132 = 12804 dots
- LCD drive circuits
  97 common outputs, 132 segment outputs
- Microcontroller interface: Can select an 8-bit parallel or serial interface
- Built-in voltage multiplier circuit for the LCD drive power supply
- Built-in LCD drive power supply adjustment circuit
- Built-in LCD drive bias resistors
- Line inversion drive/frame inversion drive (selected by a command)
- Built-in oscillator circuit (Internal RC oscillator/external clock input)
- A variety of commands
  Read/write of display data, display ON/OFF, normal/reverse display, all dots ON/all dots OFF, set page address, set display start address, etc.
- Power supply voltage
  Logic power supply: V_{DD}-V_{SS} = 1.8 V to 5.5 V
  Voltage multiplier reference voltage: V_{IN}-V_{SS} = 1.8 V to V_{DD}
  (5-times multiplier → 1.8 V to 3.6 V, 6-times multiplier → 1.8 to 3 V, 7-times multiplier → 1.8 to 2.5 V)
  LCD drive voltage: V_{BI}-V_{SS} = 6.0 to 18 V
- Package: Gold bump chip, TCP

BLOCK DIAGRAM



PIN DESCRIPTION

Function	Pin name	Number of pins	I/O	Description
MPU Interface	D0 to D7	8	I/O	This is an 8-bit bi-directional data bus that can be connected to an 8-bit or 16-bit standard MPU data bus. When a serial interface is selected (P/$\overline{S}$ = "L"): D7: Serial data input pin (SI) D6: Serial clock input pin (SCL) In this case, D0 to D5 will be in the Hi-Z state. D0 to D7 will all be in the Hi-Z state when the chip select is in the inactive state.
	A0	1	I	Normally, the lowest bit of the MPU address bus is connected and used for distinguishing between data and commands. A0 = "H": Indicates that D0 to D7 are display data. A1 = "L": Indicates that D0 to D7 are control data.
	$\overline{RES}$	1	I	Initial setting is made by making $\overline{RES}$ = "L". The reset operation is made during the active level of the RES signal.
	$\overline{CS1}$ CS2	2	I	These are the chip select signals. The Chip Select of the LSI becomes active when $\overline{CS1}$ is "L" and also CS2 is "H" and allows the input/output of data or commands.
	$\overline{RD}$ (E)	1	I	The active level of this signal is "L" when connected to an 80-series MPU. This terminal is connected to the $\overline{RD}$ signal of the 80-series MPU, and the data bus of the ML9052 goes into the output state when this signal is "L". The active level of this signal is "H" when connected to a 68-series MPU. This pin will be the Enable and clock input pin when connected to a 68-series MPU.
	$\overline{WR}$ (R/$\overline{W}$)	1	I	The active level of this signal is "L" when connected to an 80-series MPU. This terminal is connected to the $\overline{WR}$ signal of the 80-series MPU. The signal on the data bus is latched into the ML9052 at the rising edge of the $\overline{WR}$ signal. When connected to a 68-series MPU, this pin becomes the input pin for the Read/Write control signal. R/$\overline{W}$ = "H": Read, R/$\overline{W}$ = "L": Write
	C86	1	I	This is the pin for selecting the MPU interface type. C86 = "H": 68-Series MPU interface. C86 = "L": 80-Series MPU interface.

<table>
<tr><th>Function</th><th>Pin name</th><th>Number of pins</th><th>I/O</th><th>Description</th></tr>
<tr><td>MPU Interface</td><td>P/$\overline{S}$</td><td>1</td><td>I</td><td>This is the pin for selecting parallel data input or serial data input.
P/$\overline{S}$ = "H": Parallel data input.
P/$\overline{S}$ = "L": Serial data input.
The pins of the LSI have the following functions depending on the state of P/$\overline{S}$ input.
<table>
<tr><th>P/$\overline{S}$</th><th>Data/command</th><th>Data</th><th>Read/Write</th><th>Serial clock</th></tr>
<tr><td>"H"</td><td>A0</td><td>D0 to D7</td><td>$\overline{RD}$, $\overline{WR}$</td><td rowspan="2">SCL (D6)</td></tr>
<tr><td>"L"</td><td>A0</td><td>SI (D7)</td><td>Write only</td></tr>
</table>
When P/$\overline{S}$ is "L", D0 to D5 will go into the Hi-Z state. In this condition, the data on the lines D0 to D5 can be "H", "L", or open. The pins $\overline{RD}$ (E) and $\overline{WR}$ (R/$\overline{W}$) should be tied to either the "H" level or the "L" level.
During serial data input, it is not possible to read the display data in the RAM.</td></tr>
<tr><td>Oscillator Circuit</td><td>CLS</td><td>1</td><td>I</td><td>This is the pin for selecting whether to enable or disable the internal oscillator circuit for the display clock.
CLS = "H": The internal oscillator circuit is enabled.
CLS = "L": The internal oscillator circuit is disabled (External input).
When CLS = "L", the display clock is input at the pin CL.</td></tr>
<tr><td>Display Timing Generator Circuit</td><td>M/$\overline{S}$</td><td>1</td><td>I</td><td>This is the pin for selecting whether master operation or slave operation is made towards the ML9052. During master operation, the synchronization with the LCD display system is achieved by inputting the timing signals necessary for LCD display.
M/$\overline{S}$ = "H": Master operation
M/$\overline{S}$ = "L": Slave operation
The functions of the different circuits and pins will be as follows depending on the states of M/$\overline{S}$ and CLS signals.
<table>
<tr><th>M/$\overline{S}$</th><th>CLS</th><th>Oscillator circuit</th><th>Power supply circuit</th><th>CL</th><th>FR</th><th>FRS</th><th>$\overline{DOF}$</th></tr>
<tr><td rowspan="2">"H"</td><td>"H"</td><td>Enabled</td><td>Enabled</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>"L"</td><td>Disabled</td><td>Enabled</td><td>Input</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td rowspan="2">"L"</td><td>"H"</td><td>Disabled</td><td>Disabled</td><td>Input</td><td>Input</td><td>Output</td><td>Input</td></tr>
<tr><td>"L"</td><td>Disabled</td><td>Disabled</td><td>Input</td><td>Input</td><td>Output</td><td>Input</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Function</th><th>Pin name</th><th>Number of pins</th><th>I/O</th><th>Description</th></tr>
<tr><td rowspan="4">Display Timing Generator Circuit</td><td>CL</td><td>1</td><td>I/O</td><td>This is the display clock input/output pin.
The function of this pin will be as follows depending on the states of $M/\overline{S}$ and CLS signals.
<table><tr><th>$M/\overline{S}$</th><th>CLS</th><th>CL</th></tr><tr><td rowspan="2">"H"</td><td>"H"</td><td>Output</td></tr><tr><td>"L"</td><td>Input</td></tr><tr><td rowspan="2">"L"</td><td>"H"</td><td>Input</td></tr><tr><td>"L"</td><td>Input</td></tr></table>When the ML9052 is used in the master/slave mode, the corresponding CL pin has to be connected.</td></tr>
<tr><td>FR</td><td>1</td><td>I/O</td><td>This is the input/output pin for LCD display frame reversal signal.
$M/\overline{S}$ = "H": Output
$M/\overline{S}$ = "L": Input
When the ML9052 is used in the master/slave mode, the corresponding FR pin has to be connected.</td></tr>
<tr><td>$\overline{DOF}$</td><td>1</td><td>I/O</td><td>This is the blanking control pin for the LCD display.
$M/\overline{S}$ = "H": Output
$M/\overline{S}$ = "L": Input
When the ML9052 is used in the master/slave mode, the corresponding $\overline{DOF}$ pin has to be connected.</td></tr>
<tr><td>FRS</td><td>1</td><td>O</td><td>This is the output pin for static drive.
This pin is used in combination with the FR pin.</td></tr>
<tr><td rowspan="5">Power Supply Circuit</td><td>IRS</td><td>1</td><td>I</td><td>This is the pin for selecting the resistor for adjusting the voltage V1.
IRS = "H": The internal resistor is used.
IRS = "L": The internal resistor is not used. The voltage V1 is adjusted using the external potential divider resistors connected to the pins VR.
This pin is effective only in the master operation. This pin is tied to the "H" or the "L" level during slave operation.</td></tr>
<tr><td>$\overline{HPM}$</td><td>1</td><td>I</td><td>This is the power control pin for the LCD drive power supply circuit.
$\overline{HPM}$ = "H": Normal mode
$\overline{HPM}$ = "L": High power mode
This pin is effective only during master operation mode. This pin is tied to the "H" or the "L" level during slave operation.</td></tr>
<tr><td>V_{DD}</td><td>13</td><td>—</td><td>This pin is tied to the MPU power supply terminal V_{CC}.</td></tr>
<tr><td>V_{SS}</td><td>9</td><td>—</td><td>This is the 0 V pin connected to the system ground (GND).</td></tr>
<tr><td>V_{IN}</td><td>4</td><td>—</td><td>This is the reference power supply of the voltage multiplier circuit for driving the LCD.</td></tr>
</table>

<table>
<tr><th>Function</th><th>Pin name</th><th>Number of pins</th><th>I/O</th><th>Description</th></tr>
<tr><td rowspan="7">Power Supply Circuit</td><td>V_{RS}</td><td>2</td><td>—</td><td>This is the external input VREG power supply for the LCD power supply voltage adjustment circuit.
This pin is effective only in the case of optional devices with the VREG external input option.</td></tr>
<tr><td>V_{OUT}</td><td>2</td><td>O</td><td>These are the output pins during voltage multiplication. Connect a capacitor between these pins and V_{SS}.</td></tr>
<tr><td>V1
V2
V3
V4
V5</td><td>10</td><td>—</td><td>These are the multiple level power supply pins for the LCD power supply. The voltages specified for the LCD cells are applied to these pins after resistor network voltage division or after impedance transformation using operational amplifiers. The voltages are specified taking V_{SS} as the reference, and the following relationship should be maintained among them.
$V1 \geq V2 \geq V3 \geq V4 \geq V5 \geq V_{SS}$
Master operation: When the power supply is ON, the following voltages are applied to V2 to V5 from the built-in power supply circuit. The selection of voltages is determined by the LCD bias set command.
<table>
<tr><th></th><th colspan="2">ML9052</th></tr>
<tr><td>V2</td><td>10/11 × V1</td><td>8/9 × V1</td></tr>
<tr><td>V3</td><td>9/11 × V1</td><td>7/9 × V1</td></tr>
<tr><td>V4</td><td>2/11 × V1</td><td>2/9 × V1</td></tr>
<tr><td>V5</td><td>1/11 × V1</td><td>1/9 × V1</td></tr>
</table></td></tr>
<tr><td>VR</td><td>2</td><td>I</td><td>Voltage adjustment pins. Voltages between V1 and V_{SS} are applied using a resistance voltage divider.
These pins are effective only when the internal resistors for voltage V1 adjustment are not used (IRS = "L").
Do not use these pins when the internal resistors for voltage V1 adjustment are used (IRS = "H").</td></tr>
<tr><td>VC1+</td><td>2</td><td>O</td><td>These are the pins for connecting the positive side of the capacitors for voltage multiplication.
Connect capacitors between VS1– and these pins.</td></tr>
<tr><td>VS1–</td><td>2</td><td>O</td><td>These are the pins for connecting the negative side of the capacitors for voltage multiplication.
Connect capacitors between these pins and VC1+, VC3+, and VC5+.</td></tr>
<tr><td>VC2+</td><td>2</td><td>O</td><td>These are the pins for connecting the positive side of the capacitors for voltage multiplication.
Connect capacitors between VS2– and these pins.</td></tr>
</table>

<table>
<tr><th>Function</th><th>Pin name</th><th>Number of pins</th><th>I/O</th><th>Description</th></tr>
<tr><td rowspan="5">Power Supply Circuit</td><td>VS2–</td><td>2</td><td>O</td><td>These are the pins for connecting the negative side of the capacitors for voltage multiplication.
Connect capacitors between these pins and VC2+, VC4+, and VC6+ (during 7-times voltage multiplication).</td></tr>
<tr><td>VC3+</td><td>2</td><td>O</td><td>These are the pins for connecting the positive side of the capacitors for voltage multiplication.
Connect capacitors between VS1– and these pins.</td></tr>
<tr><td>VC4+</td><td>2</td><td>O</td><td>These are the pins for connecting the positive side of the capacitors for voltage multiplication.
Connect capacitors between VS2– and these pins.</td></tr>
<tr><td>VC5+</td><td>2</td><td>O</td><td>These are the pins for connecting the positive side of the capacitors for voltage multiplication.
Connect capacitors between VS1– and these pins.</td></tr>
<tr><td>VC6+</td><td>2</td><td>O</td><td>These are the pins for connecting the positive side of the capacitors for voltage multiplication.
Connect capacitors between VS2– and these pins (during 7-times voltage multiplication).
For 6-times voltage multiplication, connect these pins to the V_{OUT} pin.</td></tr>
<tr><td rowspan="2">LCD Drive Output</td><td>SEG0 to SEG131</td><td>132</td><td>O</td><td>These are the LCD segment drive outputs.
One of the levels among V1, V3, V4, and V_{SS} is selected depending on the combination of the display RAM content and the FR signal.
<table>
<tr><th rowspan="2">RAM Data</th><th rowspan="2">FR</th><th colspan="2">Output voltage</th></tr>
<tr><th>Normal display</th><th>Reverse display</th></tr>
<tr><td>H</td><td>H</td><td>V1</td><td>V3</td></tr>
<tr><td>H</td><td>L</td><td>V_{SS}</td><td>V4</td></tr>
<tr><td>L</td><td>H</td><td>V3</td><td>V1</td></tr>
<tr><td>L</td><td>L</td><td>V4</td><td>V_{SS}</td></tr>
<tr><td>Power save</td><td>—</td><td colspan="2">V_{SS}</td></tr>
</table></td></tr>
<tr><td>COM0 to COM95</td><td>96</td><td>O</td><td>These are the LCD common drive outputs.
One of the levels among V1, V2, V5, and V_{SS} is selected depending on the combination of the scan data and the FR signal.
<table>
<tr><th>Scan data</th><th>FR</th><th>Output voltage</th></tr>
<tr><td>H</td><td>H</td><td>V_{SS}</td></tr>
<tr><td>H</td><td>L</td><td>V1</td></tr>
<tr><td>L</td><td>H</td><td>V2</td></tr>
<tr><td>L</td><td>L</td><td>V5</td></tr>
<tr><td>Power save</td><td>—</td><td>V_{SS}</td></tr>
</table></td></tr>
</table>

Function	Pin name	Number of pins	I/O	Description
LCD Drive Output	COMS	2	O	These are the COM output pins only for indicators. Both pins output the same signal. Leave these pins open when they are not used. The same signal is output in both master and slave operation modes.
Test Pin	TEST0		I	These are the pins for testing the IC chip. Leave these pins open during normal use.
	TEST1		O	

FUNCTIONAL DESCRIPTION

MPU Interface

• Selection of interface type

The ML9052 carries out data transfer using either the 8-bit bi-directional data bus (D7 to D0) or the serial data input line (SI). Either the 8-bit parallel data input or serial data input can be selected as shown in Table 1 by setting the P/$\overline{\text{S}}$ pin to the "H" or the "L" level.

Table 1

P/$\overline{\text{S}}$	$\overline{\text{CS1}}$	CS2	A0	$\overline{\text{RD}}$	$\overline{\text{WR}}$	C86	D7	D6	D5 to D0
H: Parallel Input	$\overline{\text{CS1}}$	CS2	A0	$\overline{\text{RD}}$	$\overline{\text{WR}}$	C86	D7	D6	D5 to D0
L: Serial Input	$\overline{\text{CS1}}$	CS2	A0	—	—	—	SI	SCL	(HZ)

A hyphen (—) indicates that the pin can be tied to the "H" or the "L" level.

• Parallel interface

When the parallel interface is selected, (P/$\overline{\text{S}}$ = "H"), it is possible to connect this LSI directly to the MPU bus of either an 80-series MPU or a 68-series MPU as shown in Table 2 depending on whether the pin C86 is set to the "H" or "L".

Table 2

P/$\overline{\text{S}}$	$\overline{\text{CS1}}$	CS2	A0	$\overline{\text{RD}}$	$\overline{\text{WR}}$	D7 to D0
H: 68-Series MPU Bus	$\overline{\text{CS1}}$	CS2	A0	E	R/$\overline{\text{W}}$	D7 to D0
L: 80-Series MPU Bus	$\overline{\text{CS1}}$	CS2	A0	$\overline{\text{RD}}$	$\overline{\text{WR}}$	D7 to D0

The data bus signals are identified as shown in Table 3 below depending on the combination of the signals A0, $\overline{\text{RD}}$(E), and $\overline{\text{WR}}$(R/$\overline{\text{W}}$) of Table 2.

Table 3

	Common	68-Series	80-Series	
	A0	R/$\overline{\text{W}}$	$\overline{\text{RD}}$	$\overline{\text{WR}}$
Display Data Read	1	1	0	1
Display Data Write	1	0	1	0
Status Read	0	1	0	1
Control Data Write (command)	0	0	1	0

Serial interface

When the serial interface is selected ($P/\overline{S}$ = "L"), the serial data input (SI) and the serial clock input (SCL) can be accepted if the chip is in the active state ($\overline{CS1}$ = "L" and CS2 = "H"). The serial interface consists of an 8-bit shift register and a 3-bit counter. The serial data is read in from the serial data input pin in the sequence D7, D6, ... , D0 at the rising edge of the serial clock input, and is converted into parallel data at the rising edge of the 8th serial clock pulse and processed further. The identification of whether the serial data is display data or command is judged based on the A0 input, and the data is treated as display data when A0 is "H" and as command when A0 is "L". The A0 input is read in and identified at the rising edge of the ($8 \times n$) th serial clock pulse after the chip has become active. Fig. 1 shows the signal chart of the serial interface. (When the chip is not active, the shift register and the counter are reset to their initial states. No data read out is possible in the case of the serial interface. It is necessary to take sufficient care about wiring termination reflection and external noise in the case of the SCL signal. We recommend verification of operation in an actual unit.)

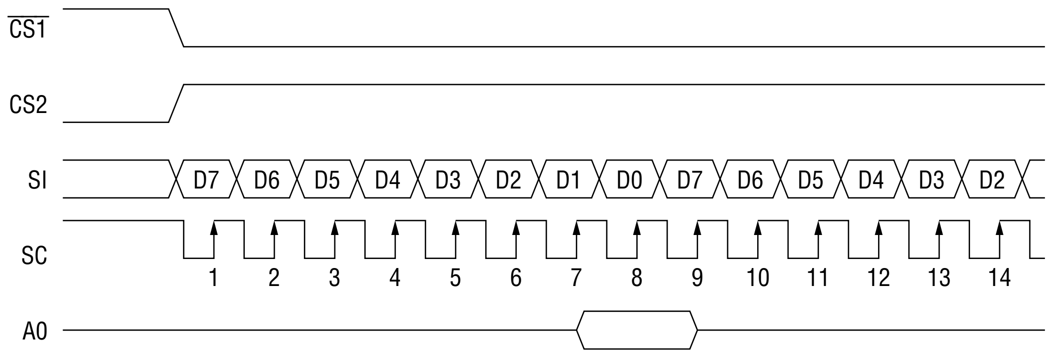


Figure 1

• Chip select

The ML9052 has the two chip select pins $\overline{CS1}$ and CS2, and the MPU interface or the serial interface is enabled only when $\overline{CS1}$ = "L" and CS2 = "H". When the chip select signals are in the inactive state, the D0 to D7 lines will be in the high impedance state and the inputs A0, $\overline{RD}$, and $\overline{WR}$ will not be effective. When the serial interface has been selected, the shift register and the counter are reset when the chip select signals are in the inactive state.

• Accessing the display data RAM and the internal registers

Accessing the ML9052 from the MPU side requires merely that the cycle time (t_{CYC}) be satisfied, and high speed data transfer without requiring any wait time is possible. Also, during the data transfer with the MPU, the ML9052 carries out a type of pipeline processing between LSIs via a bus holder associated with the internal data bus. For example, when the MPU writes data in the display data RAM, the data is temporarily stored in the bus holder, and is then written into the display data RAM before the next data read cycle. Further, when the MPU reads out data in the display data RAM, first a dummy data read cycle is carried out to temporarily store the data in the bus holder which is then placed on the system bus and is read out during the next read cycle. There is a restriction on the read sequence of the display data RAM, which is that the read instruction immediately after setting the address does not read out the data of that address, but that data is output as the data of the address specified during the second data read sequence, and hence care should be taken about this during reading. Therefore, always one dummy read is necessary immediately after setting the address or after a write cycle. This relationship is shown in Figs 2(a) and 2(b).

• Data write

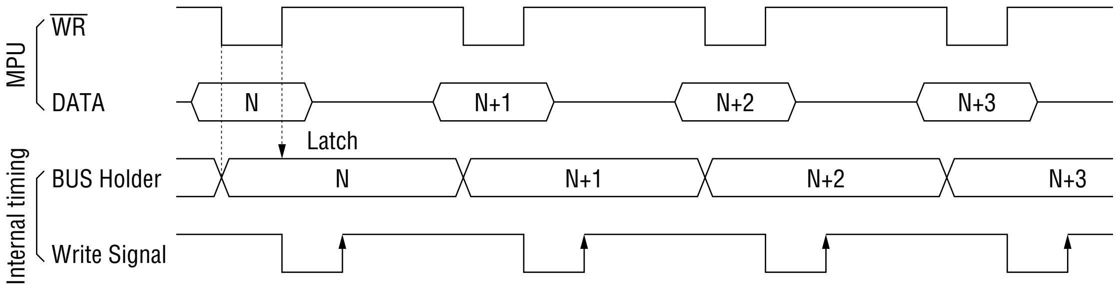


Figure 2(a)

• Data read

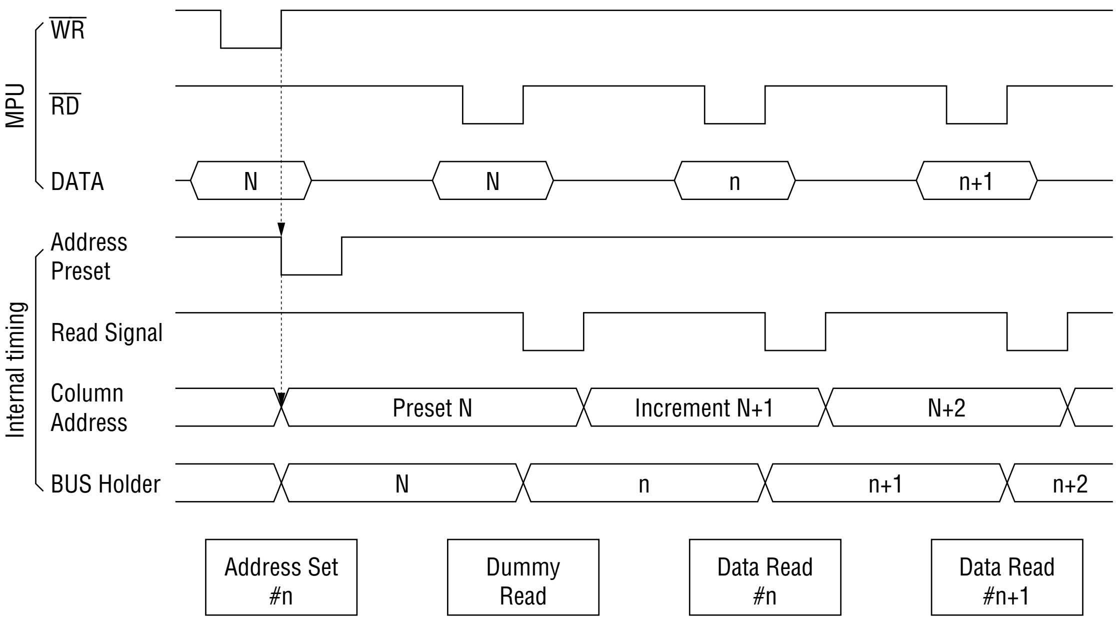


Figure 2(b)

• Busy flag

The busy flag being "1" indicates that the ML9052 is carrying out internal operations, and hence no instruction other than a status read instruction is accepted during this period. The busy flag is output at pin D7 when a status read instruction is executed. If the cycle time (t_{CYC}) is established, there is no need to check this flag before issuing every command and hence the processing performance of the MPU can be increased greatly.

Display data RAM

• Display data RAM

This is the RAM storing the dot data for display and has an organization of 97 (12 pages × 8 bits +1) × 132 bits. It is possible to access any required bit by specifying the page address and the column address. Since the display data D7 to D0 from the MPU correspond to the LCD display in the direction of the common lines as shown in Fig. 3, there are fewer restrictions during display data transfer when the ML9052 is used in a multiple chip configuration, thereby making it easily possible to implement a display with a high degree of freedom. Also, since the display data RAM read/write from the MPU side is carried out via an I/O buffer, it is done independently of the signal read operation for the LCD drive. Consequently, the display is not affected by flickering, etc., even when the display data RAM is accessed asynchronously during the LCD display operation.

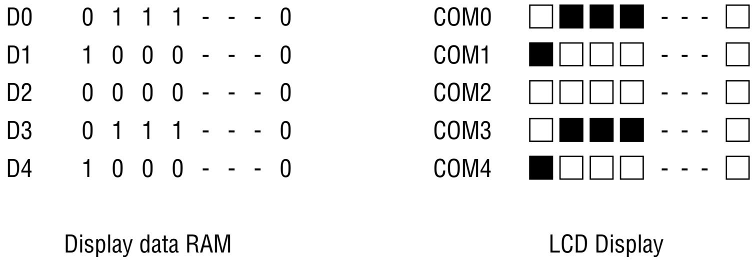


Figure 3

• Page address circuit

The page address of the display data RAM is specified using the page address set command as shown in Fig. 4. Specify the page address again when accessing after changing the page. The page address 12 (D3, D2, D1, D0 → 1, 1, 0, 0) is the RAM area dedicated to the indicator, and only the display data D0 is valid in this page.

• Column address circuit

The column address of the display data RAM is specified using the column address set command as shown in Fig. 4. Since the specified column address is incremented (by +1) every time a display data read/write command is issued, the MPU can access the display data continuously. Further, the incrementing of the column address is stopped at the column address of 83H. Since the column address and the page address are independent of each other, it is necessary, for example, to specify separately the new page address and the new column address when changing from column 83H of page 0 to column 00H of page 1. Also, as is shown in Table 4, it is possible to reverse the correspondence relationship between the display data RAM column address and the segment output using the ADC command (the segment driver direction select command). This reduces the IC placement restrictions at the time of assembling LCD modules.

Table 4

ADC	SEG Output SEG0 → SEG131
D0 = "0"	0(H) → Column Address → 83(H)
D0 = "1"	83(H) ← Column Address ← 0(H)

• Line address circuit

The line address circuit is used for specifying the line address corresponding to the COM output when displaying the contents of the display data RAM as is shown in Fig. 4. Normally, the topmost line in the display (COM0 output in the normal display state of the common output, and COM95 output in the reverse display stage) is specified using the display start line address set command. The display area is 97 lines in the direction of increasing line address from the specified display start line address. It is possible to carry out screen scrolling and page changing by dynamically changing the line address using the display start line address set command.

• Display data latch circuit

The display data latch circuit is a latch for temporarily storing the data from the display data RAM before being output to the LCD drive circuits. Since the commands for selecting normal/ reverse display and turning the display ON/OFF control the data in this latch, the data in the display data RAM will not be changed.

Oscillator circuit

This is an RC oscillator that generates the display clock. The oscillator circuit is effective only when M/$\overline{S}$ = "H" and also CLS = "H". The oscillations will be stopped when CLS = "L", and the display clock has to be input to the CL pin.

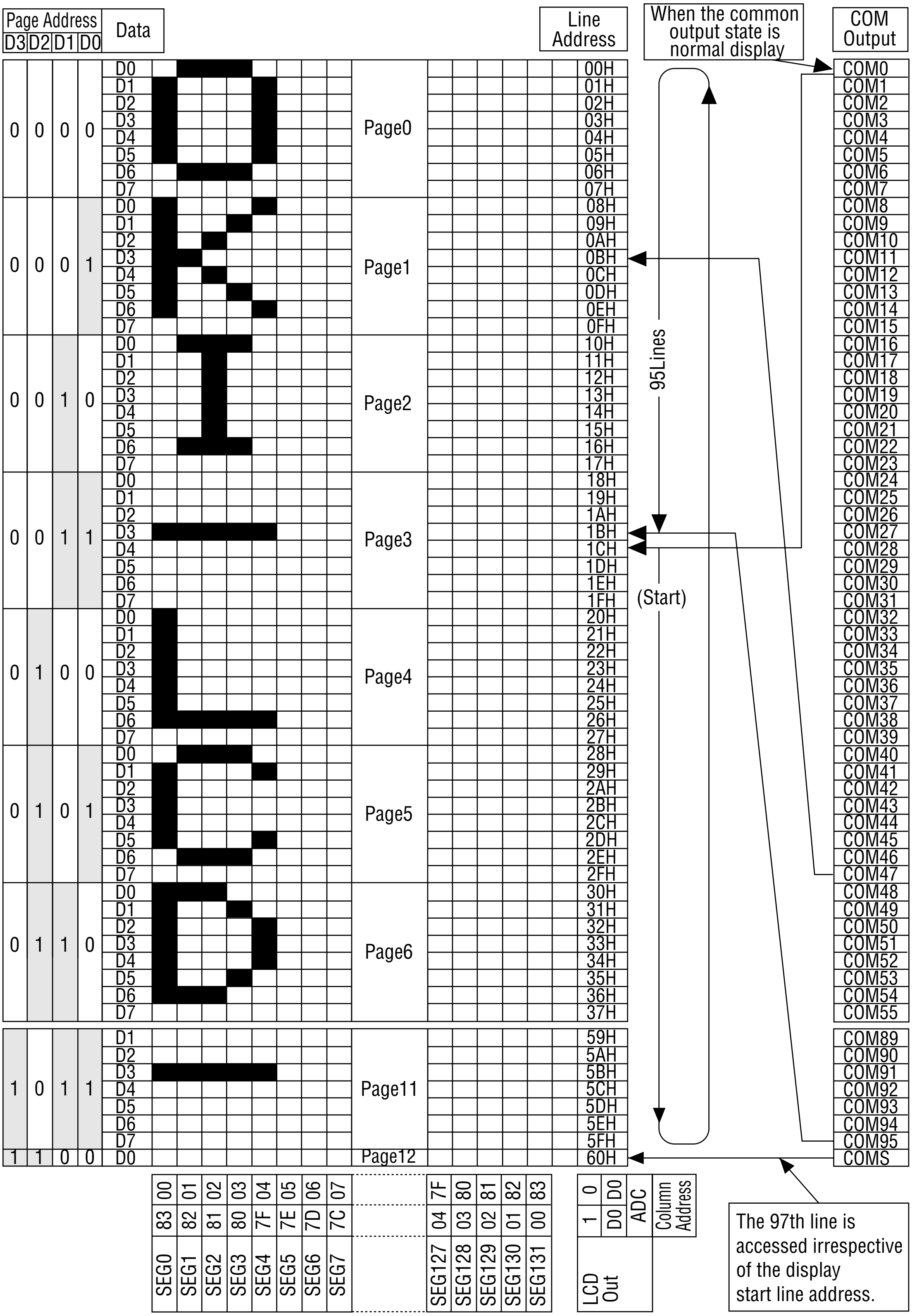

Page Address
D3 D2 D1 D0
Data
Line Address
When the common output state is normal display
COM Output
Page0
Page1
Page2
Page3
Page4
Page5
Page6
Page11
Page12
95Lines
(Start)
COMS
ADC
Column Address
LCD Out
The 97th line is accessed irrespective of the display start line address.

Figure 4

Display timing generator circuit

This circuit generates the timing signals for the line address circuit and the display data latch circuit from the display clock. The display data is latched in the display data latch circuit and is output to the segment drive output pins in synchronization with the display clock. This circuit generates the timing signals for the line address circuit and the display data latch circuit from the display clock. The display data is latched in the display data latch circuit and is output to the segment drive output pins in synchronization with the display clock. The read out of the display data to the LCD drive circuits is completely independent of the display data RAM access from the MPU. As a result, there is no bad influence such as flickering on the display even when the display data RAM is accessed asynchronously during the LCD display. Also, the internal common timing and LCD frame reversal (FR) signals are generated by this circuit from the display clock. The drive waveforms of the frame inversion drive method shown in Fig. 5(a) for the LCD drive circuits are generated by this circuit. Further, the drive waveforms of the line inversion method shown in Fig. 5(b) can also be generated depending on the issued command.

In the line inversion drive method, it is possible to carry out reverse display drive at every line to a maximum of 32 lines. Fig. 5(b) shows the waveforms of the 1 line inversion drive method.

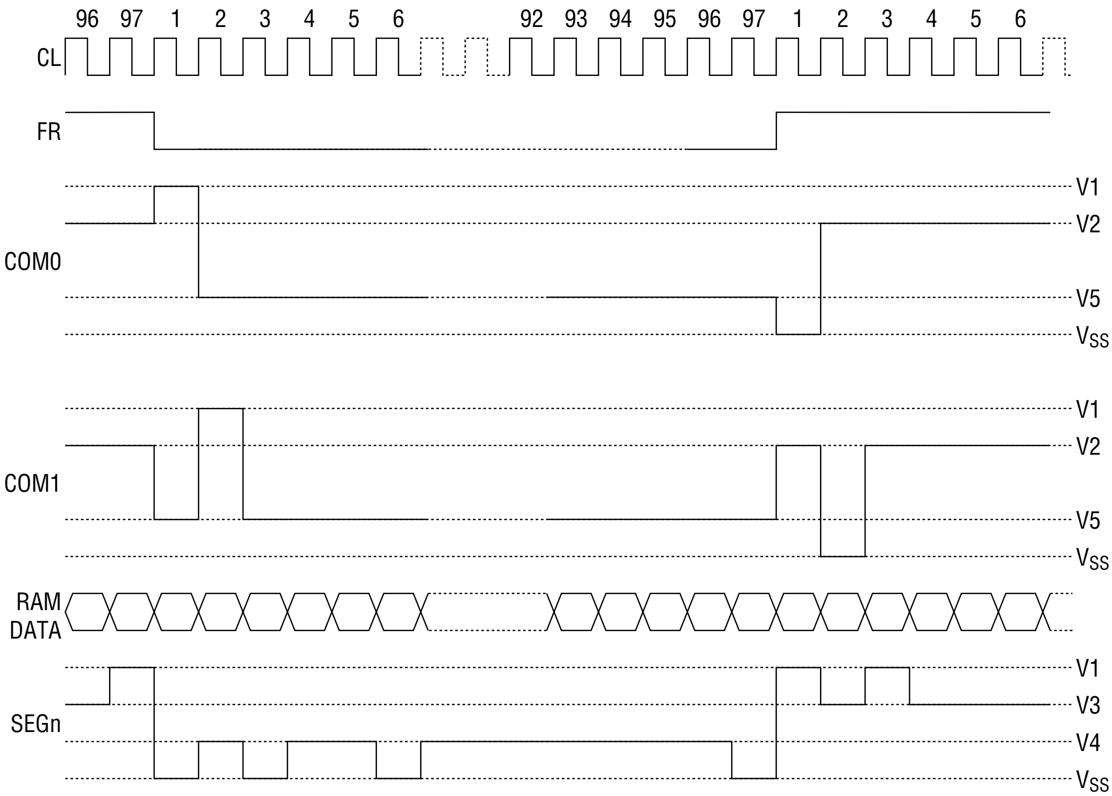


Figure 5(a) Waveforms in the frame inversion drive method

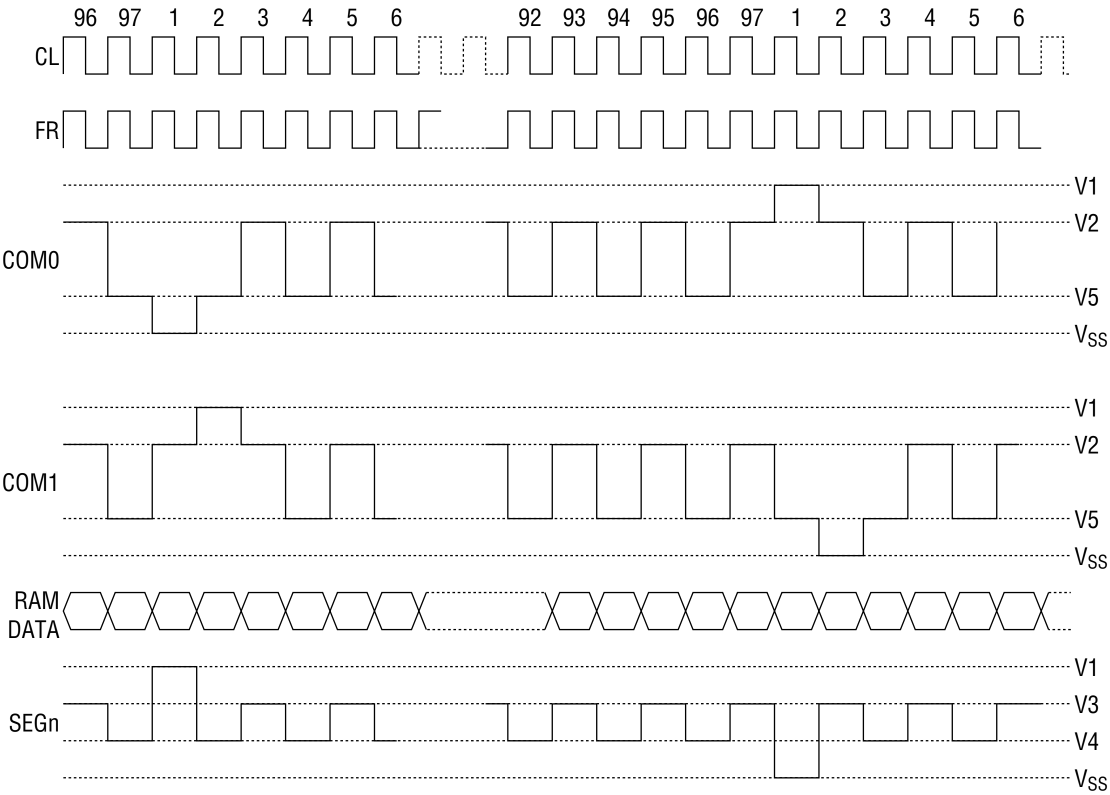


Figure 5(b) Waveforms in the line inversion drive method

When the ML9052 is used in a multiple chip configuration, it is necessary to supply the slave side display timing signals (FR, CL, and $\overline{\text{DOF}}$) from the master side.
The statuses of the signals FR, CL, and $\overline{\text{DOF}}$ are shown in Table 5.

Table 5

Operating mode		FR	CL	$\overline{\text{DOF}}$
Master Mode (M/$\overline{\text{S}}$ = "H")	Internal oscillator circuit enabled (CLS = H)	Output	Output	Output
	Internal oscillator circuit disabled (CLS = L)	Output	Input	Output
Slave Mode (M/$\overline{\text{S}}$ = "L")	Internal oscillator circuit enabled (CLS = H)	Input	Input	Input
	Internal oscillator circuit disabled (CLS = L)	Input	Input	Input

Common output state selection circuit (see Table 6)

Since the COM output scanning directions can be set using the common output state selection command in the ML9052, it is possible to reduce the IC placement restrictions at the time of assembling LCD modules.

Table 6

State	COM Scanning direction
Normal Display	COM0 → COM95
Reverse Display	COM95 → COM0

LCD Drive circuits

This LSI incorporates 229 sets of multiplexers that generate 4-level outputs for driving the LCD. These output the LCD drive voltage in accordance with the combination of the display data, COM scanning signals, and the FR signal. Fig. 6 shows examples of the SEG and COM output waveforms in the frame inversion drive method.

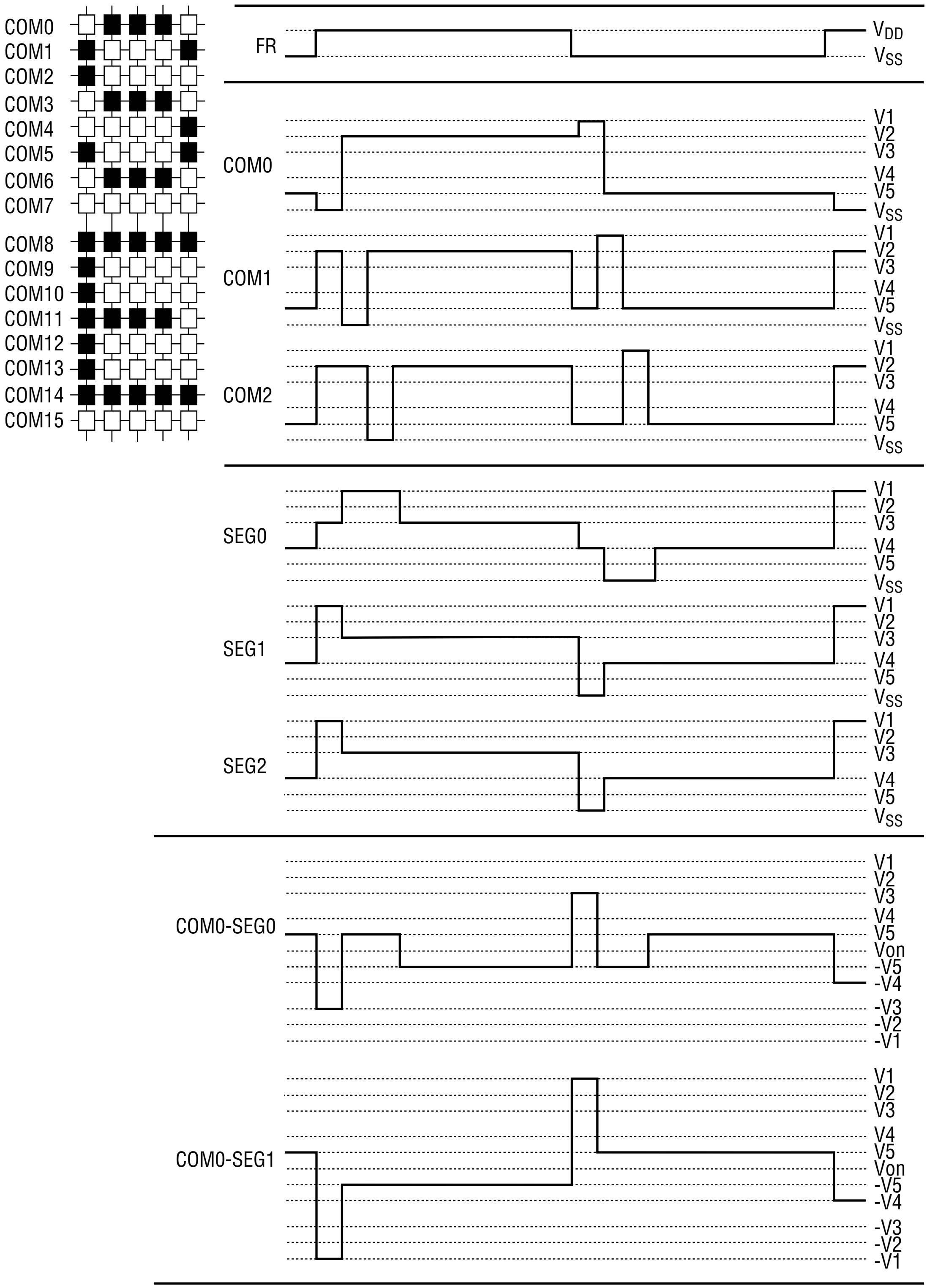

COM0
COM1
COM2
COM3
COM4
COM5
COM6
COM7
COM8
COM9
COM10
COM11
COM12
COM13
COM14
COM15
FR
VDD
VSS
COM0
COM1
COM2
SEG0
SEG1
SEG2
V1
V2
V3
V4
V5
VSS
COM0-SEG0
COM0-SEG1
Von
-V5
-V4
-V3
-V2
-V1

Figure 6

Power supply circuit

This is the low power consumption type power supply circuit for generating the voltages necessary for driving LCD devices, and consists of voltage multiplier circuits, voltage adjustment circuits, and voltage follower circuits. This circuit is effective only when the ML9052 serves as a master device. In the power supply circuit, it is possible to control the ON/OFF of each of the circuits of the voltage multiplier, voltage adjustment circuits, and voltage follower circuits using the power control set command. As a result, it is also possible to use parts of the functions of both the external power supply and the internal power supply. Table 7 shows the functions controlled by the 3-bit data of the power control set command and Table 8 shows a sample combination.

Table 7 Details of functions controlled by the bits of the power control set command

Control bit	Function controlled by the bit
D2	Voltage multiplier circuit control bit
D1	Voltage adjustment circuit (V adjustment circuit) control bit
D0	Voltage follower circuit (V/F circuit) control bit

Table 8 Sample combination for reference

State used	D2	D1	D0	Circuit			External voltage input	Voltage multiplier pins *1
				Voltage multiplier	V Adjustment	V/F		
Only the internal power supply is used	1	1	1	○	○	○	V_{IN}	Used
Only V adjustment and V/F circuits are used	0	1	1	×	○	○	V_{OUT}, V_{IN}	OPEN
Only V/F circuits are used	0	0	1	×	×	○	V1, V_{IN}	OPEN
Only the external power supply is used	0	0	0	×	×	×	V1 to V5	OPEN

*1: The voltage multiplier pins are the pins VC1+, VS1-, VC2+, VS2-, VC3+, VC4+, VC5+, and VC6+.
Although combinations other than the above can also be used, they are not recommended because they do not represent realistic methods of use.

• Voltage multiplier circuit

Using the voltage multiplier circuits incorporated in the ML9052, it is possible to carry out 7-times voltage multiplication and 6-times voltage multiplication of the voltage difference V_{IN}-V_{SS}.

7-Times multiplication

The voltage difference V_{IN} - V_{SS} is multiplied 7 times in the positive side and output at the V_{OUT} pin if capacitors (C) are connected between the pin pairs VS1- & VC1+, VS2- & VC2+, VS1- & VC3+, VS2- & VC4+, VS1- & VC5+, VS2- & VC6+, and V_{OUT} & V_{SS}.

6-Times multiplication

The voltage difference V_{IN} - V_{SS} is multiplied 6 times in the positive side and output at the V_{OUT} pin if capacitors (C) are connected between the pin pairs VS1- & VC1+, VS2- & VC2+, VS1- & VC3+, VS2- & VC4+, VS1- & VC5+, and V_{OUT} & V_{SS}, and shorting the pins VC6+ and V_{OUT}.

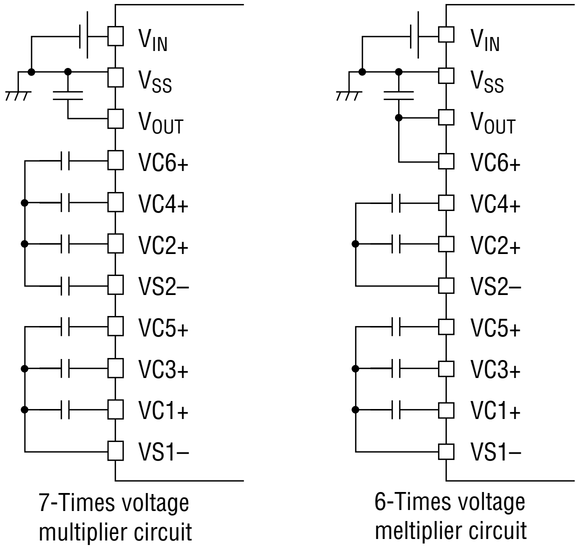


Figure 7

The voltage relationships in voltage multiplication are shown in Fig. 8.

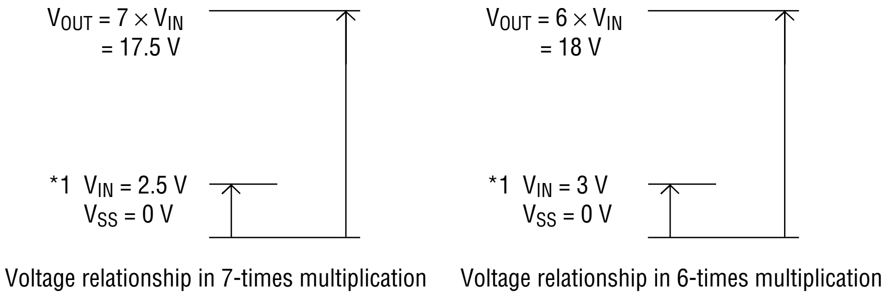


Figure 8

*1: The voltage range of V_{IN} should be set so that the voltage at the pin V_{OUT} does not exceed the absolute maximum rating.

• Voltage adjustment circuit

The voltage multiplier output V_{OUT} produces the LCD drive voltage V1 via the voltage adjustment circuit. Since the ML9052 incorporates a high accuracy constant voltage generator, a 64-level electronic potentiometer function, and also resistors for voltage V1 adjustment, it is possible to build a high accuracy voltage adjustment circuit with very few components. In addition, the ML9052 is available in three models with the temperature gradients of - (1) about -0.11%/℃, (2) about -0.3%/℃, and (3) external input (input to pin VRS), as a VREG option.

(a) When the internal resistors for voltage V1 adjustment are used

It is possible to control the LCD power supply voltage V1 and adjust the intensity of LCD display using commands and without needing any external resistors, if the internal voltage V1 adjustment resistors and the electronic potentiometer function are used. The voltage V1 can be obtained by the following equation A-1 in the range of $V1<V_{OUT}$.

$V1 = (1+(Rb/Ra)) \bullet VEV = (1+(Rb/Ra)) \bullet (1-(\alpha/162)) \bullet VREG$ (Eqn. A-1)

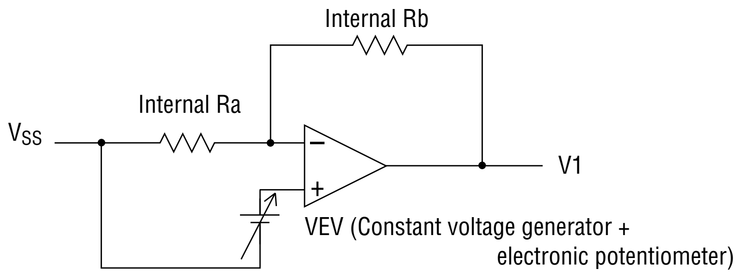


Figure 9

VREG is a constant voltage generated inside the IC and its value is constant as given in Table 9 at Ta = 25℃.

Table 9

Model	Temperature gradient	Unit	VREG	Unit
(1) Internal Power Supply	–0.11	[%/℃]	3.0	[V]
(2) Internal Power Supply	–0.3	[%/℃]	3.0	[V]
(3) External Input	—	—	VRS	[V]

Here, α is the electronic potentiometer function which allows one level among 64 levels to be selected by merely setting the data in the 6-bit electronic potentiometer register. The values of α set by the electronic potentiometer register are shown in Table 10.

Table 10

α	D5	D4	D3	D2	D1	D0
63	0	0	0	0	0	0
62	0	0	0	0	0	1
61	0	0	0	0	1	0
1	1	1	1	1	1	0
0	1	1	1	1	1	1

Rb/Ra is the voltage V1 adjustment internal resistor ratio and can be adjusted to one of 8 levels by the voltage V1 adjustment internal resistor ratio set command. The reference values of the ratio (1+Rb/Ra) according to the 3-bit data set in the voltage V1 adjustment internal resistor ratio setting register are listed in Table 11.

Table 11 Voltage V1 adjustment internal resistor ratio setting register values and the ratio (1+Rb/Ra) (For reference)

Register value			Temperature gradient of the model [unit: %/°C]		
D2	**D1**	**D0**	**–0.11**	**–0.3**	**VREG *1**
0	0	0	3.0	3.0	1.5
0	0	1	3.5	3.5	2.0
0	1	0	4.0	4.0	2.5
0	1	1	4.5	4.5	3.0
1	0	0	5.0	5.0	3.5
1	0	1	5.5	5.5	4.0
1	1	0	6.0	6.0	4.5
1	1	1	6.4	6.4	5.0

*1: VREG is the external input.

(b) When external resistors are used (voltage V1 adjustment internal resistors are not used) - Case 1

It is also possible to set the LCD drive power supply voltage V1 without using the internal resistors for voltage V1 adjustment but connecting external resistors (Ra' and Rb') between V_{SS} & VR and between VR & V1. Even in this case, it is possible to control the LCD power supply voltage V1 and adjust the intensity of LCD display using commands if the electronic potentiometer function is used.

The voltage V1 can be obtained by the following equation B-1 in the range of $V1 < V_{OUT}$ by setting the external resistors Ra' and Rb' appropriately.

V1 = (1+(Rb'/Ra')) • VEV = (1+(Rb'/Ra')) • (1–(α/162)) • VREG (Eqn. B-1)

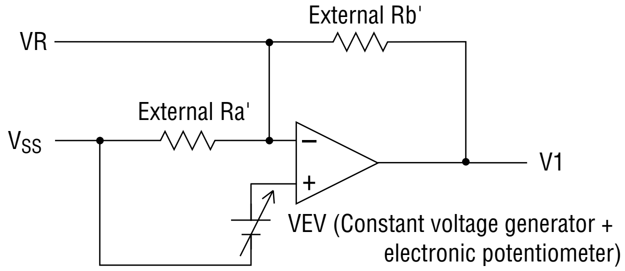


Figure 10

Setting example: Setting V1 = 7 V at Ta = 25°C using an ML9052 of the model with a temperature gradient of -0.11%/°C.

When the electronic potentiometer register value is set to the middle value of (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0), the value of α will be 31 and that of VREG will be 3.0 V, and hence the equation B-1 becomes as follows:

V1 = (1+(Rb'/Ra')) • (1–(α/162)) • VREG

7 = (1+(Rb'/Ra')) • (1–(31/162)) • 3.0 (Eqn. B-2)

Further, if the current flowing through Ra' and Rb' is set as 5 µA, the value of Ra'+Rb' will be -

Ra'+Rb' = 1.4 MΩ (Eqn. B-3)

and hence,

Rb'/Ra' = 1.89, Ra' = 485 kΩ, Rb' = 915 kΩ.

In this case, the variability range of voltage V1 using the electronic potentiometer function and the increment size will be as given in Table 12.

Table 12

V1	Min.	Typ.	Max.	Unit
Variability range	5.3 (level 0)	7.0 (center value)	8.6 (level 63)	[V]
Increment size		52		[mV]

(c) When external resistors are used (voltage V1 adjustment internal resistors are not used) - Case 2
It is possible to set the LCD drive power supply voltage V1 using fine adjustment of Ra' and Rb' by adding a variable resistor to the case of using external resistors in the above case. Even in this case, it is possible to control the LCD power supply voltage V1 and adjust the intensity of LCD display using commands if the electronic potentiometer function is used.
The voltage V1 can be obtained by the following equation C-1 in the range of $V1<V_{OUT}$ by setting the external resistors R_1, R_2 (variable resistor), and R_3 appropriately and making fine adjustment of R_2 (ΔR_2).
$V1 = (1+(R_3+R_2-\Delta R_2)/(R_1+\Delta R_2)) \bullet VEV$
$= (1+(R_3+R_2-\Delta R_2)/(R_1+\Delta R_2)) \bullet (1-(\alpha/162)) \bullet VREG$ (Eqn. C-1)

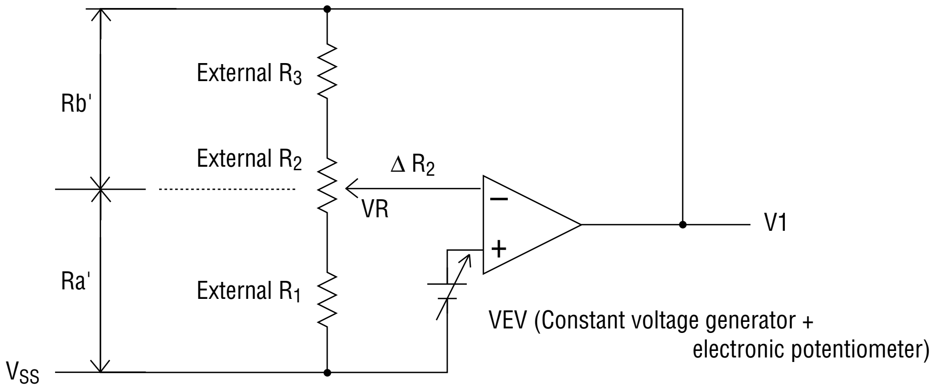


Figure 11

Setting example: Setting V1 in the range 5 V to 9 V using R_2 at Ta = 25°C using an ML9052 of the model with a temperature gradient of -0.11%/°C.

When the electronic potentiometer register value is set to the middle value of (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0), the value of α will be 31 and that of VREG will be 3.0 V, and hence in order to make V1 = 9 V when $\Delta R_2 = 0\ \Omega$, the equation C-1 becomes as follows:
$9 = (1+(R_3+R_2)/R_1) \bullet (1-(31/162)) \bullet (3.0)$ (Eqn. C-2)
In order to make V1 = 5 V when $\Delta R_2 = R_2$,
$5 = (1+R_3/(R_1+R_2)) \bullet (1-(31/162)) \bullet (3.0)$ (Eqn. C-3)
Further, if the current flowing between V_{SS} and V1 is set as 5 μA, the value of $R_1+R_2+R_3$ becomes-
$R_1+R_2+R_3 = 1.4\ M\Omega$ (Eqn. C-4)
and hence,
$R_1 = 490\ k\Omega$, $R_2 = 380\ k\Omega$, $R_3 = 930\ k\Omega$.
In this case, the variability range of voltage V1 using the electronic potentiometer function and the increment size will be as given in Table 13.

Table 13

V1	Min.	Typ.	Max.	Unit
Variability range	5.3 (level 0)	7.0 (center value)	8.7 (level 63)	[V]
Increment size		53		[mV]

* When using the voltage V1 adjustment internal resistors or the electronic potentiometer function, it is necessary to set at least the voltage adjustment circuit and the voltage follower circuits both in the operating state using the power control setting command. Also, when the voltage multiplier circuit is OFF, it is necessary to supply a voltage externally to the V_{OUT} pin.
* The pin VR is effective only when the voltage V1 adjustment internal resistors are not used (pin IRS = "L"). Leave this pin open when the voltage V1 adjustment internal resistors are being used (pin IRS = "H").
* Since the input impedance of the pin VR is high, it is necessary to take noise countermeasures such as using a short wire or shielded wire .

• LCD Drive voltage generator circuits
The voltage V1 is divided using resistors inside the IC to generate the voltages V2, V3, V4, and V5 that are necessary for driving the LCD. In addition, these voltages V2, V3, V4, and V5 are impedance transformed using voltage follower circuits and fed to the LCD drive circuits. The bias ratios of 1/11 or 1/9 can be selected in the ML9052 using the LCD bias setting command.

• High power mode
The power supply circuit incorporated in the ML9052 has an extremely low power consumption. [Normal mode: $\overline{HPM}$ = "H"]. Hence, in the case of an LCD device or panel with a large load, the display quality may become poorer. In such a case, setting the $\overline{HPM}$ pin to "L" (high power mode) can improve the quality of display. It is recommended to verify the display using an actual unit in order to decide whether or not to use this mode. Further, if the degree of display quality improvement is still not sufficient even after setting the high power mode, it is necessary to supply the LCD drive power supply from an external source.

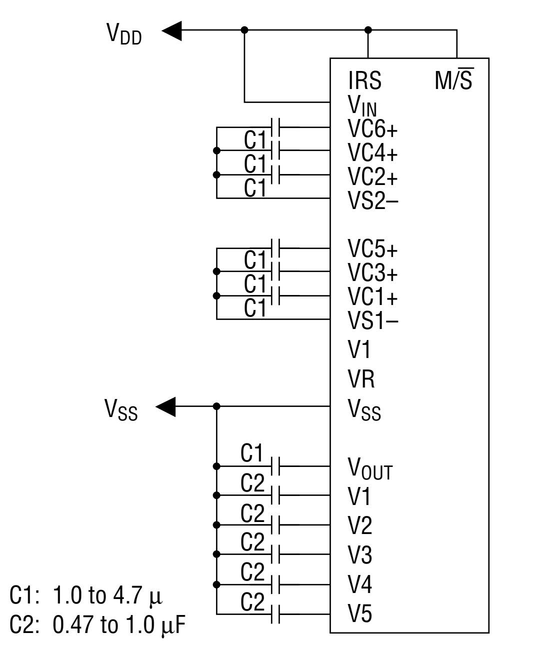
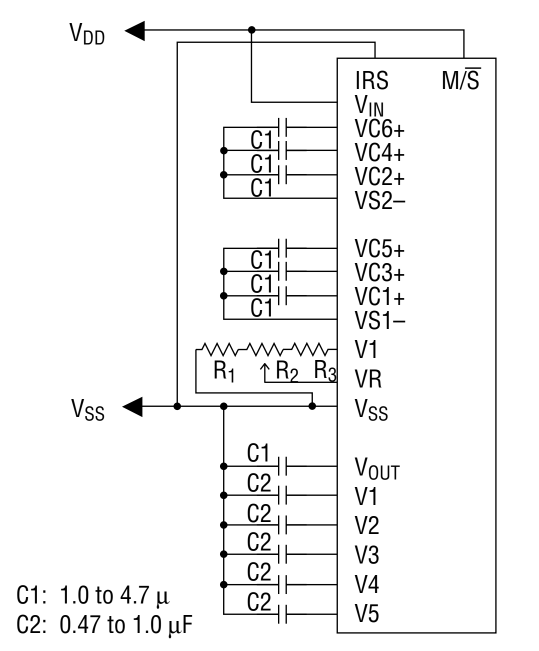
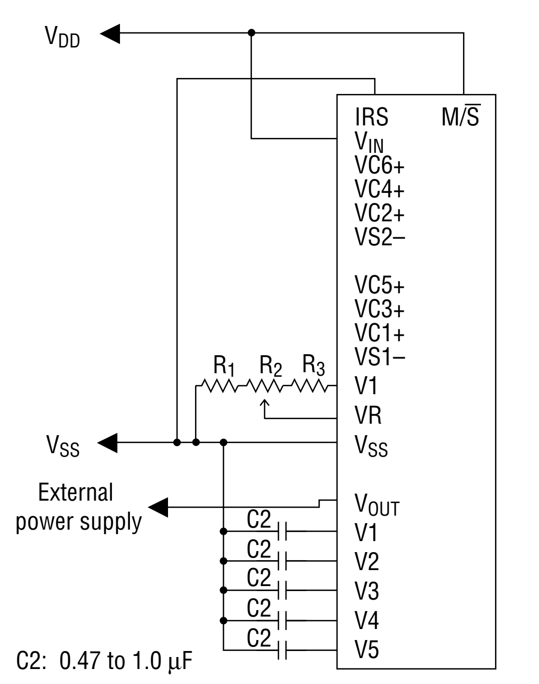
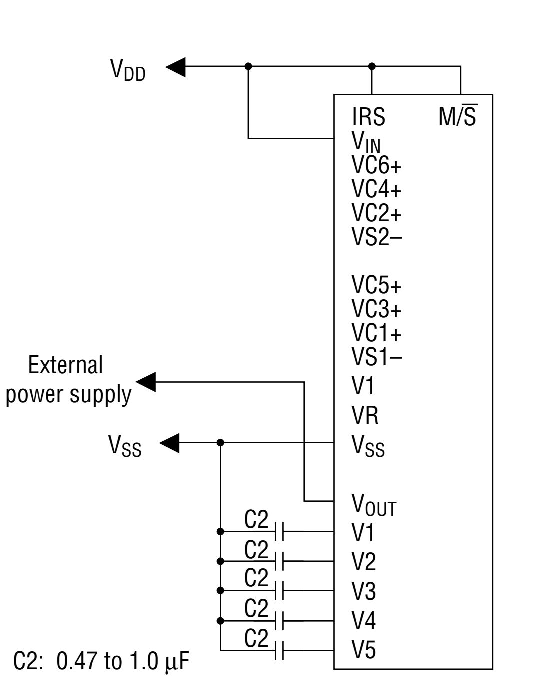
• Command sequence for shutting off the internal power supply
When shutting off the internal power supply, it is recommended to use the procedure given in Fig. 11 of switching OFF the power after putting the LSI in the power save mode using the following command sequence.

Procedure	Description (Command, status)	D7	D6	D5	D4	D3	D2	D1	D0	
Step1	Display OFF	1	0	1	0	1	1	1	0	Power save commands (multiple)
↓	↓									
Step2	Display all ON	1	0	1	0	0	1	0	1	
↓	↓									
End	Internal power supply OFF									

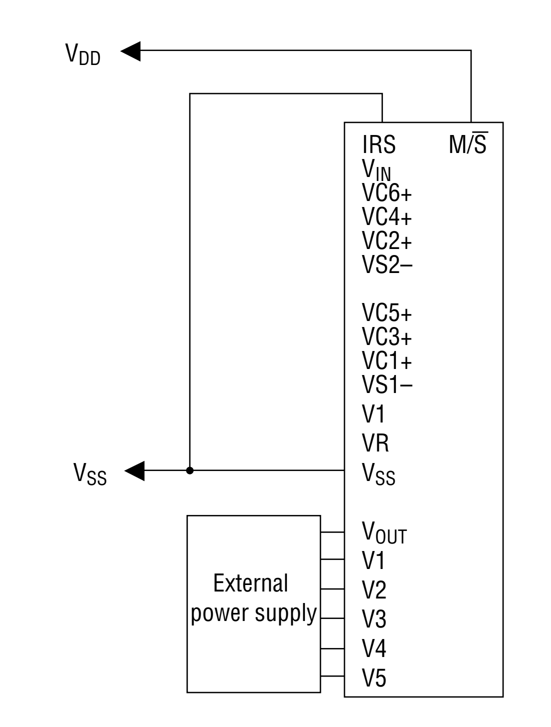
(Command address: D7–D0)

Figure 12

• APPLICATION CIRCUITS

(1) When the voltage multiplier circuit, voltage adjustment circuit, and V/F circuits are all used	(2) When the voltage multiplier circuit, voltage adjustment circuit, and V/F circuits are all used
When using the voltage V1 adjustement internal resistors	When not using the voltage V1 adjustement internal resistors
$V_{IN} = V_{DD}$ 7-Times voltage multiplication	$V_{IN} = V_{DD}$ 7-Times voltage multiplication
	
(3) When only the voltage adjustment circuit and the V/F circuits are used	(4) When only the V/F circuits are used
When not using the voltage V1 adjustment internal resistors	When using the voltage V1 adjustment internal resistors
	

(5) When not using the internal power supply



• Reset circuit

This LSI goes into the initialized condition when the $\overline{\text{RES}}$ input goes to the "L" level. The initialized condition consists of the following conditions.

(1) Display OFF
(2) Normal display mode
(3) ADC Select: Incremented (ADC command D0 = "L")
(4) Power control register: (D2, D1, D0) = (0, 0, 0)
(5) The registers and data in the serial interface are cleared.
(6) LCD Power supply bias ratio: ML9052 ... 1/11 bias
(7) Read-modify-write: OFF
(8) Static indicator: OFF
Static indicator register: (D1, D2) = (0, 0)
(9) Line 1 is set as the display start line.
(10) The column address is set to address 0.
(11) The page address is set to 0.
(12) Common output state: Normal
(13) Voltage V1 adjustment internal resistor ratio register: (D2, D1, D0) = (1, 0, 0)
(14) The electronic potentiometer register set mode is released.
Electronic potentiometer register: (D5, D4, D3, D2, D1, D0) = (1, 0, 0 ,0, 0, 0)
(15) The LCD drive method is set to the frame inversion method.
Line inversion count register: (D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0)

On the other hand, when the reset command is used, only the conditions (7) to (15) above are set. As is shown in the "MPU Interface (example for reference)", the $\overline{\text{RES}}$ pin is connected to the Reset pin of the MPU and the initialization of this LSI is made simultaneously with the resetting of the MPU. This LSI always has to be reset using the $\overline{\text{RES}}$ pin at the time the power is switched ON. Also, excessive current can flow through this LSI when the control signal from the MPU is in the Hi-Z state. It is necessary to take measures to ensure that the input terminals of this LSI do not go into the Hi-Z state after the power has been switched ON. When the built-in LCD drive power supply circuit of the ML9052 is not used, it is necessary that $\overline{\text{RES}}$ = "L" when the external LCD drive power supply goes ON. During the period when $\overline{\text{RES}}$ = "L", although the oscillator circuit is operating, the display timing generator would have stopped and the pins CL, FR, FRS, and $\overline{\text{DOF}}$ would have been tied to the "H" level. There is no effect on the pins D0 to D7.

COMMANDS

MPU Interface

MPU	Read mode	Write mode
80-Series	Pin $\overline{RD}$ = "L"	Pin $\overline{WR}$ = "L"
68-Series	Pin R/$\overline{W}$ = "H" Pin E = "H"	Pin R/$\overline{W}$ = "L" Pin E = "H"

In the case of the 80-series MPU interface, a command is started by inputting a low pulse on the $\overline{RD}$ pin or the $\overline{WR}$ pin.
In the case of the 68-series MPU interface, a command is started by inputting a high pulse on the E pin.

Description of commands

• Display ON/OFF (Write)
This is the command for controlling the turning on or off the LCD panel. The LCD display is turned on when a "1" is written in bit D0 and is turned off when a "0" is written in this bit.

	A0	D7	D6	D5	D4	D3	D2	D1	D0
Display ON	0	1	0	1	0	1	1	1	1
Display OFF	0								0

• Display start line set (Write)
This command specifies the display starting line address in the display data RAM.
Normally, the topmost line in the display is specified using the display start line set command.
It is possible to scroll the display screen by dynamically changing the address using the display start line set command.
The line address is set by writing the upper 3 bits and the lower 4 bits.

	A0	D7	D6	D5	D4	D3	D2	D1	D0
Upper bits	0	0	1	1	*	*	a6	a5	a4
Lower bits				0	*	a3	a2	a1	a0

*: Invalid bits

Line address	a6	a5	a4	a3	a2	a1	a0
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
2	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:
94	1	0	1	1	1	1	0
95	1	0	1	1	1	1	1

• Page address set (Write)

This command specifies the page address which corresponds to the lower address when accessing the display data RAM from the MPU side.

It is possible to access any required bit in the display data RAM by specifying the page address and the column address.

Page address	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	1	0	0	0	0
1						0	0	0	1
2						0	0	1	0
:						:	:	:	:
11						1	0	1	1
12						1	1	0	0

• Column address set (Write)

This command specifies the column address of the display data RAM. The column address is specified by successively writing the upper 4 bits and the lower 4 bits. Since the column address is automatically incremented (by +1) every time the display data RAM is accessed, the MPU can read or write the display data continuously. The incrementing of the column address is stopped at the address 83H.

	A0	D7	D6	D5	D4	D3	D2	D1	D0
Upper bits	0	0	0	0	1	a7	a6	a5	a4
Lower bits					0	a3	a2	a1	a0

Column address	a7	a6	a5	a4	a3	a2	a1	a0
0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:	:
130	1	0	0	0	0	0	1	0
131	1	0	0	0	0	0	1	1

• Status read (Read)

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY	When BUSY is '1', it indicates that the internal operations are being made or the LSI is being reset. Although no command is accepted until BUSY becomes '0', there is no need to check this bit if the cycle time can be satisfied.
ADC	This bit indicates the relationship between the column address and the segment driver. 0: SEG0 → SEG131; column address 0H → 83H 1: SEG131 → SEG0; column address 0H → 83H (Opposite to the polarity of the ADC command.)
ON/OFF	This bit indicates the ON/OFF state of the display. (Opposite to the polarity of the display ON/OFF command.) 0: Display ON 1: Display OFF
RESET	This bit indicates that the LSI is being reset due to the $\overline{\text{RES}}$ signal or the reset command. 0: Operating state 1: Being reset

• Display data write (Write)

This command writes an 8-bit data at the specified address of the display data RAM. Since the column address is automatically incremented (by +1) after writing the data, the MPU can write successive display data to the display data RAM.

A0	D7	D6	D5	D4	D3	D2	D1	D0
1	Write data							

• Display data read (Read)

This command read the 8-bit data from the specified address of the display data RAM. Since the column address is automatically incremented (by +1) after reading the data, the MPU can read successive display data from the display data RAM. Further, one dummy read operation is necessary immediately after setting the column data. The display data cannot be read out when the serial interface is being used.

A0	D7	D6	D5	D4	D3	D2	D1	D0
1	Read data							

• ADC Select (segment driver direction select) (Write)
Using this command it is possible to reverse the relationship of correspondence between the column address of the display data RAM and the segment driver output. It is possible to reverse the sequence of the segment driver output pin by the command.

	A0	D7	D6	D5	D4	D3	D2	D1	D0
Forward	0	1	0	1	0	0	0	0	0
Reverse									1

• Normal/reverse display mode (Write)
It is possible to toggle the display on and off condition without changing the contents of the display data RAM. In this case, the contents of the display data RAM will be retained.

	A0	D7	D6	D5	D4	D3	D2	D1	D0	RAM Data
Forward	0	1	0	1	0	0	1	1	0	LCD ON Voltage when "H"
Reverse									1	LCD ON Voltage when "L"

• Display all-on ON/OFF (Write)
Using this command, it is possible to forcibly turn ON all the dots in the display irrespective of the contents of the display data RAM. In this case, the contents of the display data RAM will be retained.
This command is given priority over the Normal/reverse display mode command.

	A0	D7	D6	D5	D4	D3	D2	D1	D0
Normal display state	0	1	0	1	0	0	1	0	0
All-on display									1

The power save mode will be entered into when the Display all-on ON command is executed in the display OFF condition.

• LCD Bias set (Write)
This command is used for selecting the bias ratio of the voltage necessary for driving the LCD device or panel.

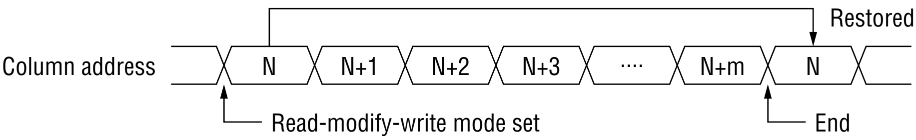
ML9052	A0	D7	D6	D5	D4	D3	D2	D1	D0
1/11 Bias	0	1	0	1	0	0	0	1	0
1/9 Bias									1

• Read-modify-write (Write)
This command is used in combination with the End command. When this command is issued once, the column address is not changed when the Display data read command is issued, but is incremented (by +1) only when the Display data write command is issued. This condition is maintained until the End command is issued. When the End command is issued, the column address is restored to the address that was effective at the time the Read-modify-write command was issued last. Using this function, it is possible to reduce the overhead on the MPU when repeatedly changing the data in special display area such as a blinking cursor.

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	0	0	0	0	0

• End (Write)
This command releases the read-modify-write mode and restores the column address to the value at the beginning of the mode.

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	0	1	1	1	0



• Reset (Write)
This command initializes the display start line number, column address, page address, common output state, voltage V1 adjustment internal resistor ratio, electronic potentiometer function, and the static indicator function, and also releases the read-modify-write mode or the test mode. This command does not affect the contents of the display data RAM.
The reset operation is made after issuing the reset command.
The initialization after switching on the power is carried out by the reset signal input to the $\overline{RES}$ pin.

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	0	0	0	1	0

• Common output state select (Write)
This command is used for selecting the scanning direction of the COM output pins.

	ML9052	A0	D7	D6	D5	D4	D3	D2	D1	D0
Forward	COM0 → COM95	0	1	1	0	0	0	*	*	*
Reverse	COM95 → COM0						1	*	*	*

*: Invalid bits

• Power control set (Write)
This command sets the functions of the power supply circuits.

ML9052	A0	D7	D6	D5	D4	D3	D2	D1	D0
Voltage multiplier circuit: OFF	0	0	0	1	0	1	0		
Voltage multiplier circuit: ON							1		
Voltage adjustment circuit: OFF								0	
Voltage adjustment circuit: ON								1	
Voltage follower circuits: OFF									0
Voltage follower circuits: ON									1

• Voltage V1 adjustment internal resistor ratio set
This command sets the ratios of the internal resistors for adjusting the voltage V1.

Resistor ratio	A0	D7	D6	D5	D4	D3	D2	D1	D0
Small	0	0	0	1	0	0	0	0	0
							0	0	1
							0	1	0
⋮							⋮	⋮	⋮
							1	1	0
Large							1	1	1

• Electronic potentiometer (2-Byte command)
This command is used for controlling the LCD drive voltage V1 output by the voltage adjustment circuit of the internal LCD power supply and for adjusting the intensity of the LCD display.
This is a two-byte command consisting of the Electronic potentiometer mode set command and the Electronic potentiometer register set command, both of which should always be issued successively as a pair.

• Electronic potentiometer mode set (Write)
When this command is issued, the electronic potentiometer register set command becomes effective.
Once the electronic potentiometer mode is set, it is not possible to issue any command other than the Electronic potentiometer register set command. This condition is released after data has been set in the register using the Electronic potentiometer register set command.

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	0	1

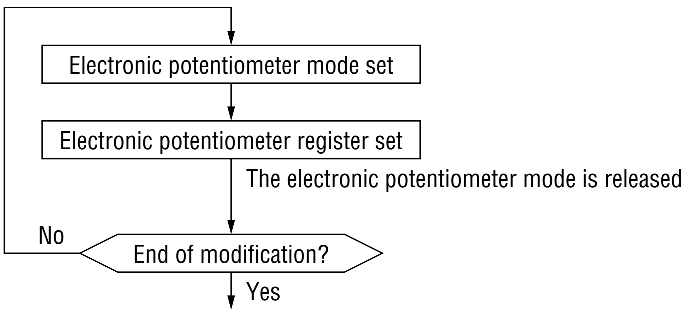
• Electronic potentiometer register set (Write)
By setting a 6-bit data in the electronic potentiometer register using this command, it is possible to set the LCD drive voltage V1 to one of the 64 voltage levels.
The electronic potentiometer mode is released after some data has been set in the electronic potentiometer register using this command.

V1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Small	0	*	*	0	0	0	0	0	1
				0	0	0	0	1	0
				0	0	0	0	1	1
⋮				⋮	⋮	⋮	⋮	⋮	⋮
				1	1	1	1	1	0
Large				1	1	1	1	1	1

*: Invalid bit

Set the data (*, *, 1, 0, 0, 0, 0, 0) when not using the electronic potentiometer function.

Sequence of setting the electronic potentiometer register:



• Static indicator (2-Byte command)
This command is used for controlling the static drive type indicator display.
Static indicator display is controlled only by this command and is independent of all other display control commands. One of the electrodes for driving the static indicator LCD is connected to the pin FR and the other pin is connected to the pin FRS. It is recommended to place the wiring pattern for the electrodes for static indicators far from those of the electrodes for dynamic drive. If these interconnection patterns are too close to each other, they may cause deterioration of the LCD device and the electrodes.

Since the Static indicator ON command is a two-byte command used in combination with the static indictor register set command, these two commands should always be used together.
(The Static indicator OFF command is a single byte command.)

• Static indicator ON/OFF (Write)

When the Static indicator ON command is issued, the Static indicator register set command becomes effective. Once the Static indicator ON command is issued, it is not possible to issue any command other than the Static indicator register set command. This condition is released only after some data is written into the register using the static indicator register set command.

Static indicator	A0	D7	D6	D5	D4	D3	D2	D1	D0
OFF	0	1	0	1	0	1	1	0	0
ON									1

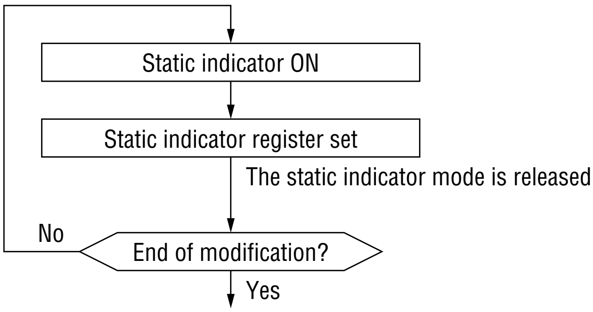
• Static indicator register set (Write)

This command is used to set data in the 2-bit static indicator register thereby setting the blinking state of the static indicator.

Indicator	A0	D7	D6	D5	D4	D3	D2	D1	D0
OFF	0	*	*	*	*	*	*	0	0
ON (Blinking at about 1 sec intervals)								0	1
ON (Blinking at about 0.5 sec intervals)								1	0
ON (Continuously ON)								1	1

*: Invalid bits

Sequence of setting the static indicator register:



• Line inversion drive (2-byte command) / frame inversion drive selection

It is possible to select the LCD driving method between the line inversion drive method and the frame inversion drive methods. When the line inversion method is selected, the command should be used as a two-byte command in combination with the line inversion number set command and hence these two commands should always be issued successively.

• LCD Drive method set (Write)
This command sets the LCD driving method.
Once the line inversion method has been set, no command other than the Line inversion number set command is accepted. This state is released only after some data is set in the register using the Line inversion number set command.
The frame inversion set command is a single byte command.

	A0	D7	D6	D5	D4	D3	D2	D1	D0
Frame inversion	0	1	1	0	1	0	*	*	*
Line inversion						1	*	*	*

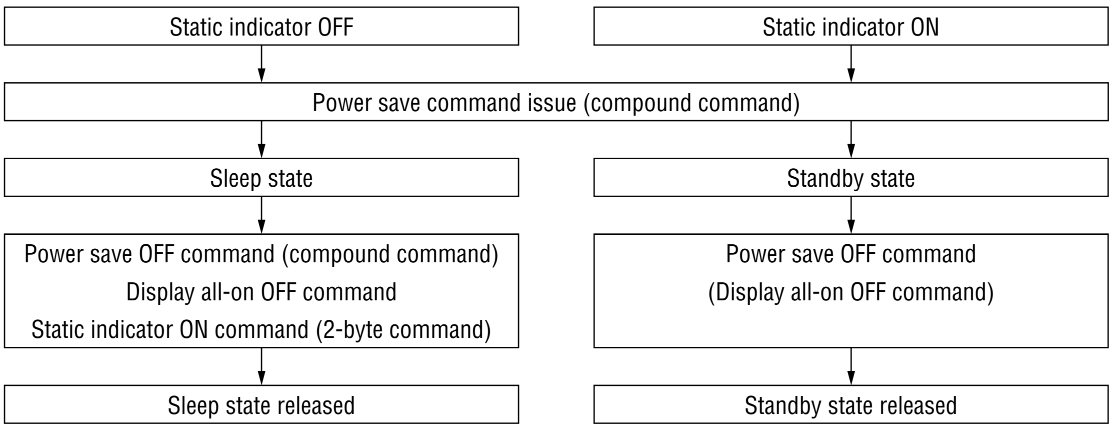
*: Invalid bits

• Line inversion number set (Write)
When the line inversion method has been set using the LCD drive method set command, it is necessary to set immediately the number of inverted lines.

Number of inverted lines	A0	D7	D6	D5	D4	D3	D2	D1	D0
1	0	*	*	*	0	0	0	0	0
2					0	0	0	0	1
:					:	:	:	:	:
31					1	1	1	1	0
32					1	1	1	1	1

*: Invalid bits

• Power save (Compound command)
The LSI goes into the power save state when the Display all-on ON command is issued when the LSI is in the display OFF state, and it is possible to greatly reduce the current consumption in this state. The power save state is of two types, namely, the sleep state and the standby state, and the LSI goes into the standby state when the static indicator has been made ON.
The display data and the operating mode just before entering the power save mode are retained in both the sleep state and the standby state, and also the MPU can access the display data RAM in these states.
The power save mode is released by issuing the Display all-on OFF command.



• Sleep state
In this state, all the operations of the LCD display system are stopped and it is possible to reduce the current consumption to a level near the idle state current consumption unless there are accesses from the MPU. The internal conditions in the sleep state are as follows:
(1) The oscillator circuit and the LCD power supply are stopped.
(2) All the LCD drive circuits are stopped and the segment and common driver outputs will be at the V_{SS} level.

• Standby state
All operations of the dynamic LCD display section are stopped, only the static display circuits for the indicators operate and hence the current consumption will be the minimum necessary for static drive. The internal conditions in the standby state are as follows:
(1) The power supply circuit for LCD drive is stopped. The oscillator circuit will be operating.
(2) The LCD drive circuits for dynamic display are stopped and the segment and common driver outputs will be at the VSS level. The static display section will be operating.
When a reset command is issued in the standby state, the LSI goes into the sleep state.

• NOP (Write)
This is a No Operation command.

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	0	0	0	1	1

• Test (Write)
This is a command for testing the IC chip. Do not use this command. When the test command is issued by mistake, this state can be released by issuing a NOP command. This command will be ineffective if the TEST0 pin is open or at the "L" level.

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	1	*	*	*	*

*: Invalid bits

LIST OF COMMANDS

No	Operation	Dn 7 6 5 4 3 2 1 0	A0	$\overline{RD}$	$\overline{WR}$	Comment
1	Display OFF Display ON	1 0 1 0 1 1 1 0 1	0 0	1 1	0 0	LCD OFF when D0 = 0 ON when D0 = 1
2	Display start line set (upper bits) Display start line set (lower bits)	011**Address (upper) 010*Address (lower)	0	1	0	Upper 3 bits of the display starting line address in the display RAM is set. Lower 4 bits of the display starting line address in the display RAM is set.
3	Page address set	1011Address	0	1	0	The page address in the display RAM is set.
4	Column address set (upper bits) Column address set (lower bits)	0001Address (upper) 0000Address (lower)	0 0	1 1	0 0	The upper 4 bits of the column address in the display RAM is set. The lower 4 bits of the column address in the display RAM is set.
5	Status read	Status0000	0	0	1	The status information is read out from the upper 4 bits.
6	Display data write	Write data	1	1	0	Writes data to the display data RAM.
7	Display data read	Read data	1	0	1	Reads data from the display data RAM.
8	ADC Select Forward Reverse	1 0 1 0 0 0 0 0 1	0 0	1 1	0 0	Correspondence between the display data RAM address and SEG output. Forward when D0 = 0; reverse when D0 = 1
9	Normal display Reverse display	1 0 1 0 0 1 1 0 1	0 0	1 1	0 0	Normal or reverse LCD mode. Normal mode when D0 = 0; reverse when D0 = 1
10	LCD Normal display All-on display	1 0 1 0 0 1 0 0 1	0 0	1 1	0 0	LCD Normal display when D0 = 0; all-on display when D0 = 1
11	LCD Bias set	1 0 1 0 0 0 1 0 1	0 0	1 1	0 0	Sets the LCD drive voltage bias ratio. ML9052: 1/11 when D0 = 0 and 1/9 when D0 = 1
12	Read-modify-write	1 1 1 0 0 0 0 0	0	1	0	Incrementing column address During a write: +1; during a read: 0
13	End	1 1 1 0 1 1 1 0	0	1	0	Releases the read-modify-write state.
14	Reset	1 1 1 0 0 0 1 0	0	1	0	Internal reset
15	Common output state select	1 1 0 0 0 * * * 1 * * *	0 0	1 1	0 0	Selects the COM output scanning direction. Forward when D3 = 0; reverse when D3 = 1
16	Power control set	0 0 1 0 1 Operating state	0	1	0	Selects the operating state of the internal power supply.
17	Voltage V1 adjustment internal resistor ratio set	0 0 1 0 0 Resistor ratio setting	0	1	0	Selects the internal resistor ratio.

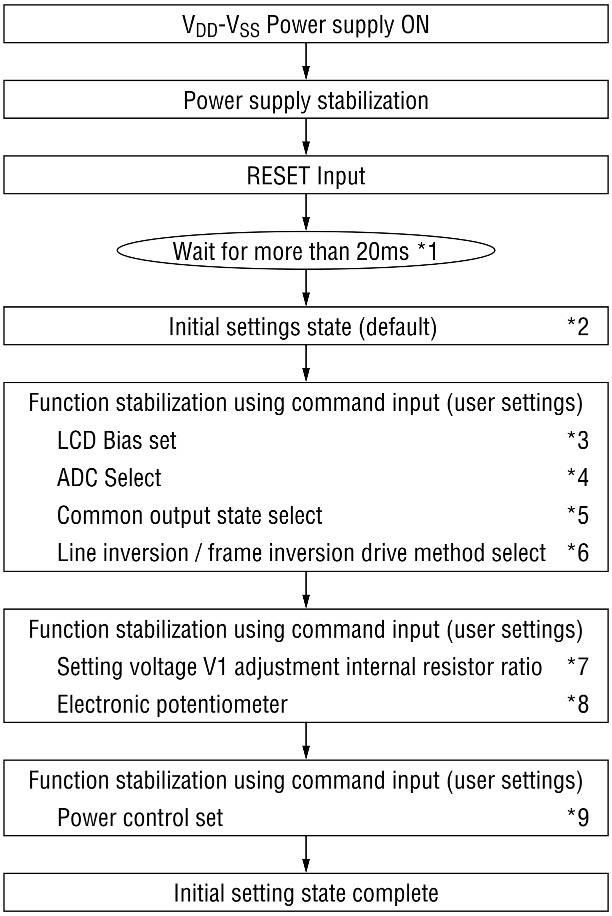
No	Operation	Dn 7 6 5 4 3 2 1 0	A0	$\overline{RD}$	$\overline{WR}$	Comment
18	Electronic potentiometer mode set	1 0 0 0 0 0 0 1	0	1	0	Sets the V1 output voltage in the electronic potentiometer register.
	External potentiometer register set	**Electronic potentiometer value	0	1	0	
19	Static indicator ON/OFF	1 0 1 0 1 1 0 0	0	1	0	OFF when D0 = 0
		1	0	1	0	ON when D0 = 1
	Static indicator register set	******State	0	1	0	Sets the blinking state.
20	LCD Drive method set	1 1 0 1 0 * * *	0	1	0	Frame inversion when D3 = 0.
		1 * * *	0	1	0	Line inversion when D3 = 1.
	Line inversion number set	***Line number	0	1	0	Sets the number of lines inverted.
21	Power save					Compound command of Display OFF and Display all-on.
22	NOP	1 1 1 0 0 0 1 1	0	1	0	The "No Operation" command.
23	Test	1 1 1 1 * * * *	0	1	0	The command for factory testing of the IC chip.

*: Invalid bits

DESCRIPTION OF COMMANDS

Examples of settings for the instructions (reference examples)

• Initial setting



Notes: Sections to be referred to

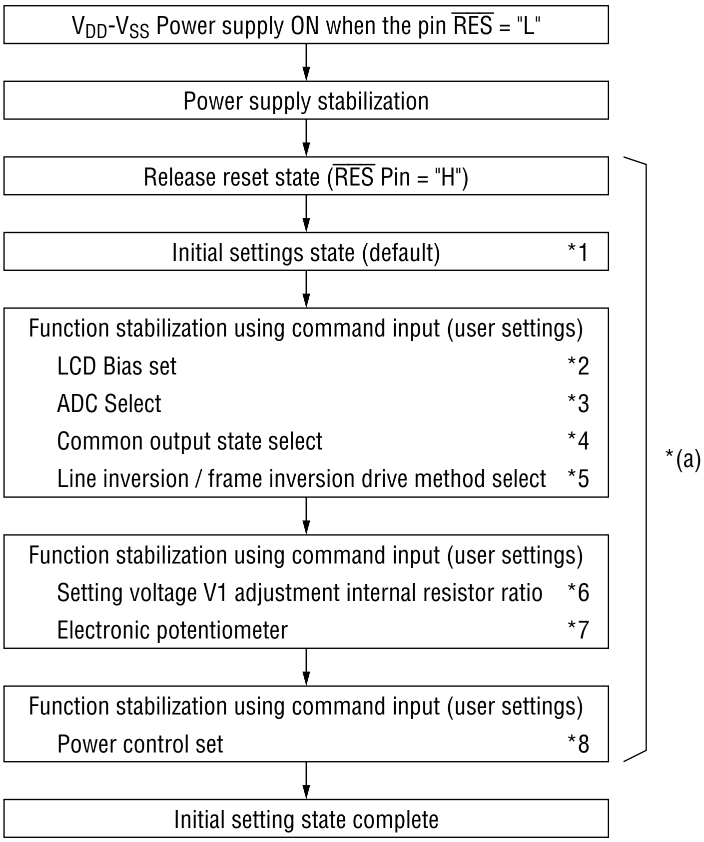
*1: Stabilization time of the internal oscillator
*2: Function description "Reset circuit"
*3: Command description "LCD Bias set"
*4: Command description "ADC Select"
*5: Command description "Common output state select"
*6: Command description "Line inversion/frame inversion drive select"
*7: Function description "Power supply circuit", Command description "Voltage V1 adjustment internal resistor ratio set"
*8: Function description "Power supply circuit", Command description "Electronic potentiometer"
*9: Function description "Power supply circuit", Command description "Power control set"

Examples of settings for the instructions (reference examples)

• Initial setting

Note: After the power is switched ON, this LSI outputs at the LCD drive output pins SEG and COM the voltages V3, V4 (SEG pins) and V2, V5 (COM pins) which are voltages that do not select LCD display. If any charge is remaining on the smoothing capacitors connected between the V_{OUT} pin and the pins for the LCD drive voltage outputs (V1 to V5), there may be some abnormality in the display such as temporary blacking out of the display screen when the power is switched ON.
The following procedure is recommended for avoiding such abnormalities at the time the power is switched ON.

• When using the internal power supply immediately after power-on

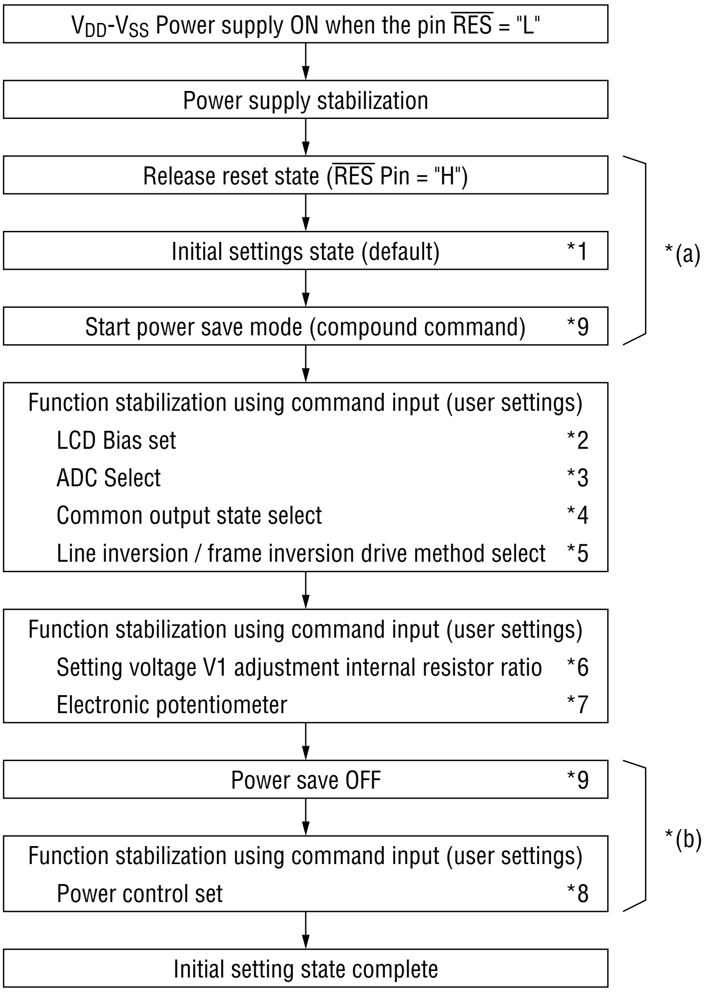


*(a): Carry out power control set within 5 ms after releasing the reset state.
The 5 ms duration changes depending on the panel characteristics and the value of the smoothing capacitor. We recommend verification of operation using an actual unit.

Notes: Sections to be referred to

*1: Function description "Reset circuit"
*2: Command description "LCD Bias set"
*3: Command description "ADC Select"
*4: Command description "Common output state select"
*5: Command description "Line inversion /frame inversion drive select"
*6: Function description "Power supply circuit", Command description "Voltage V1 adjustment internal resistor ratio set"
*7: Function description "Power supply circuit", Command description "Electronic potentiometer"
*8: Function description "Power supply circuit", Command description "Power control set"

• When not using the internal power supply immediately after power-on



*(a): Enter the power save state within 5 ms after releasing the reset state.

*(b): Carry out power control set within 5 ms after releasing the power save state.
The 5 ms duration in *(a) and *(b) changes depending on the panel characteristics and the value of the smoothing capacitor. We recommend verification of operation using an actual unit.

Notes: Sections to be referred to

*1: Function description "Reset circuit"

*2: Command description "LCD Bias set"

*3: Command description "ADC Select"

*4: Command description "Common output state select"

*5: Command description "Line inversion /frame inversion drive select"

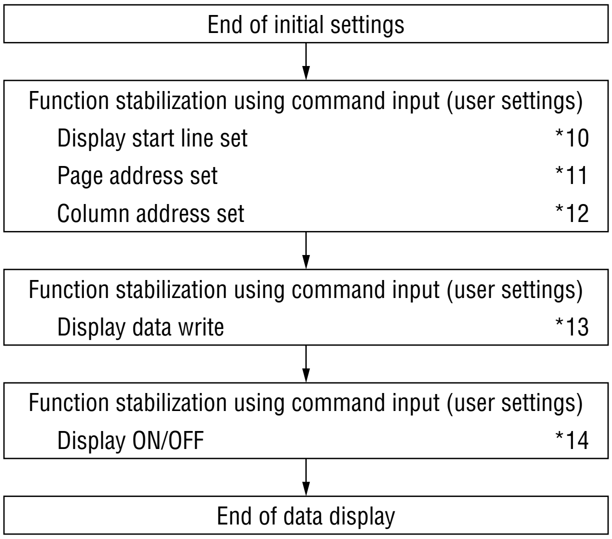
*6: Function description "Power supply circuit", Command description "Voltage V1 adjustment internal resistor ratio set"

*7: Function description "Power supply circuit", Command description "Electronic potentiometer"

*8: Function description "Power supply circuit", Command description "Power control set"

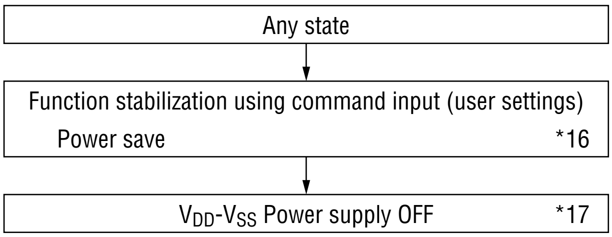
*9: The power save state can be either the sleep state or the standby state.
Command description "Power save (compound command)"

• Data display



Notes: Sections to be referred to
*10: Command description "Display start line set"
*11: Command description "Page address set"
*12: Command description "Column address set"
*13: Command description "Display data write"
*14: Command description "Display ON/OFF"

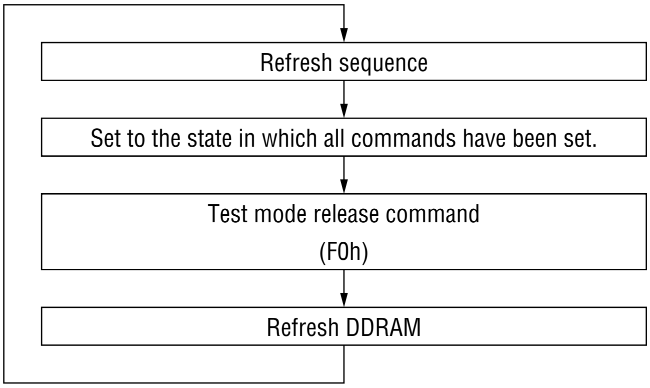
• Power supply OFF (*15)



Notes: Sections to be referred to
*15: The power supply of this LSI is switched OFF after switching OFF the internal power supply. Function description "Power supply circuit"
If the power supply of this LSI is switched OFF when the internal power supply is still ON, since the state of supplying power to the built-in LCD drive circuits continues for a short duration, it may affect the display quality of the LCD panel. Always follow the power supply switching OFF sequence.
*16: Command description "Power save"
*17: Do not enter Reset when switching the power supply OFF.

• Refresh

Use the refresh sequence at regular intervals.



ABSOLUTE MAXIMUM RATINGS

V_{SS} = 0 V

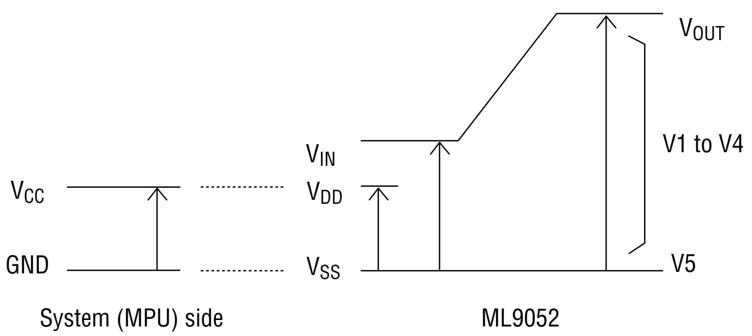
Parameter	Symbol	Condition	Rated value	Unit	Applicable pins
Power Supply Voltage	V_{DD}	Ta = 25˚C	–0.3 to +7	V	V_{DD}, V_{SS}
Bias Voltage	V_{BI}	Ta = 25˚C	–0.3 to +20	V	V_{OUT}, V1 to V5
Voltage Multiplier Reference Voltage	V_{IN}	6-Times multiplication 7-Times multiplication	–0.3 to +3.3 –0.3 to +2.8	V	V_{IN}, V_{SS}
Input Voltage	V_I	Ta = 25˚C	–0.3 to V_{DD}+0.3	V	All inputs
Storage Temperature Range	T_{stg}	TCP Chip	–55 to +100 –55 to +125	˚C	—

Ta: Ambient temperature

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Rated value	Unit	Applicable pins
Power Supply Voltage	V_{DD}	—	1.8 to 5.5	V	V_{DD}, V_{SS}
Bias Voltage	V_{BI}	—	6 to 18	V	V_{OUT}, V1 to V5
Voltage Multiplier Reference Voltage	V_{IN}	6-Times multiplication 7-Times multiplication	1.8 to 3 1.8 to 2.5	V	V_{IN}, V_{SS}
Voltage Multiplier Output Voltage	V_{OUT}		18	V	V_{OUT}
Reference Voltage	V_{REG0} V_{REG1}	–0.11%/˚C *1 –0.3%/˚C *1		V	—
Operating Temperature Range	T_{op}		–40 to +85	˚C	—

*1: Ta = 25˚C



Note 1: The voltages V_{DD}, V1 to V5, and V_{OUT} are values taking V_{SS} = 0 V as the reference.
Note 2: The highest bias potential is V1 and the lowest is V_{SS}.
Note 3: Always maintain the relationship $V1 \geq V2 \geq V3 \geq V4 \geq V5 \geq V_{SS}$ among these voltages.

ELECTRICAL CHARACTERISTICS

DC Characteristics

[Ta = –40 to +85°C]

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pins
"H" Input Voltage		V_{IH}		0.8 × V_{DD}		V_{DD}	V	*1
"L" Input Voltage		V_{IL}		V_{SS}		0.2 × V_{DD}	V	*1
"H" Output Voltage		V_{OH}	I_{OH} = –0.5mA	0.8 × V_{DD}		V_{DD}	V	*2
"L" Output Voltage		V_{OL}	I_{OL} = 0.5mA	V_{SS}		0.2 × V_{DD}	V	*2
"H" Input Current		I_{IH}	$V_I = V_{DD}$	–1.0		+1.0	µA	*3
"L" Input Current		I_{IL}	V_I = 0 V	–3.0		+3.0	µA	*4
LCD Driver ON Resistance		R_{ON}	I_o = ±50 µA			10	kΩ	SEG1 to 132 COM1 to 97
Current Consumption		I_{DDS}	Standby			5	µA	V_{DD}
Input Pin Capacitance		C_{IN}	Ta = 25°C, f = 1MHz		5	8	PF	
Oscillator Frequency	Internal Oscillations	f_{OSC}	Ta = 25°C	25	33	40	kHz	*5
Oscillator Frequency	External Input	f_{CL}	Ta = 25°C	25	33	40	kHz	CL*5

*1: A0, D0 to D5, D6 (SCL), D7 (SI), $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, CLS, CL, FR, M/$\overline{S}$, C86, P/$\overline{S}$, $\overline{DOF}$, $\overline{RES}$, IRS, $\overline{HPM}$ Pins
*2: D0 to D7, FR, FRS, $\overline{DOF}$, CL Pins
$\overline{DOF}$, $\overline{RES}$, IRS, $\overline{HPM}$ Pins
*3: A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, CLS, M/$\overline{S}$, C86, P/$\overline{S}$, $\overline{RES}$, IRS, $\overline{HPM}$ Pins
*4: Applicable to the pins D0 to D5, D6 (SCL), D7 (SI), CL, FR, and $\overline{DOF}$ in the high impedance state.
*5: See Table 24 for the relationship between the oscillator frequency and the frame frequency.

Table 24. Relationship among the oscillator frequency (f_{OSC}), display clock frequency (f_{CL}), and LCD frame frequency (f_{FR})

Parameter	Display clock frequency (f_{CL})	LCD Frame frequency (f_{FR})
When the internal oscillator circuit is used	f_{OSC}/4	f_{OSC}/(4 × 97)
When the internal oscillator circuit is not used	f_{CL}/4	f_{CL}/(4 × 97)

• Operating current consumption value (Ta = 25°C)
(1) During display operation, internal power supply OFF (The current consumption of the entire IC when an external power supply is used)
Display mode: All-white

Symbol	Condition	Rated value			Unit	Remarks
		Min.	Typ.	Max.		
I_{DD}	V_{DD} = 5V, V1-V_{SS} = 14V		(80)		µA	
I_{DD}	V_{DD} = 3V, V1-V_{SS} = 14V		(75)		µA	

Display mode: Checker pattern

Symbol	Condition	Rated value			Unit	Remarks
		Min.	Typ.	Max.		
I_{DD}	V_{DD} = 5 V, V1-V_{SS} = 14 V		TBD		μA	
	V_{DD} = 3 V, V1-V_{SS} = 14 V		TBD			

(2) During display operation, internal power supply ON
Display mode: All-white

Symbol	Condition		Rated value			Unit	Remarks
			Min.	Typ.	Max.		
I_{DD}	V_{DD} = 5 V, 3-times voltage multiplication, V1-V_{SS} = 14 V	Normal mode		(90)		μA	
		High power mode		TBD			
	V_{DD} = 3 V, 6-times voltage multiplication, V1-V_{SS} = 14 V	Normal mode		(150)			
		High power mode		TBD			

Display mode: Checker pattern

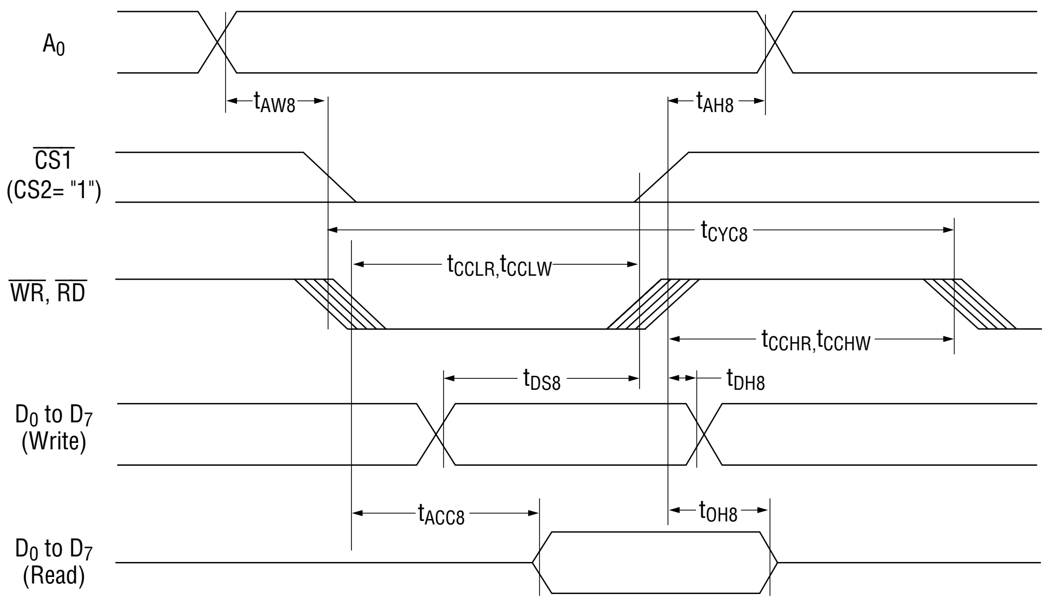
Symbol	Condition		Rated value			Unit	Remarks
			Min.	Typ.	Max.		
I_{DD}	V_{DD} = 5 V, 3-times voltage multiplication, V1-V_{SS} = 14 V	Normal mode		TBD		μA	
		High power mode		TBD			
	V_{DD} = 3 V, 6-times voltage multiplication, V1-V_{SS} = 14 V	Normal mode		TBD			
		High power mode		TBD			

- Power save mode current consumption, V_{SS} = 0 V, V_{DD} = 3 V±10%

Parameter	Symbol	Condition	Rated value			Unit	Remarks
			Min.	Typ.	Max.		
Sleep State	I_{DDS1}			(0.1)		μA	
Standby State	I_{DDS2}			(5)			

Timing Characteristics

• System bus read/write characteristics 1 (80-series MPU)



[V_{DD} = 4.5 V to 5.5 V, Ta = –40 to +85°C]

Parameter	Applicable pins	Symbol	Condition	Rated value Min.	Rated value Max.	Unit
Address Hold Time	A0	t_{AH8}		0	—	ns
Address Setup Time		t_{AW8}		0	—	
System Cycle Time	A0	t_{CYC8}		166	—	
Control L Pulse Width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		30	—	
Control L Pulse Width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		70	—	
Control H Pulse Width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		30	—	
Control H Pulse Width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		30	—	
Data Setup Time	D0 to D7	t_{DS8}		30	—	
Data Hold Time		t_{DH8}		10	—	
$\overline{RD}$ Access Time		t_{ACC8}	CL = 100pF	—	70	
Output Disable Time		t_{OH8}		5	50	

[V_{DD} = 2.7 V to 4.5 V, Ta = –40 to +85°C]

Parameter	Applicable pins	Symbol	Condition	Rated value		Unit
				Min.	Max.	
Address Hold Time	A0	t_{AH8}		0	—	ns
Address Setup Time		t_{AW8}		0	—	
System Cycle Time	A0	t_{CYC8}		300	—	
Control L Pulse Width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		60	—	
Control L Pulse Width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		120	—	
Control H Pulse Width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		60	—	
Control H Pulse Width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		60	—	
Data Setup Time	D0 to D7	t_{DS8}		40	—	
Data Hold Time		t_{DH8}		15	—	
$\overline{RD}$ Access Time		t_{ACC8}	CL = 100pF	—	140	
Output Disable Time		t_{OH8}		10	100	

[V_{DD} = 1.8 V to 2.7 V, Ta = –40 to +85°C]

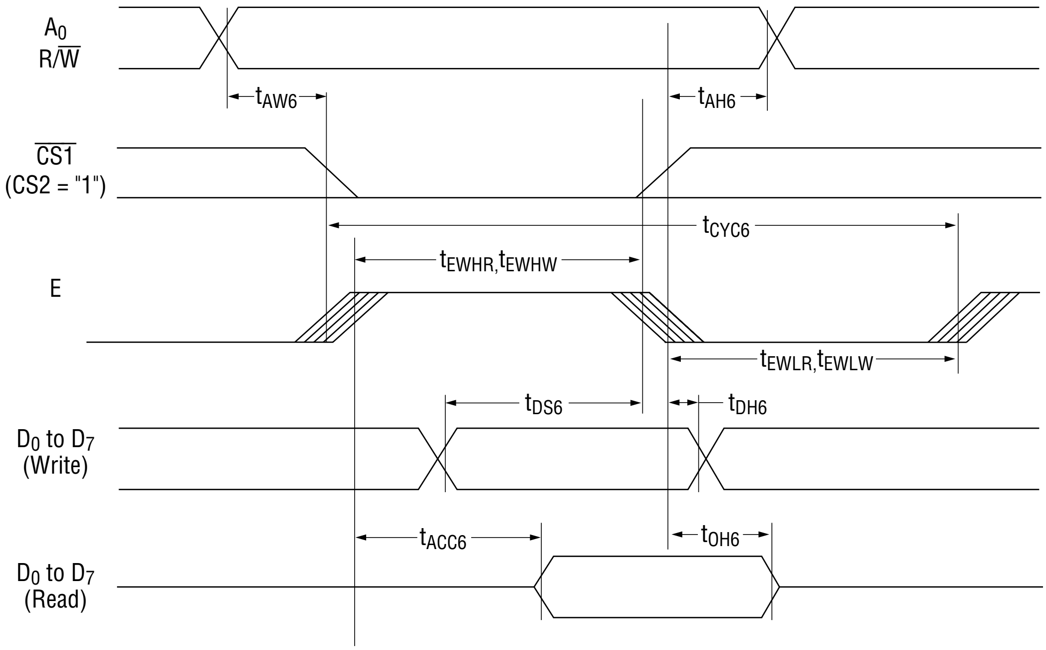
Parameter	Applicable pins	Symbol	Condition	Rated value		Unit
				Min.	Max.	
Address Hold Time	A0	t_{AH8}		0	—	ns
Address Setup Time		t_{AW8}		0	—	
System Cycle Time	A0	t_{CYC8}		1000	—	
Control L Pulse Width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		120	—	
Control L Pulse Width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		240	—	
Control H Pulse Width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		120	—	
Control H Pulse Width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		120	—	
Data Setup Time	D0 to D7	t_{DS8}		80	—	
Data Hold Time		t_{DH8}		30	—	
$\overline{RD}$ Access Time		t_{ACC8}	CL = 100pF	—	280	
Output Disable Time		t_{OH8}		10	200	

Note 1: The input signal rise and fall times are specified as 15 ns or less.
When using the system cycle time for fast speed, the specified values are (tr+tf) ≤ (t_{CYC8}-t_{CCLW}-t_{CCHW}) or (tr+tf) ≤ (t_{CYC8}-t_{CCLR}-t_{CCHR}).

Note 2: All timings are specified taking the levels of 20% and 80% of V_{DD} as the reference.

Note 3: The values of t_{CCLW} and t_{CCLR} are specified during the overlapping period of $\overline{CS1}$ at "L" (CS2 = "H") and the "L" levels of $\overline{WR}$ and $\overline{RD}$, respectively.

• System bus read/write characteristics 2 (68-series MPU)



[V_{DD} = 4.5 V to 5.5 V, Ta = –40 to +85°C]

Parameter		Applicable pins	Symbol	Condition	Rated value Min.	Rated value Max.	Unit
Address Hold Time		A0	t_{AH6}		0	—	ns
Address Setup Time			t_{AW6}		0	—	
System Cycle Time		A0	t_{CYC6}		166	—	
Data Setup Time		D0 to D7	t_{DS6}		30	—	
Data Hold Time			t_{DH6}		10	—	
Access Time			t_{ACC6}	CL = 100pF	—	70	
Output Disable Time			t_{OH6}		10	50	
Enable H Pulse Width	Read	E	t_{CCLW}		70	—	
	Write		t_{CCLR}		30	—	
Enable L Pulse Width	Read	E	t_{CCHW}		30	—	
	Write		t_{CCHR}		30	—	

[V_{DD} = 2.7 V to 4.5 V, Ta = –40 to +85°C]

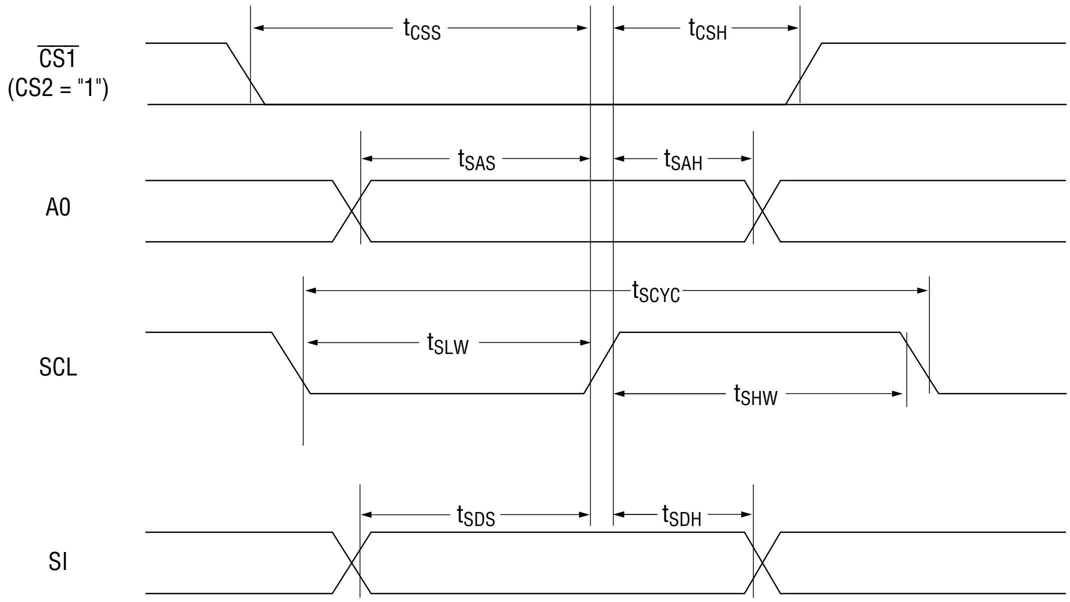
Parameter		Applicable pins	Symbol	Condition	Rated value		Unit
					Min.	Max.	
Address Hold Time		A0	t_{AH6}		0	—	ns
Address Setup Time			t_{AW6}		0	—	
System Cycle Time		A0	t_{CYC6}		300	—	
Data Setup Time		D0 to D7	t_{DS6}		40	—	
Data Hold Time			t_{DH6}		15	—	
Access Time			t_{ACC6}	CL = 100pF	—	140	
Output Disable Time			t_{OH6}		10	100	
Enable H Pulse Width	Read	E	t_{CCLW}		120	—	
	Write		t_{CCLR}		60	—	
Enable L Pulse Width	Read	E	t_{CCHW}		60	—	
	Write		t_{CCHR}		60	—	

[V_{DD} = 1.8 V to 2.7 V, Ta = –40 to +85°C]

Parameter		Applicable pins	Symbol	Condition	Rated value		Unit
					Min.	Max.	
Address Hold Time		A0	t_{AH6}		0	—	ns
Address Setup Time			t_{AW6}		0	—	
System Cycle Time		A0	t_{CYC6}		1000	—	
Data Setup Time		D0 to D7	t_{DS6}		80	—	
Data Hold Time			t_{DH6}		30	—	
Access Time			t_{ACC6}	CL = 100pF	—	280	
Output Disable Time			t_{OH6}		10	200	
Enable H Pulse Width	Read	E	t_{CCLW}		240	—	
	Write		t_{CCLR}		120	—	
Enable L Pulse Width	Read	E	t_{CCHW}		120	—	
	Write		t_{CCHR}		120	—	

Note 1: The input signal rise and fall times are specified as 15 ns or less.
When using the system cycle time for fast speed, the specified values are $(tr+tf) \leq (t_{CYC6}-t_{EWLW}-t_{EWHW})$ or $(tr+tf) \leq (t_{CYC6}-t_{EWLR}-t_{EWHR})$.
Note 2: All timings are specified taking the levels of 20% and 80% of V_{DD} as the reference.
Note 3: The values of t_{EWLW} and t_{EWLR} are specified during the overlapping period of $\overline{CS1}$ at "L" (CS2 = "H") and the "H" level of E.

• Serial interface



[V_{DD} = 4.5 V to 5.5 V, Ta = –40 to +85°C]

Parameter	Applicable pins	Symbol	Condition	Rated value Min.	Rated value Max.	Unit
Serial Clock Period	SCL	t_{SCYC}		200	—	ns
SCL "H" Pulse Width		t_{SHW}		75	—	
SCL "L" Pulse Width		t_{SLW}		75	—	
Address Setup Time	A0	t_{SAS}		50	—	
Address Hold Time		t_{SAH}		100	—	
Data Setup Time	SI	t_{SDS}		50	—	
Data Hold Time		t_{SDH}		50	—	
CS-SCL Time	CS	t_{CSS}		100	—	
		t_{CSH}		100	—	

[V_{DD} = 2.7 V to 4.5 V, Ta = –40 to +85°C]

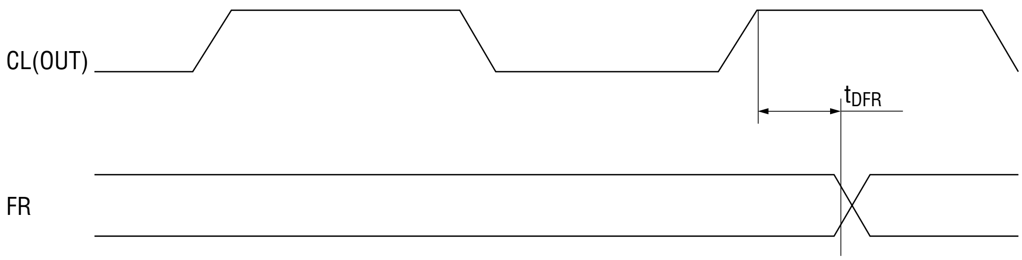
Parameter	Applicable pins	Symbol	Condition	Rated value		Unit
				Min.	Max.	
Serial Clock Period	SCL	t_{SCYC}		250	—	ns
SCL "H" Pulse Width		t_{SHW}		100	—	
SCL "L" Pulse Width		t_{SLW}		100	—	
Address Setup Time	A0	t_{SAS}		150	—	
Address Hold Time		t_{SAH}		150	—	
Data Setup Time	SI	t_{SDS}		100	—	
Data Hold Time		t_{SDH}		100	—	
CS-SCL Time	CS	t_{CSS}		150	—	
		t_{CSH}		150	—	

[V_{DD} = 1.8 V to 2.7 V, Ta = –40 to +85°C]

Parameter	Applicable pins	Symbol	Condition	Rated value		Unit
				Min.	Max.	
Serial Clock Period	SCL	t_{SCYC}		400	—	ns
SCL "H" Pulse Width		t_{SHW}		150	—	
SCL "L" Pulse Width		t_{SLW}		150	—	
Address Setup Time	A0	t_{SAS}		250	—	
Address Hold Time		t_{SAH}		250	—	
Data Setup Time	SI	t_{SDS}		150	—	
Data Hold Time		t_{SDH}		150	—	
CS-SCL Time	CS	t_{CSS}		250	—	
		t_{CSH}		250	—	

Note 1: The input signal rise and fall times are specified as 15 ns or less.
Note 2: All timings are specified taking the levels of 20% and 80% of V_{DD} as the reference.

• Display control output timing



[V_{DD} = 4.5 V to 5.5 V, Ta = –40 to +85°C]

Parameter	Applicable pins	Symbol	Condition	Rated value			Unit
				Min.	Typ.	Max.	
FR Delay Time	FR	t_{DFR}	CL = 50pF	—	10	40	ns

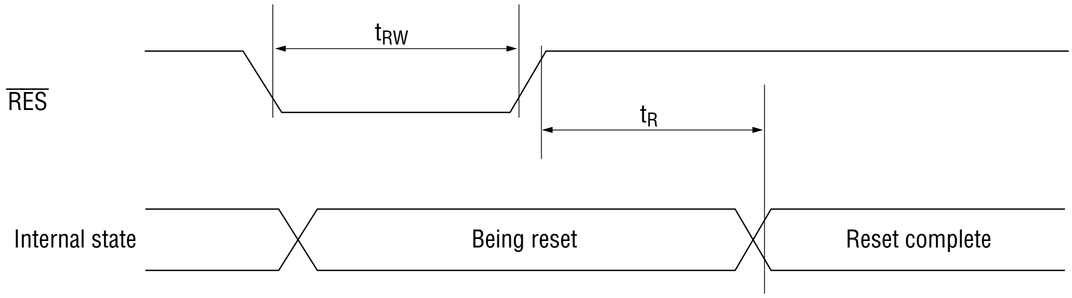
[V_{DD} = 2.7 V to 4.5 V, Ta = –40 to +85°C]

Parameter	Applicable pins	Symbol	Condition	Rated value			Unit
				Min.	Typ.	Max.	
FR Delay Time	FR	t_{DFR}	CL = 50pF	—	20	80	ns

[V_{DD} = 1.8 V to 2.7 V, Ta = –40 to +85°C]

Parameter	Applicable pins	Symbol	Condition	Rated value			Unit
				Min.	Typ.	Max.	
FR Delay Time	FR	t_{DFR}	CL = 50pF	—	50	200	ns

• Reset input timing



[V_{DD} = 4.5 V to 5.5 V, Ta = –40 to +85°C]

Parameter	Applicable pins	Symbol	Condition	Rated value Min.	Rated value Typ.	Rated value Max.	Unit
Reset Time	—	t_R		—	—	0.5	µs
Reset "L" Pulse Width	$\overline{RES}$	t_{RW}		0.5	—	—	

[V_{DD} = 2.7 V to 4.5 V, Ta = –40 to +85°C]

Parameter	Applicable pins	Symbol	Condition	Rated value Min.	Rated value Typ.	Rated value Max.	Unit
Reset Time	—	t_R		—	—	1	µs
Reset "L" Pulse Width	$\overline{RES}$	t_{RW}		1	—	—	

[V_{DD} = 1.8 V to 2.7 V, Ta = –40 to +85°C]

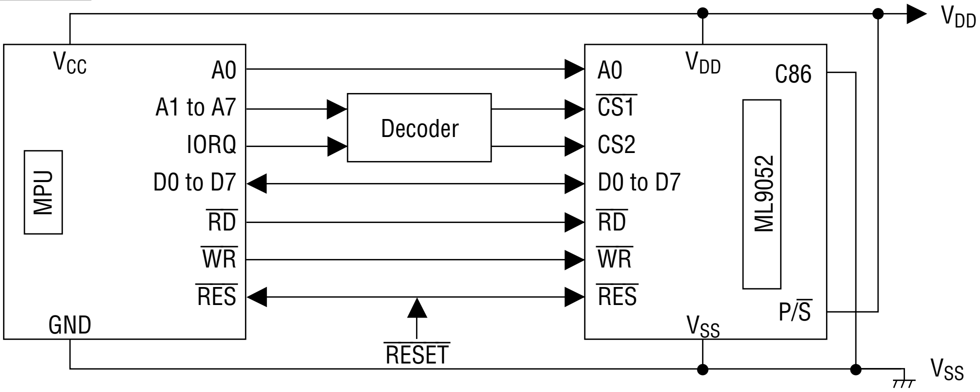
Parameter	Applicable pins	Symbol	Condition	Rated value Min.	Rated value Typ.	Rated value Max.	Unit
Reset Time	—	t_R		—	—	1.5	µs
Reset "L" Pulse Width	$\overline{RES}$	t_{RW}		1.5	—	—	

Note : All timings are specified taking the levels of 20% and 80% of V_{DD} as the reference.

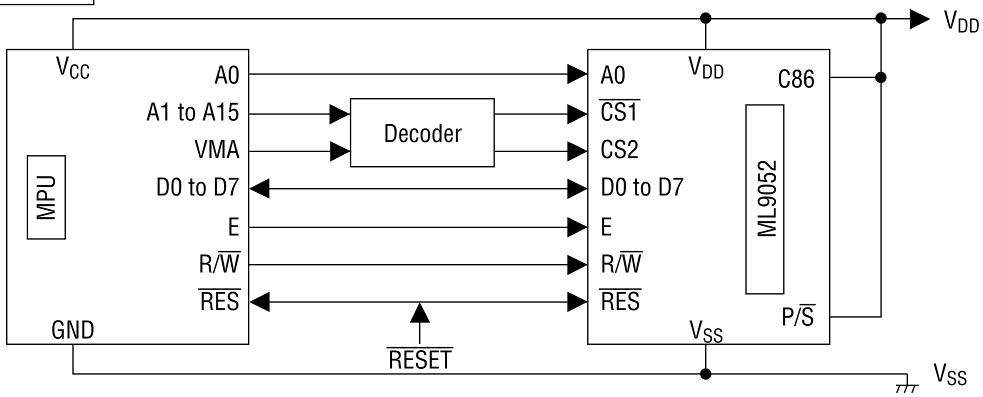
MPU INTERFACE

The ML9052 IC can be connected directly to the 80-series and 68-series MPUs.
Further, by using the serial interface, it is possible to operate the LSI with a minimum number of signal lines.
In addition, it is possible to expand the display area by using the ML9052 LSI in a multiple chip configuration. In this case, it is possible to select the individual LSI to be accessed using the chip select signals.

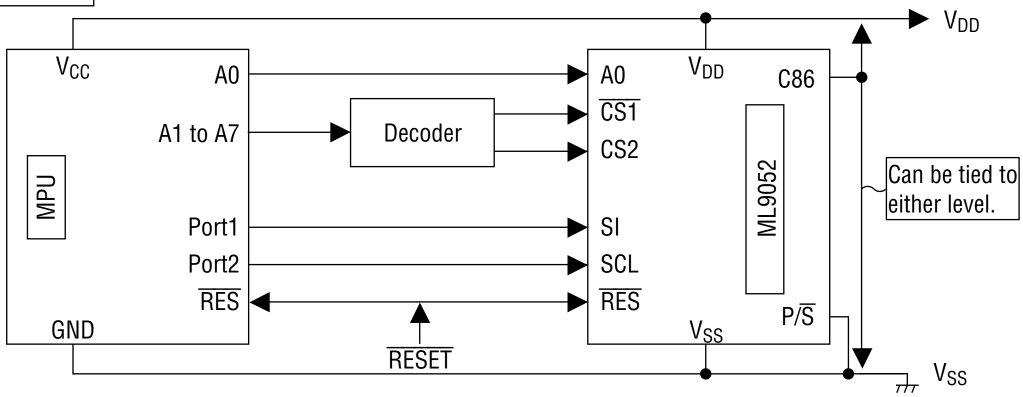
• 80-Series MPU



• 68-Series MPU



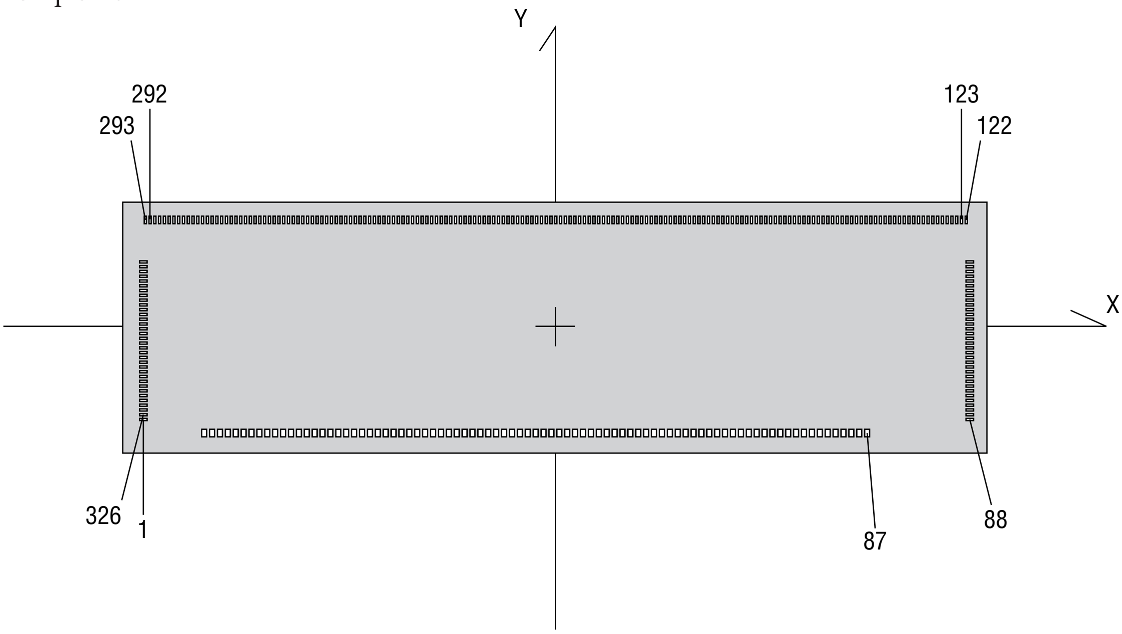
• Serial interface



PAD CONFIGURATION

Pad Layout

Chip Size : 11.44 × 3.32mm



Pad Coordinates

PAD	Symbol	X (μm)	Y (μm)
1	DUMMY	–5535	–1452
2	DUMMY	–4785	–1515
3	FRS	–4673	–1515
4	FR	–4561	–1515
5	M/$\overline{S}$	–4449	–1515
6	$\overline{DOF}$	–4337	–1515
7	TEST0	–4225	–1515
8	V_{SS}	–4113	–1515
9	$\overline{CS1}$	–4001	–1515
10	CS2	–3889	–1515
11	V_{DD}	–3777	–1515
12	$\overline{RES}$	–3665	–1515
13	A0	–3553	–1515
14	V_{SS}	–3441	–1515
15	$\overline{WR}$	–3329	–1515
16	$\overline{RD}$	–3217	–1515
17	V_{DD}	–3105	–1515
18	D0	–2993	–1515
19	D1	–2881	–1515
20	D2	–2769	–1515
21	D3	–2657	–1515
22	D4	–2545	–1515
23	D5	–2433	–1515
24	D6	–2321	–1515
25	D7	–2209	–1515
26	V_{DD}	–2097	–1515
27	V_{DD}	–2017	–1515
28	V_{DD}	–1937	–1515
29	V_{DD}	–1857	–1515
30	V_{IN}	–1777	–1515
31	V_{IN}	–1697	–1515
32	V_{IN}	–1617	–1515
33	V_{IN}	–1537	–1515
34	V_{SS}	–1457	–1515
35	V_{SS}	–1377	–1515
36	V_{SS}	–1297	–1515
37	V_{OUT}	–1197	–1515
38	V_{OUT}	–1072	–1515
39	VC2+	–947	–1515
40	VC2+	–822	–1515

PAD	Symbol	X (μm)	Y (μm)
41	VC4+	–697	–1515
42	VC4+	–572	–1515
43	VC6+	–447	–1515
44	VC6+	–322	–1515
45	VS2–	–197	–1515
46	VS2–	–72	–1515
47	VS1–	53	–1515
48	VS1–	178	–1515
49	VC5+	303	–1515
50	VC5+	428	–1515
51	VC3+	553	–1515
52	VC3+	678	–1515
53	VC1+	803	–1515
54	VC1+	928	–1515
55	V_{SS}	1053	–1515
56	V_{SS}	1178	–1515
57	V_{RS}	1303	–1515
58	V_{RS}	1423	–1515
59	V_{DD}	1553	–1515
60	V_{DD}	1678	–1515
61	V1	1803	–1515
62	V1	1928	–1515
63	V2	2053	–1515
64	V2	2178	–1515
65	V3	2303	–1515
66	V3	2428	–1515
67	V4	2553	–1515
68	V4	2678	–1515
69	V5	2803	–1515
70	V5	2928	–1515
71	VR	3053	–1515
72	VR	3178	–1515
73	V_{DD}	3303	–1515
74	V_{DD}	3428	–1515
75	TEST1	3553	–1515
76	V_{DD}	3665	–1515
77	CL	3777	–1515
78	CLS	3889	–1515
79	V_{SS}	4001	–1515
80	C86	4113	–1515

PAD	Symbol	X (μm)	Y (μm)
81	$P/\overline{S}$	4225	–1515
82	V_{DD}	4337	–1515
83	$\overline{HPM}$	4449	–1515
84	V_{SS}	4561	–1515
85	IRS	4673	–1515
86	V_{DD}	4785	–1515
87	DUMMY	4897	–1515
88	DUMMY	5535	–1452
89	COM47	5535	–1387
90	COM46	5535	–1322
91	COM45	5535	–1257
92	COM44	5535	–1192
93	COM43	5535	–1127
94	COM42	5535	–1062
95	COM41	5535	–997
96	COM40	5535	–932
97	COM39	5535	–867
98	COM38	5535	–802
99	COM37	5535	–737
100	COM36	5535	–672
101	COM35	5535	–607
102	COM34	5535	–542
103	COM33	5535	–477
104	COM32	5535	–412
105	COM31	5535	–347
106	COM30	5535	–282
107	COM29	5535	–217
108	COM28	5535	–152
109	COM27	5535	–87
110	COM26	5535	–22
111	COM25	5535	43
112	COM24	5535	108
113	COM23	5535	173
114	COM22	5535	238
115	COM21	5535	303
116	COM20	5535	368
117	COM19	5535	433
118	COM18	5535	498
119	COM17	5535	563
120	COM16	5535	628

PAD	Symbol	X (μm)	Y (μm)	PAD	Symbol	X (μm)	Y (μm)
121	DUMMY	5535	693	161	SEG19	3022	1509
122	DUMMY	5562	1509	162	SEG20	2958	1509
123	COM15	5498	1509	163	SEG21	2892	1509
124	COM14	5432	1509	164	SEG22	2828	1509
125	COM13	5368	1509	165	SEG23	2762	1509
126	COM12	5302	1509	166	SEG24	2698	1509
127	COM11	5238	1509	167	SEG25	2632	1509
128	COM10	5172	1509	168	SEG26	2568	1509
129	COM9	5108	1509	169	SEG27	2502	1509
130	COM8	5042	1509	170	SEG28	2438	1509
131	COM7	4978	1509	171	SEG29	2372	1509
132	COM6	4912	1509	172	SEG30	2308	1509
133	COM5	4848	1509	173	SEG31	2242	1509
134	COM4	4782	1509	174	SEG32	2178	1509
135	COM3	4718	1509	175	SEG33	2112	1509
136	COM2	4652	1509	176	SEG34	2048	1509
137	COM1	4588	1509	177	SEG35	1982	1509
138	COM0	4522	1509	178	SEG36	1918	1509
139	COMS1	4458	1509	179	SEG37	1852	1509
140	DUMMY	4388	1509	180	SEG38	1788	1509
141	DUMMY	4322	1509	181	SEG39	1722	1509
142	SEG0	4258	1509	182	SEG40	1658	1509
143	SEG1	4192	1509	183	SEG41	1592	1509
144	SEG2	4128	1509	184	SEG42	1528	1509
145	SEG3	4062	1509	185	SEG43	1462	1509
146	SEG4	3998	1509	186	SEG44	1398	1509
147	SEG5	3932	1509	187	SEG45	1332	1509
148	SEG6	3868	1509	188	SEG46	1268	1509
149	SEG7	3802	1509	189	SEG47	1202	1509
150	SEG8	3738	1509	190	SEG48	1138	1509
151	SEG9	3672	1509	191	SEG49	1072	1509
152	SEG10	3608	1509	192	SEG50	1008	1509
153	SEG11	3542	1509	193	SEG51	942	1509
154	SEG12	3478	1509	194	SEG52	878	1509
155	SEG13	3412	1509	195	SEG53	812	1509
156	SEG14	3348	1509	196	SEG54	748	1509
157	SEG15	3282	1509	197	SEG55	682	1509
158	SEG16	3218	1509	198	SEG56	618	1509
159	SEG17	3152	1509	199	SEG57	552	1509
160	SEG18	3088	1509	200	SEG58	488	1509

PAD	Symbol	X (µm)	Y (µm)
201	SEG59	422	1509
202	SEG60	358	1509
203	SEG61	292	1509
204	SEG62	228	1509
205	SEG63	162	1509
206	SEG64	98	1509
207	SEG65	32	1509
208	SEG66	–32	1509
209	SEG67	–98	1509
210	SEG68	–162	1509
211	SEG69	–228	1509
212	SEG70	–292	1509
213	SEG71	–358	1509
214	SEG72	–422	1509
215	SEG73	–488	1509
216	SEG74	–552	1509
217	SEG75	–618	1509
218	SEG76	–682	1509
219	SEG77	–748	1509
220	SEG78	–812	1509
221	SEG79	–878	1509
222	SEG80	–942	1509
223	SEG81	–1008	1509
224	SEG82	–1072	1509
225	SEG83	–1138	1509
226	SEG84	–1202	1509
227	SEG85	–1268	1509
228	SEG86	–1332	1509
229	SEG87	–1398	1509
230	SEG88	–1462	1509
231	SEG89	–1528	1509
232	SEG90	–1592	1509
233	SEG91	–1658	1509
234	SEG92	–1722	1509
235	SEG93	–1788	1509
236	SEG94	–1852	1509
237	SEG95	–1918	1509
238	SEG96	–1982	1509
239	SEG97	–2048	1509
240	SEG98	–2112	1509

PAD	Symbol	X (µm)	Y (µm)
241	SEG99	–2178	1509
242	SEG100	–2242	1509
243	SEG101	–2308	1509
244	SEG102	–2372	1509
245	SEG103	–2438	1509
246	SEG104	–2502	1509
247	SEG105	–2568	1509
248	SEG106	–2632	1509
249	SEG107	–2698	1509
250	SEG108	–2762	1509
251	SEG109	–2828	1509
252	SEG110	–2892	1509
253	SEG111	–2958	1509
254	SEG112	–3022	1509
255	SEG113	–3088	1509
256	SEG114	–3152	1509
257	SEG115	–3218	1509
258	SEG116	–3282	1509
259	SEG117	–3348	1509
260	SEG118	–3412	1509
261	SEG119	–3478	1509
262	SEG120	–3542	1509
263	SEG121	–3608	1509
264	SEG122	–3672	1509
265	SEG123	–3738	1509
266	SEG124	–3802	1509
267	SEG125	–3868	1509
268	SEG126	–3932	1509
269	SEG127	–3998	1509
270	SEG128	–4062	1509
271	SEG129	–4128	1509
272	SEG130	–4192	1509
273	SEG131	–4258	1509
274	DUMMY	–4322	1509
275	DUMMY	–4338	1509
276	COM48	–4458	1509
277	COM49	–4522	1509
278	COM50	–4588	1509
279	COM51	–4652	1509
280	COM52	–4718	1509

PAD	Symbol	X (µm)	Y (µm)
281	COM53	–4782	1509
282	COM54	–4848	1509
283	COM55	–4912	1509
284	COM56	–4978	1509
285	COM57	–5042	1509
286	COM58	–5108	1509
287	COM59	–5172	1509
288	COM60	–5238	1509
289	COM61	–5302	1509
290	COM62	–5368	1509
291	COM63	–5432	1509
292	COM64	–5498	1509
293	DUMMY	–5562	1509
294	DUMMY	–5535	693
295	COM65	–5535	628
296	COM66	–5535	563
297	COM67	–5535	498
298	COM68	–5535	433
299	COM69	–5535	368
300	COM70	–5535	303
301	COM71	–5535	238
302	COM72	–5535	173
303	COM73	–5535	108

PAD	Symbol	X (µm)	Y (µm)
304	COM74	–5535	43
305	COM75	–5535	–22
306	COM76	–5535	–87
307	COM77	–5535	–152
308	COM78	–5535	–217
309	COM79	–5535	–282
310	COM80	–5535	–347
311	COM81	–5535	–412
312	COM82	–5535	–477
313	COM83	–5535	–542
314	COM84	–5535	–607
315	COM85	–5535	–672
316	COM86	–5535	–737
317	COM87	–5535	–802
318	COM88	–5535	–867
319	COM89	–5535	–932
320	COM90	–5535	–997
321	COM91	–5535	–1062
322	COM92	–5535	–1127
323	COM93	–5535	–1192
324	COM94	–5535	–1257
325	COM95	–5535	–1322
326	COMS0	–5535	–1387

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