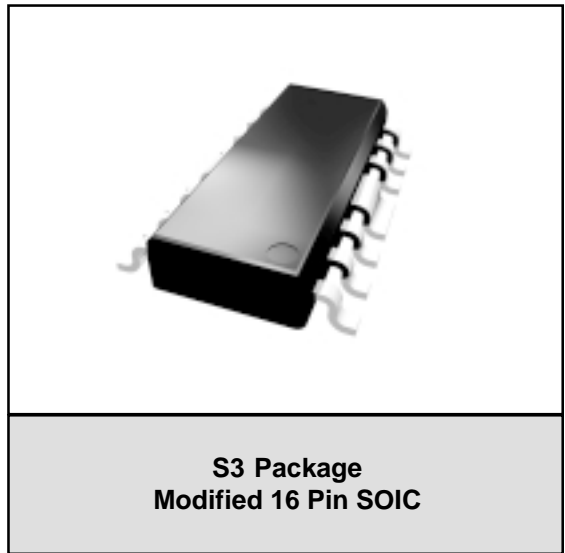## FEATURES
- 12 dB Gain
- Balanced Design
- High Linearity
- Low Noise Figure
- Single Supply Operation
- Wide Bandwidth
- -40 to +85 °C

APPLICATIONS
- Driver Amplifier
- CATV - Distribution / Drop Amplifiers
- Set Top Boxes
- Home Gateway

S3 Package
Modified 16 Pin SOIC

PRODUCT DESCRIPTION

The ABA3100 is a monolithic IC intended for use in applications requiring high linearity, such as Cellular Telephone Base Station Driver Amplifiers, CATV Fiber Receiver and Distribution Amplifiers, CATV Drop Amplifiers, CATV Set Top Boxes and Home Gateways.

Offered in a modified 16 lead surface mount SOIC package, it is well suited for use in amplifiers where small size, reduced component count, and high reliability are important.
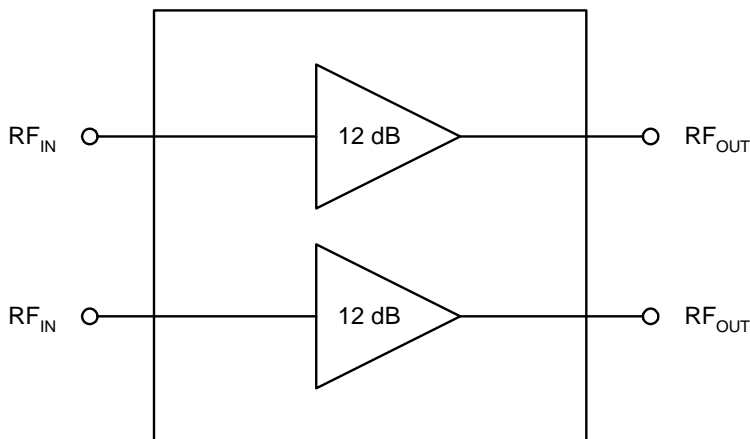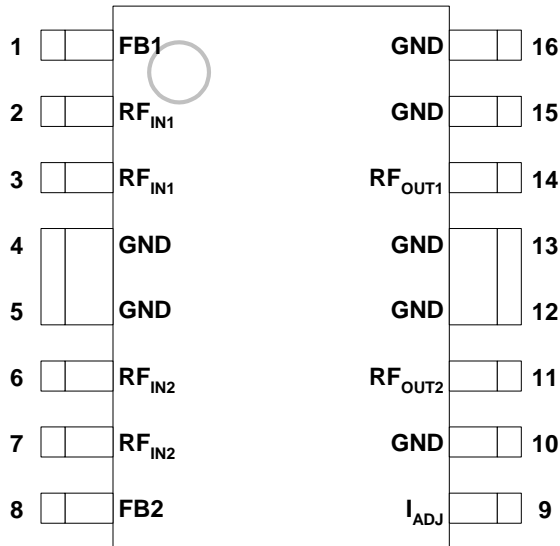

Figure 1: Block Diagram

Figure 2: Pin Out

Table 1: Pin Description

PIN	NAME	DESCRIPTION	PIN	NAME	DESCRIPTION
1	FB1	Feedback for Amplifier A1	9	I_{ADJ}	Current Adjust
2	RF_{IN1}	RF Input of Amplifier A1	10	GND	Ground
3	RF_{IN1}	RF Input of Amplifier A1	11	RF_{OUT2}	RF Output of Amplifier A2
4	GND	Ground	12	GND	Ground
5	GND	Ground	13	GND	Ground
6	RF_{IN2}	RF Input of Amplifier A2	14	RF_{OUT1}	RF Output of Amplifier A1
7	RF_{IN2}	RF Input of Amplifier A2	15	GND	Ground
8	FB2	Feedback for Amplifier A2	16	GND	Ground

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ELECTRICAL CHARACTERISTICS

Table 2: Absolute Minimum and Maximum Ratings

PARAMETER	MIN	MAX	UNIT
Analog Supply (pins 11, 14)	0	+12	VDC
RF Power at Inputs (pins 2, 3, 6, 7)	-	+10	dBm
Storage Temperature	- 65	+150	°C
Soldering Temperature	-	260	°C
Soldering Time	-	5	sec

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability.
Notes:
1. Pins 1, 2, 3, 6, 7 and 8 should be AC-coupled. No external DC bias should be applied.
2. Pin 9 should be AC-grounded. No external DC bias should be applied.

Table 3: Operating Ranges

PARAMETER	MIN	TYP	MAX	UNIT
RF Input / Output Frequency	50	-	1000	MHz
Analog Supply: V_{DD} (pins 11, 14)	+4.5	+5	+9	VDC
Case Temperature: T_A	-40	-	+85	°C

The device may be operated safely over these conditions; however, parametric performance is guaranteed only over the conditions defined in the electrical specifications.

Table 4: Electrical Specifications
(T_A = +25 °C, V_{DD} = + 5 VDC, Test System = 75Ω)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Gain	11	12	14	dB	
Noise Figure	- - -	2.5 2.7 3.2	3.0 3.5 4.0	dB	50 - 350 MHz 350 - 550 MHz 550 - 860 MHz
Input / Output Return Loss	10	18	-	dB	
CSO [1]	-	-72	-70	dBc	
CTB [1]	-	-75	-73	dBc	
2nd Order output Intercept Point (OIP2) [2]	-	+60	-	dBm	
3rd Order Output Intercept Point (OIP3) [2]	-	+35	-	dBm	
Thermal Resistance	-	-	33	ºC/W	
Current Consumption	120	150	170	mA	

Notes:
(1) 132 channels, +25dBmV per channel (measured at the output), 6MHz channel spacing
(2) Two tones: 397 MHz and 403 MHz, +4dBm per tone

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PERFORMANCE DATA

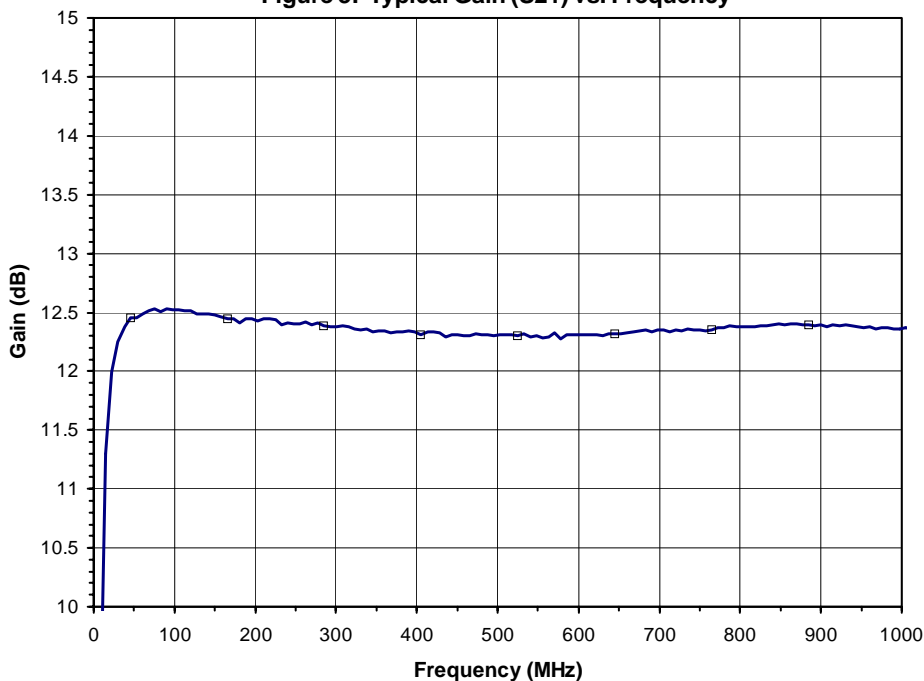**Figure 3: Typical Gain (S21) vs. Frequency**

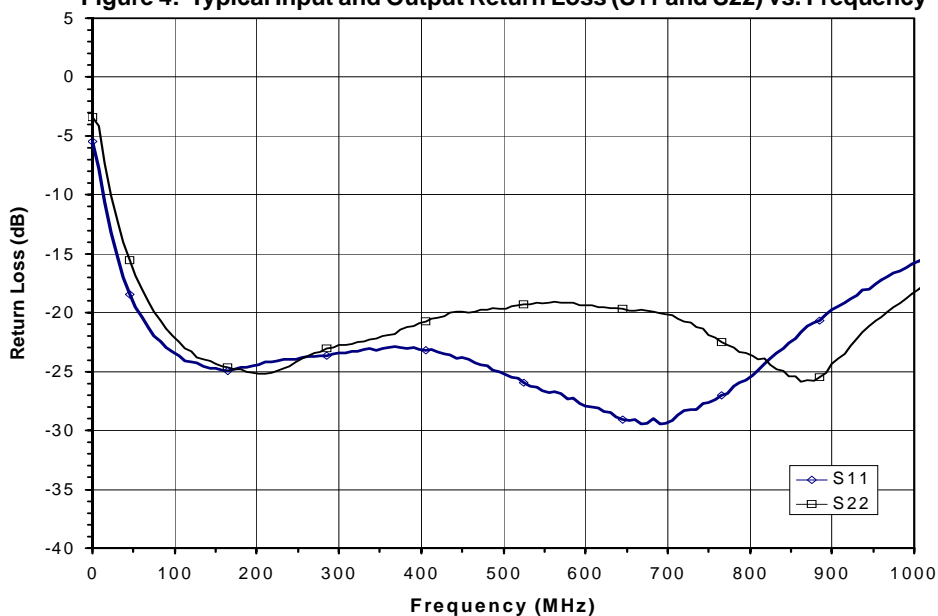**Figure 4: Typical Input and Output Return Loss (S11 and S22) vs. Frequency**

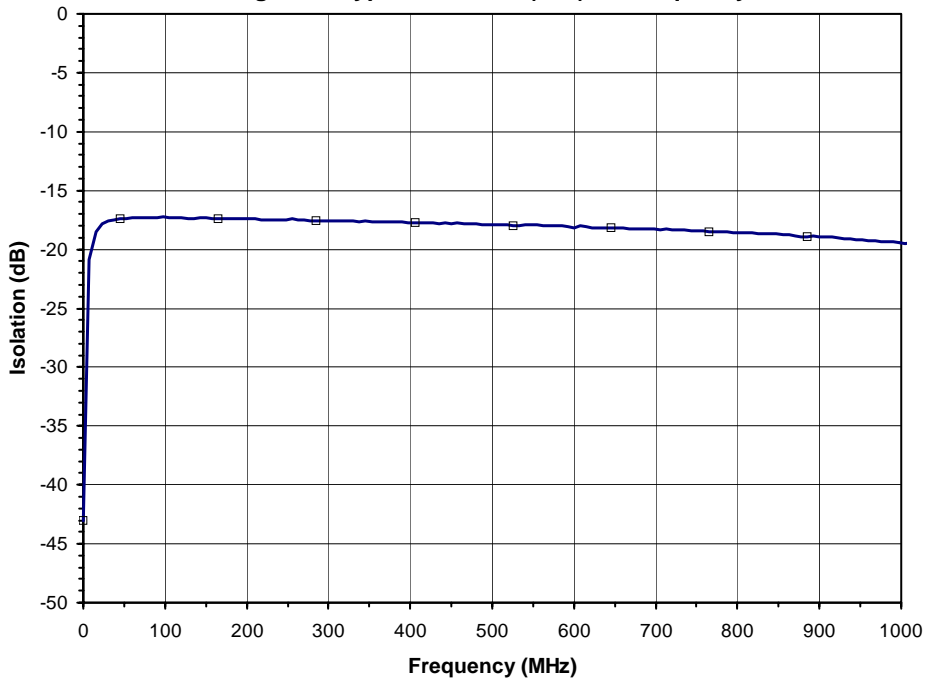**Figure 5: Typical Isolation (S12) vs. Frequency**

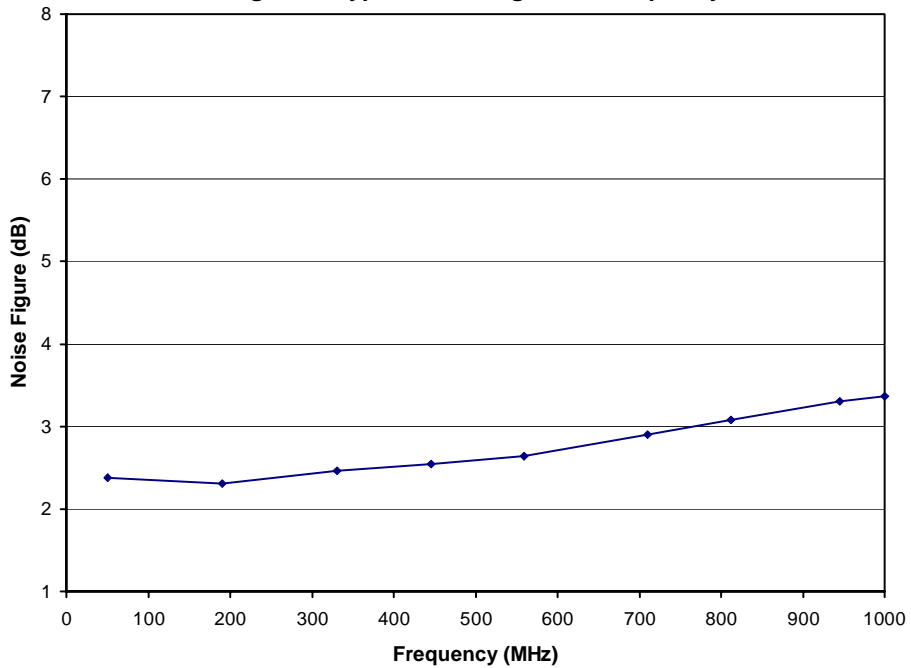**Figure 6: Typical Noise Figure vs. Frequency**

Data Sheet - Rev 2.3
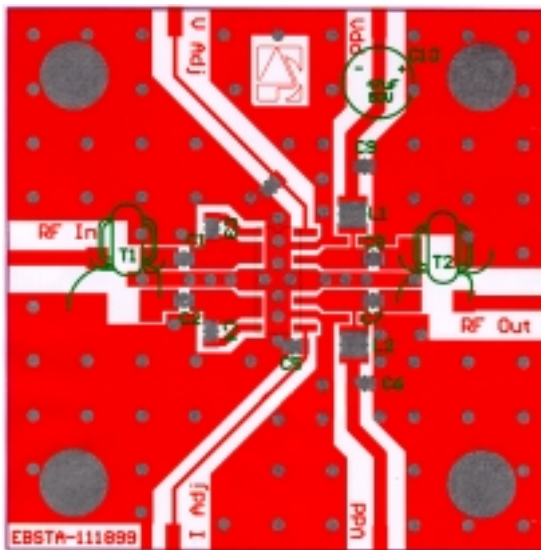*10/2002*

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APPLICATION INFORMATION
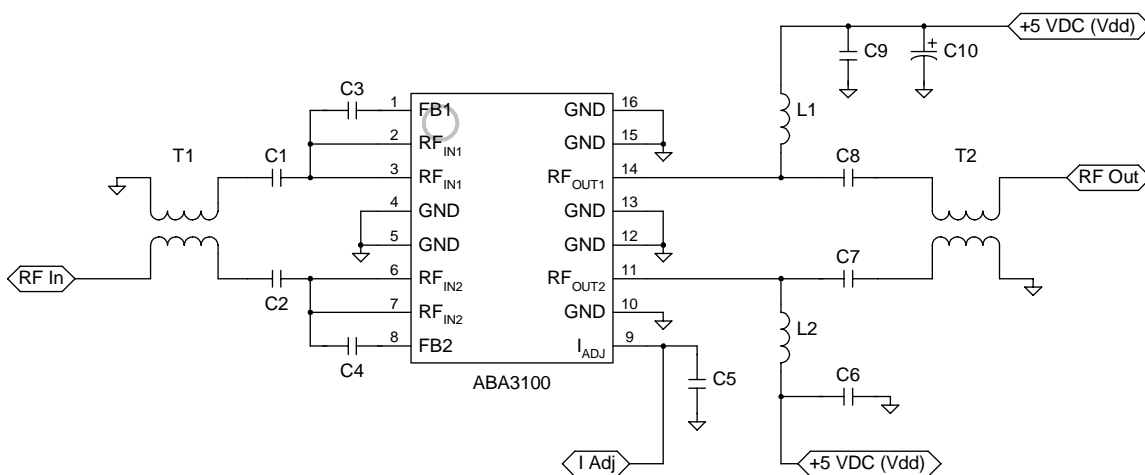

Figure 7: Evaluation Board Layout

**Figure 8: Evaluation Board Schematic**

Table 5: Evaluation Board Parts List

ITEM	DESCRIPTION	QTY	VENDOR	VENDOR PART NUMBER
C1-C4, C6, C9	0.01uF CHIP CAP.	6	MURATA	GRM39X7R1103K25V
C7, C8	470 pF CHIP CAP.	2	MURATA	GRM39COG471J25V
C10	47 uF ELEC. CAP.	1	DIGI-KEY CORP	P5275-ND
C5, C11	(not installed)			
L1, L2	390 nH CHIP INDUCTOR	2	COILCRAFT	1008CS-391XKBC
CONNECTORS	75 OHMS N MALE PANEL MOUNT	2	PASTERNACK ENTERPRISES	PE4504
T1, T2	BALUN	2	PULSE ENGINEERING	CX2024
	PCB	1	STANDARD PRINTED CIRCUITS, INC.	EBSTA-111899

Notes:
1. *"N" Connector center pin should be approximately 80 mils in length.*
2. *Connector tabs must be reduced by 150 mils.*
3. *Device must be soldered on PC board.*

PACKAGE OUTLINE
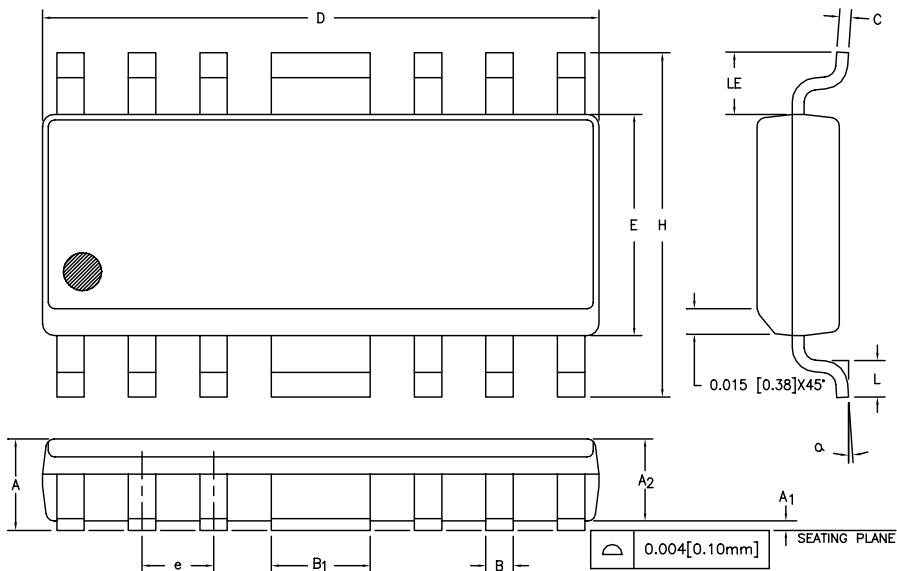
SYMBOL	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	0.058	0.068	1.47	1.73	
A1	0.004	0.010	0.10	0.25	
A2	0.055	0.065	1.40	1.65	
B	0.013	0.020	0.33	0.50	
B1	0.062	0.070	1.58	1.78	
C	0.008	0.010	0.20	0.25	4
D	0.380	0.400	9.66	10.16	2
E	0.150	0.160	3.81	4.06	3
e	0.050 BSC		1.27 BSC		
H	0.226	0.244	5.74	6.20	
L	0.016	0.040	0.41	1.02	
LE	0.030	——	0.76	——	
α	0°	8°	0°	8°	

NOTES:

1. CONTROLLING DIMENSION: INCHES

2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.006 [0.15mm] PER SIDE.

3. DIMENSION "E" DOES NOT INCLUDE INTER−LEAD FLASH OR PROTRUSIONS. INTER−LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.010 [0.25mm] PER SIDE.

4. MAXIMUM LEAD TWIST/SKEW TO BE ±0.005 [0.13mm].

5. LEAD THICKNESS AFTER PLATING TO BE 0.013 [0.33mm] MAXIMUM.

Figure 9: S3 Package Outline - Modified 16 Pin SOIC

NOTES

Data Sheet - Rev 2.3
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NOTES

ORDERING INFORMATION

ORDER NUMBER	TEMPERATURE RANGE	PACKAGE DESCRIPTION	COMPONENT PACKAGING
ABA3100S3P1	-40 to +85 °C	Modified 16 Pin SOIC	3,500 piece Tape and Reel
ABA3100S3P0	-40 to +85 °C	Modified 16 Pin SOIC	Plastic tubes (50 pieces per tube)

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