Programmable Peripheral
PSD5XX Family
Field-Programmable Microcontroller Peripherals

Key Features

- Complete family of Field Programmable Microcontroller Peripherals enables the user to efficiently implement a highly integrated embedded control system in a short time. The PSD5XX family has a variety of functions such as ZPLDs , I/O Ports, Counter/Timers, Interrupt Controller, Power Management, EPROM and SRAM.
- "No Glue-Logic" user programmable interface to 8 or 16 bit microcontroller multiplexed and non-multiplexed bus. The bus control logic can directly decode control signals generated by 8031, 80196, 80186, 68HC11, 68HC16, 683XX, 16000, Z80, and Z8 architecture. Extended address capability up to 24 bits of address.
- A range of ZPLD (Zero Power PLD) architectures have up to 30 macrocells, 61 inputs and 140 output product terms. Includes 3 functional ZPLDs which enable the user to efficiently implement a variety of state machines, logic functions, address decoding and control of the internal PSD5XX functional blocks .
- The ZPLDs use a Zero Power CMOS technology that reduces the device standby current to 10 µA typical. Unused product terms are disabled to reduce operating power.
- Up to 40 I/O Ports that can be individually configured by the user as standard MCU I/O ports, PLD I/O, latched address outputs and special function I/O. Two eight bit I/O ports can be configured as Open Drain Outputs.
- Four 16 bit Counter/Timers, that have 5 modes of operation and can be controlled by the Peripheral PLD (PPLD) macrocells. Modes of operation are pulse, waveform, time capture, event counting and watch dog timer (or Real Time Clock). The Counter/Timer clock input has a prescaler that can scale the input frequency from 4 to 280.
- Eight input priority encoded Interrupt Controller. Four interrupts are generated by the PPLD and are user defined. The other four interrupts are generated by the Counter/Timers Terminal Count flags. Each interrupt input can be individually masked and configured as edge or level sensitive.
- The PSD5XX family contains EPROM densities of 256 Kbit, 512 Kbit and 1 Mbit that can be configured as 8 or 16 bit data width. The EPROM is divided into 4 equal blocks that can be mapped to different address spaces. Access time is 70 ns which includes address latching and Decoder PLD (DPLD) decoding. The EPROM has a low power mode that is controlled by the CMiser-Bit.
- The PSD5XX family contains a 16Kbit standby SRAM that can be configured as 8 or 16 bit data width. Access time is 70 ns which includes address latching and Decoder PLD (DPLD) decoding. The SRAM can be used as standby storage if standby power is supplied to the Vstby pin. Switching between V_{CC} and Vstby occurs automatically.
- Page Logic is connected to the ZPLDs and enables address space expansion of Microcontrollers with limited address space capability. Up to 16 pages are available.

Key Features (Cont.)

- A security bit prevents reading the PSD5XX configuration, ZPLD and EPROM contents. This inhibits copying the device on a programmer.
- Port A can be used as a buffered microcontroller data bus (Peripheral I/O Mode) of the microcontroller bus. This provides easy access to sub-systems that require more drive on the data bus or accessing a resource that is shared by another MCU or DMA Controller.
- Low power operation is achieved by using a Power Management Unit (PMU) that enables automatic standby modes in the EPROM, SRAM, and ZPLDs. It also disables the clock to the ZPLD and Counter/Timer. Also available is an automatic power down mode using the ALE signal. A Sleep mode is available that consumes only 10 µA standby power consumption.
- PSD5XX standard versions are ideal for general purpose applications.
- PSD5XXM mask-programmable versions are ideal for code-stable, high-volume low cost applications.
- Package choices include 68 pin plastic (J) and ceramic (L) chip carriers.
- The PSD5XX family is supported with PC based PSDsoft™ MS-Windows® compatible development tools. Offering ABEL® as a design entry method, (PSDabel™), an efficient Fitter, Address Translator, MagicPro® programmer and a full chip simulator (PSDsilos III™) are included.

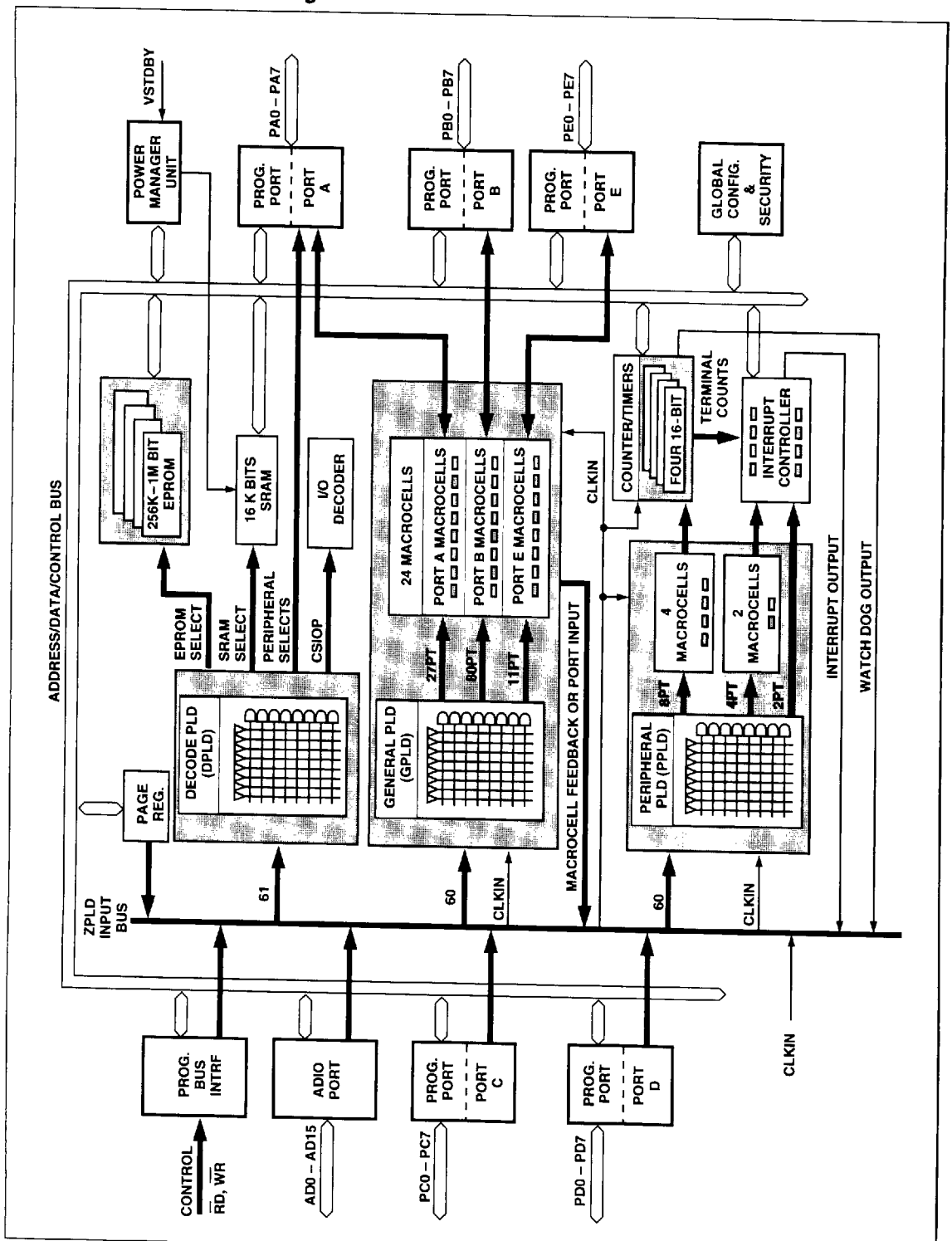
General Description

The PSD5XX series of Field Programmable Microcontroller Peripherals represent a major advance in the evolution of Programmable Peripherals. They combine an innovative architecture with state of the art technology to provide user programmability (logic, functions, memory), flexibility, high integration, optimum performance, low power . For example, the PSD513B1 can implement a full peripheral subsystem and has the following features:

- Three ZPLDs with a total of 61 inputs, 140 product terms outputs, 30 macrocells and 24 I/O pins.
- 40 individually programmable I/O pins that are divided into 5 Ports.
- Four 16-bit Peripheral PLD (PPLD)-controlled Counter/Timers that can perform pulse, waveform, time capture, event counting and watch dog functions.
- Eight input priority encoded Interrupt Controller. Four interrupts are generated by the Counter/Timer unit and the other four can be user defined through the PPLD.
- 4-Bit Page Register
- 1 Mbit Reprogrammable EPROM consists of four 256 Kbit blocks.
- 16 Kbit of standby SRAM that can automatically switch into standby mode.
- Power management unit with automatic standby and sleep modes.
- Security mode.

Figure 1 is a top level block diagram of the PSD5XX. Refer to Table 1 and other sections for details on functionality, DC/AC specification, packages and ordering information.

Figure 1. PSD5XX Block Diagram



General Description (Cont.)

At the core of the PSD5XX are dedicated ZPLDs based on the functions they perform:

- ❑ **Decoding ZPLD (DPLD)**
- ❑ **General Purpose ZPLD (GPLD)**
- ❑ **Peripheral ZPLD (PPLD)**

All ZPLDs receive the same inputs through the ZPLD bus and are differentiated by their output destinations. The Decoder PLD (DPLD) has as its main function to perform address space decoding for the internal I/O Ports, Peripherals, four blocks of EPROM, standby SRAM and peripheral mode of Port A. The address decoding can be based on any address input, control signal ($\overline{RD}$, $\overline{PSEN}$, etc.) and page logic. Address inputs originate from either the microcontroller interface (ADIO Port) or other I/O Ports for additional decoding. The DPLD also supports special requirements of 8031 architecture based designs that need to store data in the EPROM or execute programs from the SRAM.

The general purpose PLD (GPLD) is a general purpose ZPLD that can be used to implement state machines and logic . The GPLD has up to 61 inputs, 118 product terms, 24 flexible macrocells and 24 I/O pins that are connected to Ports A, B and E. The GPLD can also decode the microcontroller address bus and generate chip selects to external peripherals or memories.

The peripheral PLD (PPLD) generates outputs to the Counter/Timer unit and the Interrupt Controller. The PPLD outputs to the Counter/Timer enable, disable or trigger counting or time capture. This unique capability enables the user to implement in the PPLD the exact conditions for the timer to count or generate an output. The PPLD also generates four outputs to the Interrupt Controller which enables the user to define the exact conditions for interrupt generation.

The ZPLDs are designed to consume minimum power using Zero Power design techniques. A configuration bit (Turbo bit), that can be set by the MCU, will automatically place the ZPLDs into standby if no inputs are changing. Any unused product terms will be turned off during programming and will not consume any power in the system.

The PSD5XX has 40 I/O pins that are divided into 5 ports. Each I/O pin can be individually configured to provide many functions. Ports A, B and E have the capability to be configured as standard MCU I/O ports, GPLD I/O, latched address outputs for multiplexed address/data controllers, or special function I/O (e. g., Counter/Timer and Interrupts). Ports C and D are standard I/O ports that can also be configured as ZPLD inputs or data bus for microcontrollers with non-multiplexed bus.

The PSD5XX can easily interface with no "glue-logic" to a variety of 8 and 16-bit microcontrollers with a multiplexed or non-multiplexed bus. All of the control signals are connected to the three ZPLDs enabling the user to generate timing and decoding signals for external peripherals. For controllers that do not have a Reset output, the PSD5XX can generate a RESET output based on its RESET input that includes hysteresis.

The Counter/Timer unit provides four 16 bit highly flexible Counter/Timers. Each Counter/Timer has five modes of operation: pulse, waveform, event counting, time capture and watchdog (Real Time Clock). Counter 2 can operate as a Watch Dog Timer. Each Counter/Timer can be programmed to count up or down. The inputs to the Counter/Timer unit, which enable/disable counting or triggering an operation, can originate from the PPLD or directly from the pins. The maximum operating frequency of each counter is 7.5 MHz. The input clock can be divided (up to 280) before driving the Counter/Timer unit using the 4 to 280 range prescaler .

General Description (Cont.)

The PSD5XX includes an 8 level priority encoded Interrupt Controller. The Interrupt Controller accepts 4 user defined interrupts and 4 Terminal Counts from the Counter/Timer. Each interrupt can be individually masked and configured to be level or edge sensitive. A 3 bit interrupt vector is generated that can be read by the microcontroller. The serviced interrupt will be cleared automatically after the microcontroller has read the interrupt vector.

The PSD5XX contains EPROM and scratchpad SRAM. The EPROM densities are 256K, 512K bit and 1M bit and are divided into four blocks. Each block can be located in a different address location. The access time of the EPROM includes the address latching and DPLD decoding. The 16 Kbit Standby SRAM may be used as an extension of the microcontroller SRAM and also to store backup information that is necessary after a system power down or power failure. Power to the SRAM is supplied by the Vstby pin. Switching between V_{CC} and Vstby occurs automatically when V_{CC} power is removed.

A four bit Page Register enables microcontrollers with limited address space easy access to the I/O Section, EPROM and SRAM . The Page Register outputs are connected to all ZPLDs and can be used to page external devices as well as the internal PSD5XX functional units.

A Power Management Unit (PMU) in the PSD5XX enables the user to control the power consumption on selected functional blocks based on system requirements. For microcontrollers that do not generate a Chip Select input (CSI) to the peripheral device, the PMU includes an Automatic Power Down unit (APD) that will turn off the PSD5XX (into standby or sleep mode) based on inactivity of the ALE. The polarity of ALE inactivity can be defined by the user. In addition to power down mode, the PSD5XX includes a SLEEP mode that will reduce the power consumption to 10 µA.

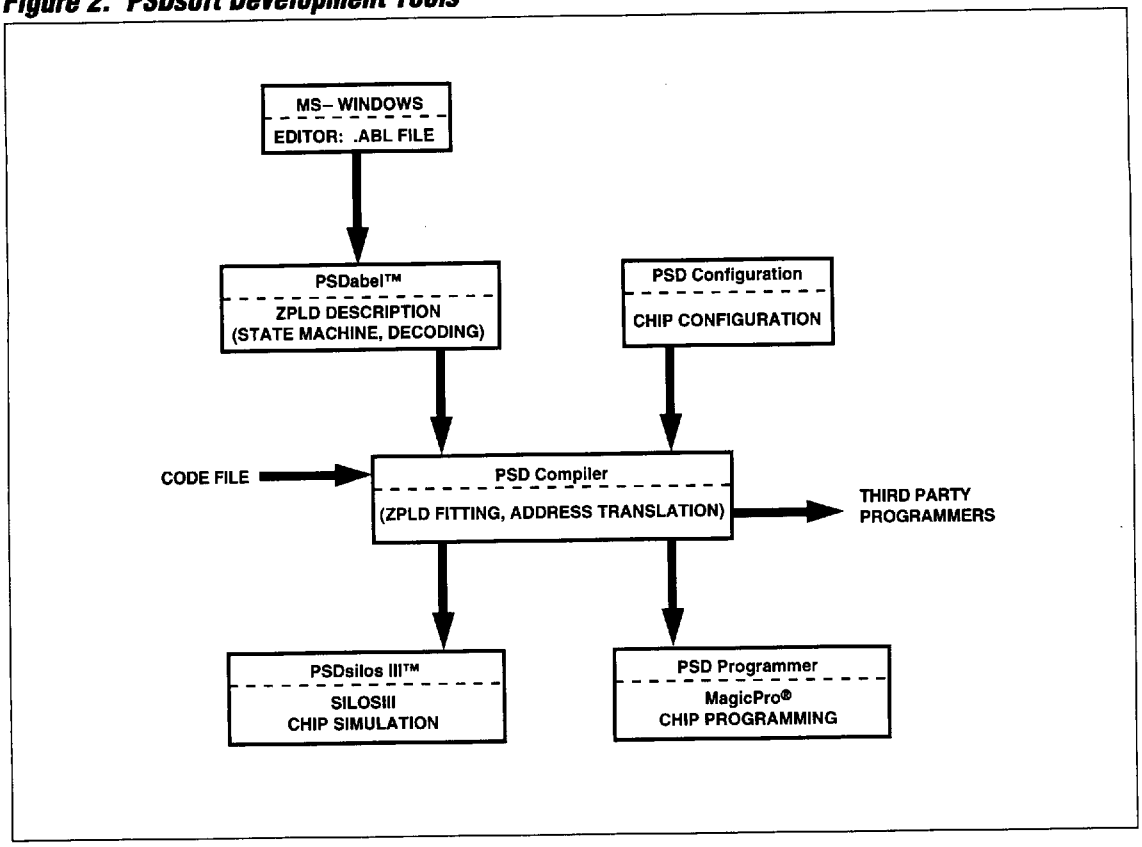
The PSD5XX family is supported by the PSD Development System (PSDsoft, see Figure 2) which runs under MS-Windows on the PC. Design entry is done using PSDabel which creates a minimized logic implementation. PSDabel also provides logic simulation of the ZPLD. The PSD5XX desired configuration is entered using a simple Window based menu. The PSD Compiler, which consists of a Fitter and Address Translator, generates an object file from the PSDabel and MCU code files. The object file can be down loaded to a programmer (MagicPro®, Data I/O or other third party) or to PSDsilos III providing full chip simulation.

The PSD5XX standard versions include up to 1 Mb of EPROM, 16 Kbit SRAM, Decode PLD (DPLD), General Purpose PLD (GPLD), Peripheral PLD (PPLD), four 16-bit Counter/Timers, an 8-level maskable Interrupt Controller and five 8-bit I/O Ports. They are ideal for general purpose embedded systems applications.

The PSD5XXM mask-programmable versions deliver the lowest cost PSD5XX solution. See the Masked-PSD Ordering Information chapter in this databook for the mask-programmable PSD5XXM ordering procedure.

References in this document to PSD5XX versions are generic and include PSD5XX and PSD5XXM products.

Figure 2. PSDsoft Development Tools



PSD5XX Family

There are 6 unique devices in the PSD5XX family. The part classifications are based on EPROM size and data bus width. The features of each part are listed in Table 1.

Table 1. PSD5XX Product Matrix

Part #	Bus Bit	DPLD + GPLD + PPLD			I/O Pins	Timers	Inter. Contr.	WD*	PMU	EPROM K bit	SRAM K bit
		Inputs	Product Terms	Registered Macrocells							
501B1	x8/x16	61	140	30	40	4 * 16	8	1 * 16	Yes	256	16
511B1	x8	61	140	30	40	4 * 16	8	1 * 16	Yes	256	16
502B1	x8/x16	61	140	30	40	4 * 16	8	1 * 16	Yes	512	16
512B1	x8	61	140	30	40	4 * 16	8	1 * 16	Yes	512	16
503B1	x8/x16	61	140	30	40	4 * 16	8	1 * 16	Yes	1024	16
513B1	x8	61	140	30	40	4 * 16	8	1 * 16	Yes	1024	16

WD = WatchDog Timer.
PMU = Power Management Unit.

*One of the four 16-Bit Timers.

Table 2. PSD5XX Pin Descriptions

The following table describes the pin names and pin functions of the PSD5XX. Pins that have multiple names and/or functions are defined by user configuration.

Pin Name	Pin Function	Type	Function Descriptions
ADIO0 – ADIO15	Address/ data bus	I/O	1. Address/data bus, multiplexed bus mode 2. Address bus, non-multiplexed bus mode
RD	Multiple Names 1. $\overline{\text{Read}}$ 2. $\overline{\text{E}}$ 3. $\overline{\text{DS}}$ 4. $\overline{\text{LDS}}$	I	Multiple functions 1. Read signal 2. E signal (Clock) 3. Data strobe signal 4. Low byte data strobe
WR	Multiple Names 1. $\overline{\text{WR}}$ 2. R/W 3. $\overline{\text{WRL}}$	I	Multiple functions 1. Write signal 2. Read-write signal 3. Low byte write signal
CSI	Chip Select Input	I	Active low, select PSD5XX. standby mode if high.
RESET	Reset Input	I	Reset I/O ports, ZPLD/macrocells, Timers and Configuration Registers. Active low.
CLKIN	Input clock	I	Clock input to Timers, ZPLD macrocells, ZPLD array, and APD counter; connect to ground if clock input not used.
PA0 – PA7	I/O Port A	I/O	Multiple functions 1. I/O port 2. ZPLD/macrocell I/O port 3. Latched address outputs (PA0–PA7) → (A0–A7) 4. High address inputs (A16 – A23) 5. Timer outputs (PA0 – PA3)
PB0 – PB7	I/O Port B	I/O	Multiple functions 1. I/O port 2. ZPLD/macrocell I/O port 3. Latched address outputs (PB0–PB7) → (A0–A7) or (A8–A15) 4. Timer outputs (PB0-PB3)
PC0 – PC7	I/O Port C	I/O CMOS or OD	Multiple functions 1. I/O port 2. ZPLD input port 3. Latched address outputs (PC0 – PC7) → (A0–A7) 4. Data Port (D0 – D7, non-multiplexed bus)
PD0 – PD7	I/O Port D	I/O CMOS or OD	Multiple functions 1. I/O port 2. ZPLD input port 3. Latched address outputs (PD0–PD7) → (A0–A7) or (A8–A15) 4. Data Port (D8-D15, non-multiplexed bus)

Table 2. PSD5XX Pin Descriptions (Cont.)

Pin Name	Pin Function	Type	Function Descriptions
PE0	Port PE, pin 0 1. $\overline{BHE}$ 2. $\overline{PSEN}$ 3. $\overline{WRH}$ 4. $\overline{UDS}$ 5. SIZ0 6. PE0 7. PE0 8. PE0	I/O	Multiple functions 1. High byte enable, 16 bit data 2. Read program memory, 8031 signal write high data byte 4. Upper Data Strobe 5. Byte enable, 68300 signal 6. I/O pin 7. ZPLD I/O pin 8. Latched Address Out – A0
PE1	Port PE, pin 1 1. ALE 2. PE1 3. PE1 4. PE1	I/O	Multiple functions 1. Address strobe 2. I/O pin 3. ZPLD I/O pin 4. Latched Address Out – A1
PE2	Port PE, pin 2 1. Intr Out 2. PE2 3. PE2 4. PE2	I/O	Multiple functions 1. Interrupt Controller Output 2. I/O pin 3. ZPLD I/O pin 4. Latched Address Out – A2
PE3	Port PE, pin 3 1. Timer0-In 2. PE3 3. PE3 4. PE3	I/O	Multiple functions 1. Timer0 control input 2. I/O pin 3. ZPLD I/O pin 4. Latched Address Out – A3
PE4	Port PE, pin 4 1. Timer1-In 2. PE4 3. PE4 4. PE4 5. TC0	I/O	Multiple functions 1. Timer1 control input 2. I/O pin 3. ZPLD I/O pin 4. Latched Address Out – A4 5. Timer0 Terminal Count
PE5	Port PE, pin 5 1. Timer2-In 2. PE5 3. PE5 4. PE5 5. TC1	I/O	Multiple functions 1. Timer2 control input 2. I/O pin 3. ZPLD I/O pin 4. Latched Address Out – A5 5. Timer1 Terminal Count
PE6	Port PE, pin 6 1. Timer3-In 2. PE6 3. PE6 4. PE6 5. TC2	I/O	Multiple functions 1. Timer3 control input 2. I/O pin 3. ZPLD I/O pin 4. Latched Address Out – A6 5. Timer2 Terminal Count
PE7	Port PE, pin 7 1. APD CLK 2. PE7 3. PE7 4. PE7 5. TC3	I/O	Multiple functions 1. Automatic Power Down Clock Input 2. I/O pin 3. ZPLD I/O pin 4. Latched Address Out – A7 5. Timer3 Terminal Count
VSTBY	VSTBY	I	SRAM power pin for standby operation (battery backup)
V_{CC}	V_{CC}	I	Chip V_{CC} power pin
GND	GND	I	Chip ground pin

The PSD5XX Architecture

PSD5XX consists of seven major functional blocks:

- ZPLD Block
- Bus Interface
- I/O Ports
- Memory Block
- Power Management Unit
- Counter/Timer
- Interrupt Controller

The functions of each block are described in the following sections. Many of the blocks perform multiple functions, and are user configurable. The chip configurations are specified by the user in the PSDsoft Development Software; some are specified by setting up the appropriate bits in the configuration registers during run time.

ZPLD Block

Key Features

- 3 Embedded ZPLD devices
- Maximum 30 macrocells
- Combinatorial/registered outputs
- Maximum 140 product terms
- Programmable output polarity
- User configured register clear/preset
- User configured register clock input
- 61 Inputs
- Accessible via 24 I/O pins
- Power Saving Mode
- UV-Erasable
- Generate user defined interrupts to Interrupt Controller and controls to Counter/Timer

General Description

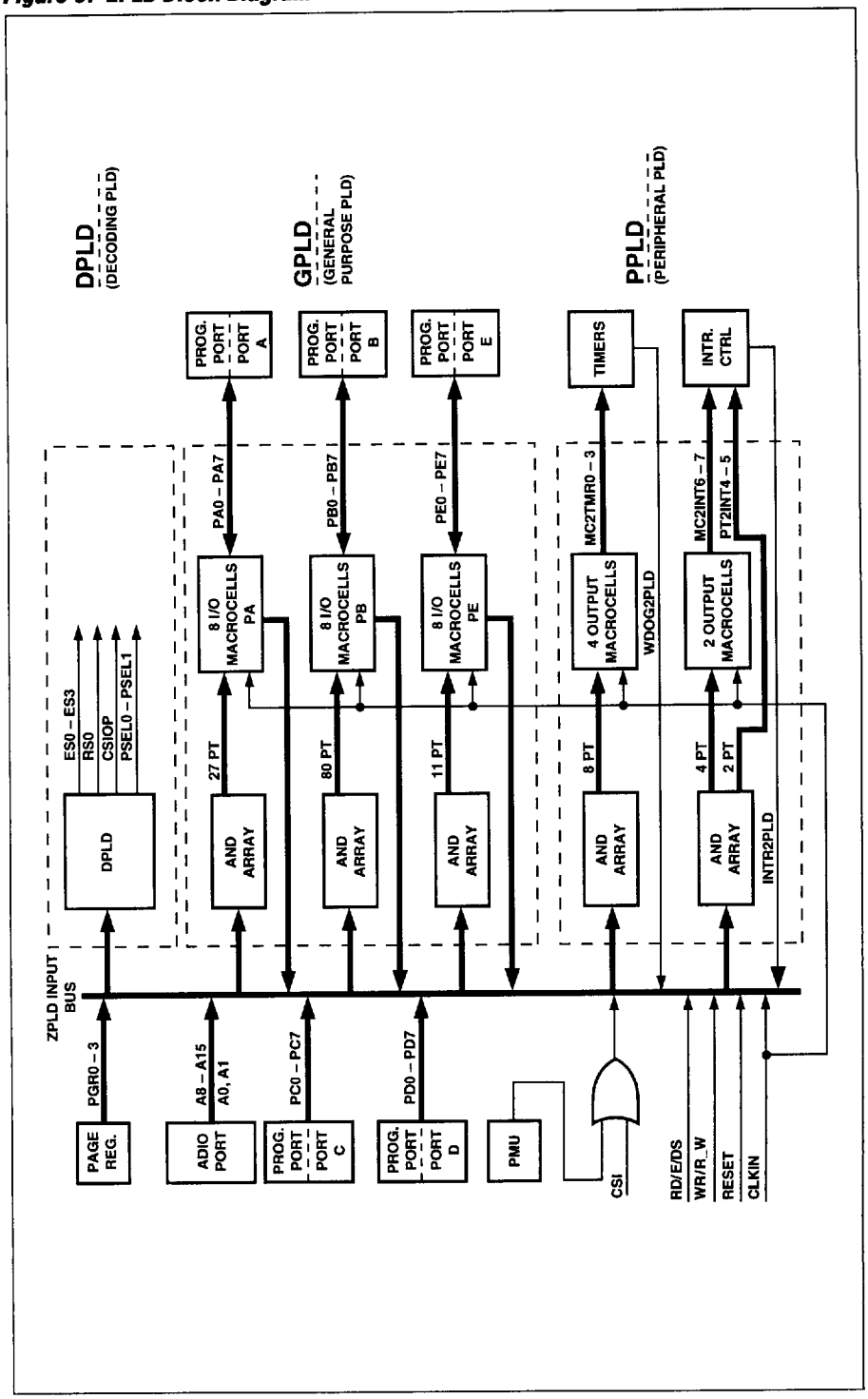
The ZPLD block has 3 embedded PLD devices:

- **DPLD**
  The Address Decoding PLD, generating select signals to internal I/O or memory blocks.
- **GPLD**
  The General Purpose PLD provides 24 programmable macrocells for general or complex logic implementation; dedicated to user application.
- **PPLD**
  The Peripheral PLD, includes 6 programmable macrocells. The PPLD provides control to the operation of the Counter/Timer and Interrupt Controller.

Figure 3 shows the architecture of the ZPLD. The PLD devices all share the same input bus. The true or complement of the 61 input signals are fed to the programmable AND-ARRAY. Names and source of the input signals are shown in Table 3. The PA, PB, PE signals, depending on user configuration, can either be macrocell feedbacks or inputs from Port A, B or E.

ZPLD Block
(Cont.)

Figure 3. ZPLD Block Diagram



ZPLD Block (Cont.)

Table 3. ZPLD Input Signals

Signal Name	From
PA0 – PA7	Port A inputs or Macrocell PA feedback
PB0 – PB7	Port B inputs or Macrocell PB feedback
PE0 – PE7	Port E inputs or Macrocell PE feedback
PC0 – PC7	Port C inputs
PD0 - PD7	Port D inputs
PGR0 – PGR3	Page Mode Register
WDOG2PLD	Counter/Timer
INTR2PLD	Interrupt Controller
A8 – A15, A0, A1	MCU Address Lines
RD/E/DS	MCU bus signal
WR/R_W	MCU bus signal
CLKIN	Input Clock
RESET	Reset input
CSI	$\overline{CSI}$ input (ORed with power down from PMU)

ZPLD Block (Cont.)

The DPLD

The DPLD is used for internal address decoding generating the following eight chip select signals:

- ***ES0 – ES3***
  EPROM selects, block 0 to block 3
- ***RS0***
  SRAM block select
- ***CSIOP***
  I/O Decoder chip select
- ***PSEL0 – PSEL1***
  Peripheral I/O mode select signals

The I/O Decoder enabled by the CSIOP generates chip selects for on-chip registers or I/O ports based on address inputs A[7:0].

As shown in Figure 4, the DPLD consists of a large programmable AND ARRAY. There are a total of 61 inputs and 8 outputs. Each output consists of a single product term. Although the user can generate select signals from any of the inputs, the select signals are typically a function of the address and Page Register inputs. The select signals, which are active High, are defined by the user in the ABEL file (PSDabel).

The address line inputs to the DPLD include A0, A1 and A8 – A15. If more address lines are needed, the user can bring in the lines through Port A to the DPLD.

The GPLD

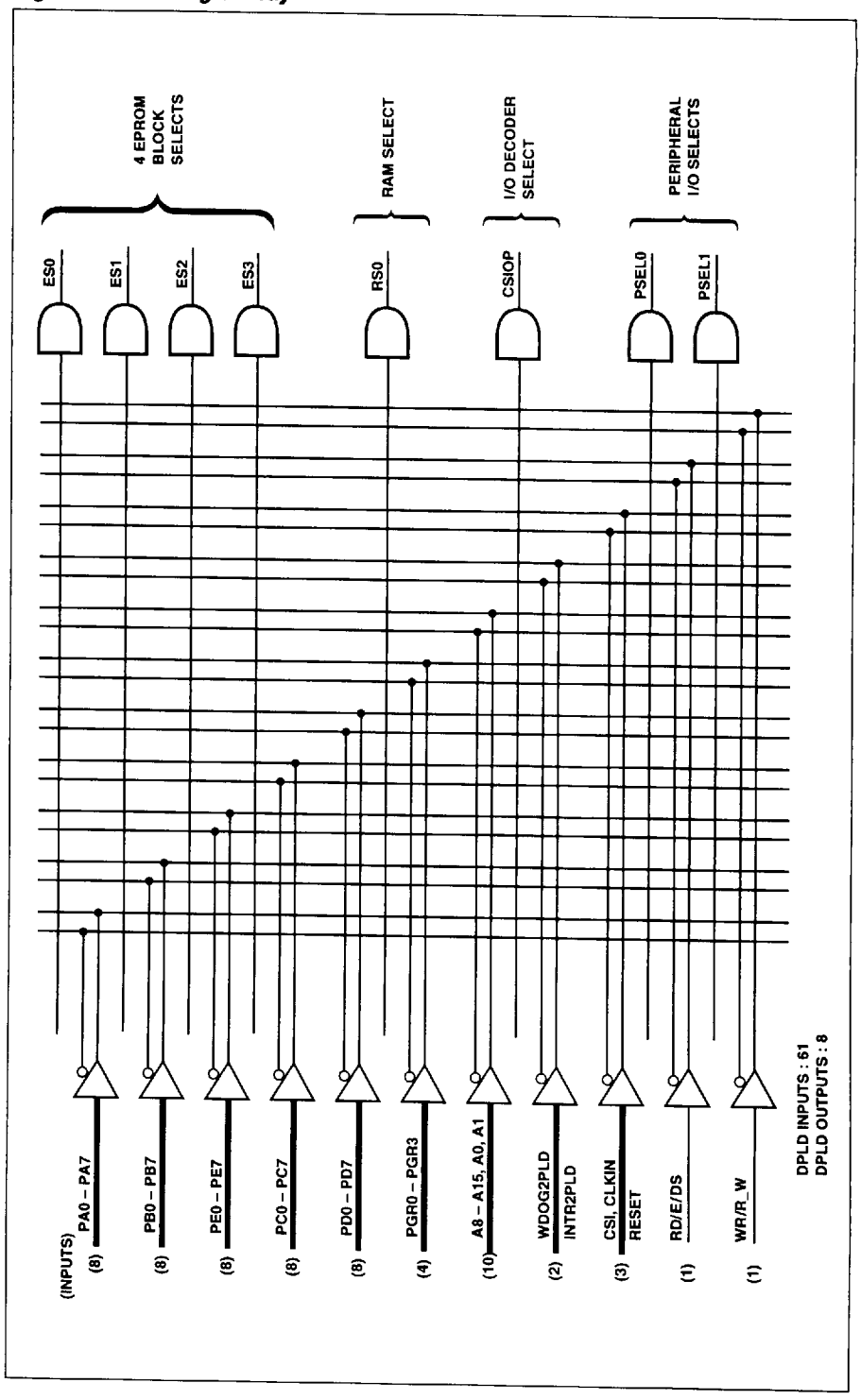
The structure of the General Purpose PLD consists of a programmable AND ARRAY and 3 sets of I/O Macrocells. The ARRAY has 61 input signals, same as the DPLD. From these inputs, "ANDed" functions are generated as product term inputs to the macrocells. The I/O Macrocell sets are named after the I/O Ports they are linked to, e.g., the macrocells connected to Port A are named PA Macrocells. The 3 sets of macrocells, PA, PB and PE, are similar in structure and function.

Figure 5 shows the output/input path of a GPLD macrocell to the Port pin with which it is associated. If the Port pin is specified as a GPLD output pin in PSDsoft, the MUX in the I/O Port Cell selects the GPLD macrocell as an output of the Port pin. The output enable signal to the buffer in the I/O cell can be controlled by a product term from the AND ARRAY.

If the Port pin is specified as a ZPLD input pin, the MUX in the GPLD macrocell selects the Port input signal to be one of the 61 signals in the ZPLD Input Bus.

ZPLD Block
(Cont.)

Figure 4. DPLD Logic Array



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ZPLD Block (Cont.)

Port A Macrocell Structure

Figure 5a shows the PA Macrocell block, which consists of 8 identical macrocells. Each macrocell output can be connected to its own I/O pin on Port A. There are 3 user programmable global product terms output from the GPLD's AND ARRAY which are shared by all the macrocells in Port A:

- **PA.OE**
  Enable or tri-state Port A output pins
- **PA.PR**
  Preset D flip flop in the macrocells
- **PA.RE**
  Reset/Clear D flip flop in the macrocells

Two other inputs, CLKIN and MACRO-RST, are used as clock and clear inputs to the D flip flop. The CLKIN comes directly from the CLKIN input pin. The MACRO-RST is the same as the Reset input pin except it is user configurable.

The circuit of a Port A Macrocell is shown in Figure 6. There are 6 product terms from the GPLD's AND ARRAY as inputs to the macrocell. Users can select the polarity of the output, and configure the macrocell to operate as:

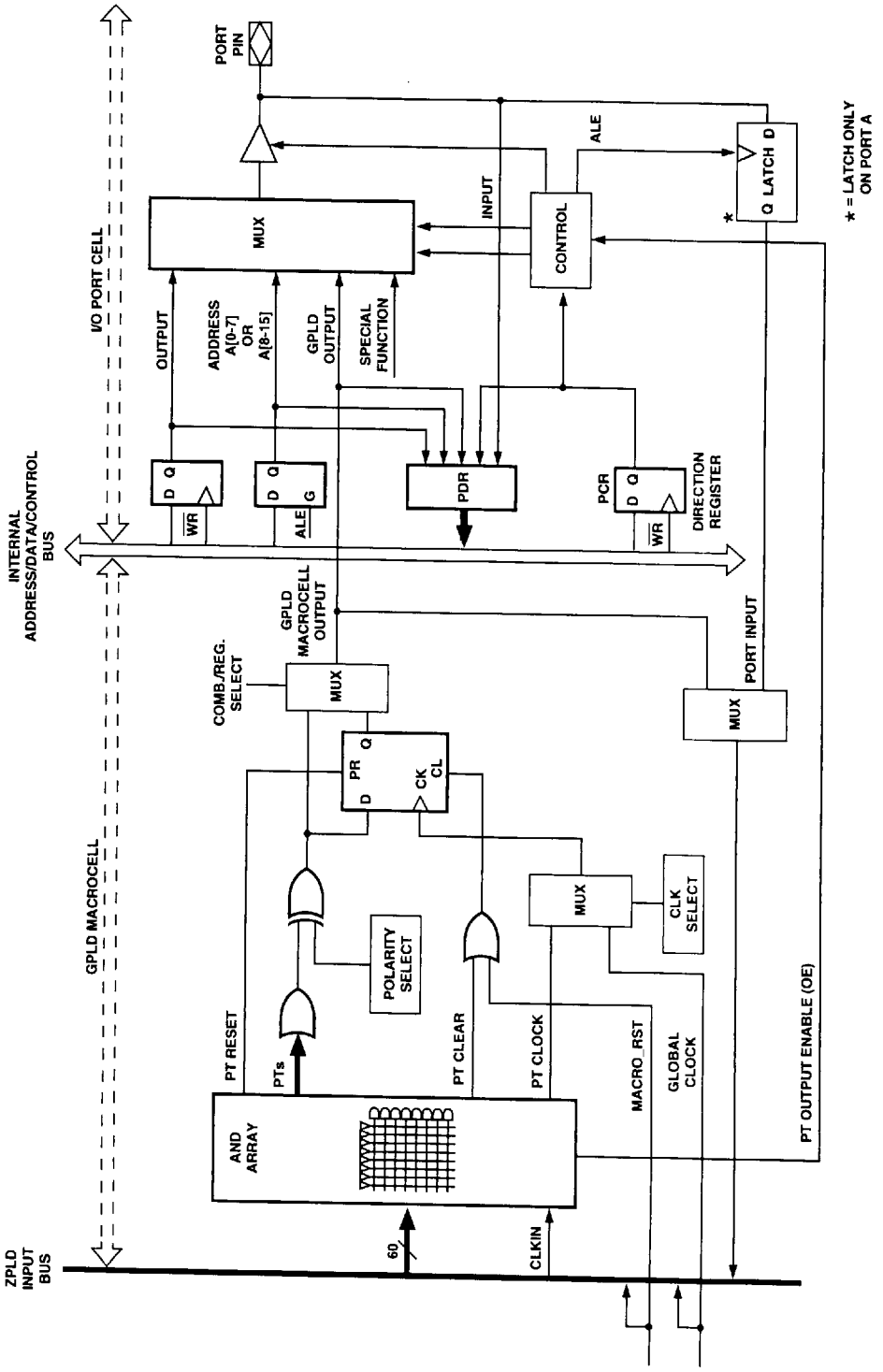
- **Registered Output**
  Select output from D flip flop
- **Combinatorial Output**
  Select output from OR gate
- **GPLD Input**
  Use Port A pin as dedicated input
- **GPLD Output**
  Use Port A pin as dedicated output
- **GPLD I/O**
  Use Port A pin as bidirectional pin
- **Macrocell Feedback**
  Register feedback for state machine implementations or expander feedback from the combinatorial output, to expand the number of product terms available to another macrocell.

  In case of "Buried Feedback", where the output of the macrocell is not connected to a Port A pin, Port A can be configured to perform other user defined I/O functions.

The two global product terms assigned for asynchronous clear (PA.RE) and preset (PA.PR) are mainly for proper Port A Macrocell initialization. The macrocell flip-flop can also be cleared during reset by MACRO-RST, if such an option is chosen. The clock source is always the input clock CLKIN.

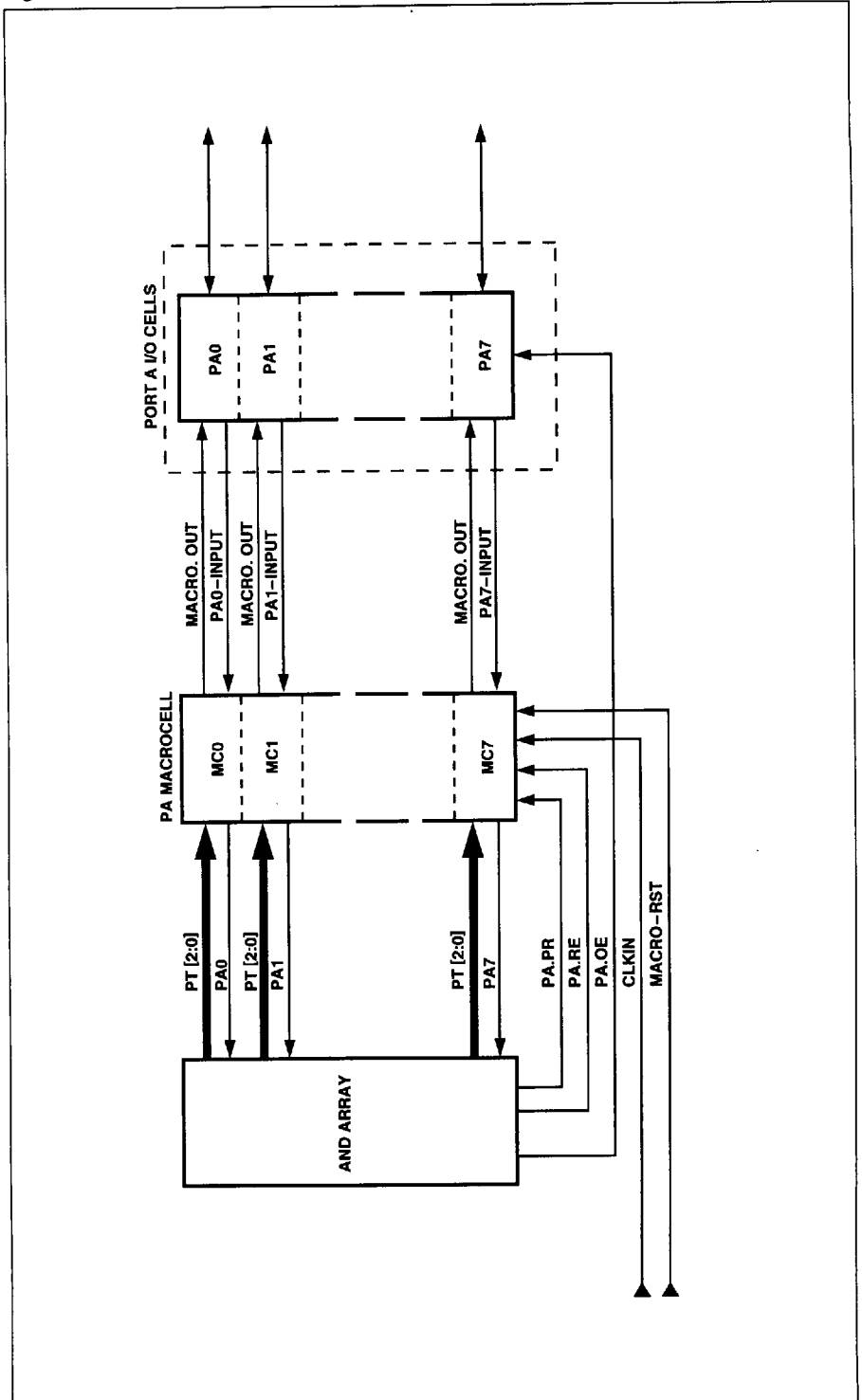
ZPLD Block (Cont.)

Figure 5. GPLD Macrocell Input/Output Port



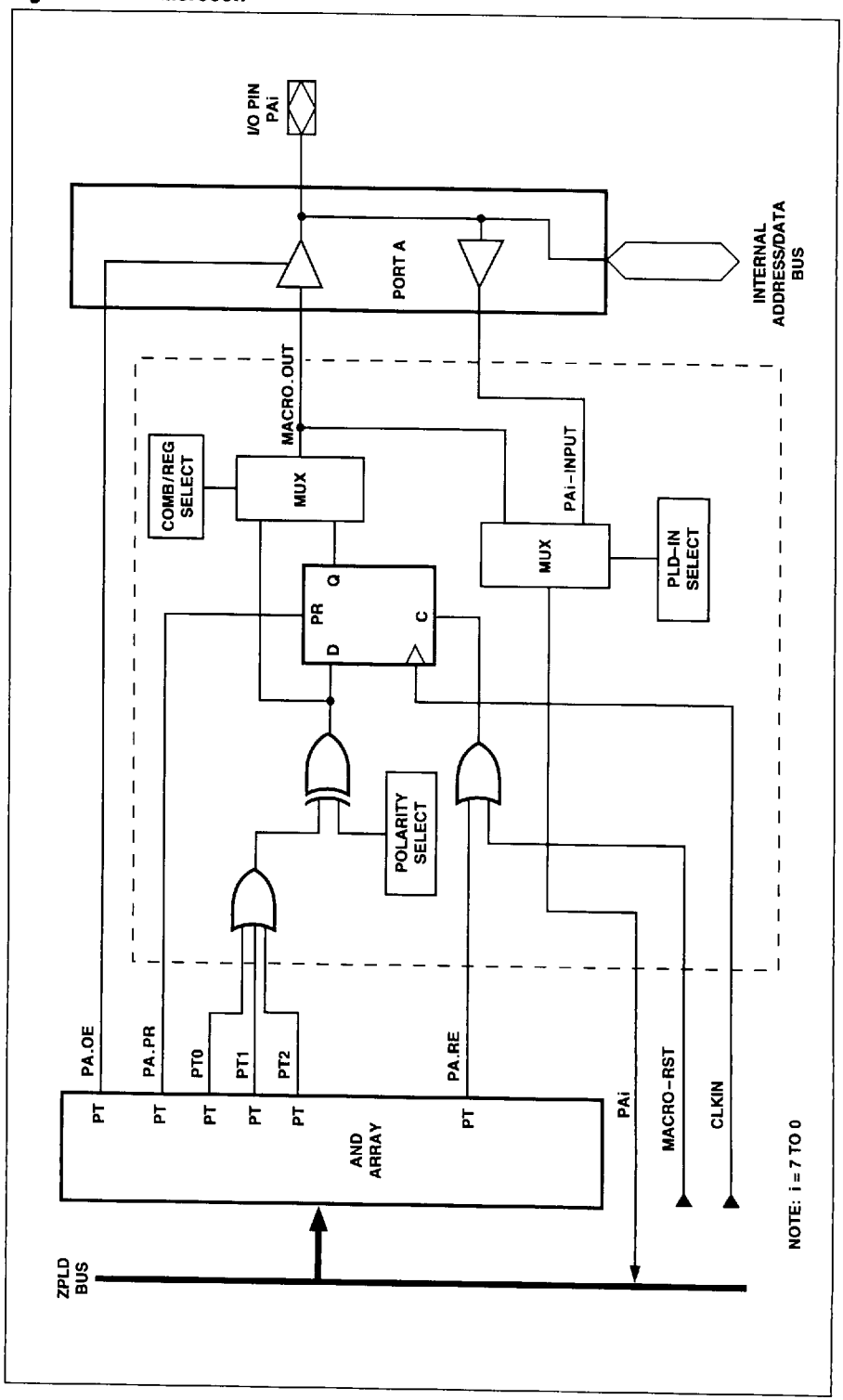
ZPLD Block
(Cont.)

Figure 5a. PA Macrocell Block Diagram



ZPLD Block (Cont.)

Figure 6. PA Macrocell



ZPLD Block (Cont.)

Port B Macrocell Structure

Figure 7 shows the PB Macrocell block, which consists of 8 identical macrocells. Each macrocell output can be connected to its own I/O pin on Port B. The two inputs, CLKIN and MACRO-RST, are used as clock and clear inputs to all the macrocells. The CLKIN comes directly from the CLKIN input pin. The MACRO-RST is the same as the Reset input pin except it is user configurable.

The circuit of a PB Macrocell is shown in Figure 8. There are 10 product terms from the GPLD's AND ARRAY as inputs to the macrocell. Users can select the polarity of the output, and configure the macrocell to operate as:

- **Registered Output**
  Select output from D flip flop.
- **Combinatorial Output**
  Select output from OR gate.
- **GPLD Input**
  Use Port B pin as dedicated input.
- **GPLD Output**
  Use Port B pin as dedicated output.
- **GPLD I/O**
  Use Port B pin as bidirectional pin.
- **Macrocell Feedback**
  Register feedback for state machine implementations or expander feedback from the combinatorial output, to possibly expand the number of product terms available to another macrocell.

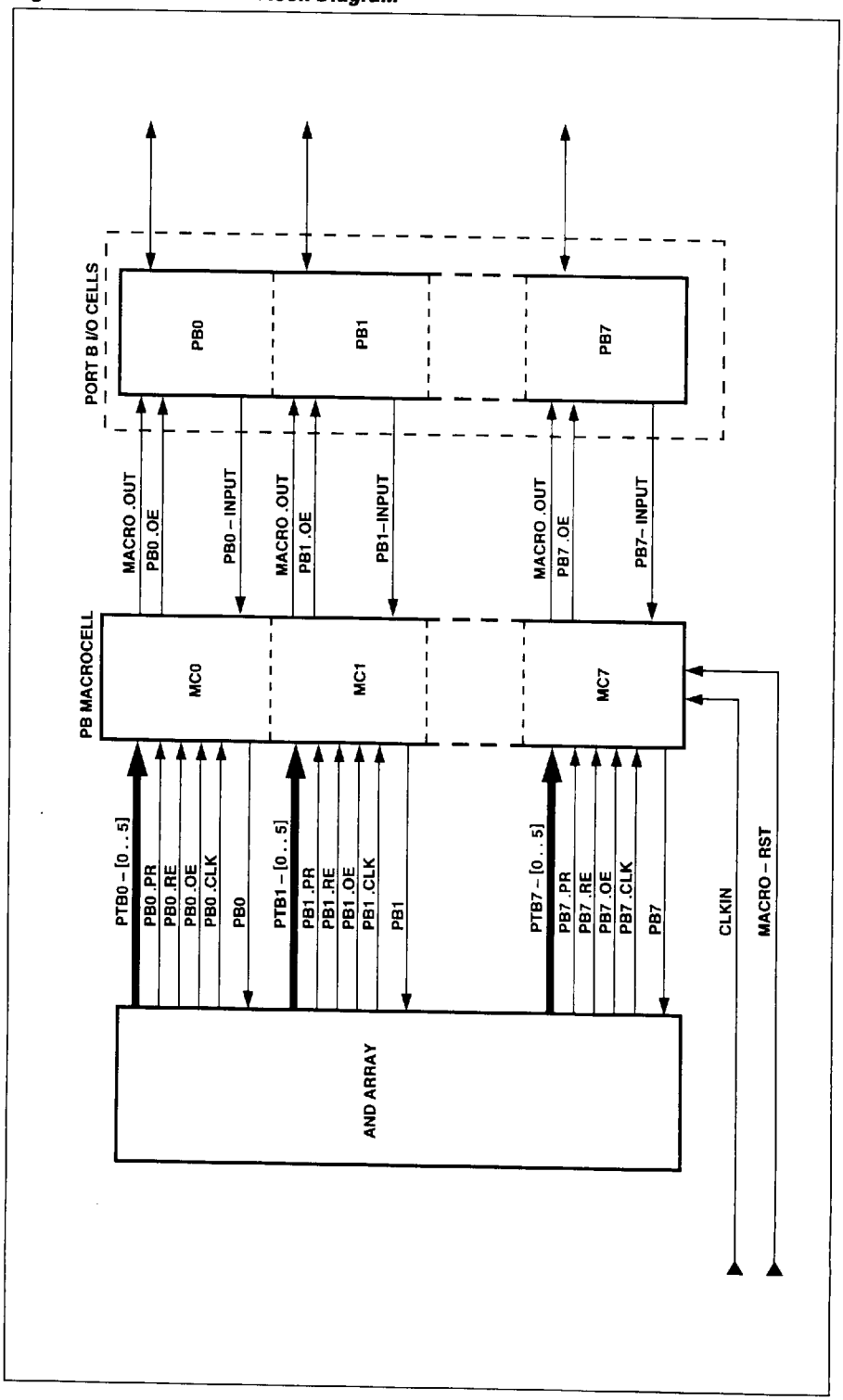
  In case of "Buried Feedback", where the output of the macrocell is not connected to a Port B pin, Port B can be configured to perform other user defined I/O functions.

Each D flip flop in the macrocells has its own dedicated asynchronous clear, preset and clock input. The signals are defined as follow:

- **PRESET**
  Active only if defined by a product term (PBx.PR)
- **CLEAR**
  Two selectable inputs: Reset input or user defined product term (PBx.RE)
- **CLK**
  Two selectable inputs – CLKIN input or user defined product term (PBx.CLK). The macrocell is operated in Synchronous Mode if the clock input is CLKIN, and is in Asynchronous Mode if the clock is a product-term clock defined by the user.

ZPLD Block (Cont.)

Figure 7. PB Macrocell Block Diagram



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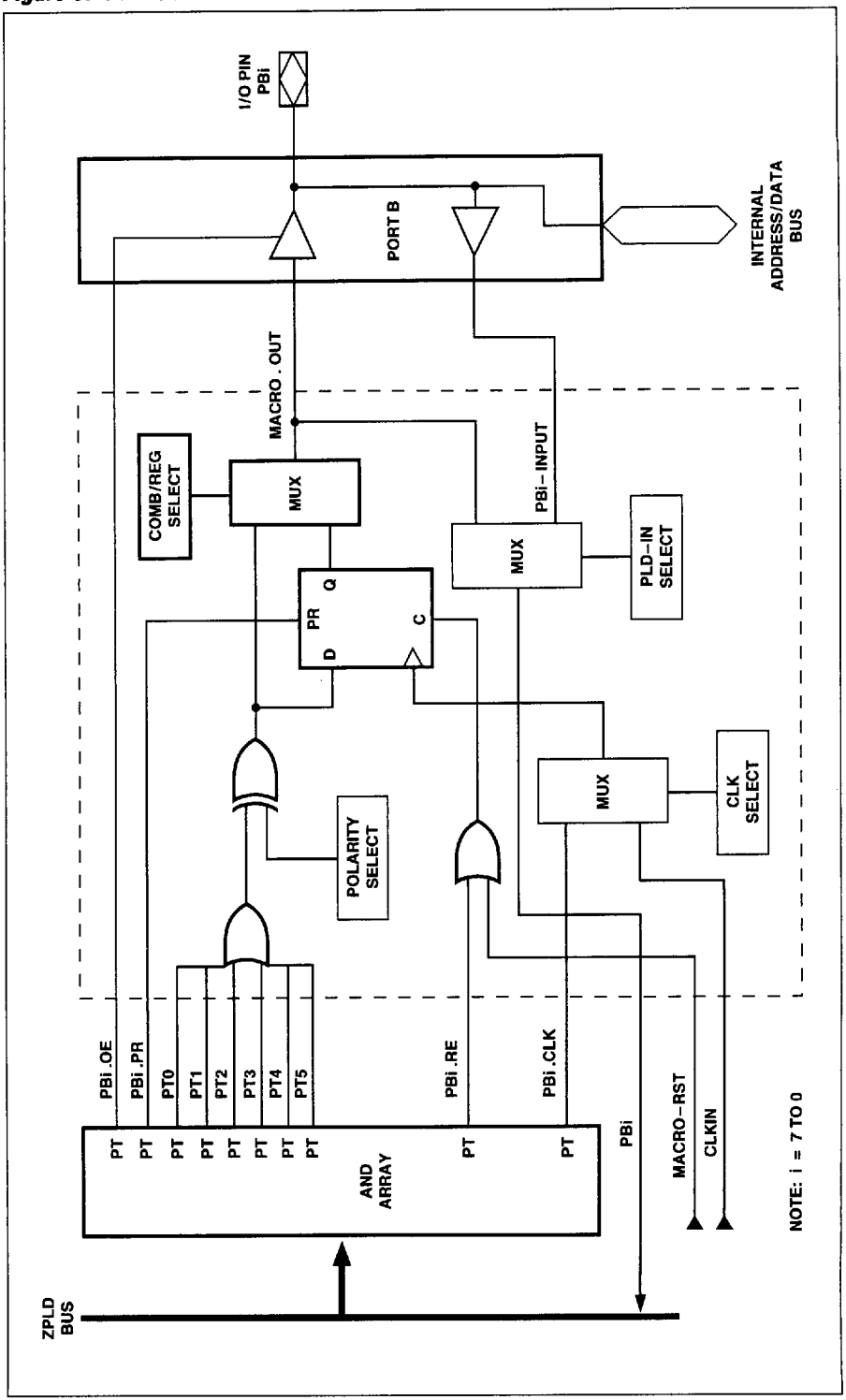
ZPLD Block
(Cont.)

Figure 8. PB Macrocell



ZPLD Block (Cont.)

Port E Macrocell Structure

Figure 9 shows the PE Macrocell block, which consists of 8 identical macrocells. Each macrocell output can be connected to its own I/O pin on Port E. There are 3 user programmable global product terms output from the GPLD's AND ARRAY which are shared by all the macrocells in Port E:

- **PE.OE**
  Enable or tri-state Port PE output pins
- **PE.PR**
  Preset D flip flop in the macrocells
- **PE.RE**
  Reset/Clear D flip flop in the macrocells

Two other inputs, CLKIN and MACRO-RST, are used as clock and clear inputs to the D flip flop. The CLKIN comes directly from the CLKIN input pin. The MACRO-RST is the same as the Reset input pin except it is user configurable.

The circuit of a PE Macrocell is shown in Figure 10. There are 4 product terms from the GPLD's AND ARRAY as input to the macrocell. Users can select the polarity of the output and configure the macrocell to operate as:

- **Registered Output**
  Select output from D flip flop
- **Combinatorial Output**
  Select output from OR gate
- **GPLD Input**
  Use Port E pin as dedicated input
- **GPLD Output**
  Use Port E pin as dedicated output
- **GPLD I/O**
  Use Port E pin as bidirectional pin
- **Macrocell Feedback**
  Register feedback for state machine implementations or expander feedback from the combinatorial output, to possibly expand the number of product terms available to another macrocell.

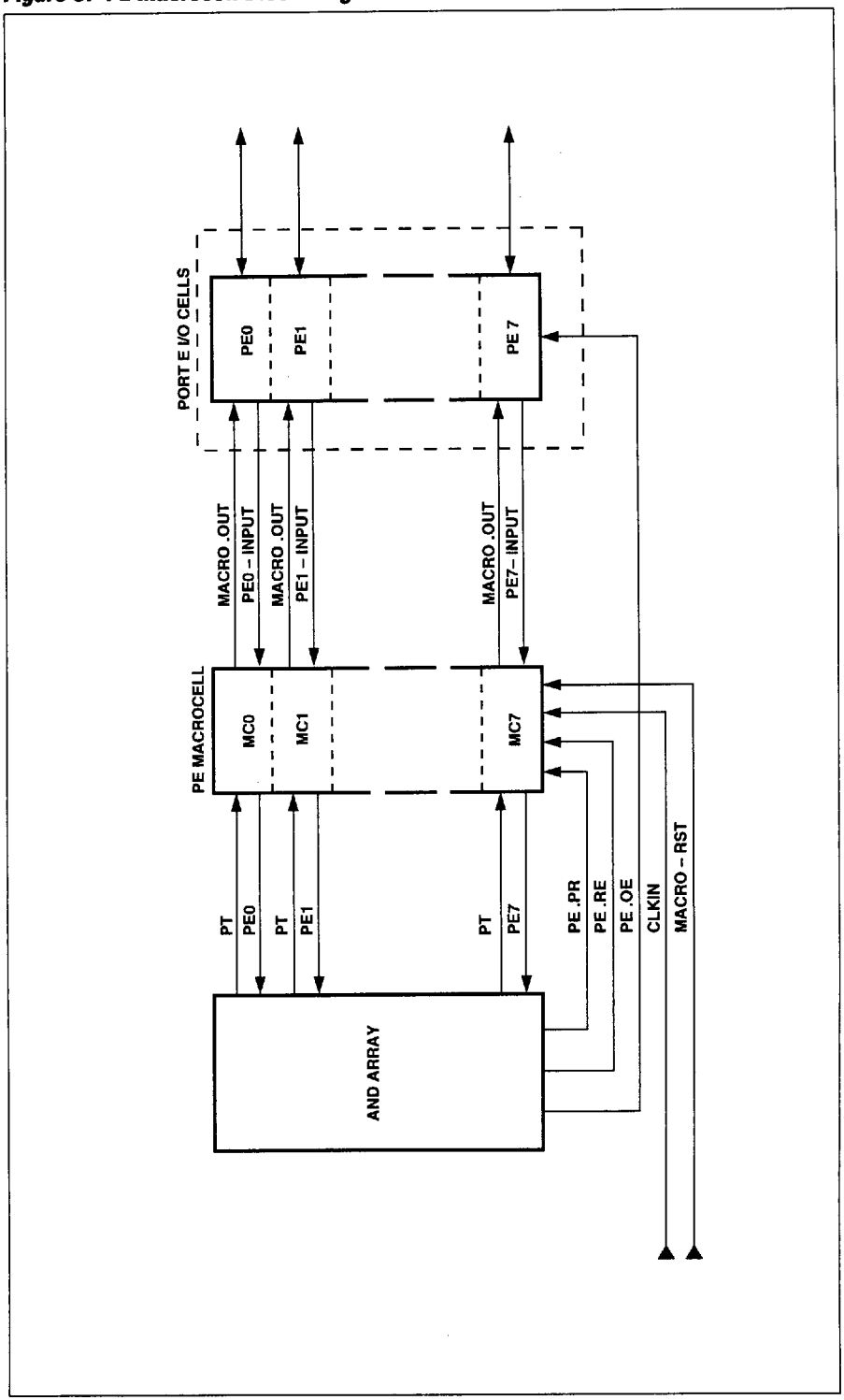
  In case of "Buried Feedback", where the output of the macrocell is not connected to Port E pin, Port E can be configured to perform other user defined I/O functions. If pins PE0 and PE1 are used as bus control signal inputs (ALE, PSEN/BHE), the corresponding macrocells' feedbacks are disabled. The bus control signals are connected to the ZPLD Input Bus.

The two global product terms assigned for asynchronous clear (PE.RE) and preset (PE.PR) are mainly for proper PE Macrocell initialization.

The macrocell flip-flop can also be cleared during reset by MACRO-RST, if such an option is chosen. The clock source is always the input clock CLKIN.

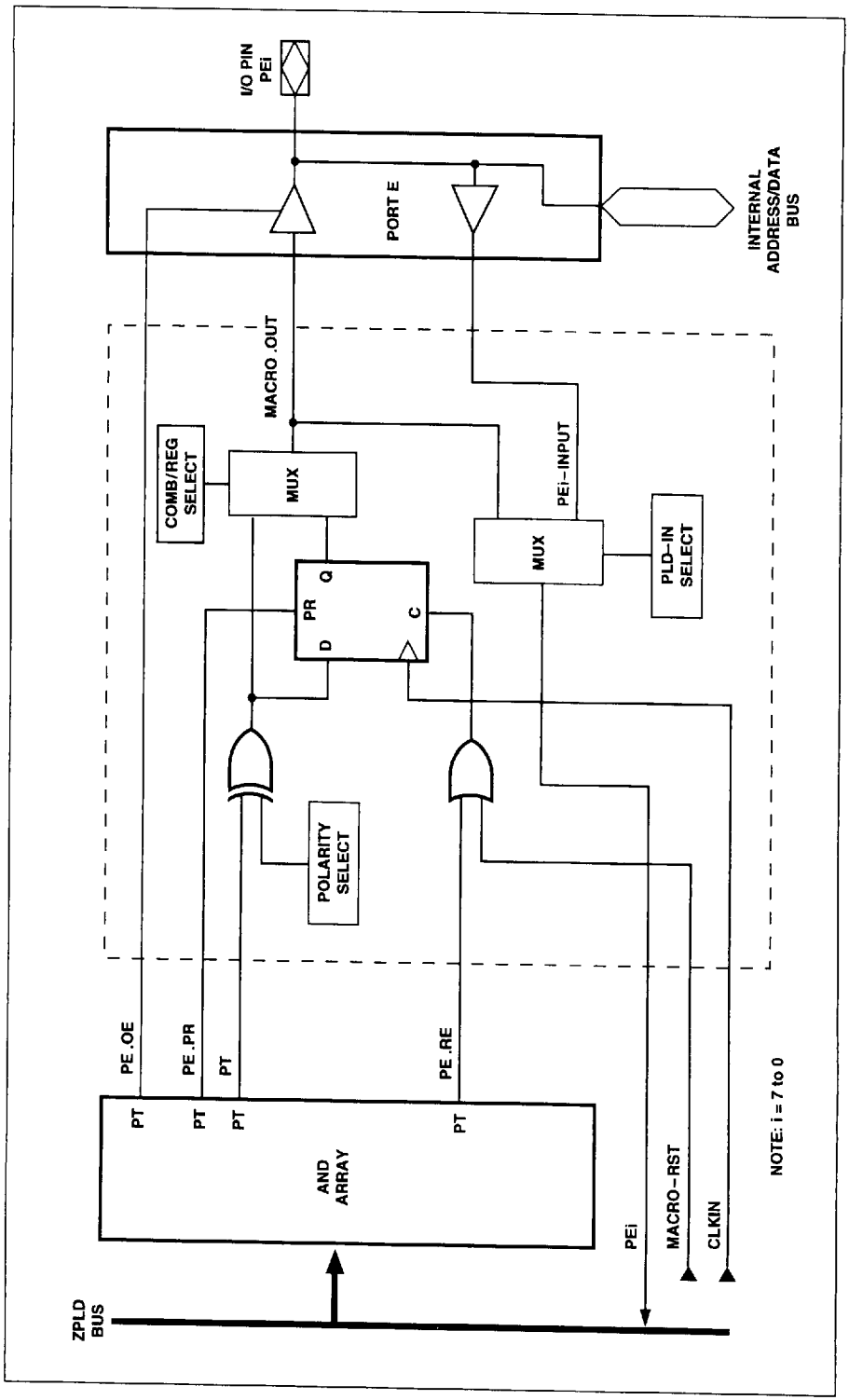
ZPLD Block
(Cont.)

Figure 9. PE Macrocell Block Diagram



ZPLD Block
(Cont.)

Figure 10. PE Macrocell



ZPLD Block (Cont.)

The PPLD

The Peripheral Programmable Logic Device (PPLD) provides a powerful mechanism for the user to control the operations of the Counter/Timer and Interrupt Controller. Figure 11 is the PPLD block diagram. There are six Peripheral Macrocells, four are dedicated to the Counter/Timer, and two to the Interrupt Controller.

The outputs from the four Peripheral Macrocells, MC2TMR[3:0], are used as load/store/enable inputs to the Counter/Timer (multiplexed with pin inputs TIMER[3:0]_IN). The remaining two macrocell outputs (MC2INT[6:7]), together with two other product terms (PT2INT4, PT2INT5), can generate up to 4 user defined interrupts to the Interrupt Controller. The watch-dog output of the Timer (WDOG2PLD) and Interrupt Controller (INTR2PLD) are available as inputs to the ZPLD's AND ARRAY.

The structure of a Peripheral Macrocell is shown in Figure 12. The cell has two product term inputs from the AND ARRAY. The user can select the registered or combinatorial output of the macrocell, as well as the output polarity. The registers are clocked by the CLKIN clock, and are cleared by the RESET input during power up.

The ZPLD Power Management

The ZPLD implements a Zero Power Mode, which provides considerable power savings for low to medium frequency operations. To enable this feature, the ZPLD Turbo bit in the Power Management Mode Register 0 (PMMR0) has to be turned off.

If none of the 61 inputs to the ZPLD are switching for a time period of 70ns, the ZPLD puts itself into Zero Power Mode and the current consumption is minimal. The ZPLD will resume normal operation as soon as one or more of the inputs change state.

Two other features of the ZPLD provide additional power savings:

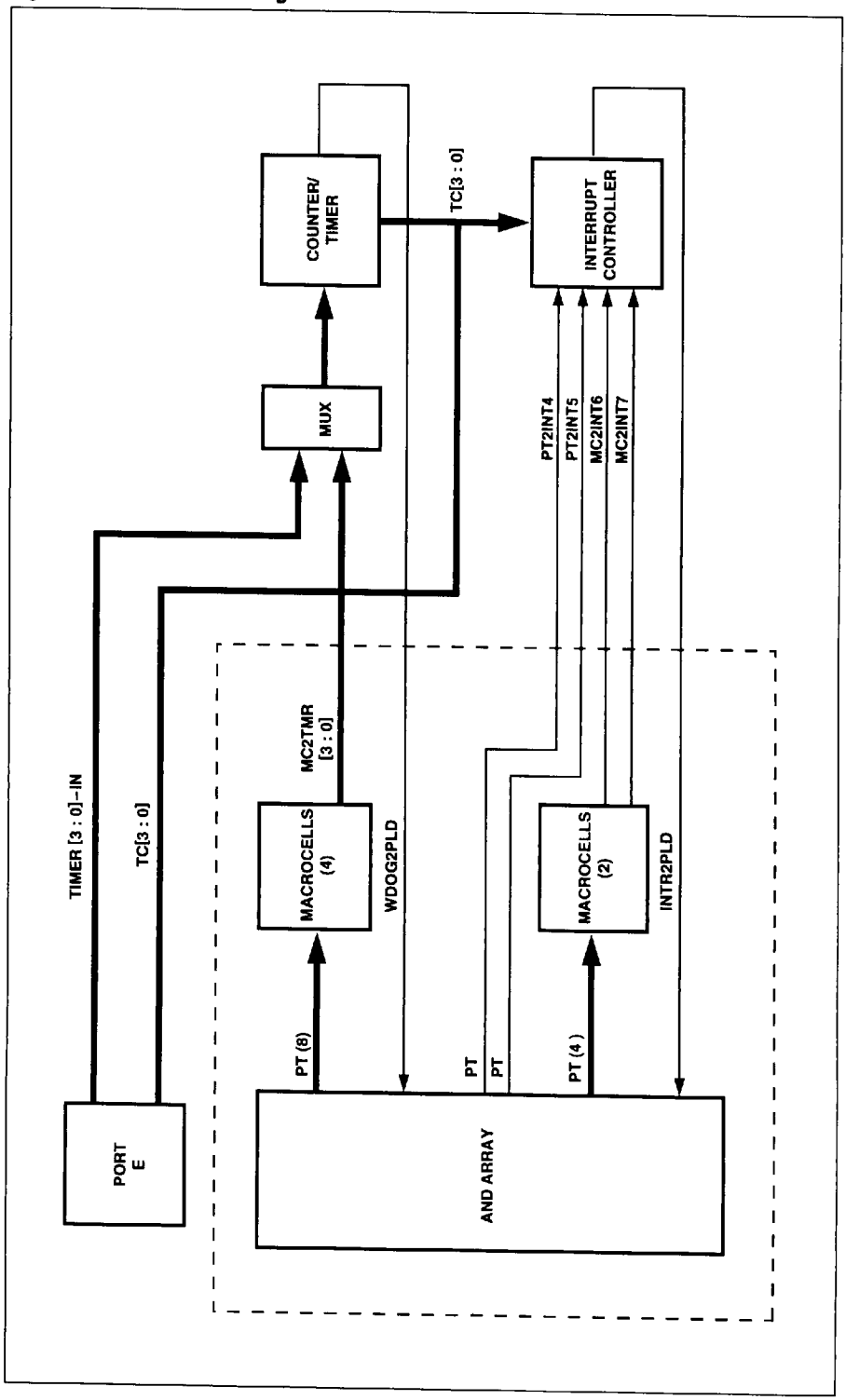
1. **Clock Disable:**
   Users can disable the clock input to the ZPLD and/or macrocells, thereby reducing AC power consumption.

2. **Product Term Disable:**
   Unused product terms in the ZPLD are disabled by the PSDsoft Software automatically for further power savings.

The ZPLD power configuration is described in the Power Management Unit section.

ZPLD Block
(Cont.)

Figure 11. PPLD Block Diagram



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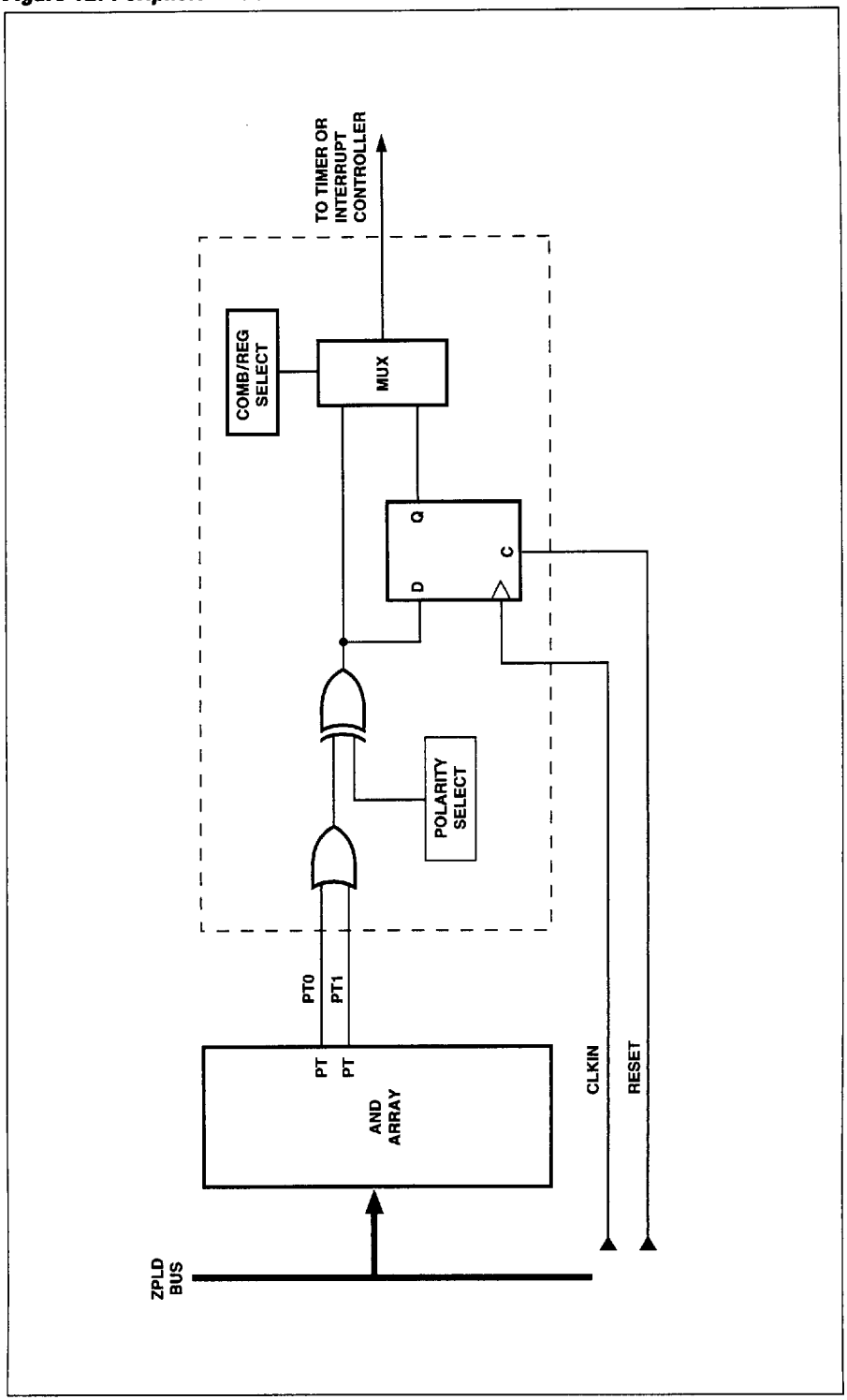
The ZPLD Block (Cont.)

Figure 12. Peripheral Macrocell



Bus Interface

The Bus Interface is very flexible and can be configured to interface to most microcontrollers with no glue logic. Table 4 lists some of the bus types to which the Bus Interface is able to interface.

Table 4. Typical Microcontroller Bus Types

Multiplexed	Data Bus Width	Bus Control Signals	Microcontroller
Mux	8	$\overline{WR}$, $\overline{RD}$, $\overline{PSEN}$, A0	8031
Mux/ Non-mux	8/16	R/W, E, $\overline{BHE}$, A0	6811
Mux	8/16	$\overline{WR}$, $\overline{RD}$, $\overline{BHE}$, A0	80196/80186
Mux	16	$\overline{WRL}$, $\overline{RD}$, $\overline{WRH}$, A0	80196SP
Non-mux	16	R/W, $\overline{LDS}$, $\overline{UDS}$	68302
Non-mux	8/16	R/W, $\overline{DS}$, SIZ0, A0	68340
Non-mux	16	R/W, $\overline{DS}$, $\overline{BHE}$, $\overline{BLE}$	68330

Bus Interface Configuration

The Bus Interface Logic is user configurable. The type of bus interface is specified by the user in the PSDsoft software (PSD configuration). The bus control input pins have multi-function capabilities. By choosing the right configuration, the PSD5XX is able to interface to most microcontrollers, including the ones listed in Table 4. In Table 5, the names of the bus control input signal pins and their multiple functions are shown. For example, Pin PE0 can be configured by the PSD configuration software to perform any one of the five functions. Examples on the interface between the PSD5XX and some typical microcontrollers are shown in following sections.

Table 5. Alternate Pin Functions

Pin Name	Pin Function 1	Pin Function 2	Pin Function 3	Pin Function 4	Pin Function 5
RD	$\overline{RD}$	E	$\overline{DS}$	$\overline{LDS}$	
WR	$\overline{WR}$	R/W	$\overline{WRL}$		
PE0	$\overline{BHE}$	$\overline{PSEN}$	$\overline{WRH}$	$\overline{UDS}$	SIZ0
PE1	ALE				
AD0	A0	$\overline{BLE}$			

PSD5XX Interface To a Multiplexed Bus

Figure 13 shows a typical connection to a microcontroller with a multiplexed bus. The ADIO port of the PSD5XX is connected directly to the microcontroller address/data bus (AD0-AD15 for 16 bit bus). The ALE input signal latches the address lines internally. In a read bus cycle, data is driven out through the ADIO Port transceivers after the specified access time. The internal ADIO Port connection for a 16 bit multiplexed bus is shown in Figure 14. The ADIO port is in tri-state mode if none of the PSD5XX internal devices are selected.

Bus Interface (Cont.)

PSD5XX Interface To Non-Multiplexed Bus

Figure 15 shows a PSD5XX interfacing to a microcontroller with a non-multiplexed address/data bus. The address bus is connected to the ADIO Port, and the data bus is connected to Port C and/or Port D, depending on the bus width. There is no need for the ADIO Port to latch the address internally, but the user is offered the option to do so in the PSD5XX PSDsoft Software. The data ports are in tri-state mode when the PSD5XX is not accessed by the microcontroller.

Data Byte Enable

Microcontrollers have different data byte orientations with regard to the data bus. The following tables show how the PSD5XX handles the byte enable under different bus configurations. Even byte refers to locations with address A0 equal to "0", and odd byte as locations with A0 equal to "1".

Table 6. 8-Bit Data Bus

$\overline{BHE}$	A0	D7 – D0
X	0	Even Byte
X	1	Odd Byte

Table 7. 16-Bit Data Bus With $\overline{BHE}$

$\overline{BHE}$	A0	D15 – D8	D7 – D0
0	0	Odd byte	Even byte
0	1	Odd byte	–
1	0	–	Even byte

Table 8. 16-Bit Data Bus With $\overline{WRH}$ and $\overline{WRL}$

$\overline{WRH}$	$\overline{WRL}$	D15 – D8	D7 – D0
0	0	Odd byte	Even byte
0	1	Odd byte	–
1	0	–	Even byte

Table 9. 16-Bit Data Bus With SIZ0, A0

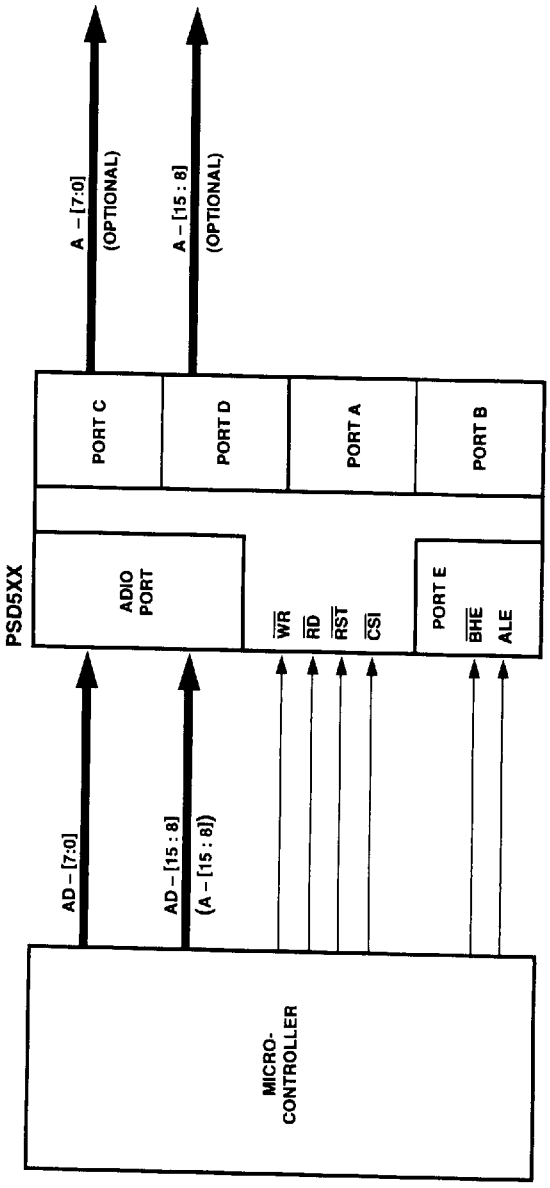
SIZ0	A0	D15 – D8	D7 – D0
0	0	Even byte	Odd byte
1	0	Even byte	–
1	1	–	Odd byte

Table 10. 16-Bit Data Bus With $\overline{UDS}$, $\overline{LDS}$

$\overline{LDS}$	$\overline{UDS}$ (A0)	D15 – D8	D7 – D0
0	0	Even byte	Odd byte
1	0	Even byte	–
0	1	–	Odd byte

Bus Interface (Cont.)

Figure 13. Bus Interface – Multiplexed Bus, 8 or 16-Bit Data Bus



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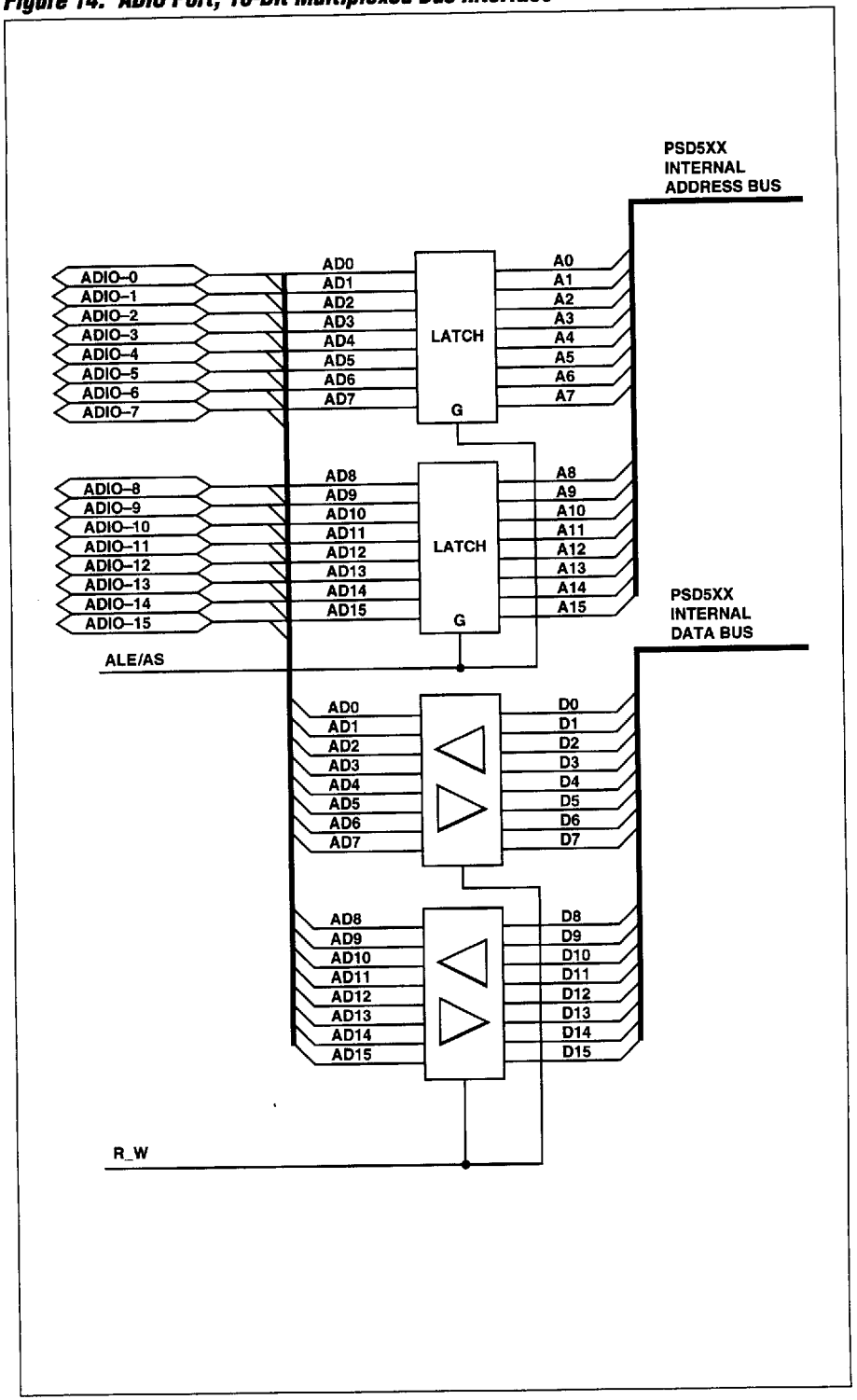
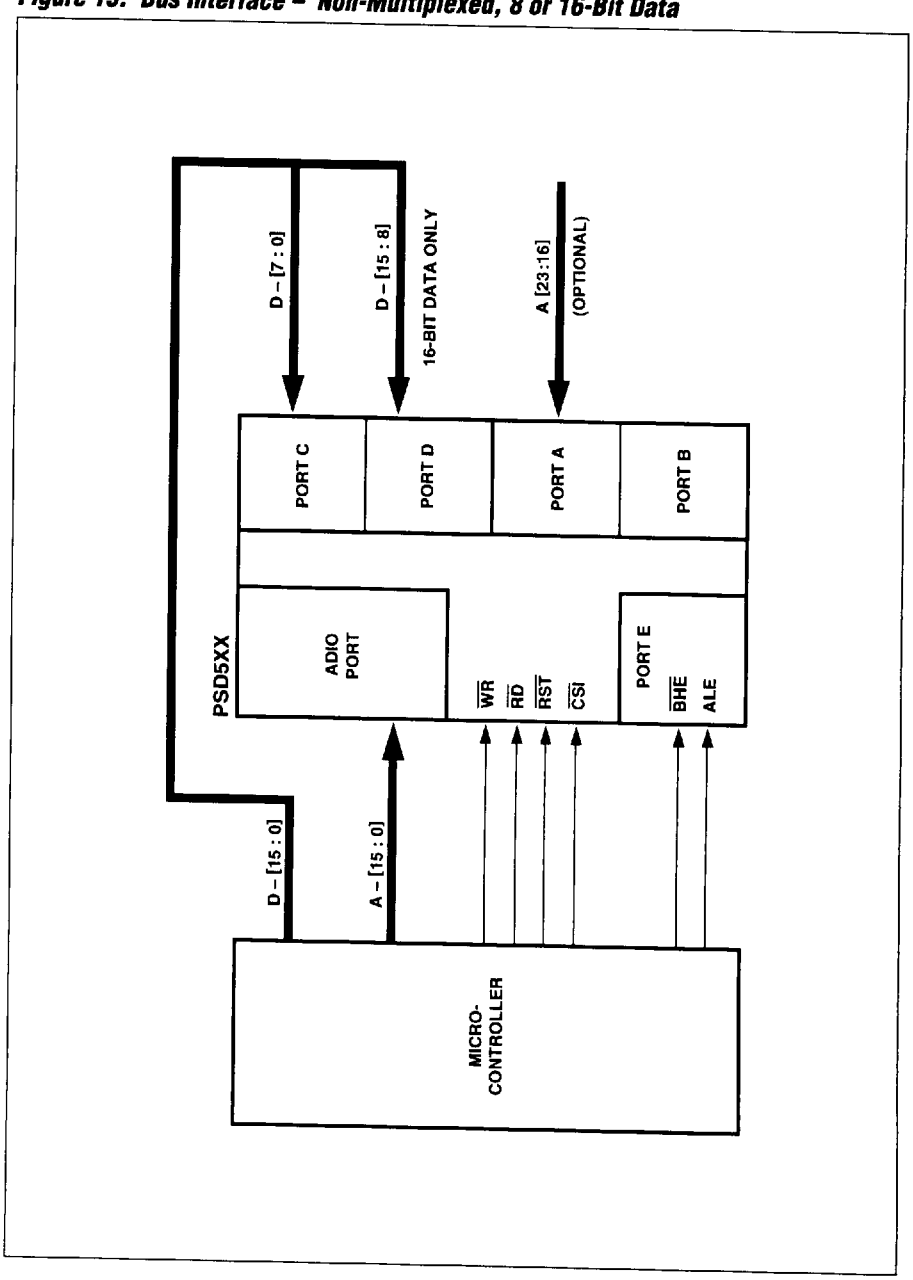
Bus Interface (Cont.)

Figure 14. ADIO Port, 16-Bit Multiplexed Bus Interface



Bus Interface (Cont.)

Figure 15. Bus Interface – Non-Multiplexed, 8 or 16-Bit Data



Bus Interface (Cont.)

Optional Features

The PSD5XX provides two optional features to add flexibility to the Bus Interface:

1. Address In

Port A can be configured as high order address (A16-A23) inputs to the ZPLD for EPROM or other decoding. Inputs are latched by ALE/AS if Multiplexed Bus is selected. Other ports can be configured as address input ports for the ZPLD. These inputs should not be used for EPROM decoding and are not latched internally.

2. Address Out

For multiplexed bus only. Latched address lines A0-A15 are available on Port A, B, C, D, or E.

Details on the optional features are described in the I/O Port section.

Bus Interface Examples

The next four figures show the PSD5XX interfacing with some popular microcontrollers. The examples show only the basic bus connections; some of the pin names on the PSD5XX parts change to reflect the actual pin functions.

Figure 16 shows an interface to the 80C31. The 80C31 has a 16 bit address bus and an 8-bit data bus. The lower address byte is multiplexed with the data bus. The $\overline{RD}$ and $\overline{WR}$ signals are used for accessing the data memory (SRAM) and the $\overline{PSEN}$ signal is for reading program memory (EPROM). The ALE signal is active high and is used to latch the address internally. Port C provides latched address outputs A[7:0]. Ports A, B, D, and E (PE2-PE7) can be configured to perform other functions. The RSTOUT reset to the 80C31 is generated by the ZPLD from the $\overline{RESET}$ input. This configuration eliminates any reset race condition between the 80C31 and the PSD5XX.

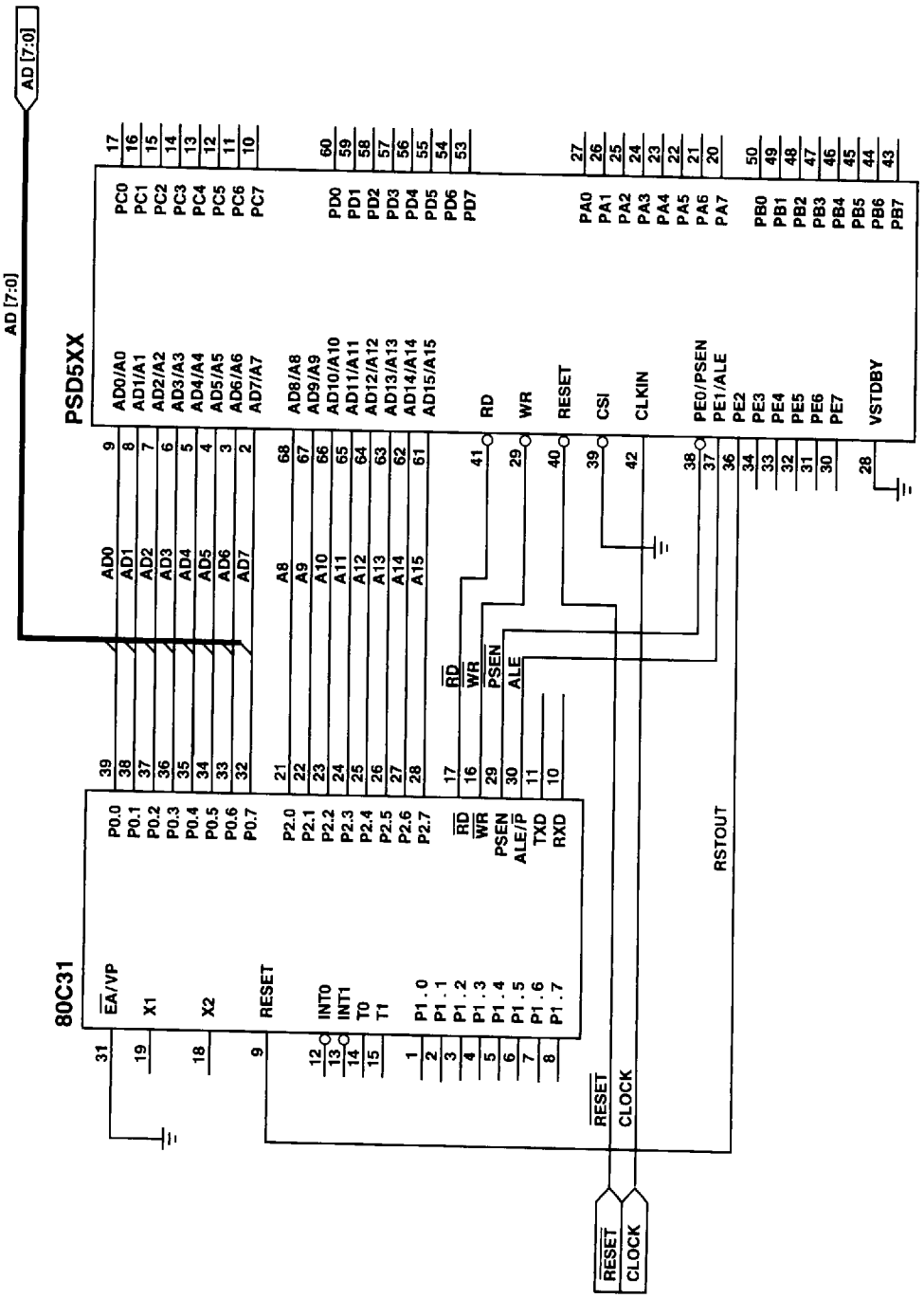
Figure 17 shows the 68HC11 interface, which is similar to the 80C31 except the PSD5XX generates internal $\overline{RD}$ and $\overline{WR}$ from the 68HC11's E and R/$\overline{W}$ signals.

In Figure 18, the Intel 80C196 microcontroller is interfaced to the PSD5XX. The 80C196 has a multiplexed 16-bit address and data bus. The $\overline{BHE}$ signal is used for data byte selection. Ports C and D are used as output ports for latched address A[15:0]. Pins PE6 and PE7 can be programmed as ZPLD outputs to provide the READY and BUSWIDTH control signals to the 80C196.

Figure 19 shows Motorola's MC68331 interfacing to the PSD5XX. The MC68331 has a 16-bit data bus and a 24-bit address bus. D15-D8 from the MC68331 are connected to Port D, and D7 – D0 are connected to Port C.

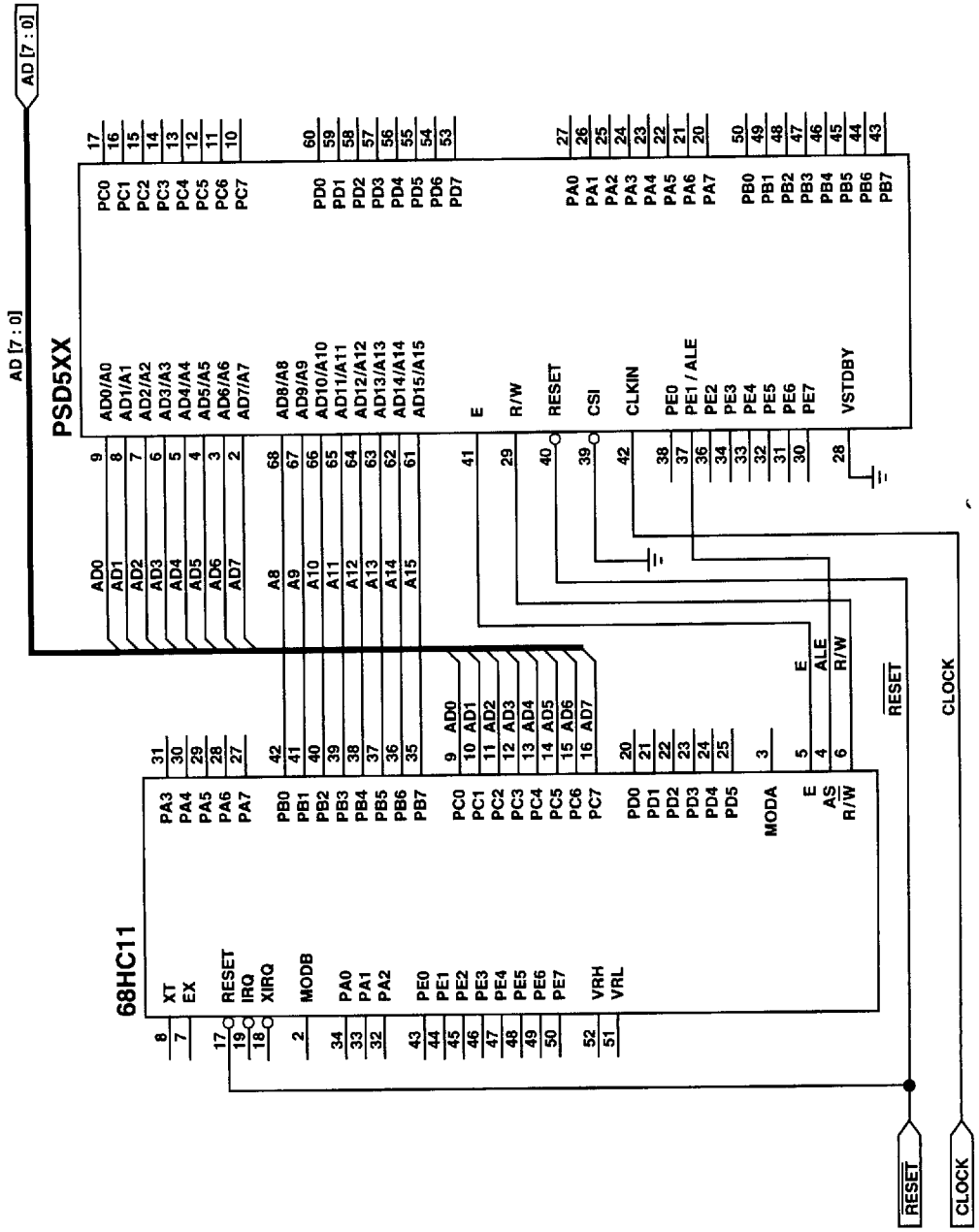
Bus Interface (Cont.)

Figure 16. Interfacing PSD5XX With 80C31



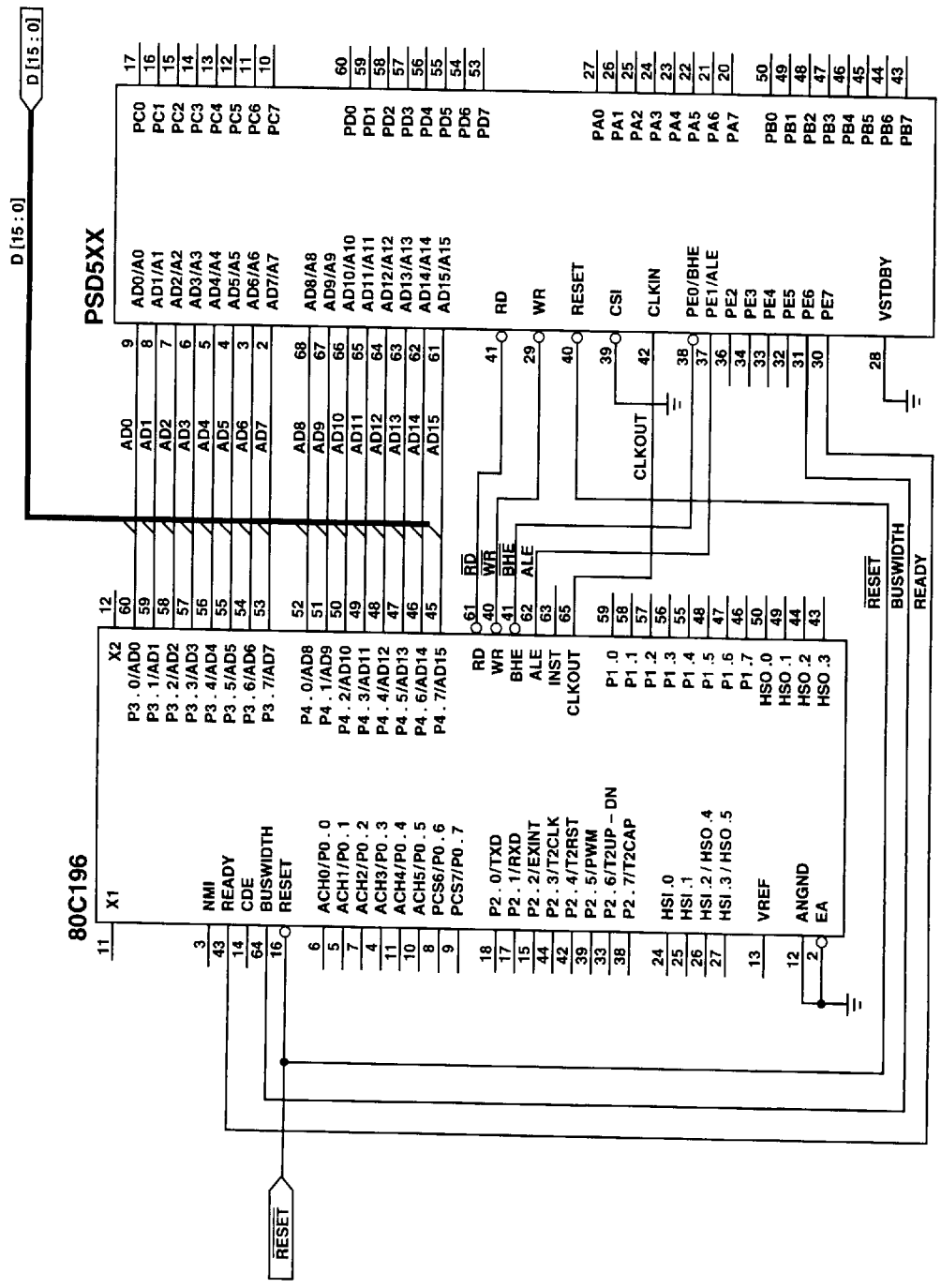
Bus Interface (Cont.)

Figure 17. Interfacing PSD5XX With 68HC11



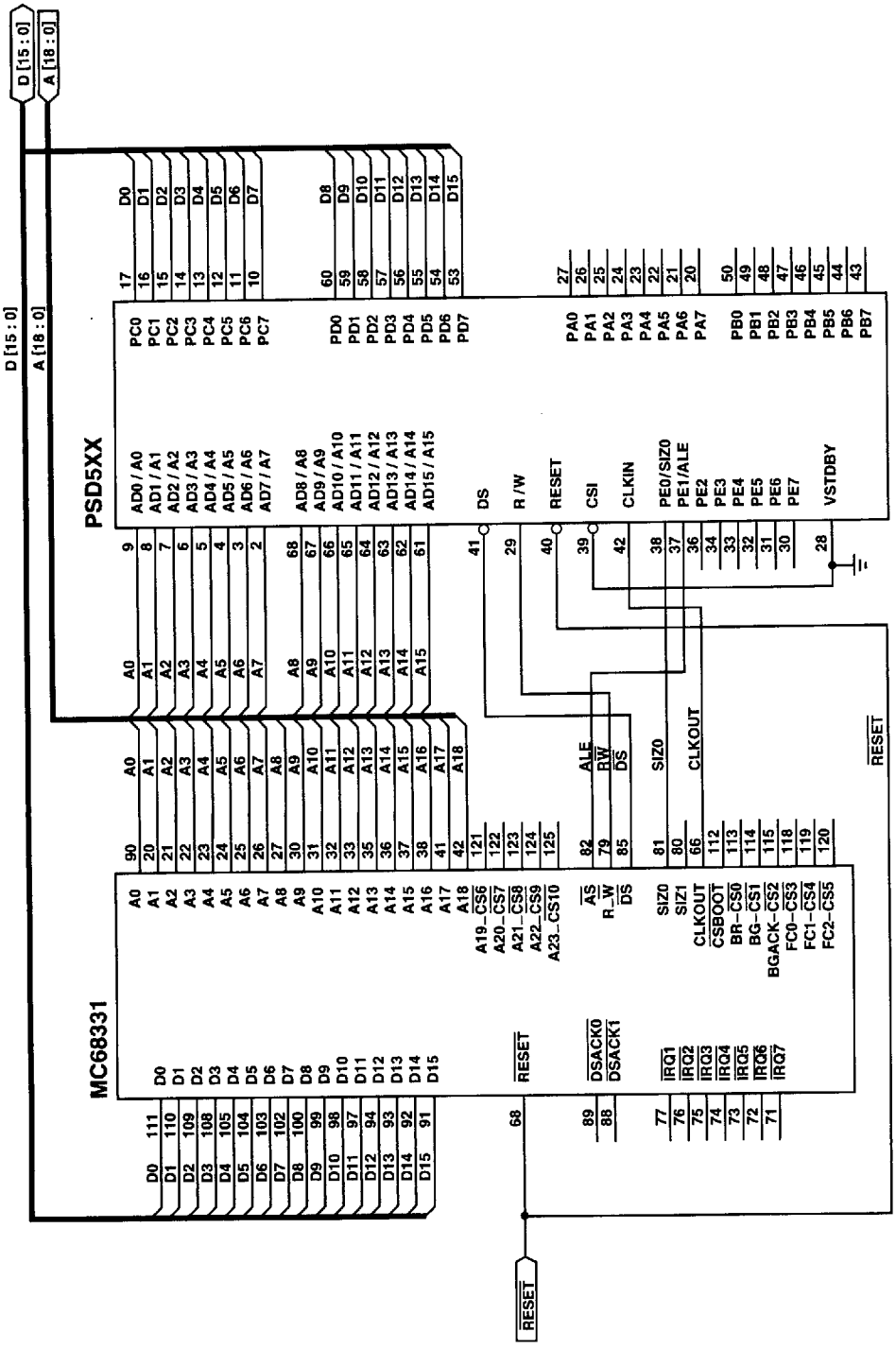
Bus Interface (Cont.)

Figure 18. Interfacing PSD5XX With 80C196



Bus Interface (Cont.)

Figure 19. Interfacing PSD5XX With Motorola 68331



I/O Ports

There are 5 programmable 8-bit I/O ports: Port A, Port B, Port C, Port D and Port E. These ports all have multiple operating modes, depending on the configuration. Some of the basic functions are providing input/output for the ZPLD, the Counter/Timer, or can be used for standard I/O. Each port pin is individually configurable, thus enabling a single 8-bit port to perform multiple functions. The I/O ports occupy 256 bytes of memory space as defined by "CSIOP". Refer to the System Configuration section for I/O register address offset.

To set up the port configuration the user is required to:

1. Define I/O port chip select (CSIOP) in the ABEL file.
2. Initialize certain port configuration registers in the user's program and/or
3. Specify the configuration in the PSD5XX PSDsoft Software.
4. Unused input pins should be tied to V_{CC} or GND.

The following is a description of the operating modes of the I/O ports. The functions of the port registers are described in later sections.

Standard MCU I/O

The Standard MCU I/O Mode provides additional I/O capability to the microcontroller. In this mode, the ports can perform standard I/O functions such as sensing or controlling various external I/O devices. Operation options of this mode are as follows:

❑ ***Configuration***

1. Declare pins or signals which are used as I/O in the ABEL file (PSDsoft).
2. Set the bit or bits in the Control Register to "1".
3. ***As Output Port***
   - Write output data to Data Out Register
   - Set Direction Register to output mode
4. ***As Input Port***
   - Set Direction Register to input mode
   - Read input from Data In Register

The port remains an output or input port as long as the Direction Register is not changed.

PLD I/O

The PLD I/O mode enables the port to be configured as an input to the ZPLD, or as an output from the GPLD macrocell. The output can be tri-stated with a control signal defined by a product term from the ZPLD. This mode is configured by the user in the PSD5XX PSDsoft Software, and is enabled upon power up. For a detailed description, see the section on the ZPLD.

❑ ***Configuration***

1. Declare pins or signals in the ABEL file (PSDsoft)
2. Write logic equations in the ABEL file.
3. PSDcompiler maps the PLD function to the PSD.

I/O Ports (Cont.)

Address Out

For microcontrollers with a multiplexed address/data bus, the I/O ports in Address-Out mode are able to provide latched address outputs (A0 – A15) to external devices. This mode of operation requires the user to:

❑ **Configuration**

1. Declare the pins used as address line outputs in the ABEL file PSDsoft.
2. Write "0" to the corresponding bit in the Control Register associated with each I/O port.
3. Set the Direction Register to Output Mode.

Address In

1. For Port A – as other address line (A2 – A7 and A16 – A23) inputs to the DPLD. Additional address inputs included in the EPROM decoding must come from Port A. The address inputs are latched internally by ALE/AS if Multiplexed Bus is specified in PSDsoft.
2. For Ports C and D – as adress inputs to the ZPLD for general decoding, should not be used in EPROM decoding.

❑ **Configuration**

1. Declare pins or signals used as Address In in the ABEL file (PSDsoft).
2. Write latch equations in the ABL file, e.g., A16.LE = ALE
3. Include latched address in logic equations.

Data Port

In this mode, the port is acting as a data bus port for a microcontroller which has a non-multiplexed address/data bus. In this configuration, the Data Port is connected to the data bus of the microcontroller and the ADIO port is connected to the address bus.

❑ **Configuration**

Select the non-multiplexed bus option in PSD configuration (PSDsoft).

Special Function Out

This mode is per-pin configurable. When enabled, the special function assigned to the particular pin is driven out. Special functions consist of Timer and Interrupt outputs.

❑ **Configuration**

1. Specify the output function in the PSD configuration (PSDsoft).
2. PSD compiler assigns pins for the selected function.
3. Write "1" to the corresponding bit in the Special Function Register.

I/O Ports (Cont.)

Alternate Function In

This mode is per-pin configurable and enables the user to define the pins in Port E to perform Alternate function. Alternate Function includes inputs to Counter/Timers and APD clock.

❑ **Configuration**

1. Select input functions in PSD configuration
2. PSD compiler assigns pins for the selected function.

Peripheral I/O

This mode enables the microcontroller to read or write to a peripheral though Port A. When there is no read/write operation, Port A is tri-stated. One of the applications of Peripheral I/O is in a DMA based design.

❑ **Configuration**

1. Declare the pins used as Peripheral I/O in the ABEL file.
2. Write logic equations for PSEL0 and PSEL1.
3. Write a "1" to the PIO bit in the VM Register to activate the Peripheral I/O operation. See the section on Peripheral I/O for a detailed description.

Open Drain Outputs

This mode enables the user to configure Port C and D pins as open drain outputs. CMOS output is the default configuration. Writing "1" to the corresponding bit in the Open Drain Register changes the pin to open drain output.

The following table summarizes the operating modes of the I/O ports. Not all functions are available to every port.

Table 11. Operating Modes of the I/O Ports

Port Mode	Port A	Port B	Port C	Port D	Port E
Standard MCU I/O	Yes	Yes	Yes	Yes	Yes
PLD I/O	Yes	Yes	Input Only	Input Only	Yes
Address Out	Yes	Yes	Yes	Yes	Yes
Address In	Yes	Yes*	Yes*	Yes*	Yes*
Data Port			Yes	Yes	
Special Function Out	Yes	Yes			Yes
Alternate Function In					Yes
Peripheral I/O	Yes				
Open Drain			Yes	Yes	

*For external decoding. Cannot be latched by ALE.

I/O Ports (Cont.)

Port Registers

There are two sets of registers per I/O port: the Port Configuration Registers (PCR) which consist of four 8-bit registers; and the Port Data Registers (PDR) which include three 8-bit registers. The PCR is used for setting up the port configuration, while the PDR enables the microcontroller to write or read port data or status bits. Tables 12 and 13 show the names and the registers and the ports to which they belong.

All the registers in the PCR and PDR are 8-bits wide and each bit is associated with a pin in the I/O port. In Table 14, the LSB of the Data In Register of Port A is connected to pin PA0, and the MSB is connected to PA7. This pin configuration also applies to other registers and ports. For example, in the Direction Register of Port A, writing a hex value of 07 to the register configures pins PA0 – PA2 as output pins, while PA3 – PA7 remain as input pins.

Registers can be accessed by the microcontroller during normal read/write bus cycles. The I/O address offset of the registers are listed in the System Configuration section.

Table 12. Port Configuration Registers (PCR)

Register Name	Port	Write/Read
Control Register	A,B,C,D,E	Write/Read
Direction Register	A,B,C,D,E	Write/Read
Open Drain Register	C,D	Write/Read
Special Function Register	A,B,E	Write/Read
PLD – I/O Register	A,B,E	Read

Table 13. Port Data Registers (PDR)

Register Name	Port	Read/Write
Data In Register	A,B,C,D,E	Read
Data Out Register	A,B,C,D,E	Write/Read
Macrocell Out Register	A,B,E	Read

Table 14.

Data In Register – Port A

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PA7 Pin	PA6 Pin	PA5 Pin	PA4 Pin	PA3 Pin	PA2 Pin	PA1 Pin	PA0 Pin

Direction Register – Port A
(Example: Pins PA0 – PA2 as Output, PA3 – PA7 as Input)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PA7 Pin	PA6 Pin	PA5 Pin	PA4 Pin	PA3 Pin	PA2 Pin	PA1 Pin	PA0 Pin
= 0	= 0	= 0	= 0	= 0	= 1	= 1	= 1

I/O Ports (Cont.)

Control Register

This register is used in both Standard MCU I/O Mode and Address Out modes. For setting a Standard MCU I/O Mode, a "1" must be written to the corresponding bit in the register. Writing a "0" to the register is required for the Address Out mode. The register has a default value of "0" after reset.

Direction Register

This register is used to control the direction of data flow in the I/O ports. Writing a "1" to the corresponding bit in the register configures the port to be an output port, and a "0" forces the port to be an input port. The I/O configuration of the port pins can be determined by reading the Direction Register. After reset, the pins are in input mode.

Open Drain Register

This register determines whether the output pin driver of Port C or D is a CMOS driver or an Open Drain driver. Writing a "0" to the register selects a CMOS driver, while a "1" selects an Open Drain driver.

Special Function Register

Writing a "1" bit to this register sets up the corresponding pin to operate in Special Function Out mode.

PLD – I/O Register

This is a read only status register. Reading a "1" indicates the corresponding pin is configured as a PLD pin. A "0" indicates the pin is an I/O pin.

Data In Register

This register is used in the Standard MCU I/O Mode configuration to read the input pins.

Data Out Register

This register holds the output data in the Standard MCU I/O Mode. The contents of the register can also be read.

Macrocell Out Register

This register enables the user to read the outputs of the GPLD macrocell (PA, PB, and PE macrocells).

I/O Register Address Offset

The I/O Register can be accessed by the microcontroller during normal read/write bus cycles. The address of a register is defined as:

CSIOP + register address offset

The CSIOP is the base address that is defined in the ABEL file and occupies a 256 byte space. The register address offset lies within this 256 byte space. Tables 15 and 15a are the address offset of the registers.

I/O Ports (Cont.)

Table 15. Register Address Offset

Register Name	Address Offset				
	Port A	Port B	Port C	Port D	Port E
Data In	00	01	10	11	20
Control	02	03	12	13	22
Data Out	04	05	14	15	24
Direction	06	07	16	17	26
Open Drain			18	19	
Special Function	08	09			28
PLD – I/O	0A	0B			2A
Macrocell Out	0C	0D			2C

Table 15a. Register Address Offset

(For 16-bit Motorola Microcontrollers in 16-bit mode. Use Table 15 if 8-bit mode is selected.)

Register Name	Address Offset				
	Port A	Port B	Port C	Port D	Port E
Data In	01	00	11	10	21
Control	03	02	13	12	23
Data Out	05	04	15	14	25
Direction	07	06	17	16	27
Open Drain			19	18	
Special Function	09	08			29
PLD – I/O	0B	0A			2B
Macrocell Out	0D	0C			2D

I/O Ports (Cont.)

Port A – Functionality and Structure

Port A is the most flexible of all the I/O ports. It can be configured to perform one or more of the following functions:

- ❑ Standard MCU I/O Mode
- ❑ PLD I/O
- ❑ Address Out – latched address lines assigned to pins PA[0-7]
- ❑ Address In – input port for other lines, inputs can be latched by ALE.
- ❑ Special Function Out – pins PA0 – PA3 can be configured as dedicated timer outputs.
- ❑ Peripheral I/O

Figure 20 shows the structure of a Port A pin. If the pin is configured as an output port, the multiplexer selects one of its four inputs as output. If the pin is configured as an input, the input connects to :

1. Data In Register as input in Standard MCU I/O Mode

or

2. PA Macrocell as PLD input

or

3. PA Macrocell as Address In input (latched for multiplexed bus).

Port B – Functionality and Structure

Port B is similar to Port A in structure. It can be configured to perform one or more of the following functions:

- ❑ Standard MCU I/O Mode
- ❑ PLD I/O
- ❑ Address Out – address lines A[0-7] for 8-bit multiplexed bus, or address lines A[8-15] for 16-bit multiplexed bus are assigned to pins PB[0-7].
- ❑ Special Function Out – pins PB0 - PB3 are configured as dedicated Timer outputs.

Figure 21 shows the structure of a Port B pin. If the pin is configured as an output port, the multiplexer selects one of its four inputs as output. If the pin is configured as input, the input connects to :

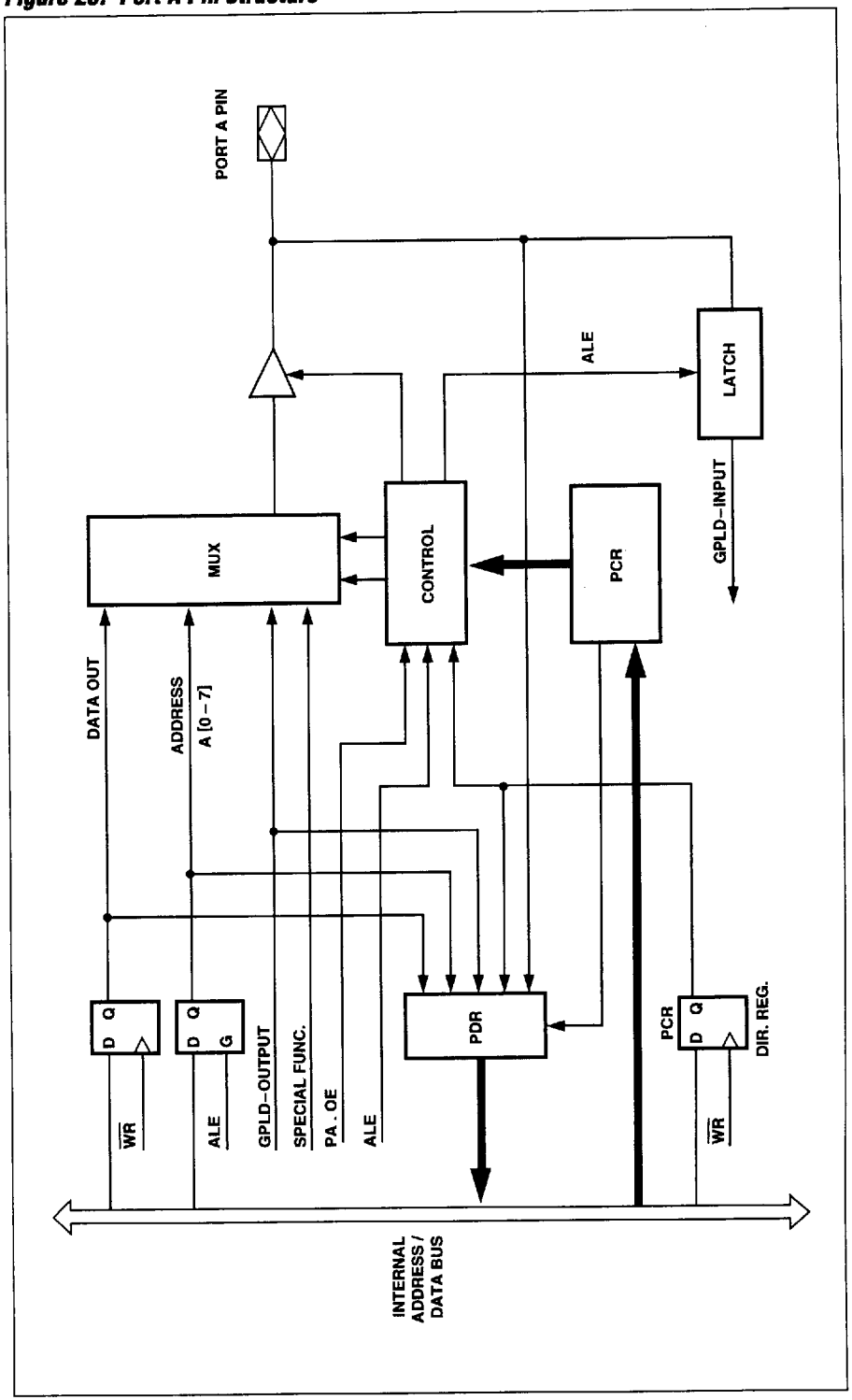
- ❑ Data In Register as input in Standard MCU I/O Mode

or

- ❑ PB Macrocell as PLD input

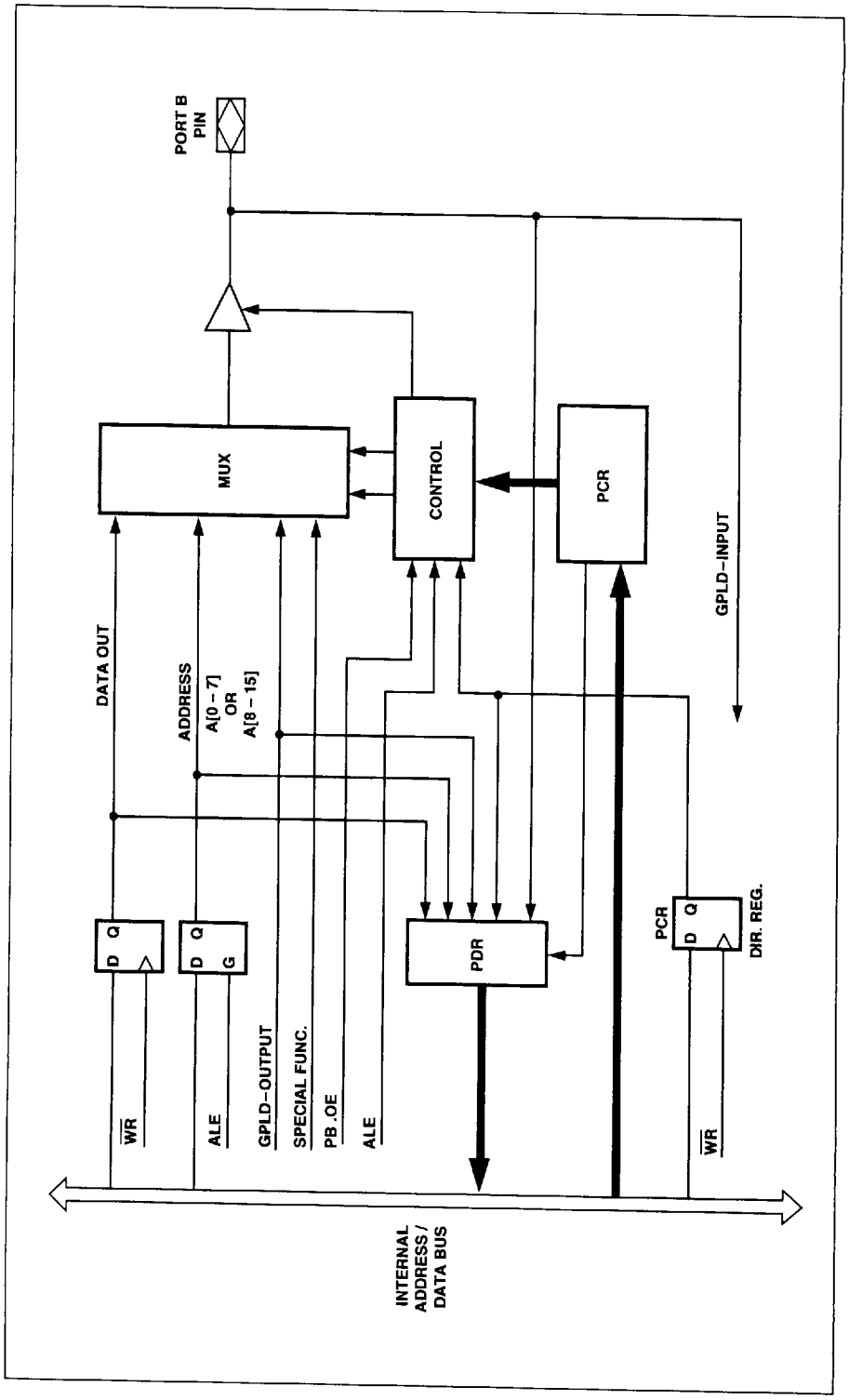
I/O Ports
(Cont.)

Figure 20. Port A Pin Structure



I/O Ports (Cont.)

Figure 21. Port B Pin Structure



6

I/O Ports (Cont.)

Port C and Port D – Functionality and Structure

Port C and D are identical in function and structure and each can be configured to perform one or more of the following operating modes:

- ❑ Standard MCU I/O Mode
- ❑ PLD Input – direct input to ZPLD
- ❑ Address Out – latched address outputs
  - Port C: A[0-7] are asigned to pins PC[0-7]
  - Port D: A[0-7] for 8-bit multiplexed bus, or A[8-15] for 16-bit multiplexed bus are assigned to pins PD[0-7]
- ❑ Data Port
  - Port C: D[0-7] for 8-bit non-multiplexed bus
  - Port D: D[8-15] for 16-bit non-multiplexed bus
- ❑ Open Drain – select CMOS or Open Drain driver

Figures 22 and 23 show the structure of a Port C or D pin. If the pin is configured as output port, the multiplexer selects one of the two inputs as output. If the pin is configured as input, the input connects to :

- ❑ Data In Register as input in the Standard MCU I/O Mode

or

- ❑ ZPLD input

Port E – Functionality and Structure

Port E can be configured to perform one or more of the following functions:

- ❑ Standard MCU I/O Mode
- ❑ PLD I/O
- ❑ Address Out – latched address lines A[0-7] are assigned to pins PE[0-7].
- ❑ Special Function Out – in this mode, Port E pin is configured as an output port for the following signals:

  PE2 – INTERRUPT – interrupt output from Interrupt Controller
  PE4 – Terminal Count output, Timer0
  PE5 – Terminal Count output, Timer1
  PE6 – Terminal Count output, Timer2
  PE7 – Terminal Count output, Timer3

- ❑ Alternate Function In – in this mode, the inputs to Port E pins are:

  PE0 – BHE/ or PSEN/ or WRH/ or UDS/ or SIZ0
  PE1 – ALE
  PE3 – TIMER0-IN :load/store/enable/ disable input to Timer 0
  PE4 – TIMER1-IN :load/store/enable/disable input to Timer 1
  PE5 – TIMER2-IN :load/store/enable/disable input to Timer 2
  PE6 – TIMER3-IN :load/store/enable/disable input to Timer 3
  PE7 – APD CLK :clock input for Automatic Power Down Counter

Figure 24 shows the structure of a Port E pin. The Control Logic block selects one of four sources through the multiplexer for pin output. If the pin is configured as input, the input goes to:

- ❑ Data In Register as input in Standard MCU I/O Mode

or

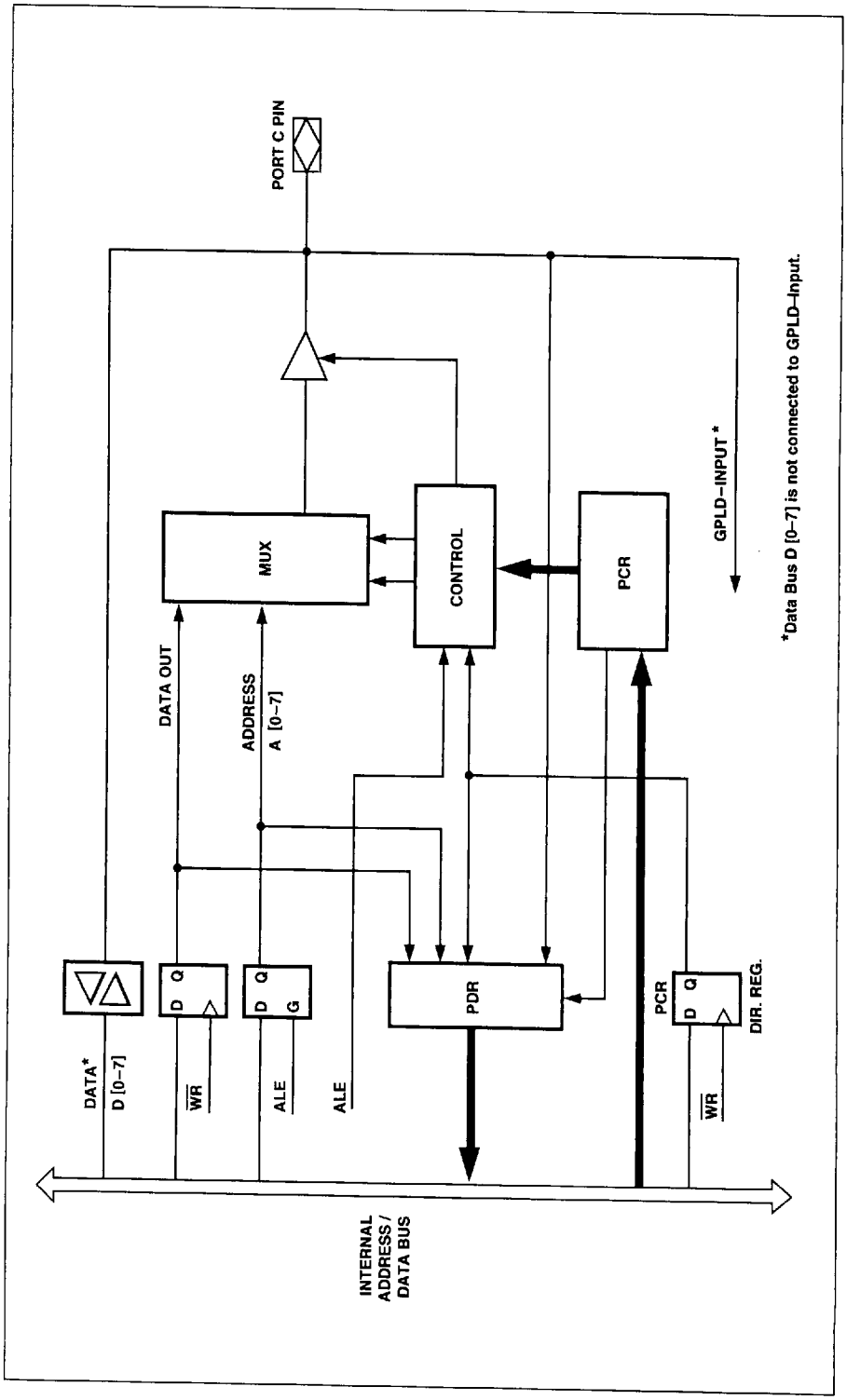
- ❑ PE Macrocell as PLD input

or

- ❑ Alternate Function In

I/O Ports
(Cont.)

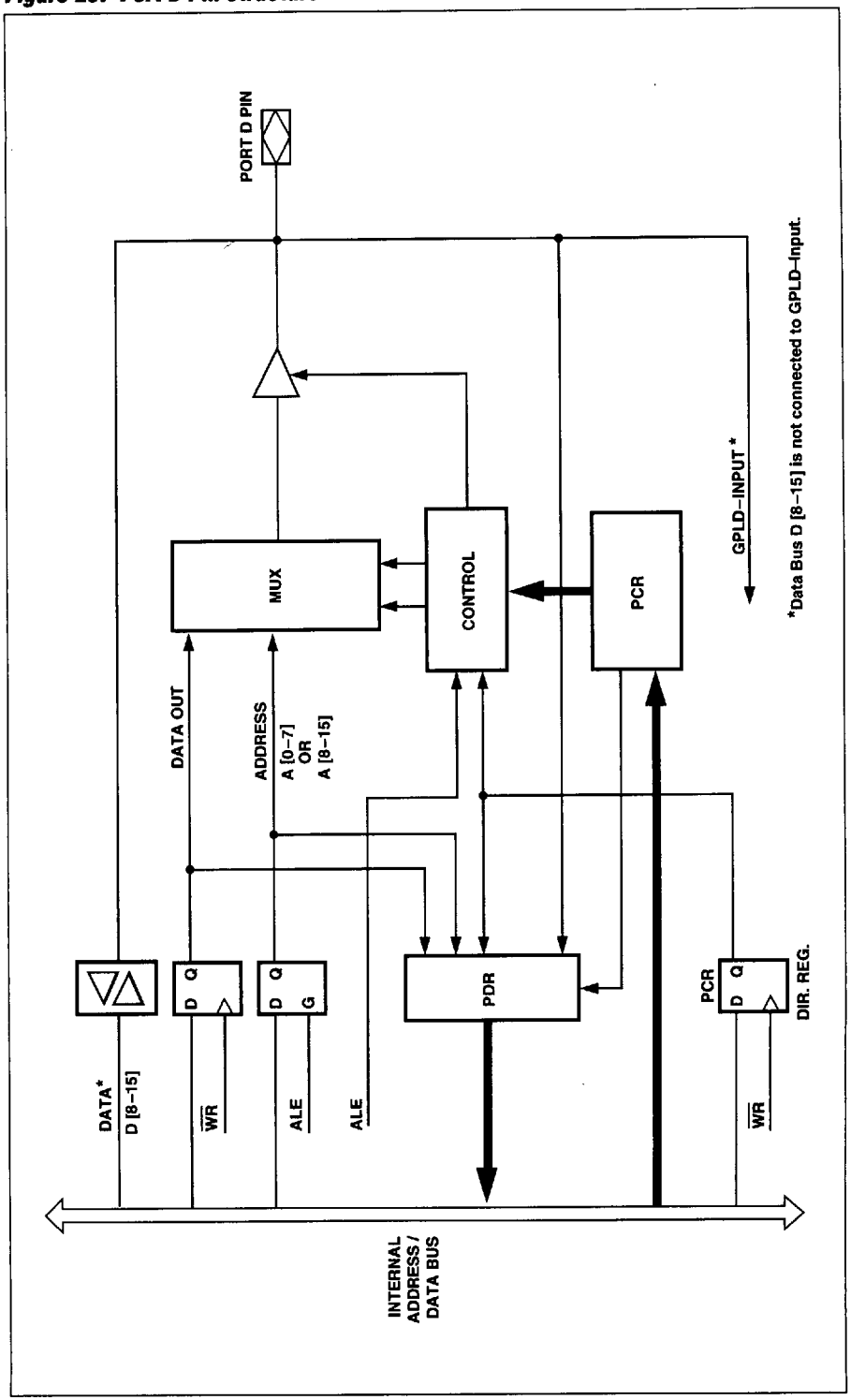
Figure 22. Port C Pin Structure



6

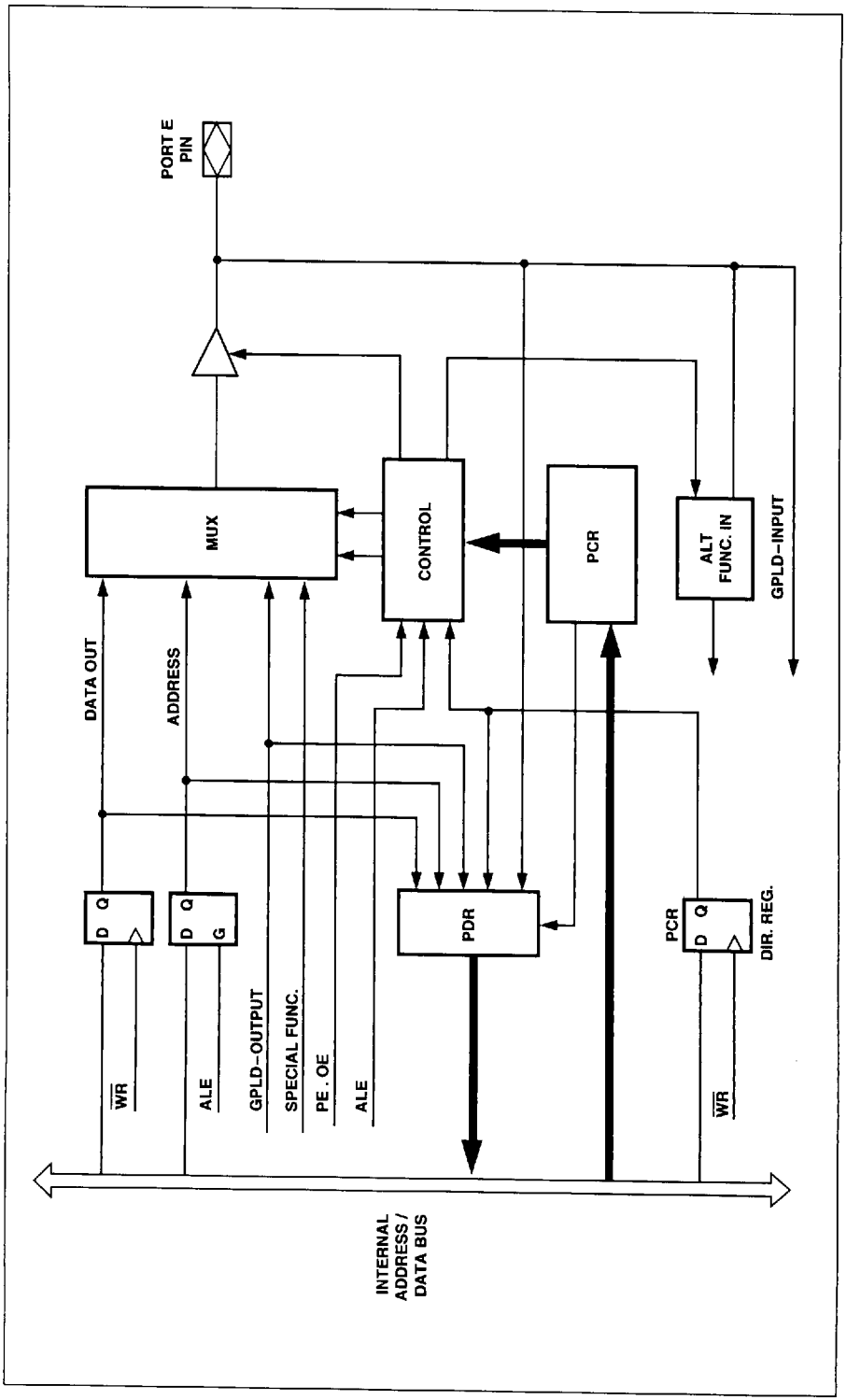
I/O Ports
(Cont.)

Figure 23. Port D Pin Structure



I/O Ports
(Cont.)

Figure 24. Port E Pin Structure



6

Memory Block

The PSD5XX provides EPROM memory for code storage and SRAM memory for scratch pad usage. Chip selects for the memory blocks come from the DPLD decoding logic and are defined by the user in the PSDsoft Software. Figure 25 shows the organization of the Memory Block.

EPROM

The PSD5XX provides three EPROM densities: 256K bit, 512K bit or 1M bit. The EPROM is divided into four 8K, 16K or 32K byte blocks. Each block has its own chip select signals (ES0 – ES3). The EPROM can be configured as 32K x 8, 64K x 8 or 128K x 8 for microcontrollers with an 8-bit data bus. For 16-bit data buses, the EPROM is configured as 16K x 16, 32K x 16 or 64K x 16.

SRAM

The SRAM has 16K bits of memory, organized as 2K x 8 or 1K x 16. The SRAM is enabled by the chip select signal RS0 from the DPLD. The SRAM has a battery back-up (STBY) mode. This back-up mode is invoked when the V_{CC} voltage drops under the VSTBY voltage by 0.6 V. The VSTBY voltage is connected only to the SRAM and cannot be lower than 2.7 volts. The SRAM Data Retention voltage is 2 volts.

Memory Select Map

The EPROM and SRAM chip select equations are defined in the ABEL file in terms of address and other DPLD inputs. The memory space for the EPROM chip select (ES0 – ES3) should not be larger than the EPROM block (8KB, 16KB or 32KB) it is selecting.

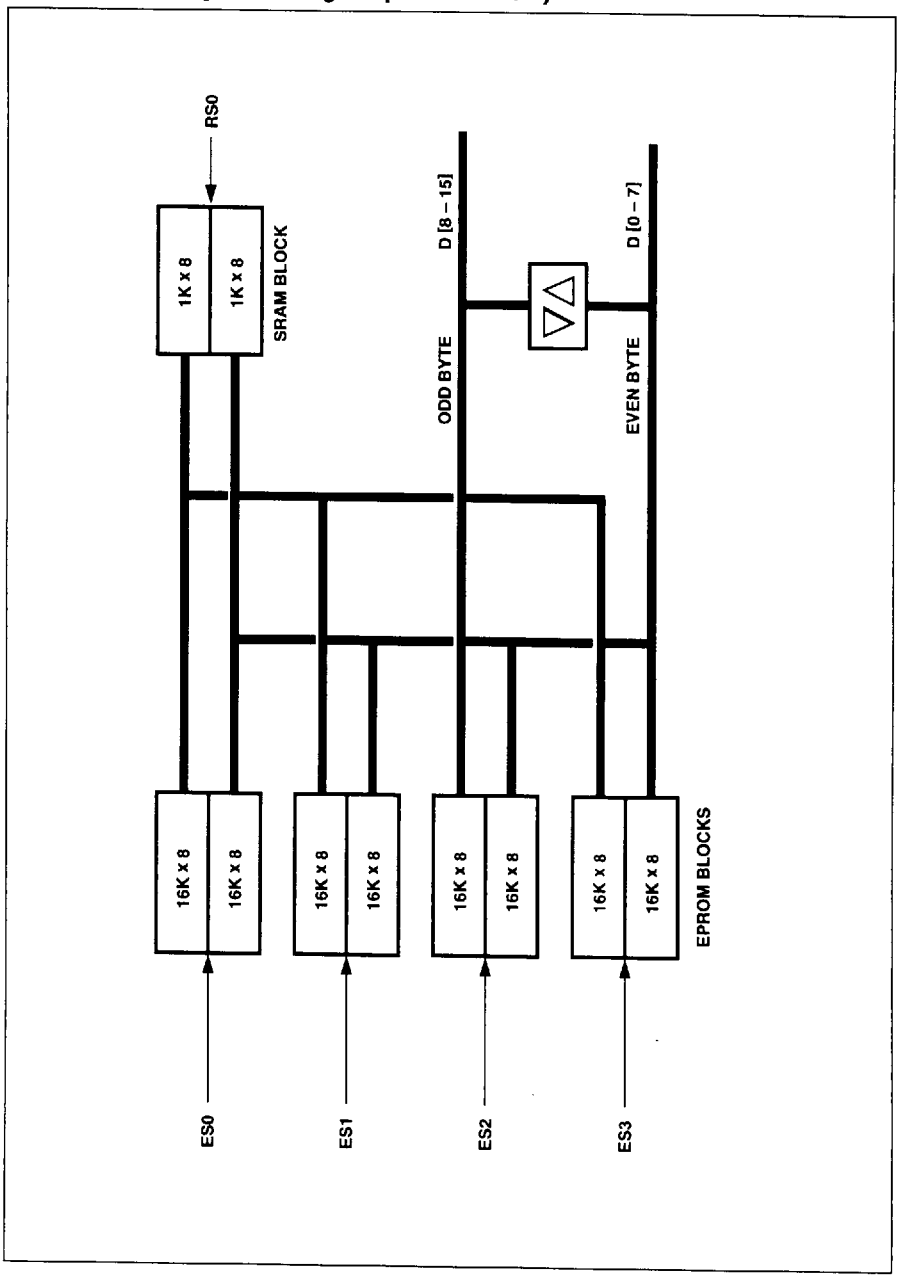
The following rules govern how the internal PSD5XX memory selects/space are defined:

- ❑ The EPROM blocks address space cannot overlap
- ❑ SRAM, internal I/O and Peripheral I/O space cannot overlap
- ❑ SRAM, internal I/O and Peripheral I/O space can overlap EPROM space, with priority given to SRAM or I/O. The portion of EPROM which is overlapped cannot be accessed.

The Peripheral I/O space refers to memory space occupied by peripherals when Port A is configured in the Peripheral I/O Mode.

Memory Block (Cont.)

Figure 25. Memory Block Diagram (128KB EPROM)



Memory Block (Cont.)

Memory Select Map For 8031 Application

The 8031 family of microcontrollers has separate code memory space and data memory space. This feature requires a different Memory Select Map. Two modes of operation are provided for 8031 applications. The selection of the modes is specified in the PSD5XX PSDsoft Software (PSDconfiguration):

- ***Separate Space Mode***
  In this mode, the PSEN signal is used to access code from EPROM, and the RD signal is used to access data from SRAM. The code memory space is separated from the data memory space.
- ***Combined Space Mode***
  In this mode, the EPROM can be accessed by PSEN or RD. The EPROM is used for code and data storage. The memory block's address space cannot overlap.

If data and code memory blocks must overlap each other, the $\overline{RD}$ signal can be included as an additional address input in generating the EPROM chip select signals (ES0 – ES3). In this case the EPROM access time is from the $\overline{RD}$ valid to data valid. Figures 26a and 26b show the memory configuration in the two modes.

In some applications it is desirable to execute program codes in SRAM. The PSD5XX provides this option by enabling PSEN to access SRAM. To activate this option, the SRCODE bit of the VM Register must be set to "1" (see Table 16). SRAM space can overlap EPROM space and has priority when PSEN is used.

Table 16. VM Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
*	*	*	*	*	*	SRCODE	PIO
						1 = ON	1 = ON

* = Reserved for future use, bits set to zero.

Memory Block (Cont.)

Figure 26a. 8031 Memory Modes

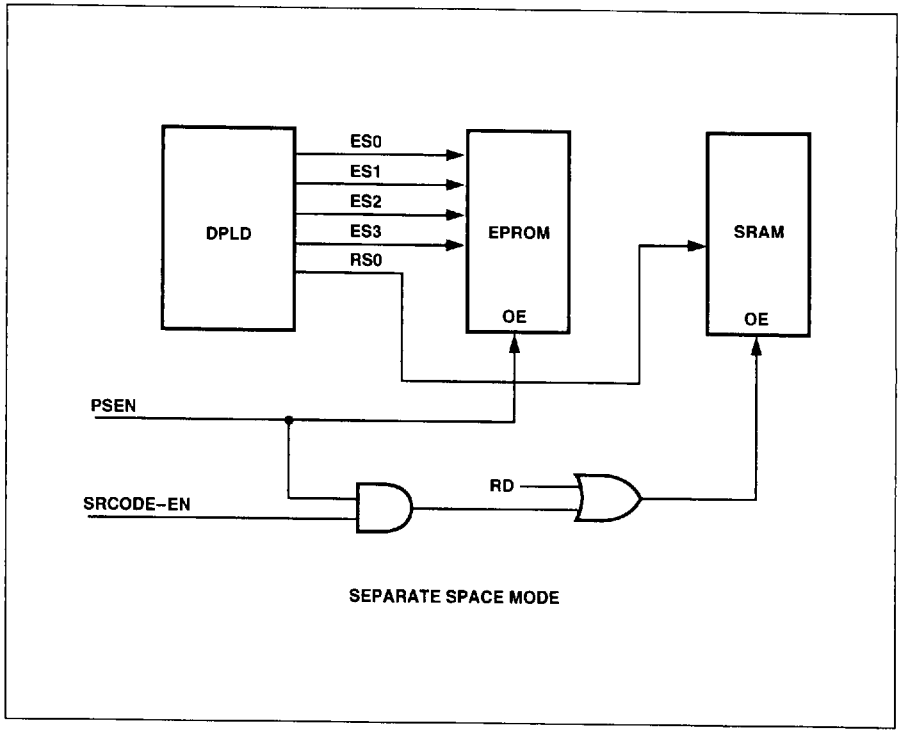
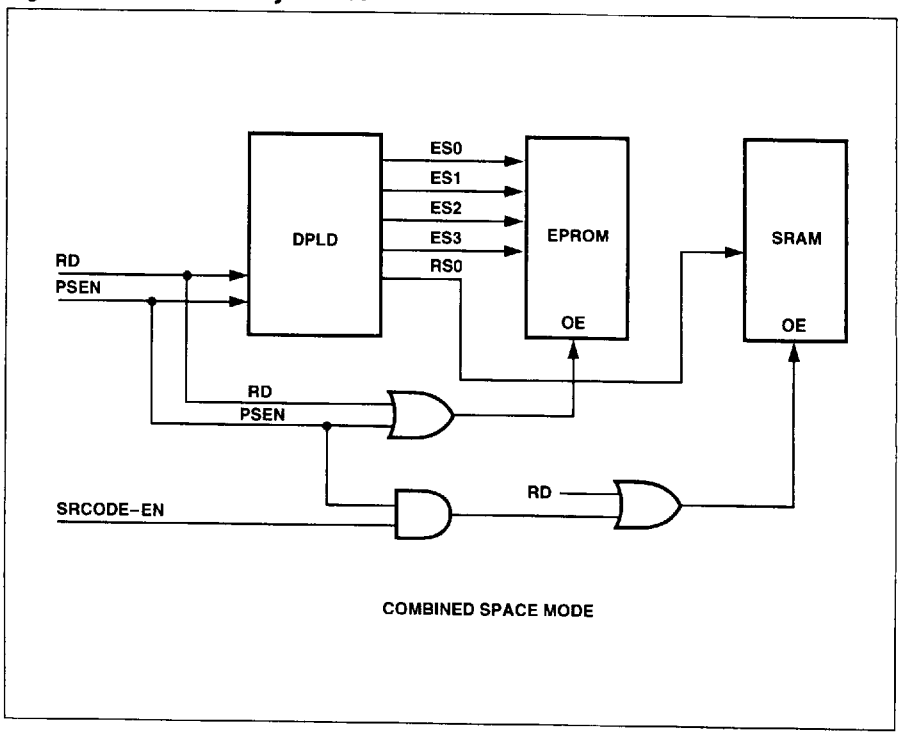


Figure 26b. 8031 Memory Modes



Peripheral I/O

Peripheral I/O

The Peripheral I/O Mode is one of the operating modes of Port A. In this mode, Port A is connected to the data bus of peripheral devices. Port A is enabled only when the microcontroller is accessing the devices, otherwise the Port is tri-stated. This feature enables the microcontroller to access external devices without requiring buffers and decoders. Figure 27 shows the structure of Port A in the Peripheral I/O Mode.

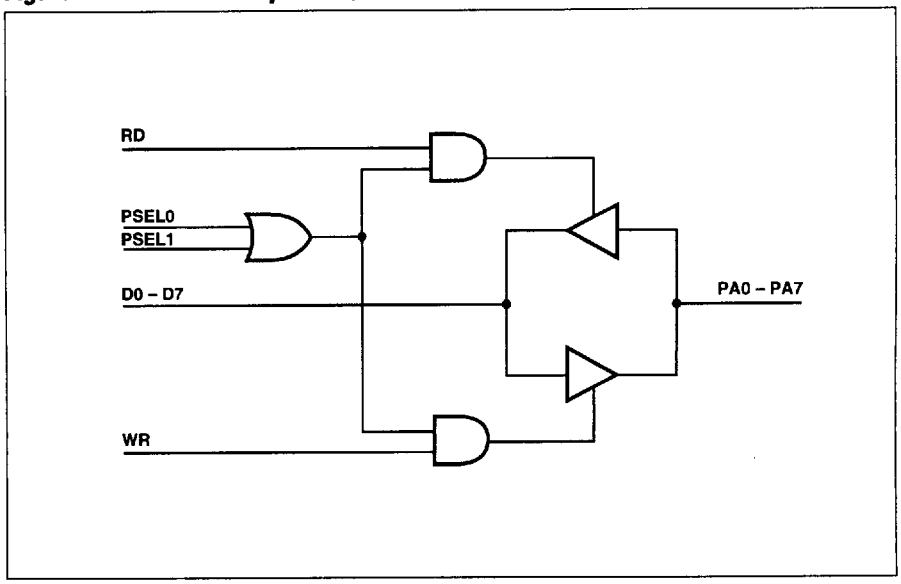
The memory address space occupied by the devices are defined by two signals: PSEL0 and PSEL1. The signals are direct outputs from the DPLD. Whenever any of the signals is active, the Port A driver is enabled, and the direction of the data flow is determined by the RD/WR signals.

The Peripheral I/O Mode and the peripheral select signals are configured and defined in the PSDsoft Software (see the section on I/O Port for configurations). The PIO bit in the VM Register (see Table 16) also needs to be set to "1" by the user to initialize the Peripheral I/O Mode.

The Peripheral I/O mode can be used, for example, in DMA applications where the microcontroller does not support DMA operations, such as tri-stating the address/data bus. Figure 28 shows a block diagram of a microcontroller and PSD5XX based design that makes use of this mode. In this application, the microcontroller has a multiplexed bus which is connected to the ADIO port. The C and D ports connect to the peripheral address bus and are both configured in Address Out Mode. Port A is configured in the Peripheral I/O mode and is connected to the peripheral data bus. Port B and E are used to generate control signals.

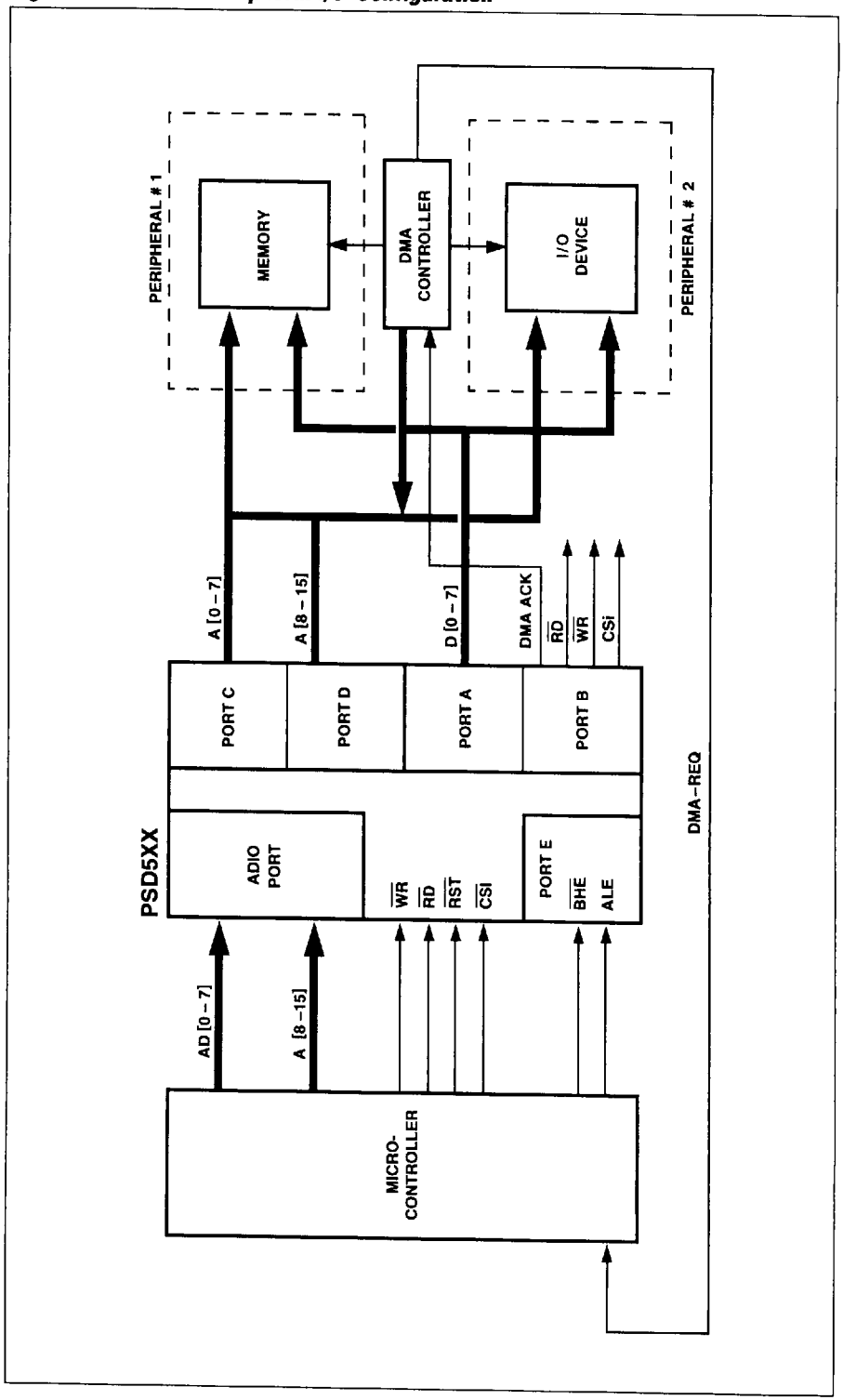
During normal activity, the microcontroller has access to any peripheral (memory or I/O device) through the PSD5XX device. When there is a DMA request, the microcontroller tri-states the address bus on Port C and D by writing a "0" to the port Direction Registers. The DMA controller then takes over the data and address buses after receiving acknowledgement from the microcontroller.

Figure 27. Port A In Peripheral I/O Mode



Peripheral I/O

Figure 28. PSD5XX Peripheral I/O Configuration

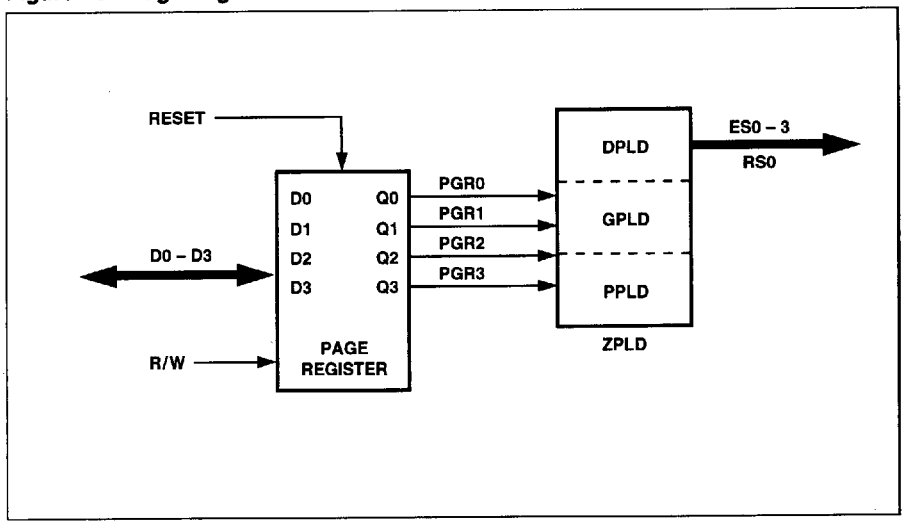


Page Register

The Page Register is 4 bits wide and consists of four D flip flops.The outputs of the Register (PGR0 – PGR3) are connected to the input bus of the ZPLD. By including the four outputs as inputs to the DPLD, the addressing capability of the microcontroller is increased by a factor of 16.

Figure 29 shows the Page Register block diagram. Inputs to the four flip flops are connected to data bus D0-D3. The output of the Register can be read by the microcontroller. The Register can operate as an independent register to the microcontroller if page mode is not implemented.

Figure 29. Page Register



Security Protection

The PSD5XX has a programmable security bit which offers protection from unauthorized duplication. When the security bit is set, the contents of the EPROM, the PSD5XX non-volatile configuration bits and ZPLD data are prevented from being read by EPROM programmers.

The security bit is set through the PSDsoft Software and is embedded in the compiled output file. The security bit is UV erasable and a secured part can be erased and then re-programmed.

Power Management Unit

The PSD5XX provides many power saving options. By configuring the PMMRs (Power Management Mode Registers), the user can reduce power consumption. Table 17 shows the bit configuration of the PMMR0 and PMMR1. The microcontroller is able to control the power consumption by changing the PMMR bits at run time.

Standby Mode

There are two Standby Modes in the PSD5XX:

- ❑ **Power Down Mode**
- ❑ **Sleep Mode**

Power Down

In this mode, the internal devices are shut down except for the I/O ports. There are three ways the PSD5XX can enter into the Power Down Mode: by controlling the CSI input, by activating the Automatic Power Down (APD) Logic, or when none of the inputs are changing and the turbo bit is off.

- ❑ **The CSI**

  The CSI input pin is an active low signal. When low, the signal selects and enables the PSD5XX. The PSD5XX enters into Power Down Mode immediately when the signal turns high. This signal can be controlled by the microcontroller, external logic or it can be grounded.

  The CSI turns off the internal bus buffers in standby mode. The address and control signals from the microcontroller are blocked from entering the ZPLD as inputs.

- ❑ **The APD Logic**

  The APD unit enables the user to enter a power down mode independent of controlling the CSI input. This feature eliminates the need for external logic (decoders and latches) to power down the PSD. The APD unit concept is based on tracking the activity on the ALE pin. If the APD unit is enabled and ALE is not active, the 4-bit APD counter starts counting and will overflow after 15 clocks, generating a PD (Power Down) signal powering down the PSD. If sleep mode is enabled, then PD signal will also activate the sleep mode. Immediately after ALE starts pulsing the PSD will get out of the power down or sleep mode.

  The operation of APD is controlled by the PMMR (see Figure 30a). PMMR1 bit 0 selects the source of the APD counter clock. After reset the APD counter clock is connected to PE7 (APD_CLK) on the PSD. In order to guarantee that the APD will not overflow there should be less than 15 APD clocks between two ALE pulses. If CLKIN frequency is adequate, then it can be connected to the APD and PE7 is used for other functions.

  The next step is to select the ALE power down polarity. Usually, MCUs entering power down will freeze their ALE at logic high or low. By programming bit 1 of PMMR0 the power down polarity can be defined for the APD. If the APD detects that the ALE is in the power down polarity for 15 APD counter clocks then the PSD will enter a power down mode. To enable the APD operation, bit 2 in the PMMR0 should be set high.

Sleep Mode

The Sleep Mode is activated if the SLEEP EN bit, the APD EN bit, and the ALE Polarity bit in the PMMR are set, and the APD Counter has overflowed after 15 clocks (see Figure 30). In Sleep Mode the PSD5XX consumes less power than the Power Down Mode, with typical I_{CC} reduced to 10 µA.

In this mode, the Counter/Timers, the Interrupt Controller and the ZPLD still monitor their inputs and respond to them. As soon as the ALE starts pulsing, the PSD5XX exits the Sleep Mode.

The PSD access time from Sleep Mode is specified by t_{LVDV1}. The ZPLD response time to an input transition is specified by t_{LVDV2}.

Power Management Unit (Cont.)

Figure 30. Power Management Unit

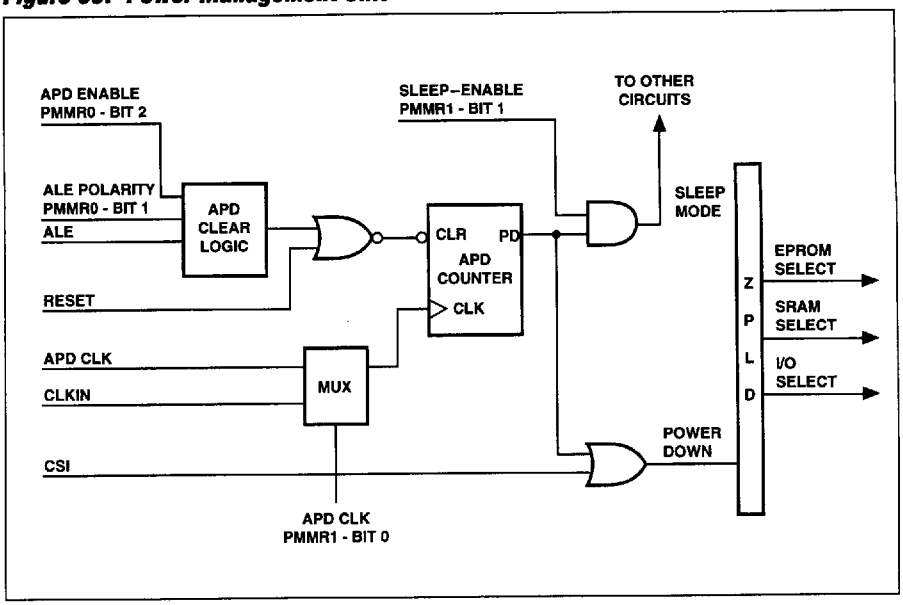
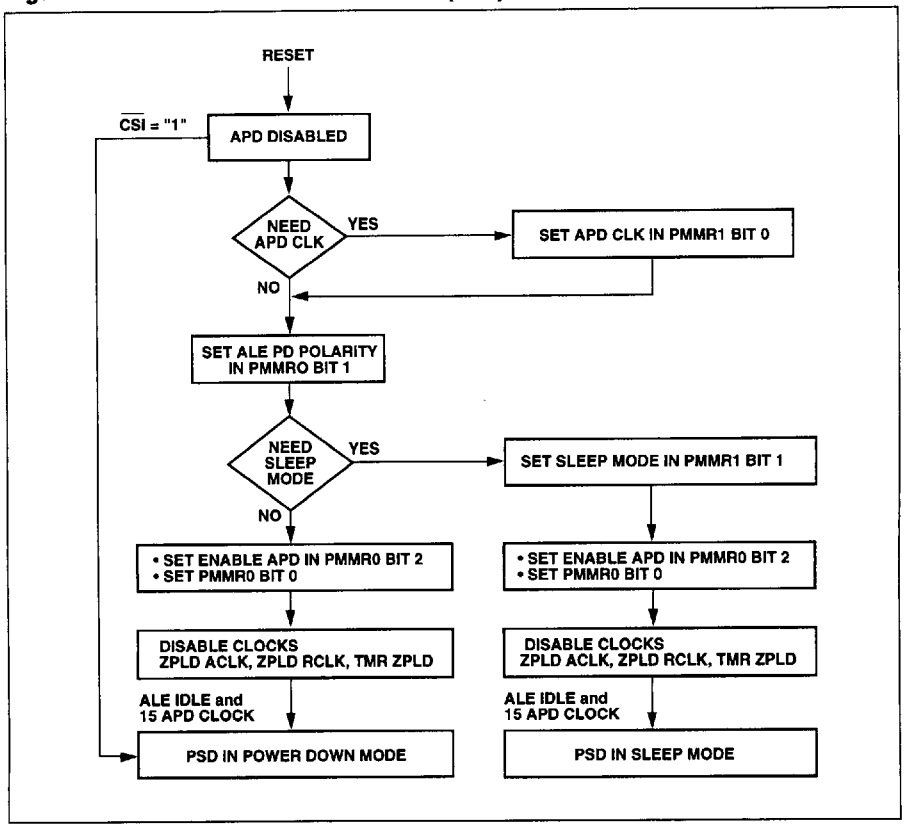


Figure 30a. Automatic Power Down Unit (APD) Flow Chart



Power Management Unit (Cont.)

Table 17. Power Management Mode Registers (PMMR0, PMMR1)

PMMR0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMR CLK	ZPLD RCLK	ZPLD ACLK	ZPLD TURBO	CMISER	APD ENABLE	ALE PD Polarity	*
1 = OFF	1 = OFF	1 = OFF	1 = OFF	1 = ON	1 = ON	1 = HIGH	

Bit 0 * = Should be set to High (1) to operate the APD.

Bit 1 0 = ALE Power Down (PD) Polarity Low.
1 = ALE Power Down (PD) Polarity High.

Bit 2 0 = Automatic Power Down (APD) Disable.
1 = Automatic Power Down (APD) Enable.

Bit 3 0 = EPROM/SRAM CMiser is OFF.
1 = EPROM/SRAM CMiser is ON.

Bit 4 0 = ZPLD Turbo is ON. ZPLD is always ON.
1 = ZPLD Turbo is OFF. ZPLD will Power Down when inputs are not changing.

Bit 5 0 = ZPLD Clock Input into the Array from the CLKIN pin input is connected. Every Clock change will Power Up the ZPLD when Turbo bit is OFF.
1 = ZPLD Clock Input into the Array from the CLKIN pin input is disconnected.

Bit 6 0 = ZPLD Clock Input into the the MacroCell registers from the CLKIN pin input is connected.
1 = ZPLD Clock Input into the the MacroCell registers from the CLKIN pin input is disconnected.

Bit 7 0 = In the PSD5XX Clock Input is connected to the Timer.
1 = In the PSD5XX Clock Input is disconnected from the Timer.

PMMR1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
*	*	*	*	*	*	Sleep Mode	APD CLK
						1 = ON	1 = CLKIN

Bit 0 0 = Automatic Power Down Unit Clock is connected to Port E7 (PE7) alternate function input.
1 = Automatic Power Down Unit Clock is connected to the PSD Clock input (CLKIN).

Bit 1 0 = Sleep Mode Disabled.
1 = Sleep Mode Enabled.

Bit 2–7 0 = Reserved for future use, should be set to zero.

Table 18. APD Counter Operation

APD EN Bit	ALE Power Down Polarity	ALE Status	APD Counter
0	X	X	Not Counting
1	X	Pulsing	Not Counting
1	1	1	Counting (Activates Standby Mode After 15 Clocks)
1	0	0	Counting (Activates Standby Mode After 15 Clocks)

6

Power Management Unit (Cont.)

Other Power Saving Options

The PSD5XX provides additional power saving options. These options, except the SRAM Standby Mode, can be enabled/disabled by setting up the corresponding bit in the PMMR.

❑ EPROM

The EPROM power consumption in the PSD is controlled by bit 3 in the PMMR0 – EPROM CMiser. Upon reset the CMiser bit is OFF. This will cause the EPROM to be ON at all times as long as CSI is enabled (low). The reason this mode is provided is to reduce the access time of the EPROM by 10 ns relative to the low power condition when CMiser is ON. If CSI is disabled (high) the EPROM will be deselected and will enter standby mode (OFF) overriding the state of the CMiser.

If CMiser is set (ON) then the EPROM will enter the standby mode when not selected. This condition can take place when CSI is high or when CSI is low and the EPROM is not accessed. For example, if the MCU is accessing the SRAM, the EPROM will be deselected and will be in low power mode.

An additional advantage of the CMiser is achieved when the PSD is configured in the by 8 mode (8 bit data bus). In this case an additional power savings is achieved in the EPROM (and also in the SRAM) by turning off 1/2 of the array even when the EPROM is accessed (the array is divided internally into odd and even arrays).

The power consumption for the different EPROM modes is given in the DC Characteristics table under I_{CC} (DC) EPROM Adder.

❑ SRAM Standby Mode

The SRAM has a dedicated supply voltage V_{STBY} that can be used to connect a battery. When V_{CC} becomes lower than $V_{STBY}-0.6$ then the PSD will automatically connect the V_{STBY} as a power source to the SRAM. The SRAM Standby Current (I_{STBY}) is typically 0.5 µA.

SRAM data retention voltage V_{DF} is 2 V minimum.

❑ Zero Power ZPLD

ZPLD power/speed is controlled by the ZPLD_Turbo bit (bit 4) in the PMMR0. After reset the ZPLD is in Turbo mode and runs at full power and speed. By setting the bit to "1", the Turbo mode is disabled and the ZPLD is consuming Zero Power current if the inputs are not switching for an extended time of 100 ns. The propagation delay time will be increased by 10ns after the Turbo bitis set to "1" (turned off) if the inputs change at a frequency of less than 15 MHz.

Power Management Unit (Cont.)

❑ Input Clock

The PSD5XX provides the option to turn off the clock inputs to save AC power consumption. The clock input (CLKIN) is used as a source for driving the following modules:

- ❑ ZPLD Array Clock Input
- ❑ ZPLD MacroCell Clock Flip Flop
- ❑ APD Counter Clock
- ❑ Counter/Timers Clock

During power down or if any of the modules are not being used the clock to these modules should be disabled. To reduce AC power consumption, it is especially important to disable the clock input to the ZPLDS array if it is not used as part of a logic equation.

The ZPLD Array Clock can be disabled by setting PMMR0 bit 5 (ZPLD ACLK). The ZPLD MacroCell Clock Input can be disabled by setting PMMR0 bit 6 (ZPLD RCLK). The Timer Clock can be disabled by setting PMMR0 bit 7 (TMR CLK). The APD Counter Clock will be disabled automatically if Power Down or Sleep Mode is entered through the APD unit. The input buffer of the CLKIN input will be disabled if bits 5 – 7 PMMR0 are set and the APD has overflowed.

The Counter/Timers can operate in Sleep Mode if the TMR CLK bit is low, but the power consumption will be based on the frequency of operation (CLKIN frequency).

Table 19. Summary of PSD5XX Timing and Standby Current During Power Down and Sleep Modes

	PLD Propagation Delay	PLD Recovery Time To Normal Operation	Access Time	Access Recovery Time To Normal Access	Typical Standby Current Consumed
Power Down	Normal t_{PD} (Note 1)	0	No Access	t_{LVDV}	40 µA (Note 4)
Sleep	t_{LVDV2} (Note 2)	t_{LVDV3} (Note 3)	No Access	t_{LVDV1}	5 µA (Note 5)

NOTES:
1. Power Down does not affect the operation of the ZPLD. The ZPLD operation in this mode is based only on the ZPLD_Turbo Bit.
2. In Sleep Mode any input to the ZPLD will have a propagation delay of t_{LVDV2}.
3. PLD recovery time to normal operation after exiting Sleep Mode. An input to the ZPLD during the transition will have a propagation delay time of t_{LVDV3}.
4. Typical current consumption assuming all clocks are disabled and ZPLD is in non-turbo mode.
5. Typical current consumption assuming all clocks are disabled.

Table 20. I/O Pin Status During Power Down And Sleep Mode

Port Configuration	Pin Status
I/O Port	Unchanged
ZPLD Output	Depend on Inputs to the ZPLD
Address Out	Undefined
Data Port	Tri-stated
Special Function Out	Depending on Status of Clock Input
Peripheral I/O	Tri-stated

PSD5XX Counter/Timer

General Description

The PSD5XX contains a powerful set of four 16 bit Counter/Timers, each controlled by either PPLD outputs, external pins or Software. The Counter/Timers aid the user in counting external events and/or generating accurate delays. These can be operated as Counters or Timers. In Event-count, time capture and WatchDog modes, the Counter/Timers work as Counters, whereas in Waveform and Pulse modes they work as Timers. All Counter/Timers are capable of generating interrupts through the On-Board Interrupt Controller. Each of the Counter/Timers consist of a Counter/Timer Command register, Counter/Timer Image register and Counter/Timer register. All four Counter/Timers share a Global command register, a Software Load/Store register, a Freeze command register and the Status register. Counter/Timer 2 can support WatchDog operations. All Counter/Timers share a common clock input and Delay Cycle register used in scaling down the input clock to the Counter/Timer. The maximum resolution of the Counter/Timer is the input clock of the PSD5XX divided by four. The maximum input clock frequency to the PSD5XX is 30 MHz. Figures 31 and 32 describe the general features of the Counter/Timers.

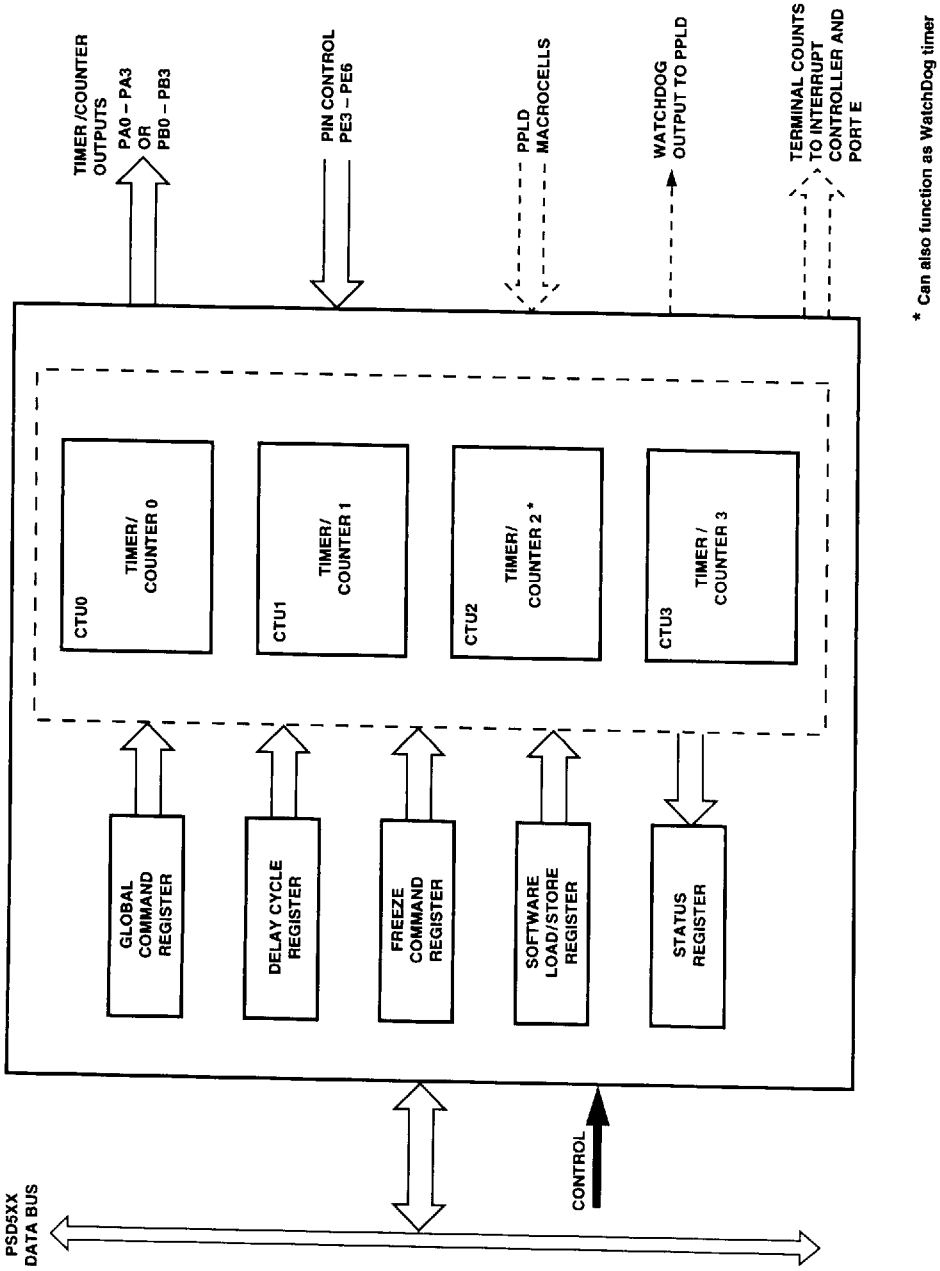
Features

- ❑ Four 16 bit Counter/Timers.
- ❑ Five modes of operation
  - Waveform Mode
  - Pulse Mode
  - Event Counter Mode
  - Time Capture Mode
  - WatchDog Mode*
- ❑ Each Counter/Timer can be controlled by an input pin, dedicated PPLD macrocell or software.
- ❑ Each Counter/Timer has an output to the Interrupt Controller.
- ❑ The WatchDog output is routed through the PLD and can be programmed to be output at any PLD output pin.
- ❑ Programmable input and output polarity.
- ❑ Counter/Timer can be programmed as UP or DOWN Counter, except in WatchDog mode.
- ❑ All Counters have the operating frequency range of DC to 7.0 MHz (i.e 143 ns maximum resolution at 7.0 MHz). Higher resolution can be achieved by using in conjunction with the GPLD macrocells.
- ❑ High resolution Divisor unit for Counter clocking purposes.
- ❑ Can easily interface with any 8 or 16 bit Microcontroller or Microprocessor.

(*) Counter/Timer-2 can operate in WatchDog mode.

PSD5XX Counter/Timer (Cont.)

Figure 31. Counter/Timer Block Diagram



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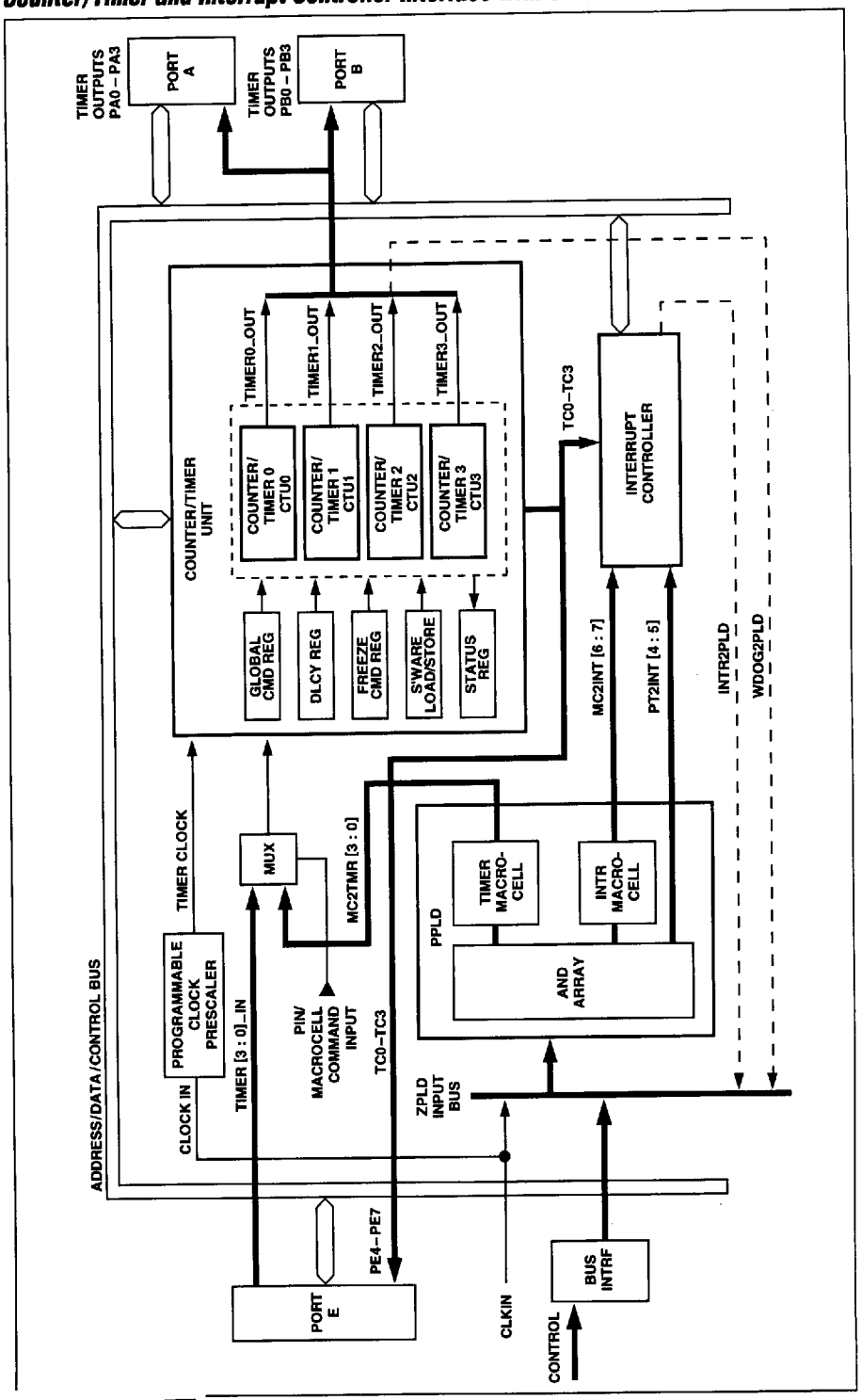
PSD5XX Counter/Timer (Cont.)

Figure 32. Counter/Timer and Interrupt Controller Interface with Other Internal Blocks



Counter/Timer Operation

There are four identical 16 bit Counter/Timers CNTR0,CNTR1,CNTR2 and CNTR3 and associated Counter/Timer image registers IMG0,IMG1,IMG2 and IMG3. Refer to Table 21 for counter name and register correspondence. All Counter/Timers share a common clock source. Each Counter/Timer can be operated in either WAVEFORM / PULSE mode or EVENT COUNTER/TIME CAPTURE mode. Counter 2 can be set up as a Watchdog timer in both modes. Note that in Event Counter/Time Capture mode COUNTER 2 can only be set up as a Watch Dog Counter/Timer, whereas in the Waveform/Pulse mode Counter 2 can be configured as a Pulse or Waveform generator or as a Watchdog timer. Refer to Table 24 for possible combinations of Counter/Timer modes and refer to Figure 33 for additional details.

Each Counter/Timer can be controlled by an input pin or through a dedicated PPLD macrocell output or by software. Counter/Timer outputs are available through port A or port B pins in alternate function mode (Refer to the chapter on I/O ports). Polarity of these inputs/outputs is software programmable. The following sections describe various command and data registers that need to be initialized for proper function of these Counter/Timers.

Counter/Timer Operating Modes

The PSD5XX Counter/Timer has five basic modes of operation: The Waveform and Pulse or Event Counter, Time Capture, and Watchdog. The Waveform and Pulse modes cannot be used in conjunction with Event and Time Capture modes. Both Waveform/Pulse or Event Count/Time Capture modes can set Counter 2 into the fifth mode of operation, the "WatchDog" mode.

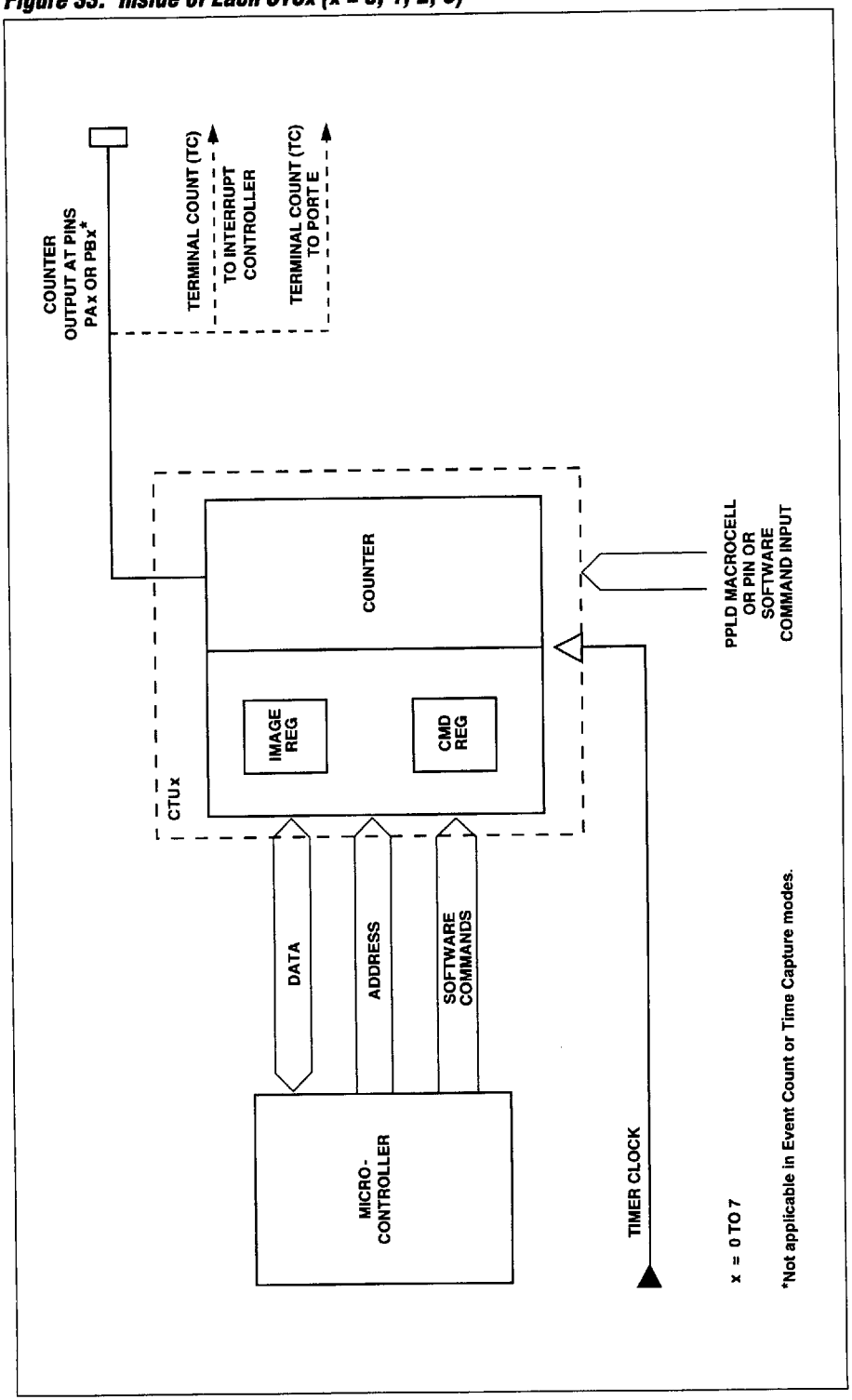
The basic functional element used in all these modes is the Counter/Timer unit (CTU) illustrated in Figure 33. This block consists of a 16 bit increment/decrement Counter, and a 16 bit image register with various control signals. The key function of the image register is to enable microcontroller access of the Counter without asynchronously interrupting the Counter. Software can configure each Counter/Timer using the associated Command register. The Counter/Timer of the PSD5XX employs four CTUs to realize the various modes of operation.

Table 21. Registers Used By Counters

Counter Name	Counting Register	Image Register
Counter 0	CNTR0	IMG0
Counter 1	CNTR1	IMG1
Counter 2	CNTR2	IMG2
Counter 3	CNTR3	IMG3

Counter/Timer Operation (Cont.)

Figure 33. Inside of Each CTUx (x = 0, 1, 2, 3)



Counter/Timer Operation (Cont.)

Waveform Mode

In Waveform mode, the Counter/Timer is capable of producing various pulse-width modulated (PWM) signals. The Waveform mode in the PSD5XX is realized using two CTUs (COUNTER/TIMER UNITs) in the following combinations:

CTU0 & CTU1 or CTU2 & CTU3.

The outputs of CTU0 and CTU2 are available at Port A and Port B. Refer to Tables 25 and 26 for further details and configuration of these ports. CTU1 and CTU3 are internally connected to CTU0 and CTU2. The Waveform mode is illustrated in Figure 34 which shows a typical PWM waveform and the time slots in which two CTUs are active. The Waveform period is the sum of the counts for CTU0 and CTU1 (see equation 1), while the duty cycle is given by equation 2. The Duty cycle of a waveform can be changed by loading a new value into the corresponding IMAGE register, and as soon as a Terminal Count is generated this new value gets loaded into the CTU. Note that the end of a CTU time slot is indicated with Terminal Count signal of the active CTU. The Terminal Count signals are used to signal the transfer of active status between CTUs. The Terminal Count is true whenever the Counter underflows while decrementing or when the Counter overflows while incrementing.

PERIOD of the waveform generated
= COUNT HIGH + COUNT LOW..(1)

DUTY Cycle of the Waveform Generated

$$= \frac{\text{COUNT HIGH}}{\text{COUNT HIGH + COUNT LOW}} \quad \text{.....(2)}$$

The timing of various pulses that create a Waveform signal in the above example is defined by the Microcontroller via image register updates of the CTU0 and CTU1. The contents of an image register are loaded or copied to the associated Counter under any of the following conditions:

- Terminal Count of CTU1 and/or CTU3 pulses to transfer active status to CTU0 and/or CTU2.
- An input pin (port E) pulses (If enabled by software).
- A PPLD macrocell output pulses (If enabled by software).
- A command register bit is written to by the Microcontroller, i.e., a software Load/Store (load).

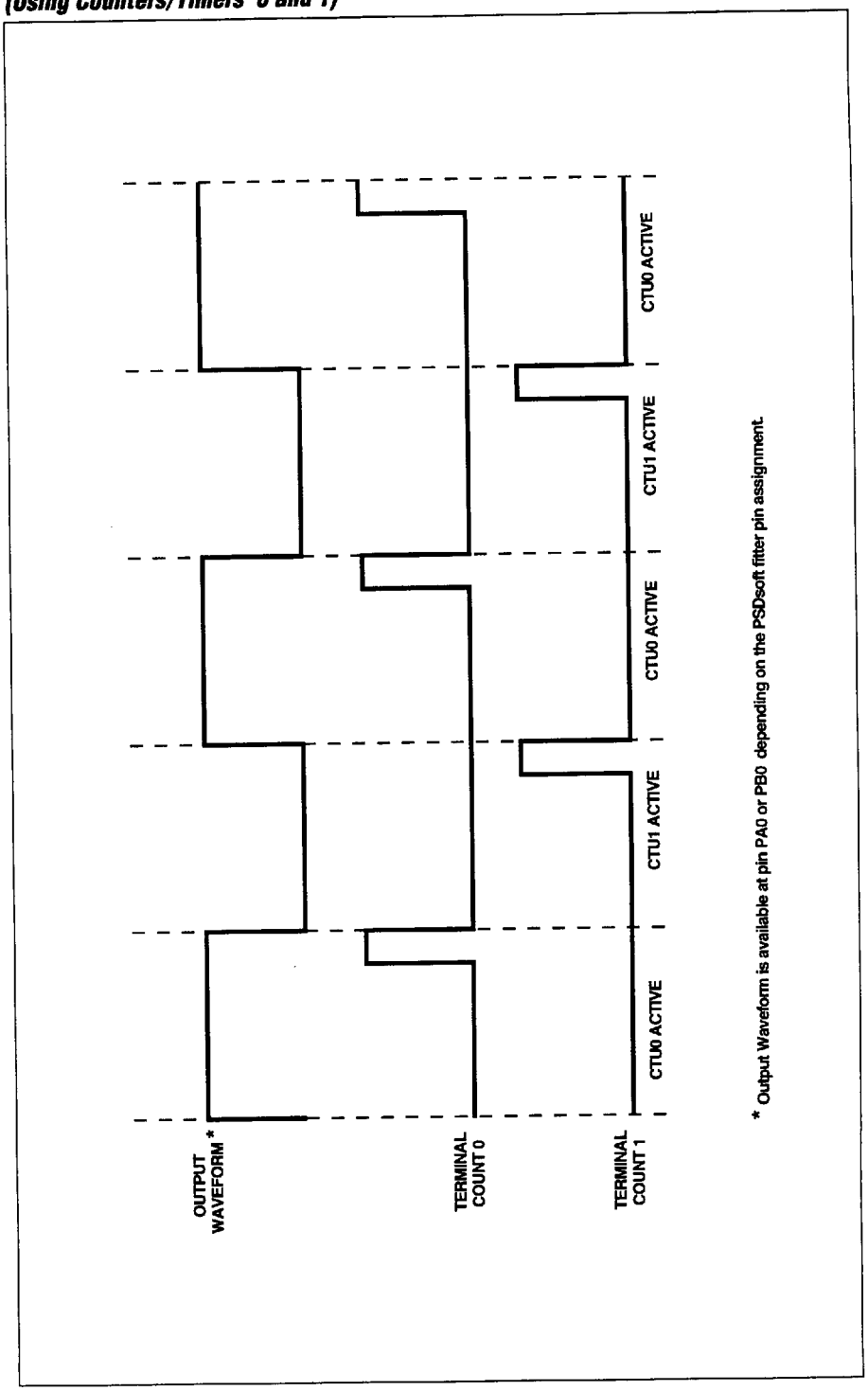
A Waveform output is first initialized and then later modified by setting its two corresponding software Load/Store bits after loading of the Image Registers. If the Counter/Timer register is directly loaded by the MCU, it gets overwritten by the associated Image register contents as soon as the Counter/Timer is active. The configuration of the CTU in the waveform mode is schematically illustrated in Figure 35.

The output polarity during the CTU0 time slot is controlled by bit 3 in the Counter/Timer command register. The output polarity during the CTU1 time slot is defined as the complement of the CTU0 polarity. Similarly, the polarity of the input pin is controlled by bit 4 in the Counter/Timer command register. This description of the waveform mode of operation applies to CTU2 and CTU3 also.

In order to change the image register values, use the Freeze/Freeze Acknowledge protocol as described in the Freeze Command Register section.

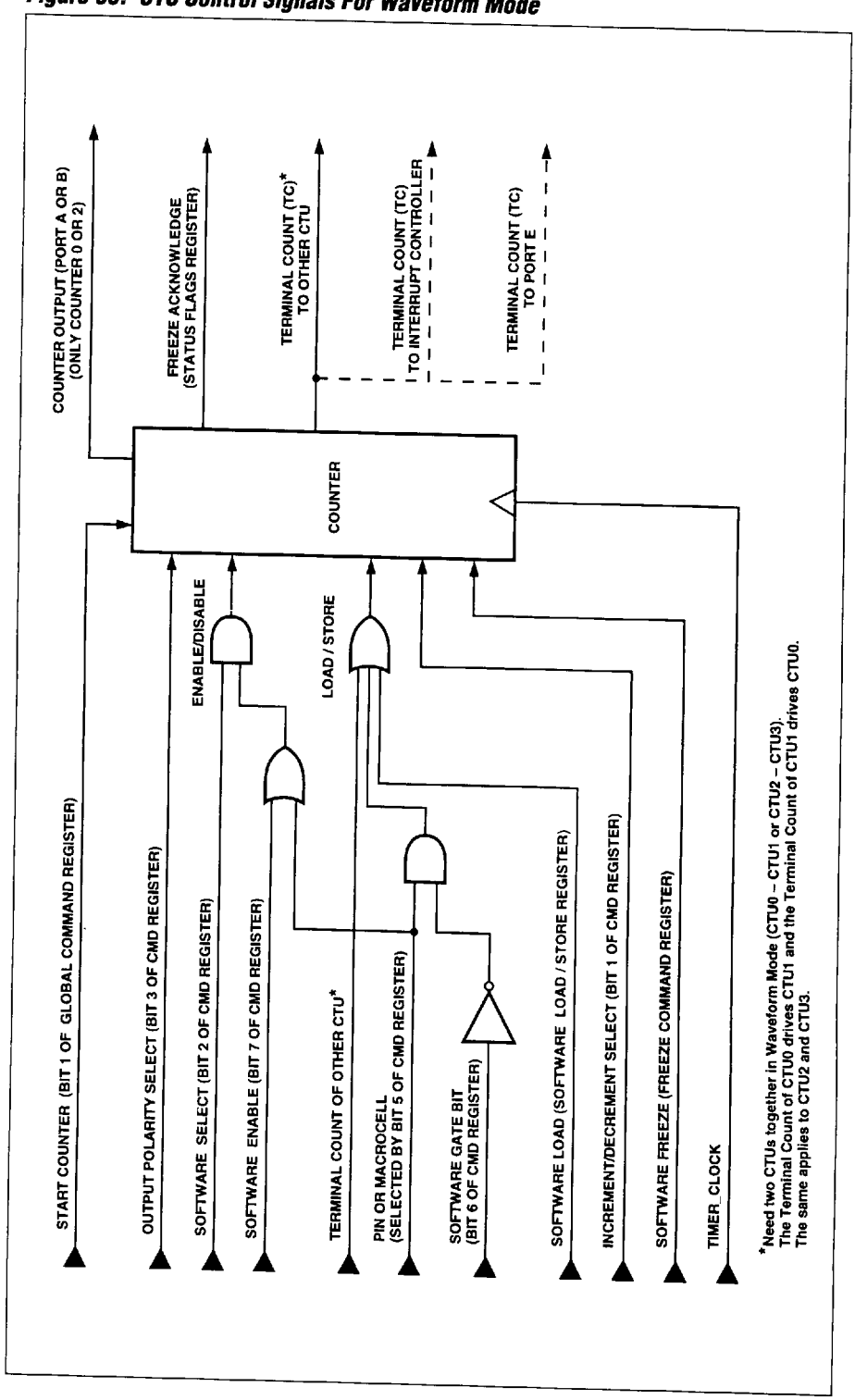
Counter/Timer Operation (Cont.)

Figure 34. Sample Waveform (PWM) and CTU Time Slots (Using Counters/Timers 0 and 1)



Counter/Timer Operation (Cont.)

Figure 35. CTU Control Signals For Waveform Mode



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Counter/Timer Operation (Cont.)

Pulse Mode

In Pulse mode, the Counter/Timer is capable of generating a one shot pulse. The Pulse width of the generated pulse is defined by the value loaded into the associated Image register of the timer. If the Counter/Timer register is directly loaded by the MCU, it gets overwritten by the associated Image register contents as soon as the Counter/Timer is active. Each CTU is capable of pulse mode. As soon as the Timer is active, i.e. decrementing or incrementing, a pulse is output until the Timer underflows or overflows. The pulse waveform is illustrated in Figure 36. The active level of this pulse is defined again by a command register bit. As can be seen in Figure 37, the pulse is triggered by any of the following events:

- ❑ Transition on the input pin (Port E) (If enabled by software).
- ❑ PPLD macrocell output pulses (If enabled by software).
- ❑ Command register bit is written to by a Microcontroller (Software load).

As in the waveform mode, the polarity of the input pin is defined by a command register bit and the Freeze/Freeze Acknowledge must be used whenever the image register is modified.

The outputs of CTU0, CTU1, CTU2 and CTU3 are available at Port A and Port B. Refer to Tables 25 and 26 for further details and configuration of these ports.

Event Counter Mode

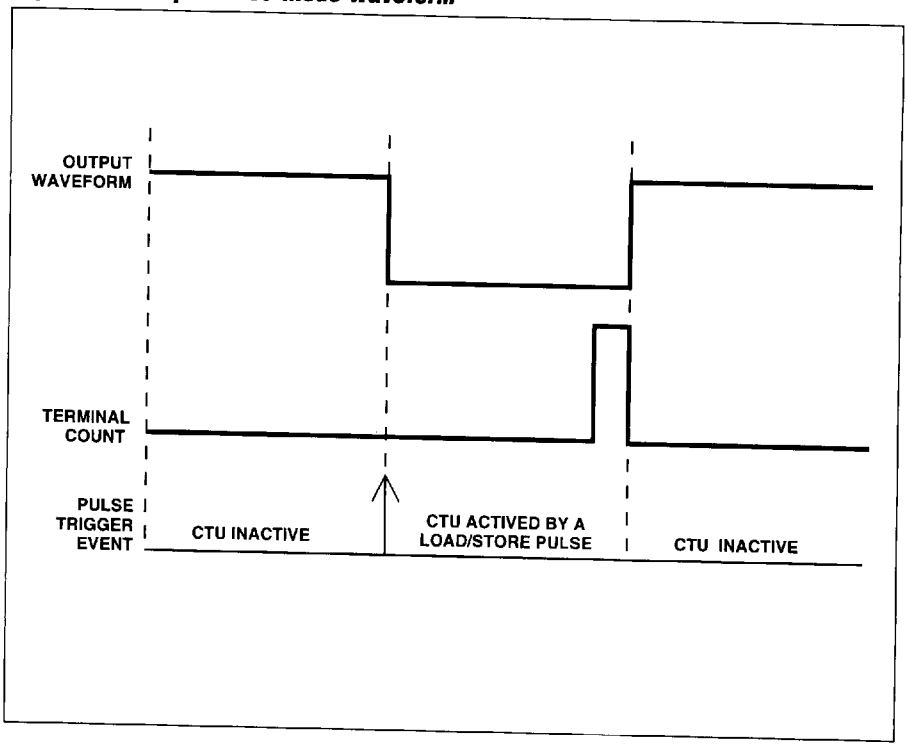
In this mode, the Counter/Timer uses the CTU to count a number of events. An event is defined as a signal-transition on the Counter's input pin as defined by the input polarity configuration bit in the Command Registers or a Low to High transition on the PPLD Macrocell output. In this mode, the image register of the CTU is used to store the contents of the Counter at the rising edge of the Load/Store signal. This is opposed to the previous two modes in which the image register was used to load the Counter. Figure 38 shows the configuration of the CTU for the event-Counter mode. Notice that the enable signal is edge sensitive. Its source is either:

- ❑ Pin Driven.
- ❑ PPLD Macrocell Driven.

All Counter/Timer registers must be assigned values during initialization in the Event Counter mode. During normal operation, the CTU increments or decrements its count when an event occurs. The image register is then immediately updated with the current count. The microcontroller can read the contents of the image register by first setting the command-register Freeze bit in order to disable count updates of the image register during its read operation. The microcontroller waits for a freeze acknowledge and then accesses the image register in the usual fashion. The Freeze signal effectively guarantees stable image register data during microcontroller read access, even though the CTU continues to count events. During the Freeze Acknowledge active state, the counter continues counting. Note that for an event to be counted the events must be separated by at least one timer clock period plus two CLKIN clock periods.

Counter/Timer Operation (Cont.)

Figure 36. Sample Pulse-Mode Waveform



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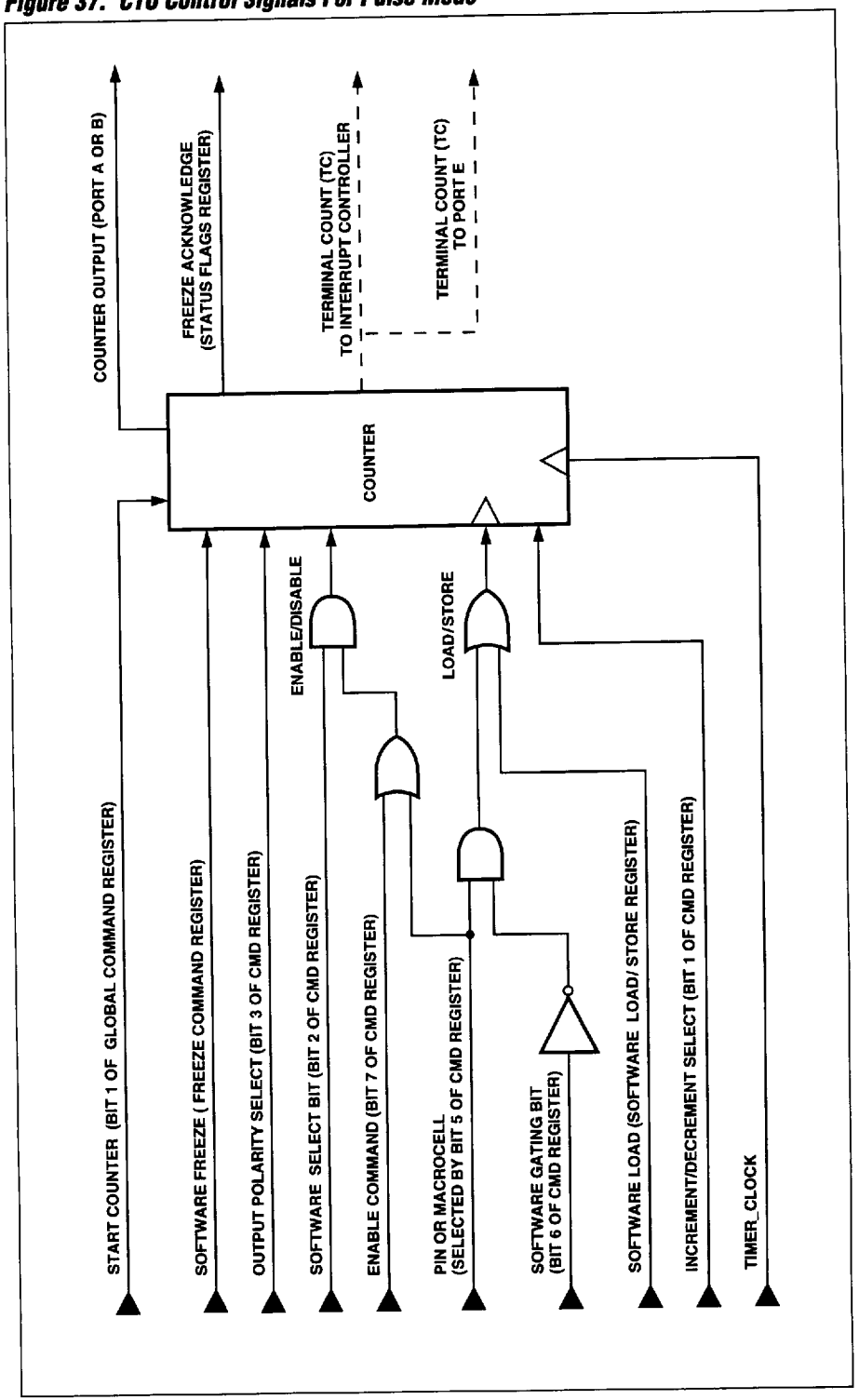
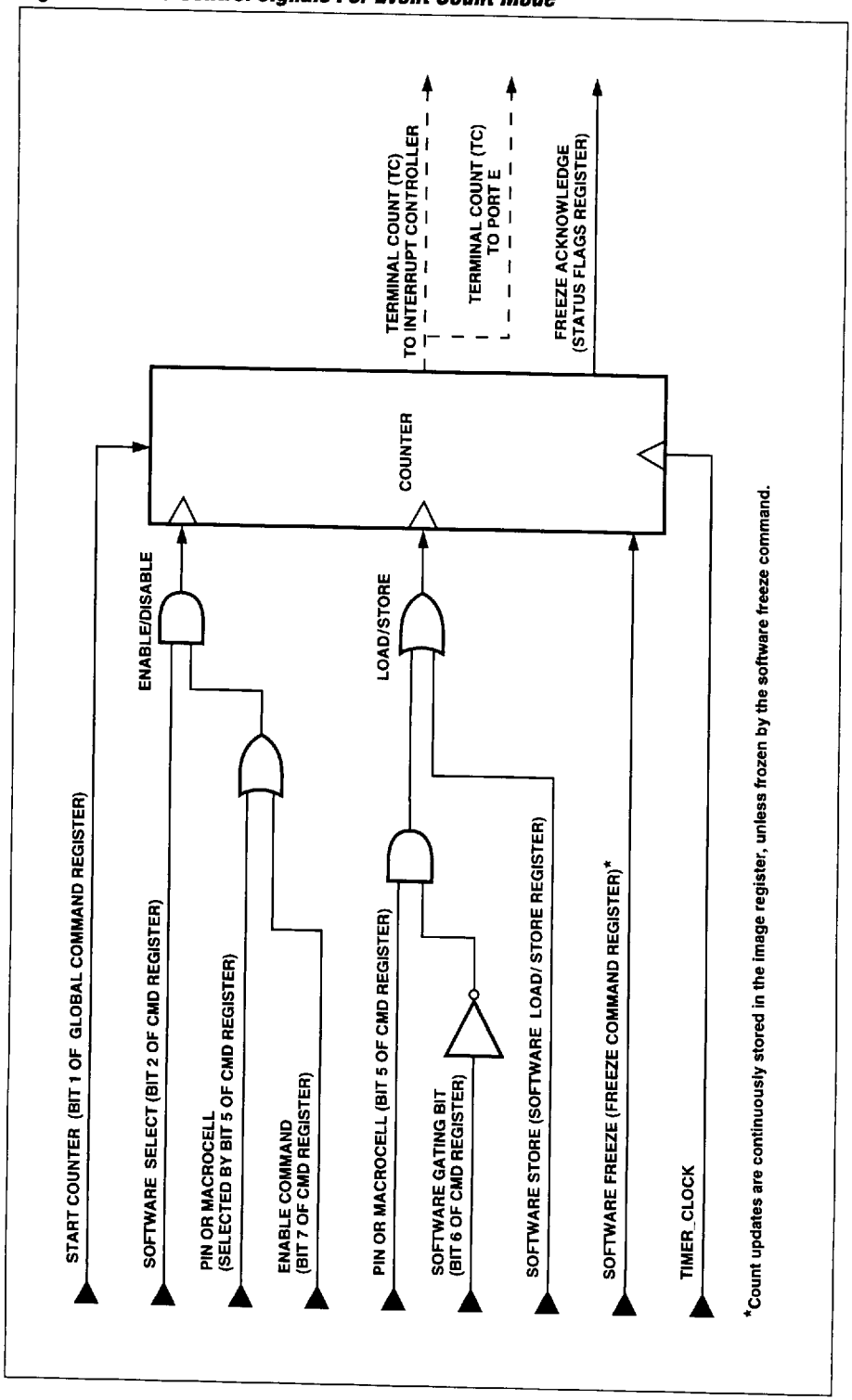
Counter/Timer (Cont.)

Figure 37. CTU Control Signals For Pulse Mode



Counter/Timer (Cont.)

Figure 38. CTU Control Signals For Event Count Mode



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Counter/Timer Operation (Cont.)

Time Capture Mode

In the time capture mode, the Counter/Timer is capable of measuring the time (by counting clock pulses) between events. Figure 39 shows the CTU configuration for time capture. All the Counter/Timer registers must be cleared during initialization of the Time Capture mode. Here the Counter is enabled to count via software only. The CTUs continuously count. A Load/Store pulse triggers the storing of the Counter's contents into the associated image register. The image register effectively contains a "snap shot" of the Counter at the time of the pulse. The CTU Store input is edge-triggered by events, the events being:

- ❑ Pin Driven.
- ❑ PPLD Macrocell Driven.
- ❑ Software Driven.

A Freeze signal is used to ensure that image data is stable during Microcontroller reads which is similar to the description of event Counter Microcontroller read accesses. Two CTUs in time capture mode can be used to capture the rising and the falling edges of a pulse, the difference of the measurements being the pulse width. The counter continues to count regardless of the Freeze Acknowledge state.

Note that the time span between two consecutive edges of Time Capture must be greater than one timer clock cycle in order to be captured.

WatchDog Counter/Timer

Counter/Timer-2 can be operated as a WatchDog Timer in both Waveform/Pulse and Event count/time capture modes. In Event count/time capture mode, Counter/Timer-2 can be configured only as WatchDog. Figure 40 shows the control signals of the CTU when in WatchDog mode. When the WatchDog mode is active, CTU2 counts down and at the terminal count of Counter-2 a WatchDog condition occurs. To avoid the WatchDog from occurring, a "Write" to the Software Load/Store Bit-2 in the "Software Load/Store Register" has to take place before the Counter-2 underflows. This action reloads the Counter-2 with the initial count value in the Image Register-2. Note that this initial count value cannot be changed after the WatchDog mode is enabled.

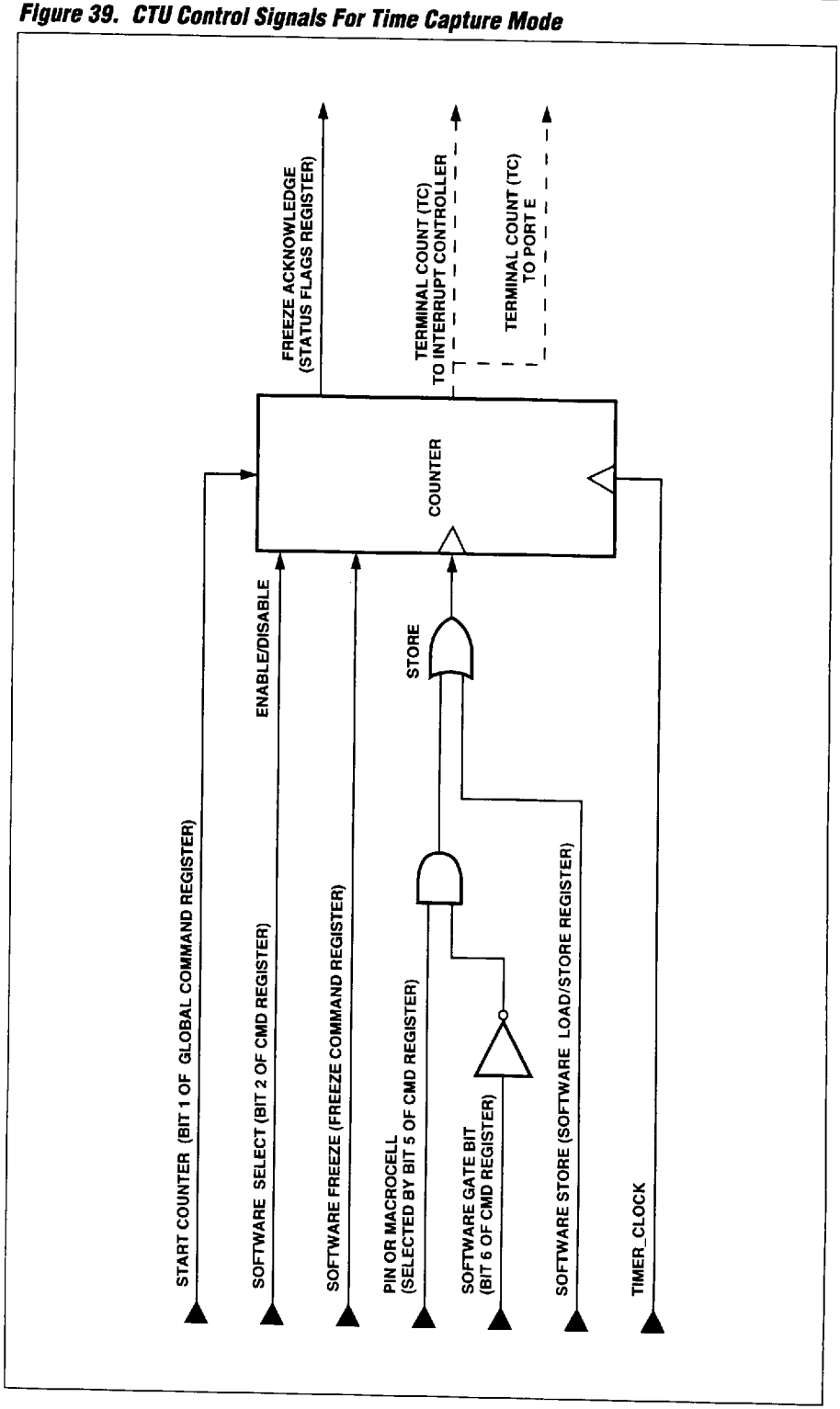
The Terminal Count signal of a WatchDog could result in a pulse width that is equal to the count value loaded into the Image Register of Counter/Timer-2. The active high WatchDog pulse from Counter 2 is routed through the PPLD, enabling the user to inverse its polarity or implement any other logic before driving the WatchDog output on a user defined I/O pin. This signal could be used to drive a RESET pin or trigger a Non-Maskable interrupt on a processor. Once Counter/Timer-2 is set to the WatchDog mode, it cannot be reconfigured by software and it can get out of the WatchDog mode only by a RESET.

When the WatchDog is enabled in Power Down and Sleep modes, it remains active regardless of the state of bit 7 (TMR CLK) in Power Management Mode Register PMMR0.

The WatchDog mode is enabled by setting the WatchDog bit in the global command register. Setting up the command register for CTU2 is not required except when CTU3 is configured in pulse mode. In this case, bit 0 of the command register for CTU2 is set to "1".

Counter/Timer Operation (Cont.)

Figure 39. CTU Control Signals For Time Capture Mode



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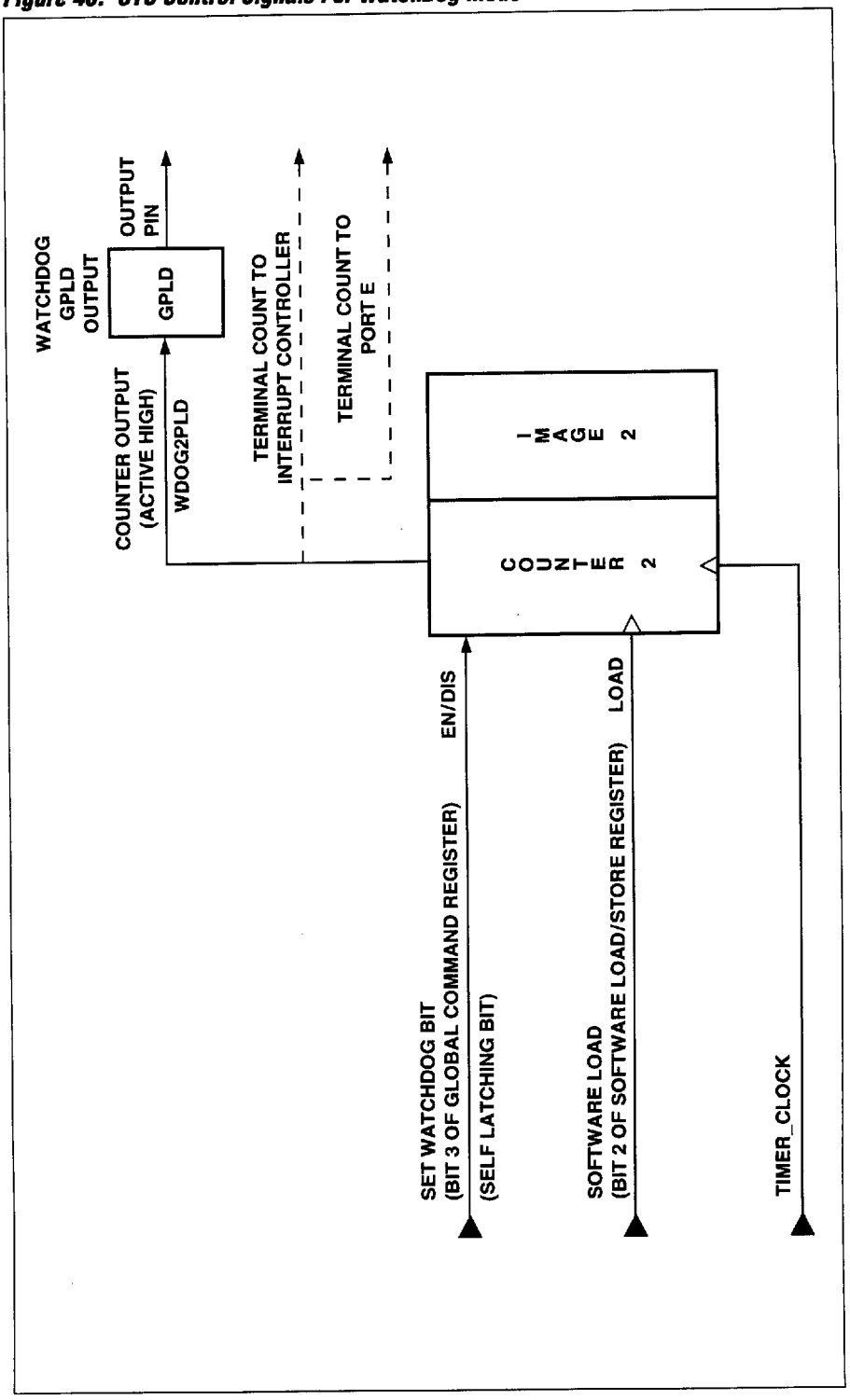
Counter/Timer Operation (Cont.)

Figure 40. CTU Control Signals For WatchDog Mode



Counter/Timer Operation (Cont.)

Terminal Counts (TCs)

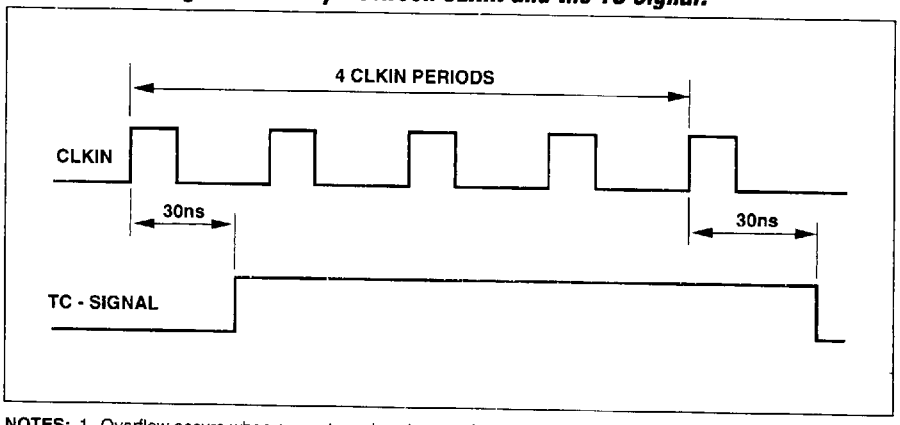
The terminal counts (TC0 – TC3) generated by the Counter/Timers are made available at Port E as outputs or as feedbacks to the ZPLD. Refer to Table 27a for pin assignments. The terminal counts can be used to concatenate the 16-bit Counter/Timers into a larger counter. Only the trailing edge of the TC signal can be used as input to another Counter/Timer. For example, concatenating CTU0 and CTU1 requires the following PPLD equation in the PSDabel file:

```
mc2tmr1 = !tc0;
```

In order for a TC signal to come out, its respective bit in the Port E Special Function Out Register must be set to 1. TC signals on Port E pins can be used as inputs to the ZPLD. A TC signal goes high for the duration of at least four CLKIN periods whenever its corresponding Timer Counting-Register overflows or underflows.

Figure 41 gives the timing relationship between CLKIN and the TC signal.

Figure 41. Timing Relationship Between CLKIN and the TC Signal.



NOTES: 1. Overflow occurs when a counter value changes from FFFFh to 0000h during incrementing.
2. Underflow occurs when a counter value changes from 0000h to FFFFh during decrementing.

Counter/Timer Clock Input

All Counter/Timers 0 through 3 have a common clock source. The Counter/Timers are clocked from the output of a highly flexible and high resolution Divisor unit. The Divisor's input is the external Clock input pin. The Divisor DIV is a number in the range of 4 <= DIV <= 280. Refer to Table 22 for exact values of DIV for different clock values. Figure 42 details the PSD5XX Counter clock generation.

The Counter/Timer CLOCK input

$$= \frac{\text{(External Clock input)}}{\text{(DIV)}}$$

where DIV = N * K and N = (4 + DLCY).

The value of K depends on the Scale-Bit (Bit 0 in the Global Command Register) in the "Global Command Register" , K = 8 when Scale-Bit is set to 1 and K = 1 when Scale-Bit is set to 0. DLCY is the number of Delay Cycles in the range of 0 <= DLCY <= 31 set up in the Delay Cycle Register. The fastest clock to service the Counter/Timer is = (Clock input / 4). The maximum External Clock input value is 28 MHz and the fastest internal count frequency is 7.0 MHz, i.e., a resolution of 143 ns. (Higher resolution can be achieved by using in conjunction with GPLD macrocells). The default value of DIV is 4 (following a reset both K and DLCY contain zeroes).

Counter/Timer Operation (Cont.)

Counter/Timer Clock Input (Cont.)

Table 22. DLCY, Scale Bit and DIV to Generate Different Clock Divisions

DLCY	Scale Bit	DIV
0	0	4
1	0	5
2	0	6
3	0	7
4	0	8
5	0	9
6	0	10
7	0	11
8	0	12
9	0	13
10	0	14
11	0	15
12	0	16
13	0	17
14	0	18
15	0	19
16	0	20
17	0	21
18	0	22
19	0	23
20	0	24
21	0	25
22	0	26
23	0	27
24	0	28
25	0	29
26	0	30
27	0	31
28	0	32
29	0	33
30	0	34
31	0	35

DLCY	Scale Bit	DIV
1	1	40
2	1	48
3	1	56
4	1	64
5	1	72
6	1	80
7	1	88
8	1	96
9	1	104
10	1	112
11	1	120
12	1	128
13	1	136
14	1	144
15	1	152
16	1	160
17	1	168
18	1	176
19	1	184
20	1	192
21	1	200
22	1	208
23	1	216
24	1	224
25	1	232
26	1	240
27	1	248
28	1	256
29	1	264
30	1	272
31	1	280

Sample Calculation of Timer Input Clock

External input clock to the PSD5XX is 8 MHz.

If required Counter/Timers 0 – 3 count frequency is 1 MHz then

The Counter/Timer CLOCK Input

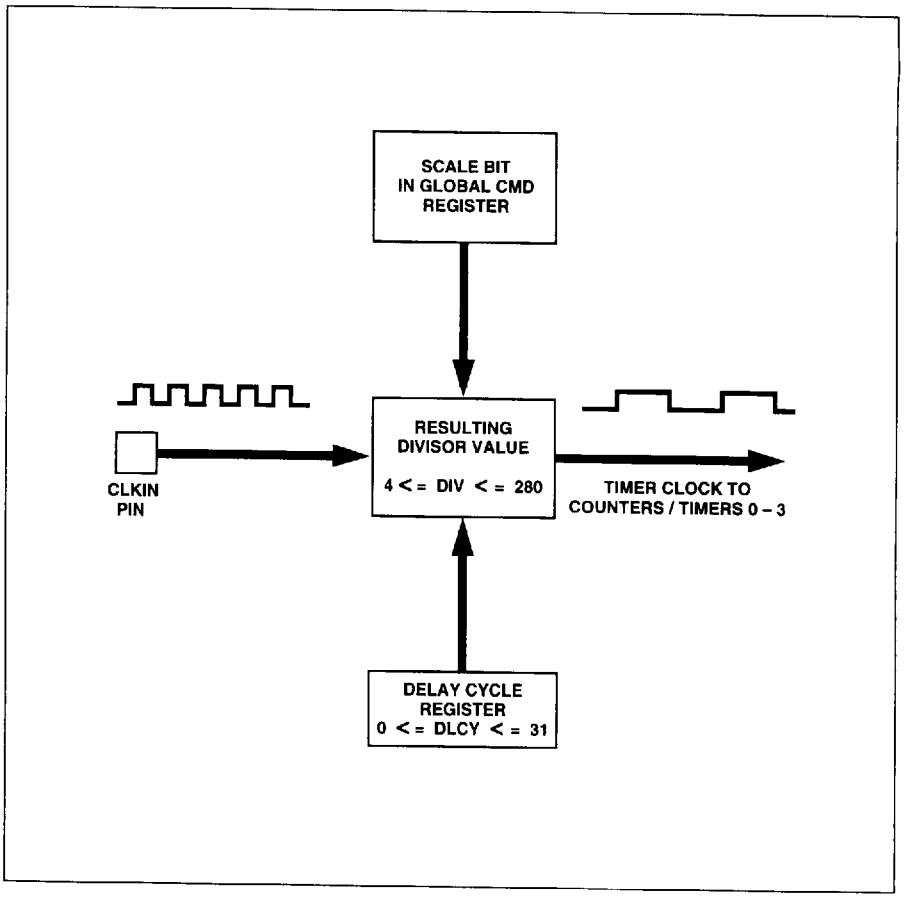
$$= \frac{\text{(External Clock input)}}{\text{(DIV)}}$$

$$1\ \text{MHz} = \frac{8\ \text{MHz}}{\text{(DIV)}} \Rightarrow \qquad \text{(DIV)} = 8$$

Therefore from Table 22 when (DIV) = 8, the Scale-Bit in the "Global Command Register" is set to a 0 and the DLCY register to a value of 4.

Counter/Timer Operation (Cont.)

Figure 42. Counter Clock Generation



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Counter/Timer Registers

Registers CNTR0,CNTR1,CNTR2 and CNTR3 serve as actual counting logic. Registers IMG0,IMG1,IMG2 and IMG3 serve as images of these Counter/Timers. Depending upon the selected mode of operation, a Counter can load a new value or transfer its content to the image register. Registers IMG0 - IMG3 and CNTR0 - CNTR3 are accessible to the Microcontroller only before setting the start bit (Bit 1 in the Global Command Register). When CNTR0-CNTR3 are active, the value in the read operation is not guaranteed to be stable and during a write operation there could be contention between the image register write and microcontroller write. Therefore the access of registers CNTR0-CNTR3 should be suspended when the Counter/Timers are active. Only IMG0, IMG1, IMG2 and IMG3 registers are accessible when the Counter/Timers are active.

Tables 23 and 23a give the address map for the various port and Counter/Timer-unit registers. This address offset map is of the host processor, relative to CSIOP (Chip Select Input Output Port) i.e. address space allocated by the host Microcontroller to access all the PSD5XX embedded peripherals.

Table 23a is for 16-bit Motorola Microcontrollers which require different address offsets.

Table 23. Offset Address Map of Counter/Timer-Unit Registers

Address Offset	Register Name	Address Offset	Register Name
+A9h	STATUS FLAGS	+A8h	GLOBAL COMMAND
		+A6h	DLCY
+A5h	SOFTWARE LOAD/STORE	+A4h	FREEZE COMMAND
+A3h	CMD3	+A2h	CMD2
+A1h	CMD1	+A0h	CMD0
+9Fh	CNTR3	+9Eh	CNTR3
+9Dh	CNTR2	+9Ch	CNTR2
+9Bh	CNTR1	+9Ah	CNTR1
+99h	CNTR0	+98h	CNTR0
+97h	IMG3	+96h	IMG3
+95h	IMG2	+94h	IMG2
+93h	IMG1	+92h	IMG1
+91h	IMG0	+90h	IMG0

Counter/Timer Registers (Cont.)

Table 23a. Offset Address Map of Counter/Timer-Unit Registers

(For 16-Bit Motorola MCUs in 16-Bit Mode. If 8-Bit Mode is selected, use Table 23.)

Address Offset	Register Name	Address Offset	Register Name
+A8h	STATUS FLAGS	+A9h	GLOBAL COMMAND
		+A7h	DLCY
+A4h	SOFTWARE LOAD/STORE	+A5h	FREEZE COMMAND
+A2h	CMD3	+A3h	CMD2
+A0h	CMD1	+A1h	CMD0
+9Eh	CNTR3	+9Fh	CNTR3
+9Ch	CNTR2	+9Dh	CNTR2
+9Ah	CNTR1	+9Bh	CNTR1
+98h	CNTR0	+99h	CNTR0
+96h	IMG3	+97h	IMG3
+94h	IMG2	+95h	IMG2
+92h	IMG1	+93h	IMG1
+90h	IMG0	+91h	IMG0

Registers IMG0 through IMG3 are written to by the microcontroller to load the Counter/Timers with required values in Waveform, Pulse and WatchDog mode only. To retrieve the count or time in Event count or Time capture modes, Counter/Timers store their values into IMG0 through IMG3.

Any access to the Image Registers must conform to the Freeze/Freeze Acknowledge protocol, described later in the Freeze Command paragraph.

6

Counter/Timer Registers (Cont.)

Global Command Register

This is used to specify the operation mode of the Counter/Timer and to start or stop the Counter/Timer. Therefore during the initialization of the Counter/Timer registers, the Global Command Register should always be configured last.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
*	*	*	*	Watch Dog	Global Mode	Counter Start	Scale

NOTE: * = Not used.

At RESET all bits come up as 0's.

Watch Dog Bit: When this bit is
0: Watch Dog mode is NOT selected.
1: Watch Dog Counter/Timer (Counter 2) is active. This bit can be turned off by RESET only.

NOTE: Whenever this bit is set to 1, the COUNTER START bit should also be set to 1. Otherwise the Counter/Timer will always be off, i.e., once this bit is set, access to Counter 2 Registers and the Global Command Registers are blocked.

Global Mode Bit: When this bit is set to a
0: All Timers/Counters are set to Waveform or Pulse Mode.
1: All Timers/Counters are set to operate in Event Counter or Time Capture Mode.

NOTE: Further selection of modes is done in individual CMD registers.

Counter Start Bit: When this bit is set to
0: ALL CTUs are disabled and can be re-initialized.
1: ALL CTUs are enabled.

Scale Bit: When this bit is set to
0: The clock to all Counter/Timers is divided by 1.
1: The clock to all Counter/Timers is divided by 8.

Counter/Timer Registers (Cont.)

Command Registers for Counter/Timers CMD0, CMD1, CMD2, CMD3:

Each of the Counter/Timer units (CTU) has one Command Register associated with it. A description of these various CTU command bits is provided below. Refer to CSIOP Tables 23 and 24 for their addresses and selection details. Figure 43 describes the Command Register bits.

The following is the description of Counter/Timer0 CMD0 register bits. Bits in CMD1, CMD2 and CMD3 have similar descriptions. Refer to Figure 43 also.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Enable/ Disable Using Pin, PPLD Macrocell or Software	Software Gating Bit for Load/ Store cmd Using Pin or PPLD Macrocell	Pin/ PPLD Macrocell	Input Polarity	Output Polarity	Select Counter	Increment/ Decrement	Mode Select

NOTES: 1. At RESET these bits come up as 0s.
2. In WatchDog Mode, CMD2 register bits are Don't Cares.

Mode Select Bit (0): This bit selects the Counter/Timer0 operation mode. After RESET Counter/Timer0 initializes in waveform/event count mode. When this bit is set to
1: The Counter/Timer0 operates in Pulse/Time capture modes.
0: The Counter/Timer0 operates in Waveform/Event count modes.

NOTE: See Table 24 for details of Timer mode set up.

Increment/Decrement Bit (1): This bit is used to set the Counter/Timer in increment or decrement mode. The RESET state is Decrement mode. When this bit is set to
1: The Counter/Timer0 is in increment mode.
0: The Counter/Timer0 is in decrement mode.

NOTE: In WatchDog mode Counter #2 is in decrement mode only.

Select Counter Bit (2): This bit is used to select or deselect Counter/Timer0. At RESET this bit initializes as 0 which means Counter/Timer0 is deselected. When this bit is set to
1: Counter/Timer0 is selected (counting enabled).
0: Counter/Timer0 is deselected (counting disabled).

After a Counter/Timer is started by the Global Command Register, it can be re-configured by changing the individual Command Register. The steps to re-configure a Counter/Timer are:

1. Disable the Counter/Timer by writing a "0" to the Select Counter Bit (bit 2) of the Command Register.
2. Change the Counter/Timer configuration by writing the new value (bit 2 remains at "0") to the Command Register.
3. Enable the Counter/Timer again by writing the new value with bit 2 set to "1" to the Command Register.

Counter/Timer Registers (Cont.)

Command Registers for Counter/Timers CMD0, CMD1, CMD2, CMD3 (Cont.)

Output Polarity Bit (3):

This bit is valid only in Waveform or Pulse mode and is used to select the polarity of the Active output signal of the Counter/Timer0. At RESET this bit initializes as 0 which means the Active output state is LOW. When this bit is set to a

1: The Active output state is HIGH.
0: The Active output state is LOW.

Input Polarity Bit (4):

The state of this bit determines the polarity of the Active input control signal to the Counter/Timer0 and is valid only for input pin. At RESET this bit initializes as 0 which means that the input Active is HIGH. When this bit is set to a

1: The input Active is LOW.

0: The input Active is HIGH.

Pin / PPLD Macrocell Bit (5):

This bit determines whether the Counter/Timer0 gets its input command for Load/Store and Enable/Disable from the PSD5XX PIN or from the PPLD macrocell output. At RESET this bit initializes as 0 which means that the input command is coming from the PSD5XX PPLD macrocell. When this bit is set to a

1: The Counter/Timer0 input command is coming from the PIN.

0: The Counter/Timer0 input command is coming from the PPLD macrocell output.

Software Gating Bit for Load/Store Commands (6):

This bit gates the Load/Store command activated by the PSD5XX PIN or PPLD macrocell. At RESET this bit initializes as 0 which means that the Load/Store command activated by the PIN or macrocell is permitted through. When this bit is set to

1: Load/Store operation activated by PIN or Macrocell is NOT permitted through.

0: Load/Store operation activated by PIN or macrocell is permitted through. To further decide between the PIN and PPLD macrocell, use bit 5 (PIN/PPLD macrocell).

Enable/Disable Using PIN, PPLD Macrocell or Software Bit (7):

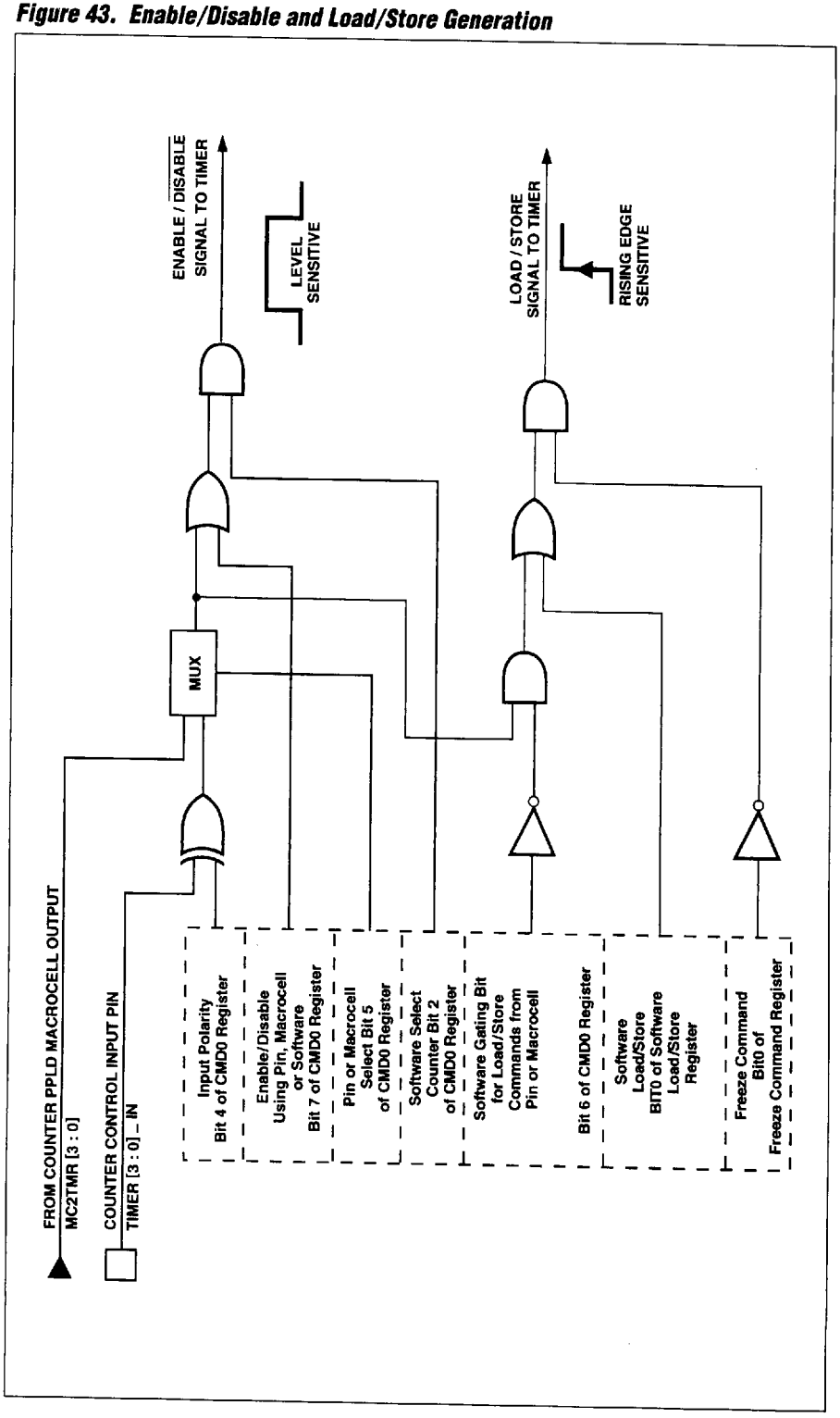
This bit determines whether the Enable/Disable command is activated by the PSD5XX Pin, PPLD macrocell or by Software. At RESET this bit initializes as 0, which means that the Enable/Disable command is activated by the PIN or PPLD macrocell. When this bit is set to

1: Enable/Disable command by PIN or macrocell is overridden by Software (only Bit 2 of this register will enable or disable the counter).

0: Enable/Disable command is activated by PIN or Macrocell output. To further decide between the PIN and PPLD macrocell use bit 5 (PIN / PPLD macrocell bit).

Counter/Timer Registers (Cont.)

Figure 43. Enable/Disable and Load/Store Generation



Counter/Timer Registers (Cont.)

Configuring the Mode of Operation of the Counter/Timers:

Using the GLOBAL MODE bit of the Global Command register and MODE SELECT bit of the Command register of Counter/Timers 0–3, individual Counter/Timer modes of operation can be set up. Refer to Table 24. Notice that all the Counter/Timers can either operate in Waveform/Pulse or Event Count/Time Capture modes, but not in all four modes at the same time.

Table 24. Counter/Timer Modes

Global Mode Bit (Global Command Register)	Mode Select Bit (Command Registers of Counter/Timers 0 – 3 CMD0, CMD1, CMD2 and CMD3)	Modes of Counter/Timers 0, 1 and 3	Modes of Counter/Timer2
0	0	Waveform	Waveform or WatchDog
0	1	Pulse	Pulse or WatchDog
1	0	Event Counter	WatchDog Only
1	1	Time Capture	WatchDog Only

Freeze Command Register

When a Microcontroller needs to access the contents of the Image Registers (IMG0-IMG3) it does so by first setting the Command Register Freeze bit in order to disable the timer state-machine accesses of the Image Register. The Microcontroller waits for the Freeze Acknowledge bit in the Counter/Timer Status Register to be set to 1 and then it accesses the Image Register as an address location. The freeze acknowledge signal effectively guarantees stable Image Register data during Microcontroller read/write cycles even though the Counter/Timer continues to count. The Freeze Acknowledge bit gets cleared after the negation of Freeze. The Freeze Command bits are set and cleared by the microcontroller software.

The Freeze Command Register and the software Load/Store Register should not be set at the same time. It is recommended that the registers be accessed individually.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
*	*	*	*	Freeze CTU3	Freeze CTU2	Freeze CTU1	Freeze CTU0

NOTE: * = Not used.

Counter/Timer Registers (Cont.)

Software Load/Store Register:

Each bit in this register enables a load to the corresponding Counter/Timer from its associated Image Register in Waveform, Pulse or WatchDog modes. The actual counts are stored in their corresponding Image Register in event Counter or time capture modes. Bit 6 of the Command Register must be set to "1" before writing to the software load/store register.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
*	*	*	*	Software Load/Store 3	Software Load/Store 2	Software Load/Store 1	Software Load/Store 0

NOTE: * = Not used.

Software Load/Store 0 Bit: If this bit is set to
1: Counter/Timer0 CNTR0 gets loaded from the Image Register IMG0 or CNTR0 stores into IMG0 based on the mode of operation**.

Software Load/Store 1 Bit: If this bit is set to
1: Counter/Timer1 CNTR1 gets loaded from the Image Register IMG1 or CNTR1 stores into IMG1 based on the mode of operation**.

Software Load/Store 2 Bit: If this bit is set to
1: Counter/Timer2 CNTR2 gets loaded from the Image Register IMG2.

Software Load/Store 3 Bit: If this bit is set to
1: Counter/Timer3 CNTR3 gets loaded from the Image Register IMG3 or CNTR3 stores into IMG3 based on the mode of operation**.

**Load operation takes place in Waveform, Pulse and WatchDog mode.
Store operation takes place in Event Count and Time Capture mode.

The Software load/store bits are automatically cleared by the served Counter.

In addition to four CTU registers, there are delay cycle and Counter/Timer status registers. These are summarized on the following pages.

Counter/Timer Registers (Cont.)

Status Flags Register

There are eight READ-ONLY status flags. The lower four bits represent Freeze Acknowledge bits.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
*	*	*	*	FrezAck3	FrezAck2	FrezAck1	FrezAck0

NOTES: At RESET all these bits intialize as 0's.
* = Not used.

FrezAck Bits

These Freeze Acknowledge bits are useful in the Freeze/Freeze Acknowledge protocol. After the Microcontroller senses that the FrezAck bit is being set it proceeds to access the Image Register for a read or write operation.

FrezAck0 Bit: When this bit is
1: Image Register Access is granted.
0: Image Register Access is not granted.

FrezAck1 Bit: When this bit is
1: Image Register Access is granted.
0: Image Register Access is not granted.

FrezAck2 Bit: When this bit is
1: Image Register Access is granted.
0: Image Register Access is not granted.

FrezAck3 Bit: When this bit is
1: Image Register Access is granted.
0: Image Register Access is not granted.

DLCY Register:

Bits <4:0> of the DLCY register are used to assign Delay Cycles to the Counter/Timer. Various Clock Scaling values possible are 0 through 31 (decimal).

At RESET these bits initialize as 0. If necessary, the user has the option to set these bits up to generate Delay Cycles (DLCY) to scale down the Counter/Timer clock (see Table 24).

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
*	*	*	DLCY4	DLCY3	DLCY2	DLCY1	DLCY0

NOTE: * = Not used.

Counter/Timer (Cont.)

Load/Store

The Load operation transacts an Image Register (e.g. IMG0) write into its Counter/Timer Register (e.g. CNTR0), whereas in the Store operation the Counter/Timer Register (e.g. CNTR0) writes back into the Image Register (e.g. IMG0).

These signals are valid only when a Counter/timer is active. They are rising edge sensitive and are used to Load a Counter with a required value or to Store the Counter value in the associated Image Register.

In Waveform, Pulse and WatchDog modes the microcontroller writes into an Image Register. The respective Counter/Timer uses that value as its initial counting value. The data transfer operation from an Image Register into its corresponding counter is called LOAD. In Event Counting and Time Capture modes the Counter/Timer counts event pulses or timer clock cycles, respectively. An external event or a software command can cause a data transfer from the counting element into its Image Register. This operation is defined as STORE.

These operations are triggered by:

- ❑ Software command
- ❑ Terminal count (in Waveform mode only)
- ❑ PPLD macrocell output
- ❑ Input Pin

Refer to Counter/Timer Command Register and Figure 43 for specific details.

Enable/Disable

These signals are used to enable or disable the counting of the Counter/Timers. These signals are controlled by:

- ❑ Software command (Bits 2 and 7 of the Command Registers).
- ❑ PPLD macrocell output
- ❑ Input Pin

Event Count Mode:

In Event Count mode the Enable/Disable signal is edge sensitive and is connected to the event input signal through the PPLD or pin. In Time Capture mode the Enable/Disable signal can be set by a software command only.

Refer to Counter/Timer Command Register and Figure 43 for specific details.

Counter/Timer Input/Output

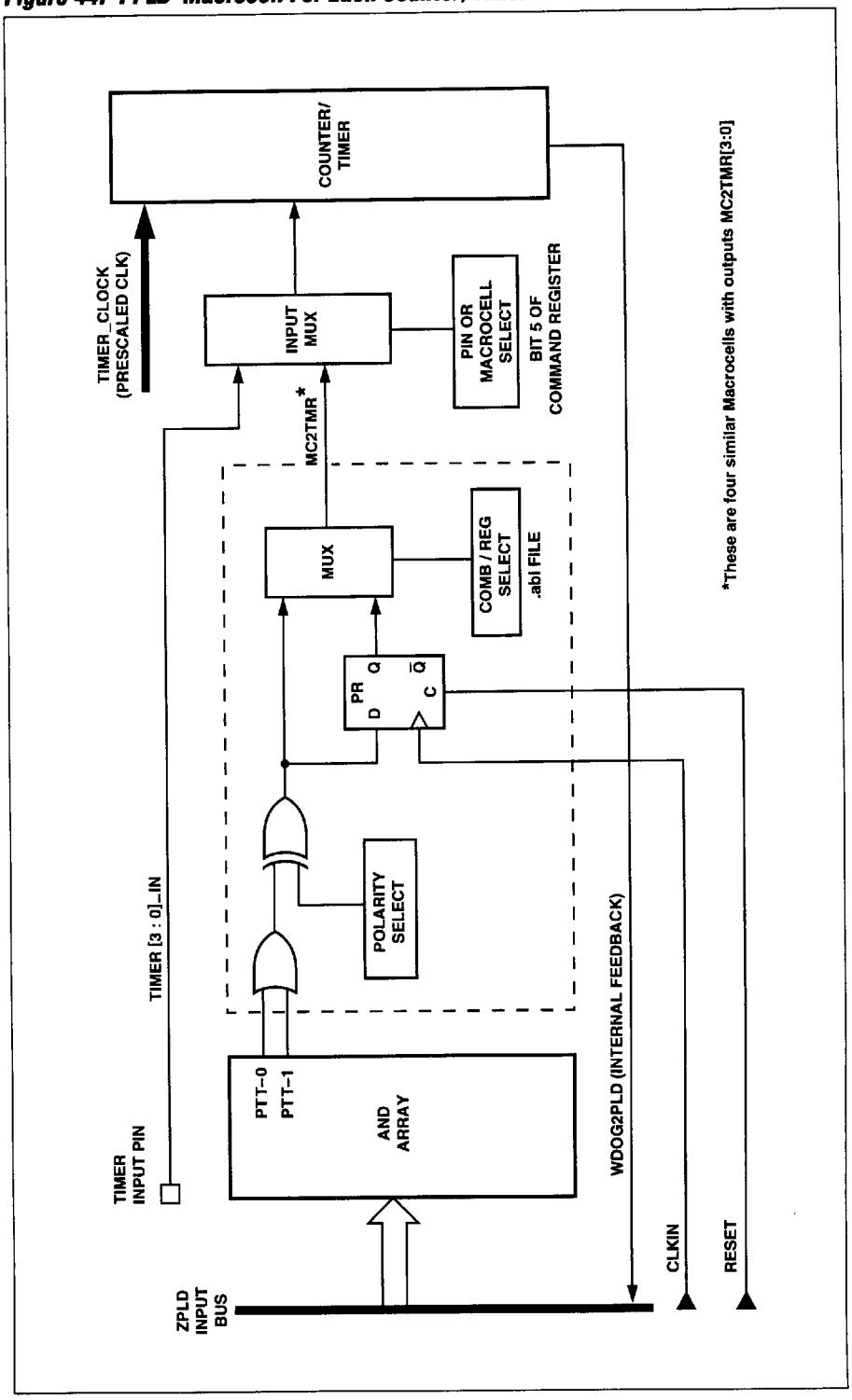
Each Counter can use individual control inputs in port E as input Load/Store or Enable/Disable signals, and Counter/Timer outputs in port A or port B by selecting alternate and special functions on the pins assigned to them. The outputs are used in waveform and pulse modes in which the Counters generate output waveforms or pulses. The inputs can be used in all modes of operation except WatchDog to create the LOAD/STORE and/or ENABLE/DISABLE control signals. Port E can be configured as outputs for Terminal Count. Terminal Count is also available as ZPLD inputs (via pin feedback). Refer to Tables 25, 26 and 27 for further details and configuration of these ports.

PPLD Macrocell

The enable/disable or load/store inputs of each Counter/Timer can be selected through a PPLD macrocell, whose inputs are two product terms PTT0 and PTT1 from the PPLD's AND-array. The polarity of the PPLD macrocell output is programmable. The output of the PPLD macrocell which is the enable/disable and/or Load/Store input to the Counter/Timer can be in a Combinatorial mode or Register mode. Figure 44 shows the details of the PPLD macrocell. Refer to the "ZPLD" section for further information on the PPLD.

Counter/Timer (Cont.)

Figure 44. PPLD Macrocell For Each Counter/Timer



Counter/Timer (Cont.)

I/O – Port A, B, E

Ports A, B and E have the capabilities for counter/timer alternate and special functions, e.g. Counter/Timer out, load/store, enable/disable, etc. Refer also to the chapter on I/O ports for further details.

Special Function Assignment

Port A:

Timer outputs in Pulse or Waveform modes can be tapped out of these pins: PA0 – PA3. In order for the following timer outputs to drive their corresponding port pins, set the respective bits in the Special Function Register of Port A to ones.

Table 25.

Port Pin	Special Function Out
PA0	Timer0_out
PA1	Timer1_out
PA2	Timer2_out
PA3	Timer3_out

Port B:

Timer outputs in Pulse or Waveform modes can be tapped out of these pins: PB0 – PB3. In order for the following timer outputs to drive their corresponding port pins, set the respective bits in the Special Function Register of Port B to ones.

Table 26.

Port Pin	Special Function Out
PB0	Timer0_out
PB1	Timer1_out (in Pulse Mode Only)
PB2	Timer2_out
PB3	Timer3_out (in Pulse Mode Only)

The decision which of Port A or B pins are used as timer outputs is done by the PSDsoft fitter.

Counter/Timer (Cont.)

I/O – Port A, B, E (Cont.)

Port E:

Timer[3:0]_inputs can have different control functions such as timer LOAD/STORE and/or ENABLE/DISABLE, based on how these pins are configured in the Timer Command Registers.

Table 27.

Port Pin	Alternate Function In
PE3	Timer0_in
PE4	Timer1_in
PE5	Timer2_in
PE6	Timer3_in

The Terminal Counts (TC0 – TC3) generated by each Counter/Timer are available at Port E (pins PE4 – PE7) as shown in Table 27a.

Table 27a.

Port Pin	Special Function Out
PE4	TC0
PE5	TC1
PE6	TC2
PE7	TC3

To Connect TC0 – TC3 to Port E pins, set the corresponding bits in the Special Function Register to "1".

Counter/Timer (Cont.)

Sample Counter/Timer0 Initialization In PULSE Mode

Following is a sample initialization routine for Counter/Timer0 to operate in PULSE mode. The assembly language commands do not correspond to any particular microcontroller. Configure CSIOP for Microcontroller access to Counter/Timer registers and I/O ports for initialization of Counter/Timers. For the values of each register, refer to Tables 30 and 31.

Use PSDsoft supplied by WSI to configure the portion related to Counter/Timers. Also refer to the Section on the PSD5XX I/O Ports.

Clear All Counter/Timers

```
LOAD CNTR0, 0000h    ; Clear Counter/Timer 0
LOAD CNTR1, 0000h    ; Clear Counter/Timer 1
LOAD CNTR2, 0000h    ; Clear Counter/Timer 2
LOAD CNTR3, 0000h    ; Clear Counter/Timer 3
```

Scaling of Clock (common to all Counter/Timers)

```
LOAD DLCY, 02h       ;Delay Cycles(DLCY) = 2, k value is selected in
                     ;Global Register by setting Scale-Bit
```

Counter/Timer 0 Initialization (Command Register0 CMD0)

```
LOAD CMD0, 6Fh       ;Pulse mode (D0 = 1)
                     ;Increment (D1 = 1)
                     ;Select Counter/Timer (D2 = 1)
                     ;Output Pulse Active High (D3 = 1)
                     ;Load Signal on Input pin High going transition (D4 = 0)
                     ;Input control from PIN (not PPLD macrocell) (D5 = 1)
                     ;Load&Store control activated by Pin (D6 = 0)
                     ;Enable count (D7 = 1)

LOAD IMG0,FFF7h      ;Load Counter/Timer0 Image Register with count (pulse width)
                     ;needed (pulse duration of 8 timer clock cycles)

LOAD Special Reg A,1 ;Configure PA0 as A timer = 0 output by writing a "1" to Port A
                     ;Special Function Register
```

Global Register Configuration

```
LOAD Global, 03h     ;Non WatchDog mode
                     ;Pulse mode
                     ;All CTUs enabled
                     ;Scale-Bit = 1
                     ;Input clock is divided by 6
```

Now if Pin PE3 on port E is input with a high going signal:

- This signal causes Counter/Timer0 to get a value (FFF7h) loaded from its associated image register (IMG0) and causes the Counter/Timer0 to start counting from FFF7h (increment) until it overflows and issues a Terminal Count0 (TC0).
- During counting Port A pin (PA0) outputs a high going one-shot pulse with a width equal to (Max count possible – initial count value loaded, i.e. 8 timer clock cycles in this example).
- If the interrupt controller is configured to receive TC0, it will cause the interrupt INT0 to occur.

Interrupt Controller

General Description

The PSD5XX includes logic for sensing, masking, priority decoding and identifying up to eight internal interrupts. The PSD5XX interrupt controller can generate interrupts from two dedicated PPLD product terms, two PPLD Macrocell outputs and four terminal-count outputs of the Counter/Timer unit.

The four interrupts generated by the PPLD can be user defined using the WSI PSDsoft Windows compatible PC based software. Figure 45 details the basic building blocks of the PSD5XX Interrupt Controller and Figure 46 shows its interface with other sections of the PSD5XX.

Features

The PSD5XX interrupt controller has the following features:

- ❑ Can accept eight interrupt inputs
- ❑ PPLD product terms, PPLD Macrocell outputs and Terminal Counts (TCs) of Counter/Timers can cause interrupts.
- ❑ Interrupts generated from the PPLD canbe user defined.
- ❑ All interrupt inputs are priority decoded, IR7 has highest priority and IR0 the lowest priority.
- ❑ Each interrupt can be configured as either EDGE or LEVEL sensitive using the EDGE/LEVEL register.
- ❑ Each interrupt can be individually masked using a mask register.
- ❑ At RESET all interrupts are MASKED.
- ❑ Interrupt Request Latch provides the status of all interrupts.
- ❑ Reading an Interrupt vector location clears the corresponding pending interrupt.
- ❑ Any of these interrupts trigger a GLOBAL interrupt output available as an output at port E (PE2) and/or as an input to the PPLD.

Interrupt Operation

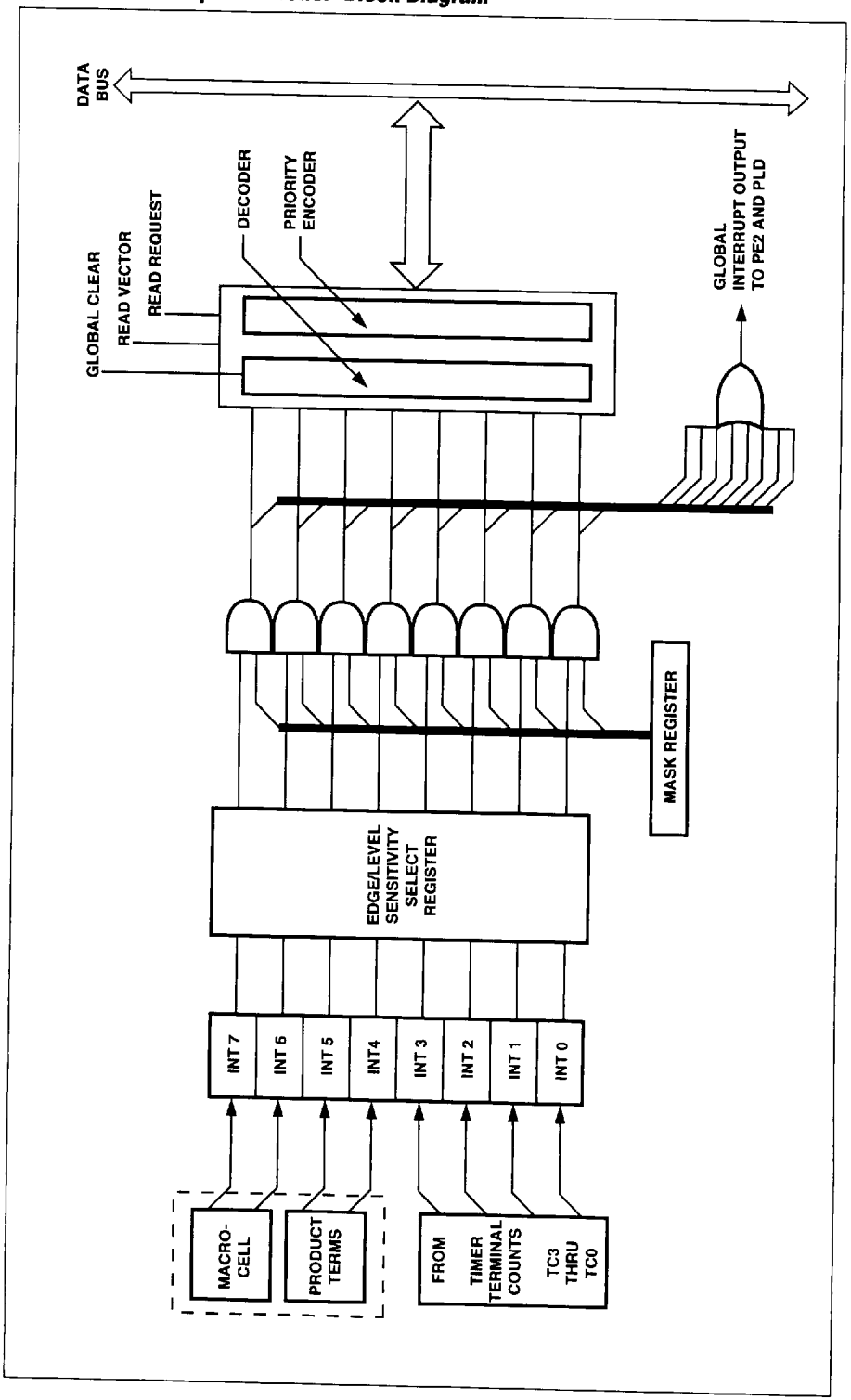
On RESET all Registers and Latches are cleared and all interrupts are masked. During initialization of the interrupt controller, relevant interrupts are un-masked and defined whether EDGE or LEVEL sensitive. When one or more interrupts are raised high, the "interrupt request latch" latches in all the non-masked interrupts. A 3-bit priority encoder assigns the priority to the non-masked pending interrupts. The MCU (microcontroller) can clear the Edge-sensitive pending interrupts by reading the "Interrupt Read Clear Register". Level-sensitive interrupts continue to be pending even after the MCU reads the "Interrupt Read Clear Register". The MCU would typically service each interrupt in sequence according to priority. Refer to Table 28 regarding priorities of various interrupts. Any of these interrupts trigger a GLOBAL interrupt output available as an input to the PPLD (INTR2PLD) and as output at port E (PE2). Refer to Figures 45 and 46 for details of the interrupt architecture.

Table 28. Interrupt Priority Table

Interrupt	Priority
IR 7	HIGHEST
IR 6	^
IR 5	^
IR 4	^
IR 3	^
IR 2	^
IR 1	^
IR 0	LOWEST

Interrupt Controller (Cont.)

Figure 45. Interrupt Controller Block Diagram



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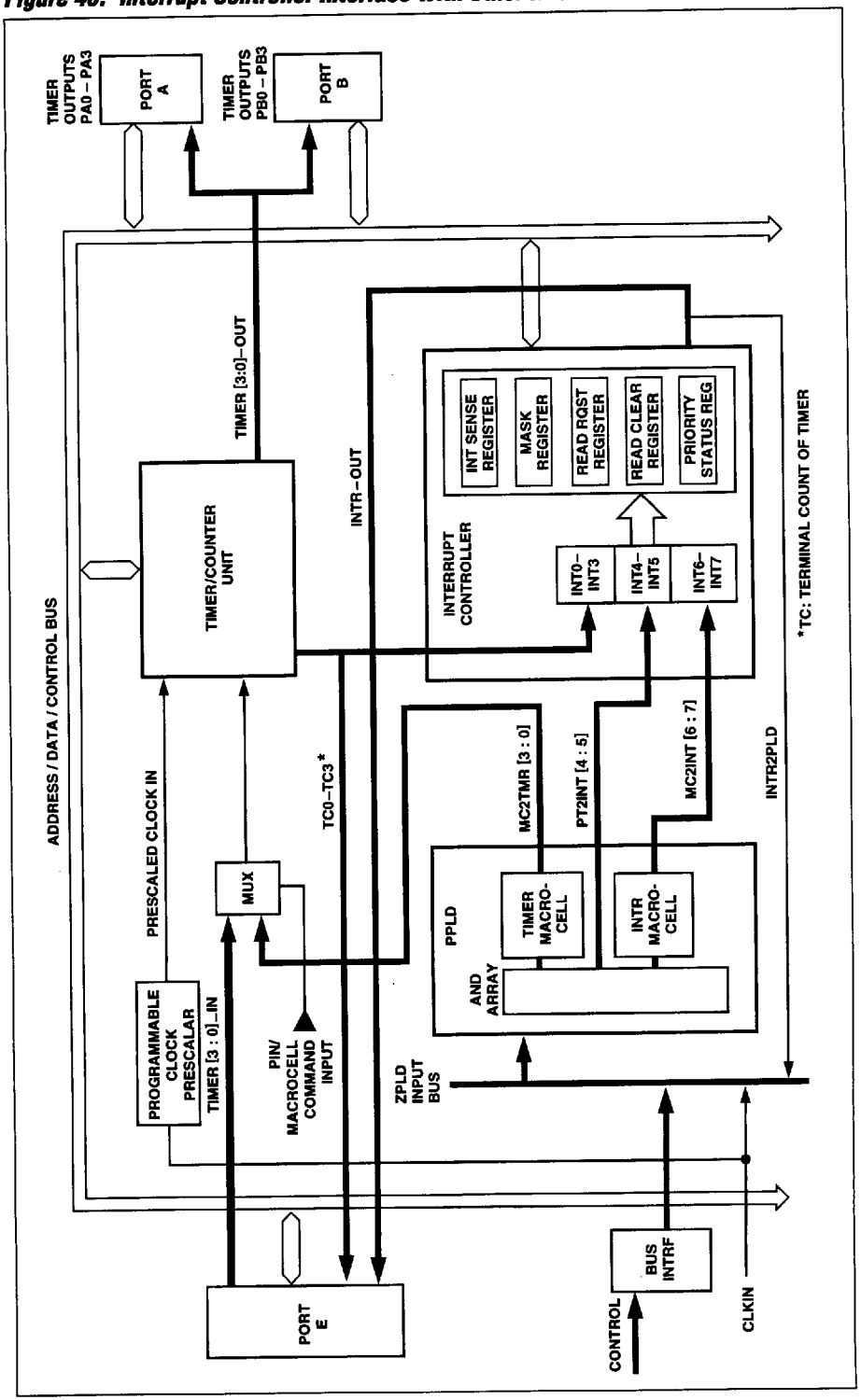
Interrupt Controller (Cont.)

Figure 46. Interrupt Controller Interface With Other Internal Blocks



Interrupt Controller (Cont.)

Interrupt Operation (Cont.)

Command Registers

All the eight interrupts can be individually masked using a mask register. Writing "ones" into these mask bits enables the associated interrupts. RESET masks all interrupts. Interrupts can also be defined as either LEVEL sensitive or EDGE sensitive using a sensitivity bit in the interrupt edge/level sensitivity select register.

Tables 29 and 29a give the address map for various port and interrupt Command/Status Registers. This address offset map is of the host processor, relative to the CSIOP (Chip Select Input Output Port) i.e., address space allocated by the host Microcontroller to access all the PSD embedded peripherals.

Table 29. Offset Address Map of Interrupt Registers

Address Offset	Register Name	Address Offset	Register Name
		+D4h	Interrupt Read Clear
+D3h	Interrupt Mask	+D2h	Interrupt Edge/Level Select
+D1h	Interrupt Request Latch	+D0h	Interrupt Priority Status

Table 29a. Offset Address Map of Interrupt Registers

(For 16-Bit Motorola MCUs in 16-Bit Mode. If 8-Bit Mode is selected, use Table 29.)

Address Offset	Register Name	Address Offset	Register Name
		+D5h	Interrupt Read Clear
+D2h	Interrupt Mask	+D3h	Interrupt Edge/Level Select
+D0h	Interrupt Request Latch	+D1h	Interrupt Priority Status

The Interrupt Registers listed in Tables 29 and 29a are described below.

Interrupt Mask Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mask7	Mask6	Mask5	Mask4	Mask3	Mask2	Mask1	Mask0

Bits mask 0 ... mask 7 correspond to interrupt 0 ... interrupt 7.
When these bits are set to

1 = Unmasked
0 = Masked

At RESET these bits initialize as 0 and all interrupts are masked.

Interrupt Controller (Cont.)

Interrupt Operation (Cont.)

Interrupt Edge/Level Select Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Sense7	Sense6	Sense5	Sense4	Sense3	Sense2	Sense1	Sense0

Bits sense 0 ... sense 7 correspond to interrupt 0 ... interrupt 7.
When these bits are set to

1 = LEVEL sensitive
0 = EDGE sensitive (positive edge)

At RESET these bits initialize as 0 i.e., all interrupts come up as Edge sensitive.

Interrupt Read Clear Register

This is a read only register. Reading this register during initialization clears all the pending edge sensitive interrupts.

Interrupt Request Latch Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ir 7	ir 6	ir 5	ir 4	ir 3	ir 2	ir 1	ir 0

Bits ir 0...ir 7 correspond to interrupt 0 ... interrupt 7.
When any of these bits are set by the interrupt controller to a "1", the corresponding Interrupt is pending service.

The MCU can read the interrupt request latch which shows the status of all interrupts. The entire interrupt request latch can be cleared by reading the Interrupt Read Clear Register, but Level sensitive interrupts cannot be cleared.

Interrupt Priority Status Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
*	*	*	*	*	vect 2	vect 1	vect 0

NOTE: * = Reserved for future use, bits set to zero.

The value of these 3 bits (vect2, vect1 and vect0) indicates the highest priority of the interrupt to be serviced among multiple interrupts pending. Refer to the table above for priorities of various interrupts. Reading this register clears the highest pending interrupt.

Interrupt Controller (Cont.)

Interrupt Operation (Cont.)

Input/Output

Interrupt inputs INT4 and INT5 originate from two dedicated PPLD product terms PT2INT4 and PT2INT5. Interrupt inputs INT6 and INT7 originate from the outputs of the PPLD Macrocells MC2INT6 and MC2INT7 as described in the next section and the remaining interrupt inputs INT0 through INT3 originate from four Terminal-Count (TC) outputs of the Counter/Timers. If an External event has to cause an interrupt in the PSD5XX, it has to be routed through the PPLD.

Regarding output from the Interrupt Controller, whenever an unmasked interrupt occurs, a Global Interrupt signal is generated. The Global Interrupt signal can be used as a ZPLD input (INTR2PLD). Refer to Figure 45 for details. It can also be driven off the chip by using the special-function out capability of Port E (PE2) as INTR_OUT. In either case, the Global Interrupt indicates to the MCU that an internal PSD5XX interrupt has occurred. Refer to the section on I/O ports for specific details of setting up the port functions.

PPLD Macrocell

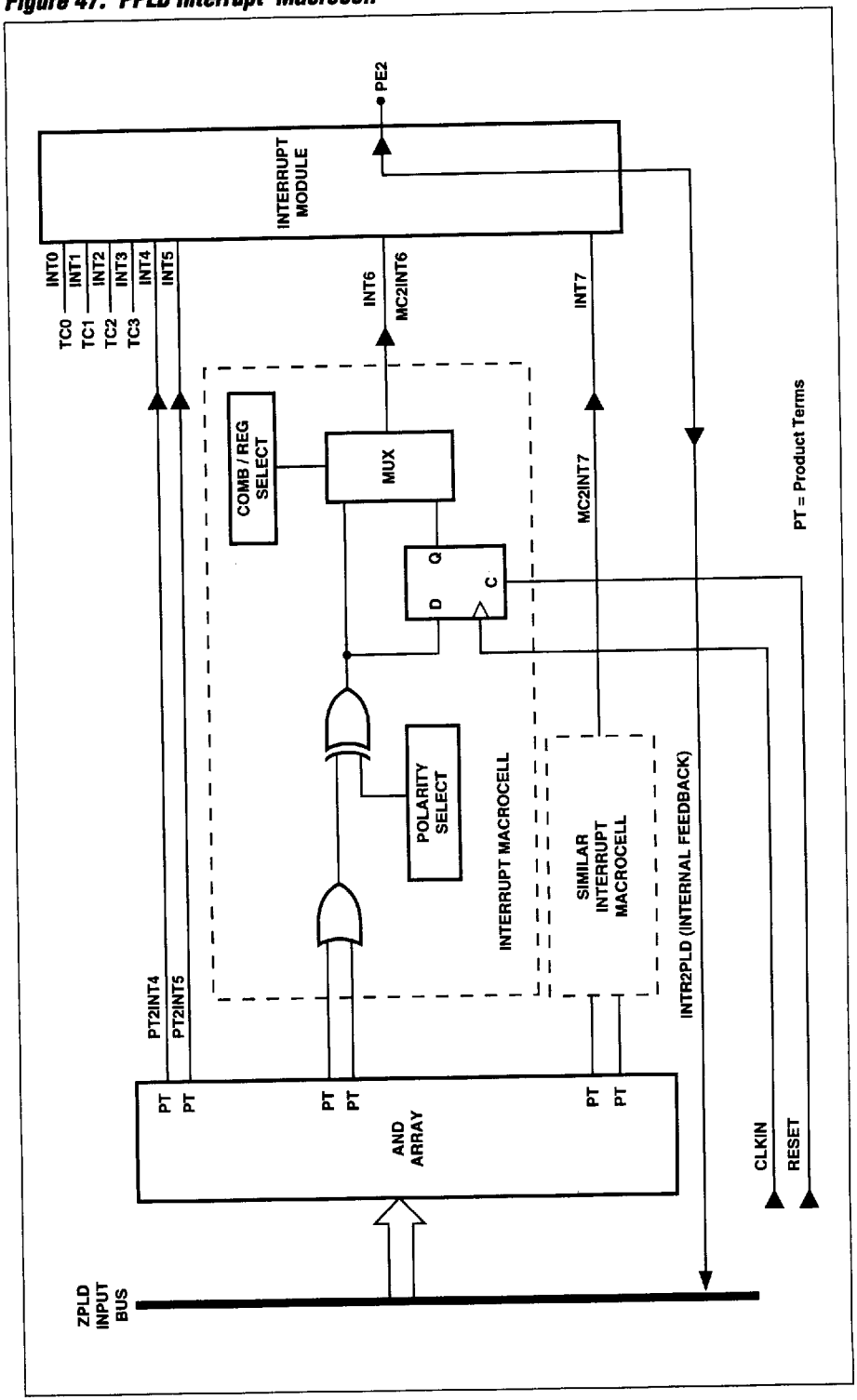
Interrupt inputs INT6 and INT7 originate two dedicated PPLD Macrocells. Each of these PPLD Macrocells have two product terms as inputs that are inputted into a PPLD Macrocell as shown in Figure 47. The outputs of both PPLD Macrocells MC2INT6 and MC2INT7 are either Combinatorial or Register mode. The polarity of the product terms is programmable. Refer to the section on "ZPLD" for further reference on the PPLD.

Interrupt Flowchart

The flowchart in Figure 48 explains the overall initialization and the servicing of the interrupts.

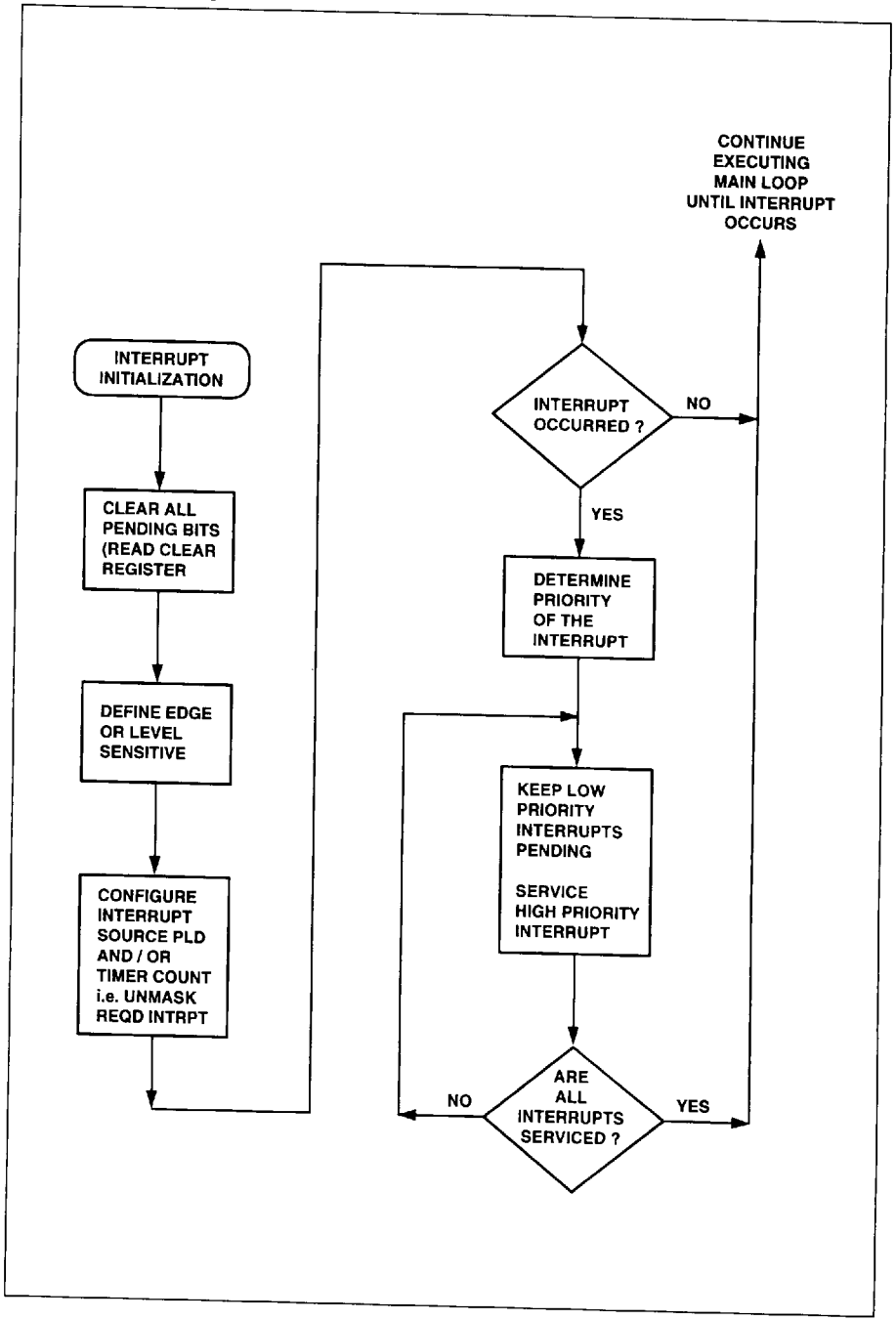
Interrupt Controller (Cont.)

Figure 47. PPLD Interrupt Macrocell



Interrupt Controller (Cont.)

Figure 48. Interrupt Flowchart



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System Configuration

The CSIOP signal, which is generated by the DPLD, selects the internal I/O devices or registers. The CSIOP signal takes up 256 bytes of address space and is defined by the user in the PSDSoft Software. The following is an address offset map for the various devices relative to the CSIOP base address.

Some Motorola 16-bit microcontrollers have a different data bus/data byte orientation. This requires a different address offset for the internal PSD5XX I/O devices or registers. Tables 30a and 31a in this section are for this group of microcontrollers which include the M68HC16, M68302 and M683XX.

The following table is the address map offset of the I/O port registers.

Table 30. I/O Register Address Offset

Register Name	Address Offset				
	Port A	Port B	Port C	Port D	Port E
Data In	00	01	10	11	20
Control	02	03	12	13	22
Data Out	04	05	14	15	24
Direction	06	07	16	17	26
Open Drain			18	19	
Special Function	08	09			28
PLD – I/O	0A	0B			2A
Macrocell Out	0C	0D			2C

Table 30a. I/O Register Address Offset

(For 16-Bit Motorola MCUs in 16-Bit Mode. If 8-Bit Mode is selected, use Table 30.)

Register Name	Address Offset				
	Port A	Port B	Port C	Port D	Port E
Data In	01	00	11	10	21
Control	03	02	13	12	23
Data Out	05	04	15	14	25
Direction	07	06	17	16	27
Open Drain			19	18	
Special Function	09	08			29
PLD – I/O	0B	0A			2B
Macrocell Out	0D	0C			2D

System Configuration (Cont.)

Table 31. Other Register Address Offset

Register Name	Address Offset	Register Name	Address Offset
		PAGE REGISTER	E0
		INTR. READ CLEAR	D4
INTR. MASK	D3	INTR. EDGE/LEVEL	D2
INTR. REQUEST LATCH	D1	INTR. PRIORITY STATUS	D0
		VM	C0
PMMR1	B1	PMMR0	B0
STATUS FLAGS	A9	GLOBAL COMMAND	A8
		DLCY	A6
SOFTWARE LOAD/STORE	A5	FREEZE COMMAND	A4
CMD3	A3	CMD2	A2
CMD1	A1	CMD0	A0
CNTR3	9F	CNTR3	9E
CNTR2	9D	CNTR2	9C
CNTR1	9B	CNTR1	9A
CNTR0	99	CNTR0	98
IMG3	97	IMG3	96
IMG2	95	IMG2	94
IMG1	93	IMG1	92
IMG0	91	IMG0	90

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System Configuration (Cont.)

Table 31a. Other Register Address Offset
(For 16-Bit Motorola MCUs in 16-Bit Mode. If 8-Bit Mode is selected, use Table 31.)

Register Name	Address Offset	Register Name	Address Offset
		PAGE REGISTER	E1
		INTR. READ CLEAR	D5
INTR. MASK	D2	INTR. EDGE/LEVEL	D3
INTR. REQUEST LATCH	D0	INTR. PRIORITY STATUS	D1
		VM	C1
PMMR1	B0	PMMR0	B1
STATUS FLAGS	A8	GLOBAL COMMAND	A9
		DLCY	A7
SOFTWARE LOAD/STORE	A4	FREEZE COMMAND	A5
CMD3	A2	CMD2	A3
CMD1	A0	CMD0	A1
CNTR3	9E	CNTR3	9F
CNTR2	9C	CNTR2	9D
CNTR1	9A	CNTR1	9B
CNTR0	98	CNTR0	99
IMG3	96	IMG3	97
IMG2	94	IMG2	95
IMG1	92	IMG1	93
IMG0	90	IMG0	91

Table 32. I/O Register Function

Register Name	Register Function
Data In	This Register is used to read the input on the port pins.
Control	A "0" sets the corresponding port pin in Address Out Mode. A "1" sets the pin in MCU I/O Mode.
Data Out	Holds the output data in the MCU I/O Mode.
Direction	This register is used to control the data flow in the I/O ports. A "0" sets the corresponding pin as an input pin. A "1" sets the pin as an output pin.
Open Drain	A "0" sets the corresponding pin driver as a CMOS driver. A "1" sets the pin driver as an Open Drain Driver.
Special Function	A "1" sets the corresponding port pin as Timer or Interrupt Output.
PLD – I/O	A read only status register; a "1" indicates the corresponding pin is configured as a PLD pin.
Macrocell Out	This register holds the outputs of the GPLD macrocells.

System Configuration (Cont.)

Table 33. Other Register Function

Register Name	Register Function
PAGE REGISTER	A 4-bit register that supports paging.
INTR. READ CLEAR	Reading this register clears all the pending edge sensitive interrupts.
INTR. EDGE/LEVEL	Define interrupt input as level or edge sensitive.
INTR. MASK	Mask selected interrupt input.
INTR. REQUEST LATCH	A "1" in the register indicates the corresponding interrupt is pending.
INTR. PRIORITY STATUS	The register indicates which pending interrupt has the highest priority.
VM	1. Configures the PSD SRAM to be accessed by "PSEN" as program space (8031 design). 2. Enable the Peripheral I/O Mode of Port A.
PMMR0 PMMR1	Power management registers; enable the PSD Power Down Mode and other power saving configurations.
STATUS FLAGS	Counter/Timer Freeze Acknowledge bits.
GLOBAL COMMAND	Specifies the Counter/Timer operation mode; and to start or stop the Counter/Timers.
DLCY	Specifies the delay cycles to the Counter/Timers.
SOFTWARE LOAD/STORE	This register enables a load (to the Counter/Timer) or store (in the Image Register) operation.
FREEZE COMMAND	This register disables the timer state-machine before access to the Image Register is allowed.
CMD3 – 0	Command Registers for the configuration of the Counter/Timers.
CNTR3 – 0	The four 16-bit Counter/Timers.
IMG3 – 0	The Image Registers for CNTR3 – 0.

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System Configuration (Cont.)

Reset Input

The reset input to the PSD5XX (RESET) is an active low signal which resets some of the internal devices and configuration registers. The Timing Diagram in the AC/DC characterization section shows the reset signal timing requirement. The active low range has a minimum T1 duration. After the rising edge of RESET, the PSD5XX remains in reset during T2 range. (See Figure 59). The PSD5XX must be reset at power up before it can be used.

ZPLD and Memory During Reset

While the Reset Input is active, the ZPLD generates outputs as defined in the PSDabel equations. The EPROM and SRAM blocks respond to the microcontroller bus cycle during reset, but the data is not guaranteed.

Register Values During and After Reset

Table 34 summarizes the status of the volatile register values during and after reset. The default values of the volatile registers are "0" after reset.

ZPLD Macrocell Initialization

The D flip flops in the macrocells in the GPLD can be cleared by:

- A product term (.RE) defined by the user, in PSDabel or
- The MACRO-RST (Reset) input, enabled and defined in PSDabel.

The Timer and Interrupt Controller macrocells in the PPLD are always cleared by the Reset input.

Table 34. Registers Reset Values

Register Name	Device	Reset State
Control	Port A, B, C, D, E	Set to "0" (Address Out Mode)
Data Out (data or address)	Port A, B, C, D, E	Set to "0"
Direction	Port A, B, C, D, E	Set to "0" – Input Mode
Open Drain	Port C, D	Set to "0" – CMOS Outputs
Page Register	Page Logic	Set to "0"
PMMR0, PMMR1	Power Management Unit	Set to "0"
VM	Volatile Memory	Set to "0"
DLCY	Timer	Set to "0"
CMD0 – CMD3	Timer	Set to "0", Clear
Status Flags	Timer	Set to "0", Clear
Global Command	Timer	Set to "0", Clear
IMG0 – IMG3, CNTR0 – CNTR3	Timer	Undefined
Interrupt	Interrupt Controller	Set to "0", Disabled

Table 35. I/O Pin Status During Reset and Standby Mode

Port Configuration	Reset	Standby Mode
Port I/O	Input	Unchanged
ZPLD Output	Active	Depend on Inputs to the ZPLD
Address Out	Tri-stated	Not Defined
Data Port	Tri-stated	Tri-stated
Special Function Out	Tri-stated	Depending on Status of Clock Input to the Counter/Timer
Peripheral I/O	Tri-stated	Tri-state

Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Max	Unit
T_{STG}	Storage Temperature	CLDCC	– 65	+ 150	°C
		PLDCC	– 65	+ 125	°C
	Operating Temperature	Commercial	0	+ 70	°C
		Industrial	– 40	+ 85	°C
		Military	– 55	+ 125	°C
	Voltage on any Pin	With Respect to GND	– 0.6	+ 7	V
V_{PP}	Programming Supply Voltage	With Respect to GND	– 0.6	+ 14	V
V_{CC}	Supply Voltage	With Respect to GND	– 0.6	+ 7	V
	ESD Protection		>2000		V

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Operating Range

Range	Temperature	V_{CC}	V_{CC} Tolerance				
			-70	-90	-12	-15	-20
Commercial	0° C to +70°C	+ 5 V	± 10%	± 10%	± 10%	± 10%	± 10%
Industrial	–40° C to +85°C	+ 5 V			± 10%	± 10%	± 10%
Military	–55° C to +125°C	+ 5 V					± 10%

Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	All Speeds	4.5	5	5.5	V

AC/DC Parameters

The following tables describe the AC/DC parameters of the PSD5XX family:

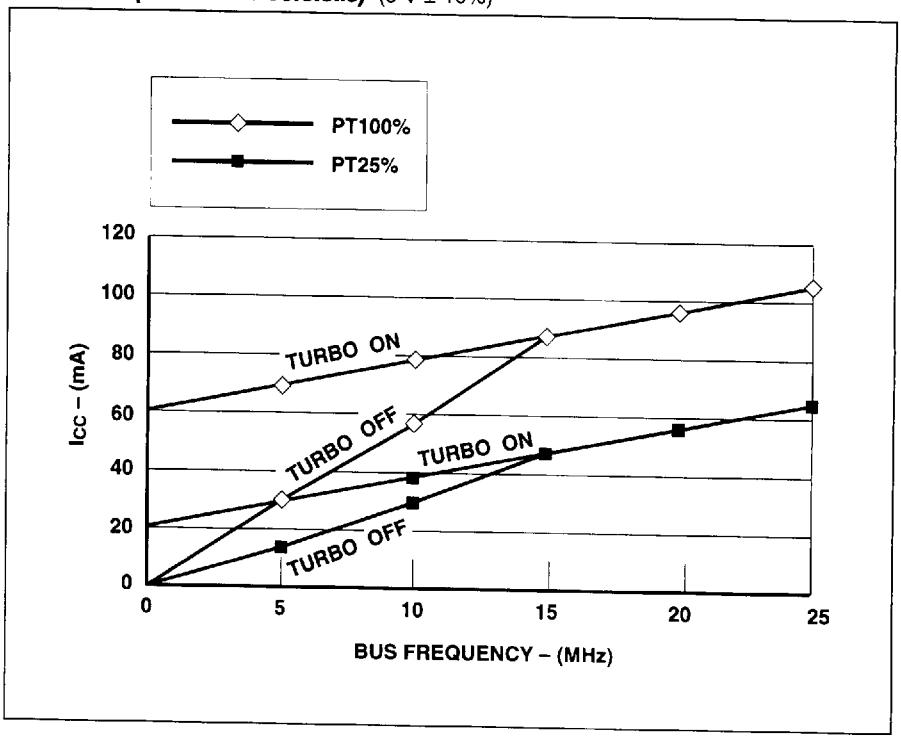
- ❑ DC Electrical Specification
- ❑ AC Timing Specification
  - • ZPLD Timing
    - – Combinatorial Delays
    - – Synchronous Clock Mode
    - – Asynchronous Clock Mode
  - • Microcontroller Timing
    - – Read Timing
    - – Write Timing
    - – Peripheral Mode Timing
    - – Power Down and Reset Timing
  - • PSD5XX Specific Timings
    - – Counter/Timer Timing
    - – Interrupt Controller Timing

Following are some issues concerning the parameters presented:

- ❑ In the DC specification, the Supply Current is given for different modes of operation. Before calculating the total power consumption, determine the percentage of time that the PSD5XX is in each mode. Also the current is considerably different if the ZPLD_TURBO bit is "OFF" and EPROM_CMISER is "ON".
- ❑ The AC power component provides the ZPLD, EPROM, SRAM and TIMER mA/MHz specification. Figure 49 shows the ZPLD mA/MHz as a function of the number of Product Terms (PT) used.
- ❑ In the ZPLD timing parameters add the required delay when ZPLD_TURBO is "OFF".
- ❑ In the MCU timing specification, add the required time delay when EPROM_CMISER is "ON".

AC/DC Parameters (Cont.)

Figure 49. ZPLD I_{CC}/Frequency Consumption (PSD5XX B1 Versions) (5 V ± 10%)



6

DC Characteristics (5 V ± 10% Versions)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage		All Speeds	4.5	5	5.5	V
V_{IH}	High Level Input Voltage		4.5 V < V_{CC} < 5.5 V	2		V_{CC} +.5	V
V_{IL}	Low Level Input Voltage		4.5 V < V_{CC} < 5.5 V	−0.5		0.8	V
V_{IH1}	Reset High Level Input Voltage		(Note 1)	.8 V_{CC}		V_{CC} +.5	V
V_{IL1}	Reset Low Level Input Voltage		(Note 1)	−0.5		.2 V_{CC} −.1	V
V_{HYS}	Reset Pin Hysteresis			0.3			V
V_{OL}	Output Low Voltage		I_{OL} = 20 µA, V_{CC} = 4.5 V		0.01	0.1	V
			I_{OL} = 8 mA, V_{CC} = 4.5 V		0.15	0.45	V
V_{OH}	Output High Voltage		I_{OH} = −20 µA, V_{CC} = 4.5 V	4.4	4.49		V
			I_{OH} = −2 mA, V_{CC} = 4.5 V	2.4	3.9		V
V_{SBY}	SRAM Standby Voltage			2.7		V_{CC}	V
I_{SBY}	SRAM Standby Current		V_{CC} = 0 V		0.5	1	µA
I_{IDLE}	Idle Current (V_{STDBY} Pin)		V_{CC} > V_{SBY}	−0.1		0.1	µA
V_{DF}	SRAM Data Retention Voltage		Only on V_{STBY}	2			V
I_{SB}	Standby Supply Current	Power Down Mode	$\overline{CSI}$ >V_{CC} −.3 V (Note 2)		40	100	µA
		Sleep Mode	$\overline{CSI}$ >V_{CC} −.3 V (Note 3)		10	20	µA
I_{LI}	Input Leakage Current		V_{SS} < V_{IN} > V_{CC}	−1	±.1	1	µA
I_{LO}	Output Leakage Current		.45 < V_{IN} > V_{CC}	−10	±5	10	µA
I_{CC} (DC) (Note 4a)	Operating Supply Current	ZPLD Adder	ZPLD_TURBO = OFF, f = 0 MHz (Note 4)		0		See Figure 49
			ZPLD_TURBO = ON, f = 0 MHz		400	700	µA/PT
		EPROM Adder	CMiser = ON and Not Selected		0	0	mA
			CMiser = ON and EPROM Selected (x8 Data Bus)		10	15	mA
			CMiser = ON and EPROM Selected (x16 Data Bus)		15	20	mA
			CMiser = OFF		15	20	mA
		SRAM Adder	SRAM Not Selected		0	0	mA
			CMiser = ON, SRAM Selected (x8 Data Bus)		25	40	mA
			CMiser = ON, SRAM Selected (x16 Data Bus)		30	45	mA
I_{CC} (AC) (Note 4a)	ZPLD		ZPLD_TURBO = OFF (Note 4)				
			ZPLD_TURBO = ON		2		mA/MHz
	EPROM or SRAM				2		mA/MHz
	Counter/Timer				1		mA/MHz

NOTES: 1. Reset input has hysteresis. V_{IL1} is valid at or below .2V_{CC} −.1. V_{IH1} is valid at or above .8V_{CC}.
2. $\overline{CSI}$ deselected or internal PD is active.
3. Sleep mode bit is set and internal PD is active.
4. See ZPLD ICC/Frequency Power Consumption graph for details.
4.a I_{OUT} = 0 mA.

Combinatorial Delays (5 V ± 10%)

Symbol	Parameter	Conditions	-70		-90**		-12		-15		-20		ZPLD_TURBO OFF*	Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
t_{PD}	I/O Input or Feedback to Combinatorial Output	Port B, E		25		30		32		34		35	Add 10	ns
t_{RPD}	Registered Input to Combinatorial Output	(Note 5)		27		32		34		36		37	Add 10	ns
t_{EA}	Input to Output Enable	Any Input		25		28		30		32		33	Add 10	ns
t_{ER}	Input to Output Disable	Any Input		25		28		30		32		33	Add 10	ns
t_{ARP}	Register Clear or Preset Delay	Any Input		27		30		32		34		35	Add 10	ns
t_{ARPW}	Register Clear or Preset Pulse Width	Any Input	20		25		28		29		30			ns
t_{ARD}	Array Delay			16		18		20		22		24		ns

NOTE: 5. Ports A, C, D and latched address from ADIO (A0, A1, A8 – A15).

****NOTE:** Revision A and previous silicon revisions are 5V ± 5% for 90 nsec version only.

Synchronous Clock Mode (5 V ± 10%)

Symbol	Parameter	Conditions	-70		-90**		-12		-15		-20		ZPLD_TURBO OFF*	Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
f_{MAX}	Maximum Frequency External Feedback	$1/(t_S + t_{CO})$		30.30		27.03		25.00		25.00		22.81		MHz
	Maximum Frequency Internal Feedback (f_{CNT})	$1/(t_S+t_{CO}-10)$		43.48		37.04		33.33		31.25		28.57		MHz
	Maximum Frequency Pipelined Data	$1/(t_{CH} + t_{CL})$		50.00		41.67		35.71		35.71		33.33		MHz
t_S	Input Setup Time	Any Input	15		17		19		20		21		Add 10	ns
t_H	Input Hold Time	Any Input	0		0		0		0		0		0	ns
t_{CH}	Clock High Time	Clock Input	10		12		14		15		16		0	ns
t_{CL}	Clock Low Time	Clock Input	10		12		14		15		16		0	ns
t_{CO}	Clock to Output Delay	Clock Input		18		20		21		22		24	0	ns
t_{ARD}	Array Delay for Product Term Expansion	Any Macrocell		16		18		20		22		24	0	ns
t_{MIN}	Minimum Clock Period	$t_{CH} + t_{CL}$	20		24		28		29		28		0	ns

***NOTE:** If ZPLD_TURBO is off and the ZPLD is operating above 15 MHz, there is no need to add 10 ns to the timing parameter.

****NOTE:** Revision A and previous silicon revisions are 5V ± 5% for 90 nsec version only.

Asynchronous Clock Mode (5 V ± 10%, Note 6)

Symbol	Parameter	Conditions	-70		-90**		-12		-15		-20		ZPLD_TURBO OFF*	Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
f_{MAXA}	Maximum Frequency External Feedback	$1/(t_{SA} + t_{COA})$		26.32		25.00		21.74		21.74		20.41		MHz
	Maximum Frequency Internal Feedback (f_{CNTA})	$1/(t_{SA}+t_{COA}-10)$ (Note 6)		35.71		33.33		27.78		27.78		25.64		MHz
	Maximum Frequency Pipelined Data	$1/(t_{CH} + t_{CL})$		41.67		41.67		35.71		35.71		33.33		MHz
t_{SA}	Input Setup Time	Any Input	8		8		10		12		13		Add 10	ns
t_{HA}	Input Hold Time	Any Input	8		8		10		12		13		0	ns
t_{CHA}	Clock High Time	Any Input	12		12		14		15		16		0	ns
t_{CLA}	Clock Low Time	Any Input	12		12		14		15		16		0	ns
t_{COA}	Clock to Output Delay	Any Input to Port B		30		32		36		37		38	Add 10	ns
t_{ARD}	Array Delay for Product Term Expansion	Any Macrocell		16		18		20		22		24	0	ns
t_{MINA}	Minimum Clock Period	$1/f_{CNT}$	28		30		36		43		39		0	ns

NOTE: 6. Only Port B has asynchronous outputs. Clock into Macrocell Flip Flop is generated by a product term.

***NOTE:** If ZPLD_TURBO is off and the ZPLD is operating above 15 MHz, there is no need to add 10 ns to the timing parameter.

****NOTE:** Revision A and previous silicon revisions are 5V ± 5% for 90 nsec version only.

Explanation of AC Symbols for Non ZPLD Timing.

Example: t_{AVLX} Time from Address Valid to ALE Invalid.

A – Address
C – Power Down
D – Input Data
E – E
H – Logic Level High
I – Interrupt
L – Logic Level Low or ALE
N – Reset
P – Port Signal
Q – Output Data
R – $\overline{WR}$, $\overline{UDS}$, $\overline{LDS}$, $\overline{DS}$, $\overline{IORD}$, $\overline{PSEN}$
S – Chip Select
T – R/$\overline{W}$
t – Time
V – Valid
X – No Longer a Valid Logic Level
Z – Float

Read Timing (5 V ± 10%)

Symbol	Parameter	Conditions	-70		-90**		-12		-15		-20		EPROM_CMiser ON	Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
t_{LVLX}	ALE or AS Pulse Width		18		20		25		28		30		0	ns
t_{AVLX}	Address Setup Time	(Note 8)	5		6		9		10		12		0	ns
t_{LXAX}	Address Hold Time	(Note 8)	7		8		10		11		12		0	ns
t_{AVQV}	Address Valid to Data Valid	(Note 8)		70		90		120		150		200	Add 10	ns
t_{SLQV}	$\overline{CS}$ Valid to Data Valid			80		100		130		150		200	Add 10	ns
t_{RLQV}	$\overline{RD}$ to Data Valid 8/16-Bit Bus	(Note 7)		20		32		38		40		45	0	ns
	$\overline{RD}$ to Data Valid 8-Bit Bus, 8031 Separate Mode	(Note 7a)		32		38		40		45		50	0	ns
	$\overline{RD}$ to Data Valid from Interrupt Controller	(Note 7b)		32		38		40		45		50	0	ns
t_{RHQX}	$\overline{RD}$ Data Hold Time	(Note 7)	0		0		0		0		0		0	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	(Note 7)	30		32		35		38		40		0	ns
t_{RHQZ}	$\overline{RD}$ to Data High-Z	(Note 7)		22		25		30		33		35	0	ns
t_{EHEL}	E Pulse Width		30		32		35		38		40		0	ns
t_{THEH}	R/$\overline{W}$ Setup Time to Enable		8		10		15		18		20		0	ns
t_{ELTL}	R/$\overline{W}$ Hold Time After Enable		0		0		0		0		0		0	ns
t_{AVPV}	Address Input Valid to Address Output Delay	In 16-Bit Data Bus Mode (Note 9)		20		30		35		38		40	0	ns
		In 8-Bit Data Bus Mode (Note 9)		22		32		45		48		50	0	ns

NOTES: 7. $\overline{RD}$ timing has the same timing as $\overline{PSEN}$, DS, $\overline{LDS}$, $\overline{UDS}$ signals (in 8031 combined mode).
7a. $\overline{RD}$ and $\overline{PSEN}$ have the same timing for 8031 separate mode.
7b. Read to Data Valid of the Interrupt Request Latch and Interrupt Priority Status. $\overline{RD}$ timing has the same timing as $\overline{PSEN}$, $\overline{DS}$, $\overline{LDS}$, $\overline{UDS}$ signals.
8. Any input used to select an internal PSD5XX function.
9. In multiplexed mode latched address generated from ADIO delay to address output on any Port.

****NOTE:** Revision A and previous silicon revisions are 5V ± 5% for 90 nsec version only.

Write Timing (5 V ± 10%)

Symbol	Parameter	Conditions	-70		-90**		-12		-15		-20		EPROM_CMiser ON	Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
t_{LVLX}	ALE or AS Pulse Width		18		20		25		28		30			ns
t_{AVLX}	Address Setup Time	(Note 8)	5		6		9		10		12			ns
t_{LXAX}	Address Hold Time	(Note 8)	7		8		10		11		12			ns
t_{AVWL}	Address Valid to Leading Edge of $\overline{WR}$	(Notes 8 and 10)	18		20		25		30		35			ns
t_{SLWL}	$\overline{CS}$ Valid to Leading Edge of $\overline{WR}$	(Note 10)	22		25		30		35		40			ns
t_{DVWH}	$\overline{WR}$ Data Setup Time	(Note 10)	12		15		20		22		25			ns
t_{WHDX}	$\overline{WR}$ Data Hold Time	(Note 10)	5		5		5		5		5			ns
t_{WLWH}	$\overline{WR}$ Pulse Width	(Note 10)	18		20		25		28		30			ns
t_{WHAX}	Trailing Edge of $\overline{WR}$ to Address Invalid	(Note 10)	0		0		0		0		0			ns
t_{WHPV}	Trailing Edge of $\overline{WR}$ to Port Output Valid	(Note 10)		25		30		35		38		40		ns
t_{AVPV}	Address Input Valid to Address Output Delay	In 16-Bit Data Bus Mode (Note 9)		20		30		35		38		40		ns
		In 8-Bit Data Bus Mode (Note 9)		22		32		45		48		50		ns

NOTE: 10. $\overline{WR}$ timing has the same timing as E, $\overline{DS}$, $\overline{LDS}$, $\overline{UDS}$, $\overline{WRL}$, $\overline{WHR}$ signals.

****NOTE:** Revision A and previous silicon revisions are 5V ± 5% for 90 nsec version only.

Port A Peripheral Data Mode Read Timing (5 V ± 10%)

Symbol	Parameter	Conditions	-70		-90**		-12		-15		-20		ZPLD_TURBO OFF	Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$t_{AVQV (PA)}$	Address Valid to Data Valid	(Note 11)		45		55		60		62		65	Add 10	ns
$t_{SLQV (PA)}$	$\overline{CS}$ Valid to Data Valid			55		55		60		62		65	Add 10	ns
$t_{RLQV (PA)}$	$\overline{RD}$ to Data Valid	(Notes 7, 12)		22		26		38		45		50	0	ns
	$\overline{RD}$ to Data Valid 8031 Mode			32		38		40		45		50	0	ns
$t_{DVQV (PA)}$	Data In to Data Out Valid			22		22		25		26		28	0	ns
$t_{QXRH (PA)}$	$\overline{RD}$ Data Hold Time	(Note 7)	0		0		0		0		0		0	ns
$t_{RLRH (PA)}$	$\overline{RD}$ Pulse Width	(Note 7)	25		30		35		38		40		0	ns
$t_{RHQZ (PA)}$	$\overline{RD}$ to Data High-Z	(Note 7)		20		25		30		33		35	0	ns

Port A Peripheral Data Mode Write Timing (5 V ± 10%)

Symbol	Parameter	Conditions	-70		-90**		-12		-15		-20		ZPLD_TURBO OFF	Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$t_{WLQV (PA)}$	$\overline{WR}$ to Data Propagation Delay	(Note 10)		25		27		32		35		38	0	ns
$t_{DVQV (PA)}$	Data to Port A Data Propagation Delay	(Note 13)		22		22		25		26		28	0	ns
$t_{WHQZ (PA)}$	$\overline{WR}$ Invalid to Port A Tri-state	(Note 10)		20		25		30		33		35		ns

NOTES: 11. Any input used to select Port A Data Peripheral Mode.
12. Data is already stable on Port A.
13. Data stable on ADIO pins to data on Port A.

****NOTE:** Revision A and previous silicon revisions are 5V ± 5% for 90 nsec version only.

Power Down and Reset Timing (5 V ± 10%)

Symbol	Parameter	Conditions	-70		-90**		-12		-15		-20		ZPLD_TURBO OFF	Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
t_{LVDV}	ALE Access Time from Power Down			100		120		140		150		170	Add 10	ns
t_{LVDV1}	ALE or $\overline{CSI}$ Access Time from Sleep			120		150		170		200		200	0	ns
t_{LVDV2}	ZPLD Propagation Delay in Sleep Mode			600		600		600		600		600	0	ns
t_{LVDV3}	ZPLD Recovery Time after Sleep Mode			250		250		250		250		250	0	ns
t_{CHCL}	APD Clock High Time	Using PE7	10		12		14		15		16		0	ns
t_{CLCH}	APD Clock Low Time	Using PE7	10		12		14		15		16		0	ns
f_{MAX}	APD Maximum Frequency	Using PE7		35.00		30.00		25.00		22.00		20.00	0	MHz
t_1	RESET Active Low Time		150		200		250		300		300		0	ns
t_2	RESET High to Operational Device			150		200		250		300		300	0	ns

**NOTE: Revision A and previous silicon revisions are 5V ± 5% for 90 nsec version only.

Counter/Timer Timing (5 V ± 10%)

Symbol	Parameter	Conditions	-70		-90**		-12		-15		-20		ZPLD_TURBO OFF	Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
f_{MAX}	Maximum Frequency			36.00		30.00		25.00		22.00		20.00	0	MHz
t_{CHCL}	Clock High Time		10		12		14		15		16		0	ns
t_{CLCH}	Clock Low Time		10		12		14		15		16		0	ns
t_{CHPV}	Clock to Output Delay			28		30		32		33		35	0	ns
t_{CHPV1}	Clock to Watchdog Output Delay			50		50		55		58		60	Add 10	ns
t_{LVCH}	Input Setup Time Relative to Rising Clock Edge	Pin Input	15		17		19		20		21		Add 10 (Note 14)	ns
t_{LVCH1}	Input Setup Time Relative to Rising Clock Edge	PLD Combinatorial Input	25		27		29		31		33		Add 10 (Note 14)	ns
t_{MIN}	Minimum Clock Period	$1/f_{MAX}$	28		33		40		45		50		0	ns

Interrupt Timing (5 V ± 10%)

Symbol	Parameter	Conditions	-70		-90**		-12		-15		-20		ZPLD_TURBO OFF	Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
t_{IVIV}	Interrupt Request Input to Interrupt Output	(Note 15)		40		50		60		65		70	0	ns
t_{RXIX}	Read Vector to Interrupt Request Clear			30		40		50		55		60	0	ns
t_{ILIL}	Interrupt Request Minimum Pulse Width		18		20		30		35		40		0	ns
t_{RLQV}	$\overline{RD}$ to Data Valid Interrupt Controller	(Note 7b)		32		38		40		45		50	0	ns

NOTES: 14. For inputs which use PPLD only.
15. This timing is only valid when read to the interrupt request latch and priority status latch are not valid.

****NOTE:** Revision A and previous silicon revisions are 5V ± 5% for 90 nsec version only.

Figure 50. Read Timing

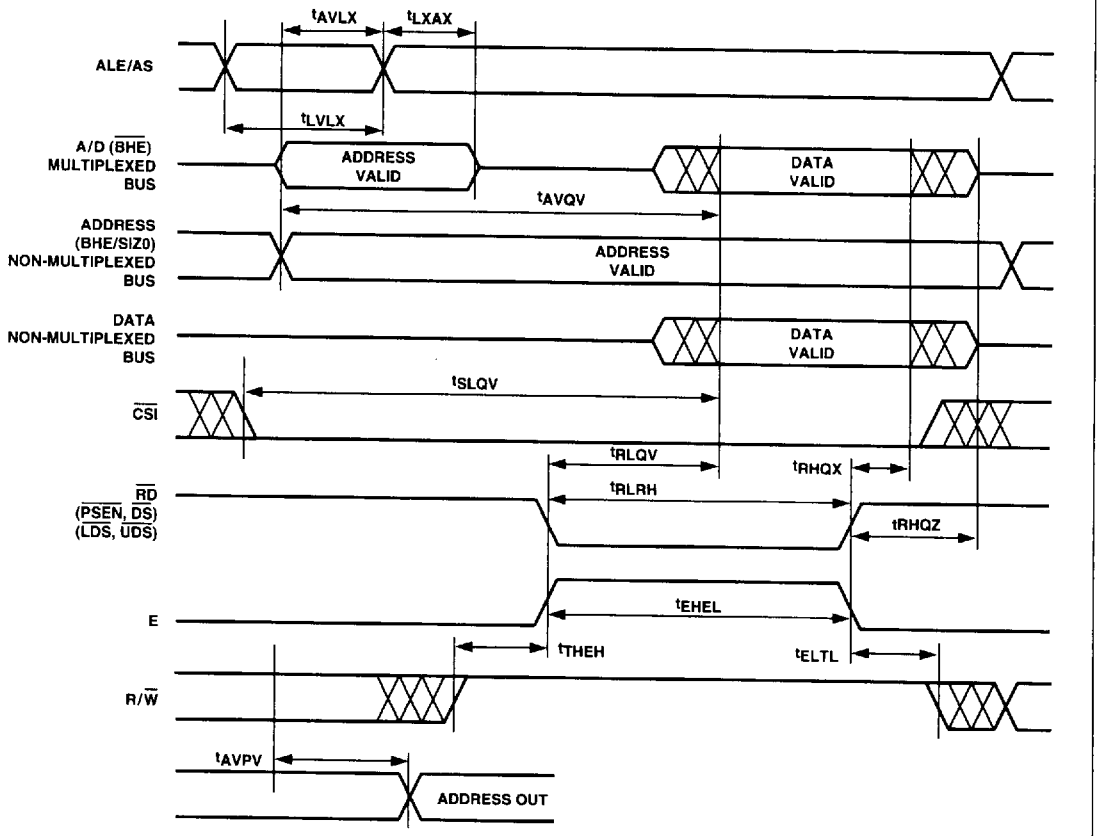


Figure 51. Write Timing

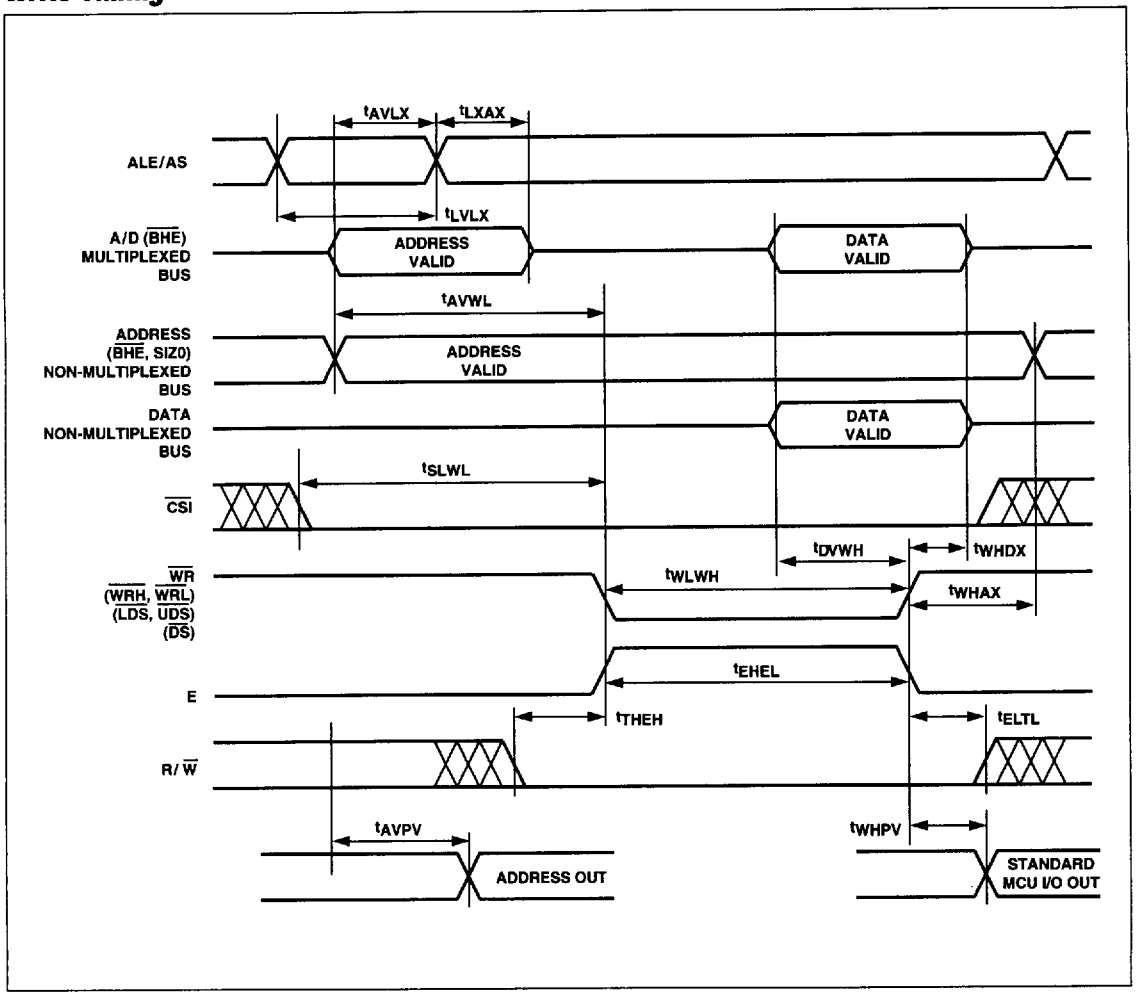
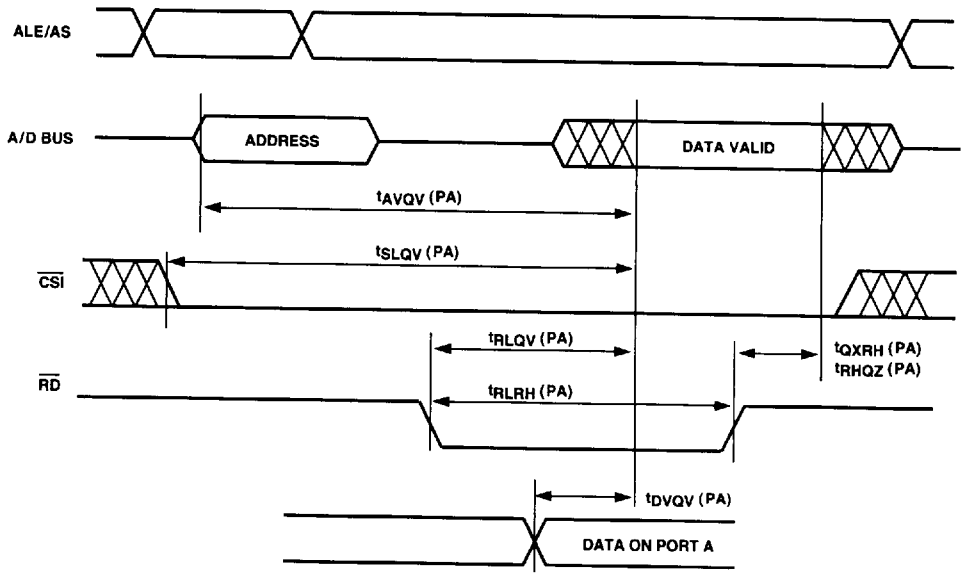


Figure 52. Peripheral I/O Read Timing



6

Figure 53. Peripheral I/O Write Timing

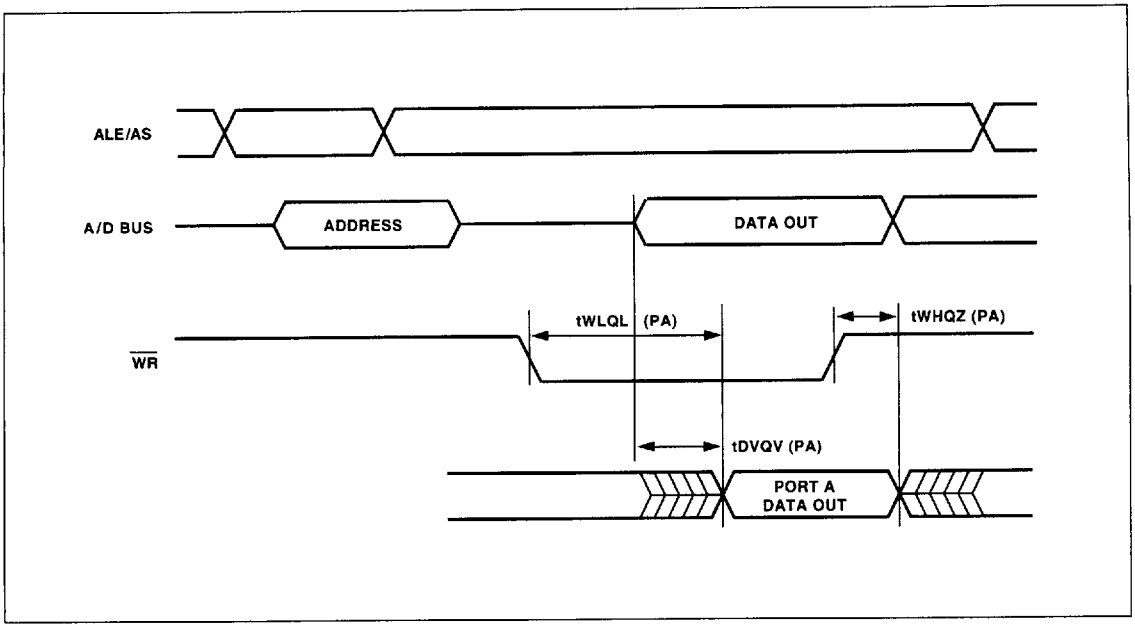


Figure 54. Combinatorial Timing – ZPLD

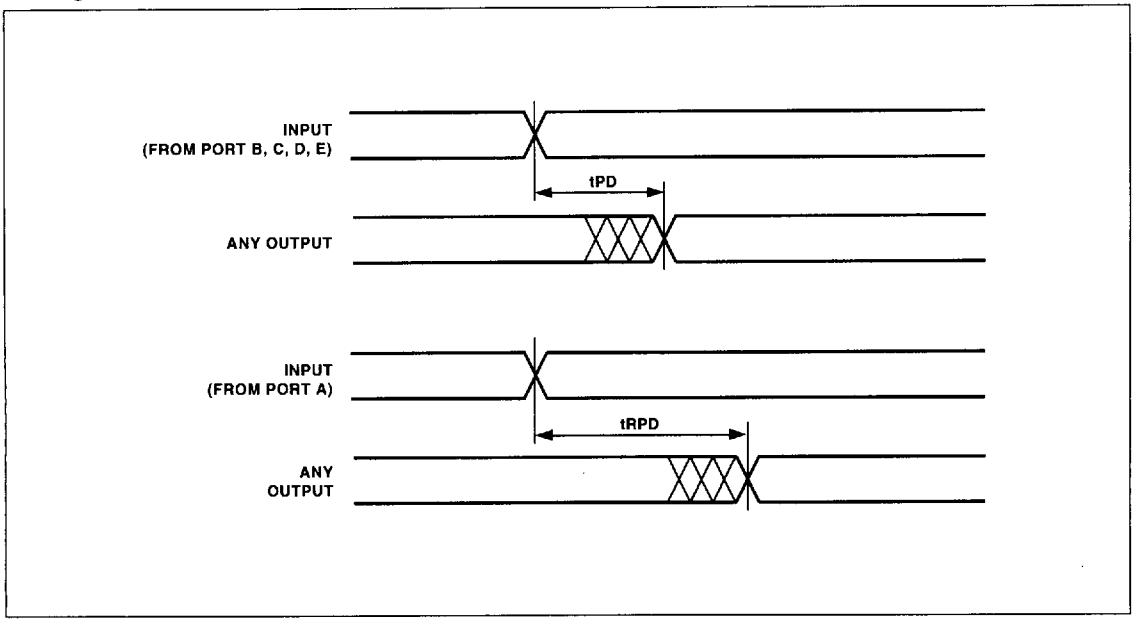


Figure 55. Synchronous Clock Mode Timing – ZPLD

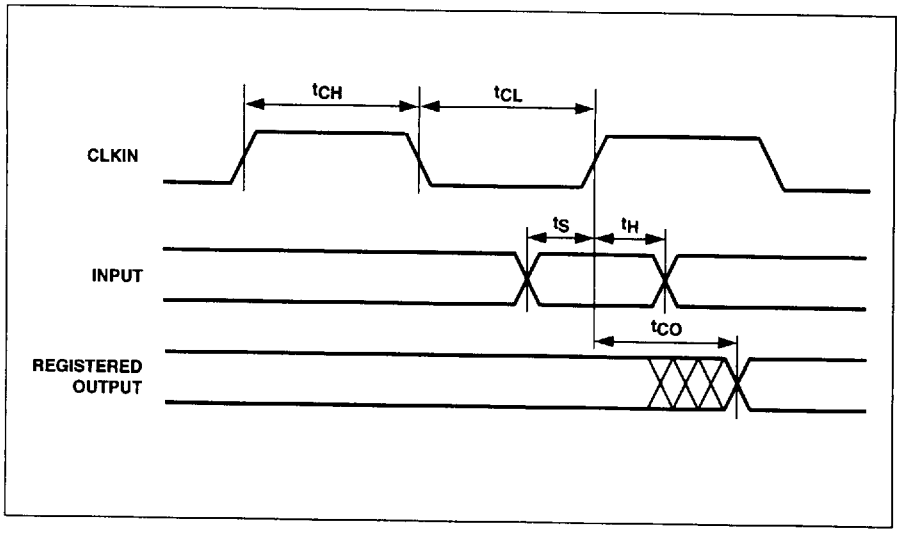


Figure 56. Asynchronous Clock Mode Timing (Product-Term Clock, PB Macrocell Only)

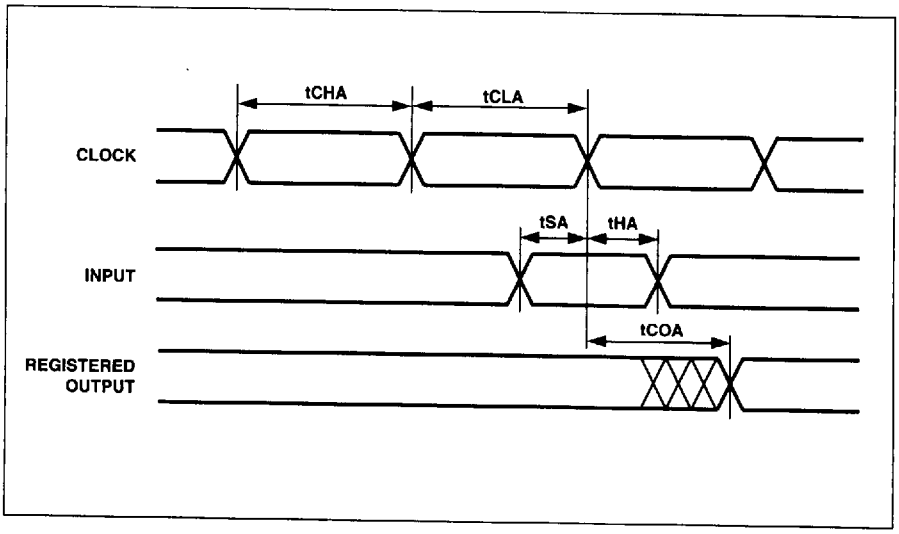


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Figure 57. Input to Output Disable/Enable

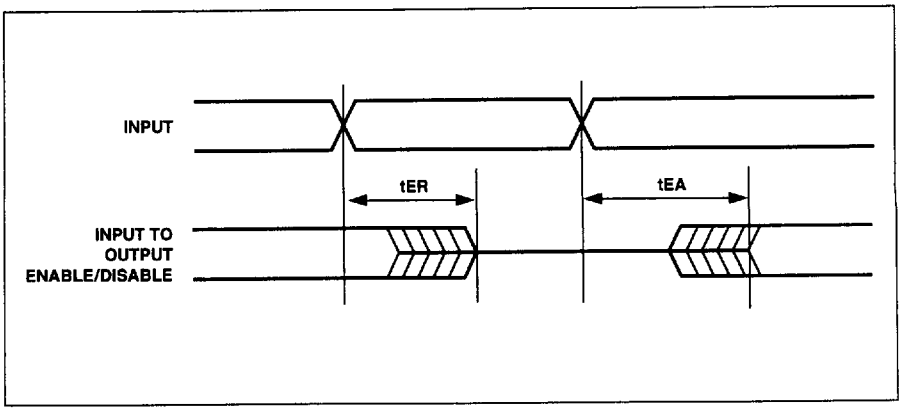


Figure 58. Asynchronous Reset/Preset

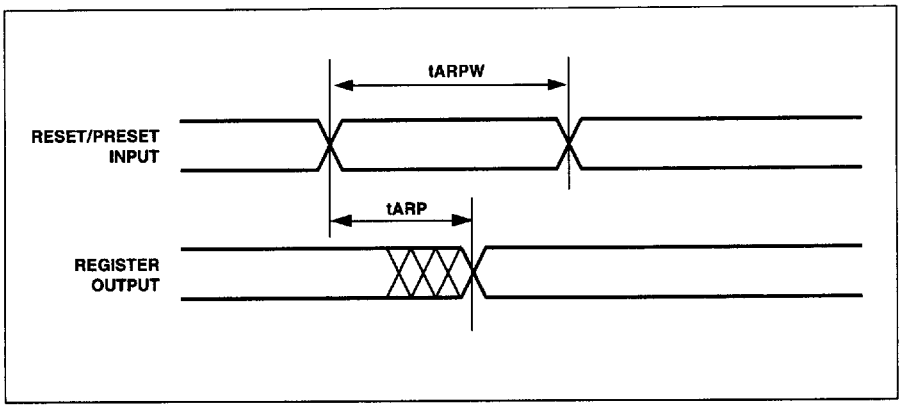


Figure 59. Reset Timing

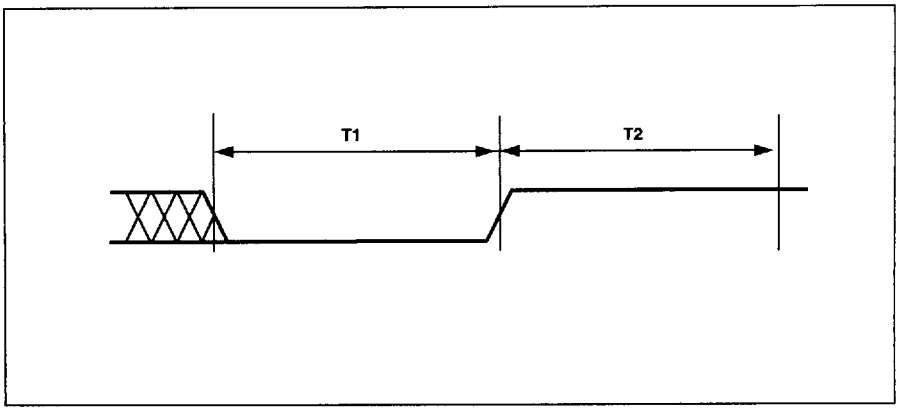
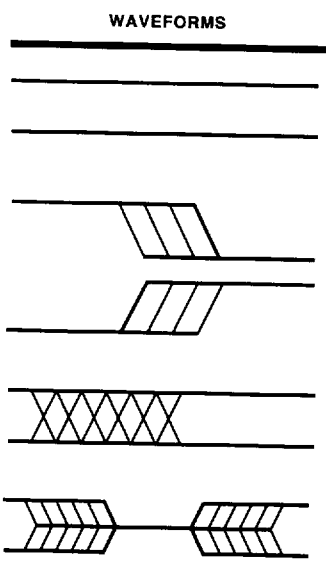


Figure 60. Key to Switching Waveforms



WAVEFORMS	INPUTS	OUTPUTS
	STEADY INPUT	STEADY OUTPUT
	MAY CHANGE FROM HI TO LO	WILL BE CHANGING FROM HI TO LO
	MAY CHANGE FROM LO TO HI	WILL BE CHANGING LO TO HI
	DON'T CARE	CHANGING, STATE UNKNOWN
	OUTPUTS ONLY	CENTER LINE IS TRI-STATE

Pin Capacitance

T_A = 25 °C, f = 1 MHz

Symbol	Parameter[16]	Conditions	Typical[17]	Max	Unit
C_{IN}	Capacitance (for input pins only)	V_{IN} = 0 V	4	6	pF
C_{OUT}	Capacitance (for input/output pins)	V_{OUT} = 0 V	8	12	pF
C_{VPP}	Capacitance (for WR/V_{PP} or R/W/V_{PP})	V_{PP} = 0 V	18	25	pF

NOTES: 16. These parameters are only sampled and are not 100% tested.
17. Typical values are for T_A = 25°C and nominal supply voltages.

Figure 61. AC Testing Input/Output Waveform

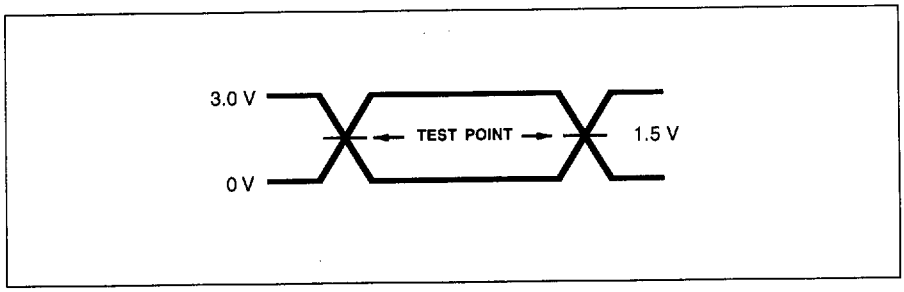
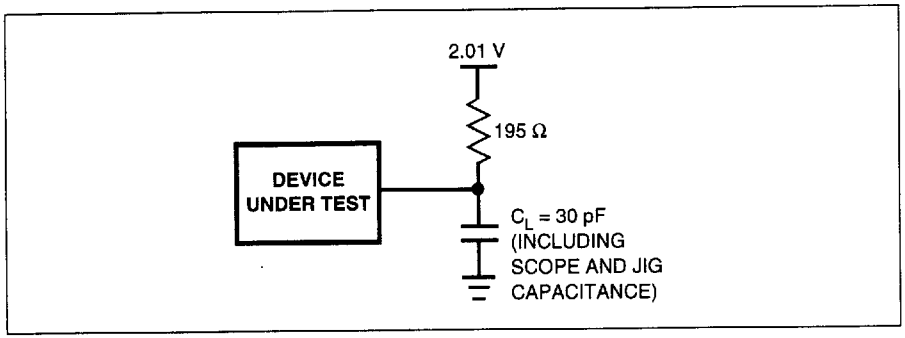


Figure 62. AC Testing Load Circuit



Erasure and Programming

To clear all locations of their programmed contents, expose the window packaged device to an ultra-violet light source. A dosage of 30 W second/cm² is required. This dosage can be obtained with exposure to a wavelength of 2537 Å and intensity of 12000 µW/cm² for 40 to 45 minutes. The device should be about 1 inch from the source, and all filters should be removed from the UV light source prior to erasure.

The PSD5XX and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although the erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight eventually erases the device. For maximum system reliability, these sources should be avoided. If used in such an environment, the package windows should be covered by an opaque substance.

Upon delivery from WSI, or after each erasure, the PSD5XX device has all bits in the PAD and EPROM in the "1" or high state. The configuration bits are in the "0" or low state. The code, configuration, and PAD MAP data are loaded through the procedure of programming

Information for programming the device is available directly from WSI. Please contact your local sales representative.

PSD5XX Pin Assignments

Pin No.	68-Pin PLDCC/CLDCC Package	Pin No.	68-Pin PLDCC/CLDCC Package
1	GND	35	GND
2	ADIO_7	36	PE2
3	ADIO_6	37	PE1
4	ADIO_5	38	PE0
5	ADIO_4	39	CSI
6	ADIO_3	40	RESET
7	ADIO_2	41	RD
8	ADIO_1	42	CLKIN
9	ADIO_0	43	PB7
10	PC7	44	PB6
11	PC6	45	PB5
12	PC5	46	PB4
13	PC4	47	PB3
14	PC3	48	PB2
15	PC2	49	PB1
16	PC1	50	PB0
17	PC0	51	GND
18	VCC	52	VCC
19	GND	53	PD7
20	PA7	54	PD6
21	PA6	55	PD5
22	PA5	56	PD4
23	PA4	57	PD3
24	PA3	58	PD2
25	PA2	59	PD1
26	PA1	60	PD0
27	PA0	61	ADIO_15
28	Vstby	62	ADIO_14
29	WR	63	ADIO_13
30	PE7	64	ADIO_12
31	PE6	65	ADIO_11
32	PE5	66	ADIO_10
33	PE4	67	ADIO_9
34	PE3	68	ADIO_8

PSD5XX Pin Assignments

Pin No.	80-Pin TQFP Package	Pin No.	80-Pin TQFP Package
1	PC7	41	PB7
2	PC6	42	PB6
3	PC5	43	PB5
4	PC4	44	PB4
5	PC3	45	PB3
6	PC2	46	PB2
7	PC1	47	PB1
8	PC0	48	PB0
9	V_{CC}	49	GND
10	V_{CC}	59	GND
11	GND	51	V_{CC}
12	GND	52	V_{CC}
13	PA7	53	PD7
14	PA6	54	PD6
15	PA5	55	PD5
16	PA4	56	PD4
17	PA3	57	PD3
18	PA2	58	PD2
19	PA1	59	PD1
20	PA0	60	PD0
21	NC	61	NC
22	NC	62	ADIO_15
23	Vstdby	63	ADIO_14
24	WR	64	ADIO_13
25	PE7	65	ADIO_12
26	PE6	66	ADIO_11
27	PE5	67	ADIO_10
28	PE4	68	ADIO_9
29	PE3	69	ADIO_8
30	GND	70	GND
31	GND	71	GND
32	PE2	72	ADIO_7
33	PE1	73	ADIO_6
34	PE0	74	ADIO_5
35	CSI	75	ADIO_4
36	RESET	76	ADIO_3
37	RD	77	ADIO_2
38	CLKIN	78	ADIO_1
39	NC	79	ADIO_0
40	NC	80	NC

Figure 63. Drawing J5 – 68-Pin Plastic Leaded Chip Carrier (PLDCC) (Package Type J)

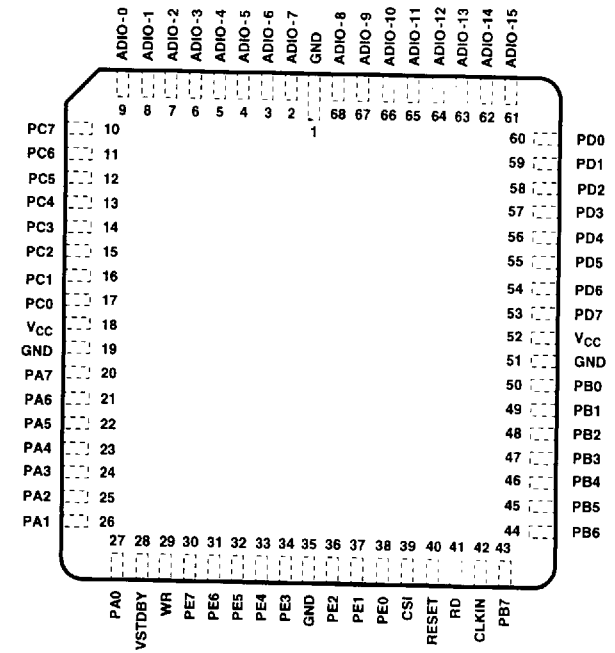


Figure 64. Drawing L5 – 68-Pin Ceramic Leaded Chip Carrier (CLDCC) with Window (Package Type L)

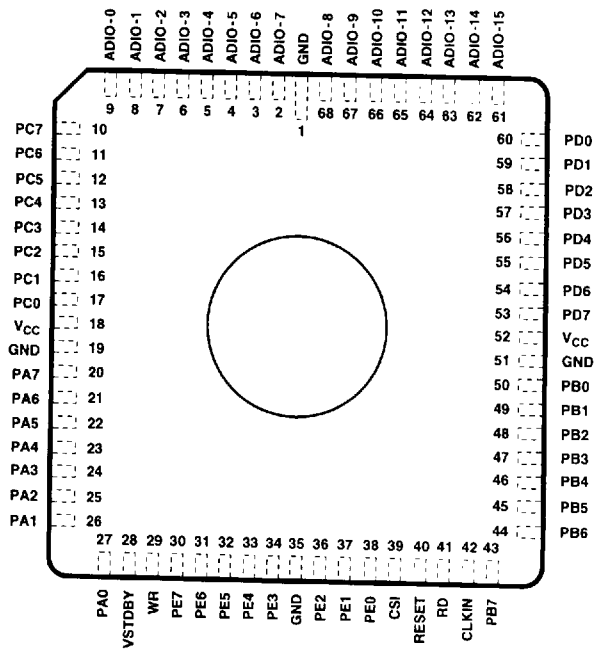


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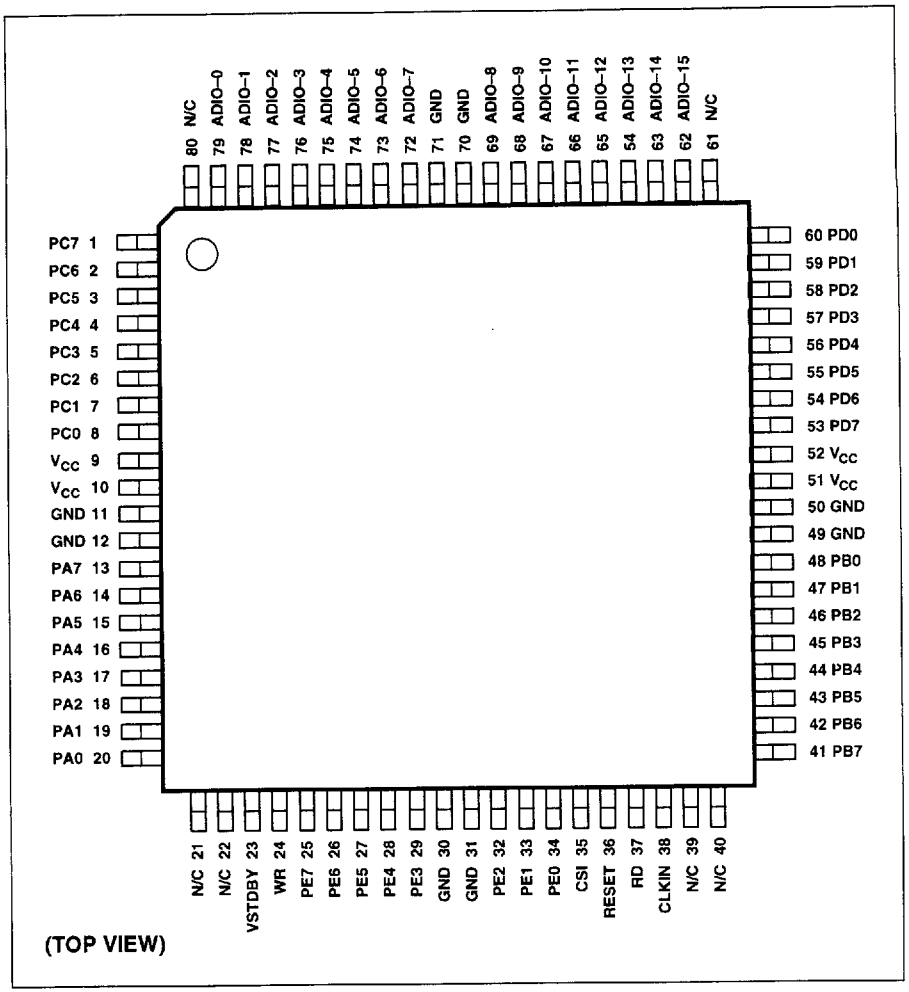
Figure 65. Drawing U2 – 80-Pin Plastic Thin Quad Flatpack (TQFP) (Package Type U)



PSD5XX Product Ordering Information

PSD5XX family devices are available in a wide range of product selections. Options and combinations include:

Architecture
Speed (Access Time)
Memory Size
Configuration
Mask Programmability
Operating Temperature Range
Packages

Please contact your local WSI Sales Representative or Distributor for the PSDXX product selection that best fits your application and objectives.