TCMD0110G
10 Gbits/s Clocked Modulator Driver

Features

- Operation to 12.5 Gbits/s NRZ.
- Internal optional retiming flip-flop to minimize output data pattern jitter.
- Adjustable output amplitude up to 3 V (R_L = 50 Ω).
- Integrated dc level adjustment to –1.5 V
- Complementary data and clock inputs, and data output.
- Complete operation and control with single –5.2 V power supply.
- 28 ps rise and fall time (20%—80%).
- 2 ps typical rms jitter (clocked mode).
- Clock disable mode for data feed-through.
- Optional 50 Ω on-chip termination for unused output (die form only).
- Single or dual-pin pulse width adjust 80 ps—120 ps.
- Available in die form or a 32-pin microlead frame package.

Applications

- Optical transmitters.
- Digital video transmission.
- SONET/SDH test equipment.
- SONET/SDH OC-192/STM-64 transmission systems.
- 10.7 Gbits/s and 12.5 Gbits/s forward error correction (FEC).
- 10G Ethernet 10.3125 Gbits/s.

Functional Description

The TCMD0110G has been designed to drive electroabsorption modulators (EAMs), electroabsorption modulated lasers (EMLs), Mach-Zehnder (M-Z) lithium niobate modulators, and direct modulated lasers (DMLs) that have a 50 Ω input impedance at speeds up to 12.5 Gbit/s NRZ. For nonclocked applications, a clock disable pin is provided.

The driver consists of an input buffer, a limiting amplifier, a selectable data retiming section, a pulse width control circuitry, an output buffer with adjustable modulation level, and a dc offset section to provide a mark level adjustment.

The output buffer is designed to provide 3 V of modulation to a 50 Ω load at each output. The dc offset adjustment networks provide down to –1.5 V offset (see Figure 7). The dc offset for the unused output can be disabled to minimize power consumption (see Table 1).

The input data is retimed using an integrated flip-flop to remove incoming pattern dependent jitter. This feature is enabled using a clock select pad (see Table 1). If no clock is available, the TCMD0110G can be operated in a nonclocked mode.

The unused output can be terminated through the integrated 50 Ω resistor when using the die form of the product (see Table 1).

Note: This advance data sheet serves as a product description and reflects design objectives and conceptual characteristics. Specifications may be incomplete and, along with functionality, packaging, and pin functions, are subject to change. The devices have not been extensively characterized and final specifications may not correspond to advanced data sheet values.

Functional Description (continued)

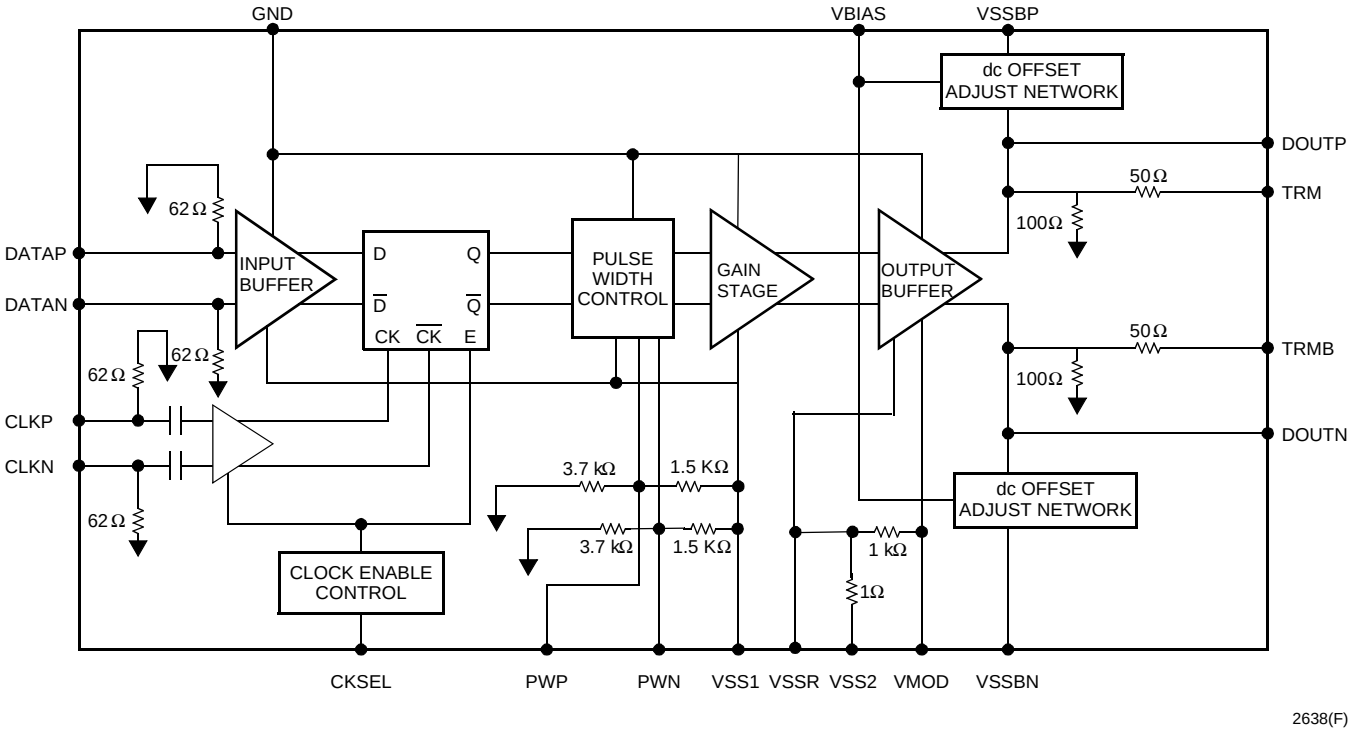

Figure 1. TCMD0110G Block Diagram

Table 1. Functional Description of Selected Pads

Pad Name	Function
CKSEL	–5.2 V = enable, float = disable
VSSBP	Float when not using DOUTP
VSSBN	Float when not using DOUTN
TRM	Ground to terminate unused DOUTP
TRMB	Ground to terminate unused DOUTN

Die Layout

Dimensions are in µm.

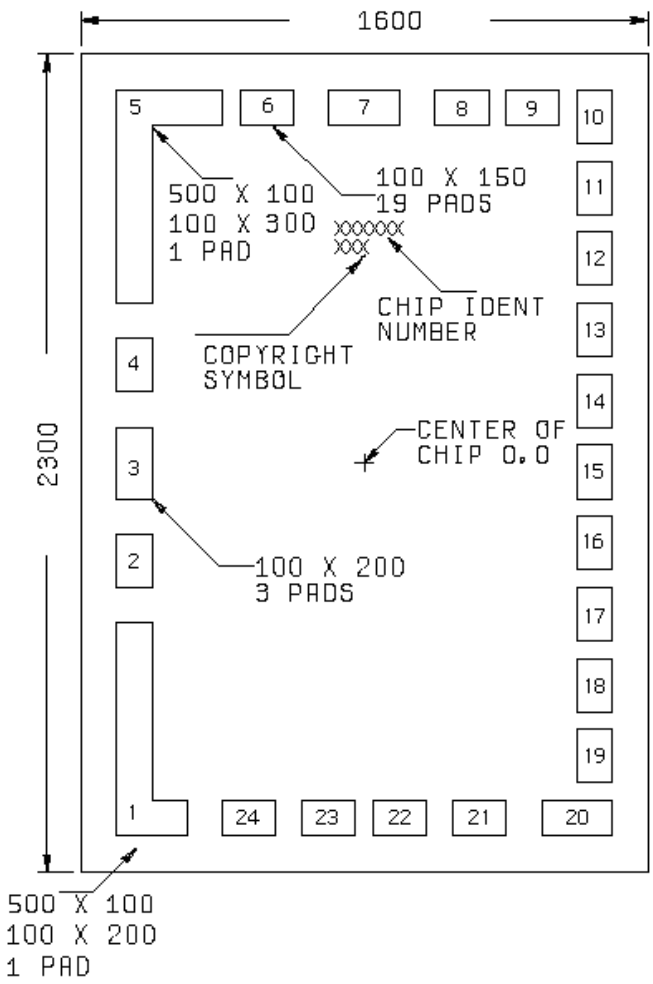

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Figure 2. TCMD0110G Pad Layout

Die Layout (continued)

Table 2. Die Pad Description

Pad Number	Symbol	Description
1, 3, 5, 7, 9	GND	Ground
2	CLKN	Complementary clock input
4	CLKP	Clock input
6	DATAN	Complementary data input
8	DATAP	Data input
10	PWP	Pulse width control positive
11	PWN	Pulse width control negative
12	VSS1	Supply voltage
13	VSS2	Supply voltage for output buffer
14	VSSR	Modulation voltage sense
15	VSSBN	Supply voltage for DOUTN mark level adjustment network
16	VSSBP	Supply voltage for DOUTP mark level adjustment network
17	VMOD	Modulation amplitude control voltage
18	VBIAS	Mark level control voltage
19	CKSEL	Clock select
21	DOUTP	Data output
22	TRM	Ground pad for termination resistor of unused DOUTP
23	TRMB	Ground pad for termination resistor of unused DOUTN
24	DOUTN	Complementary data output

Package Layout

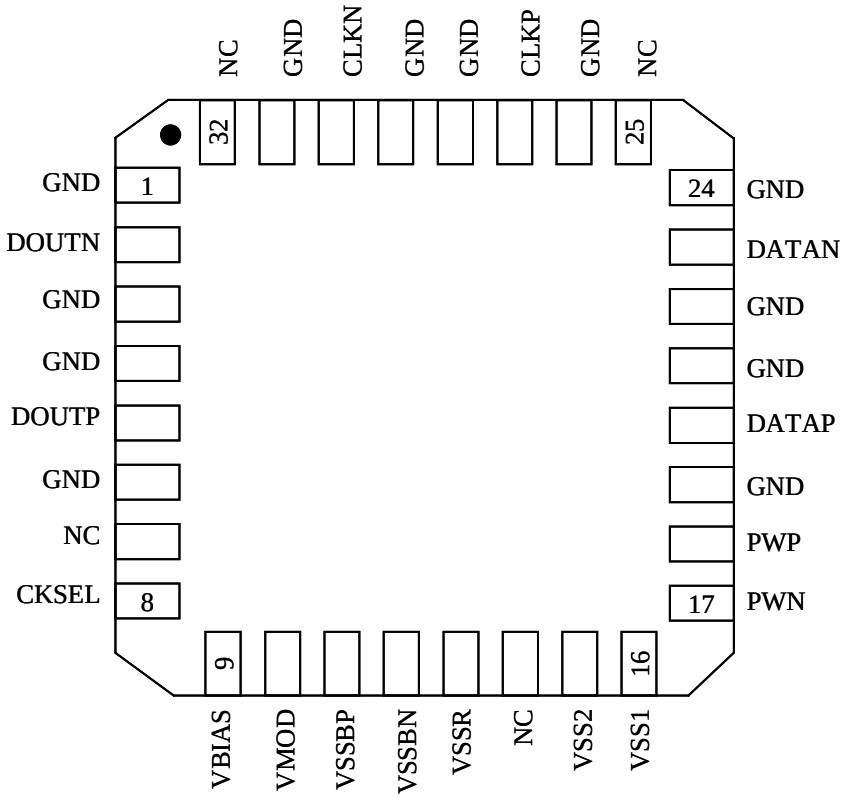


Figure 3. Package Layout of TCMD0110G (Top View)

Table 3. Micro-Lead Frame Package Pin-out for TCMD0110G

Pin Number	Symbol	Description
1, 3, 4, 6, 19, 21, 22, 24, 26, 28, 29, 31	GND	Ground
2	DOUTN	Complementary data output
5	DOUTP	Data output
7, 14, 25, 32	NC	Not connected, Intended for future use
8	CKSEL	Clock select
9	VBIAS	Mark level control voltage
10	VMOD	Modulation amplitude control voltage
11	VSSBP	Supply voltage for DOUTP mark level adjustment network
12	VSSBN	Supply voltage for DOUTN mark level adjustment network
13	VSSR	Modulation voltage sense
15	VSS2	Supply voltage for output buffer
16	VSS1	Supply voltage
17	PWN	Pulse width control negative
18	PWP	Pulse width control positive
20	DINP	Data input
23	DINN	Complementary data input
27	CLKP	Clock input
30	CLKN	Complementary clock input

Powerup Sequence

The control voltages V_{MOD}, PWP, PWN and V_{BIAS} must be referenced to Vss. To avoid damage to the device, power should be applied to the pins simultaneously or in the following sequence:

1. V_{SS1}, V_{SS2} and V_{MOD} simultaneously, or V_{SS1} then V_{MOD} then V_{SS2}, or V_{MOD} then V_{SS1} then V_{SS2} (in the latter case, a current limit of 3 mA must be applied to V_{MOD}).

2. a) V_{SSBP} and/or V_{SSBN} and V_{BIAS} simultaneously.
   b) V_{BIAS} then V_{SSBP} and/or V_{SSBN} with a current limit of 3 mA applied to V_{BIAS}

3. a) Adjust V_{MOD} to achieve desired output amplitude.
   b) Adjust V_{BIAS} to get desired offset.

4. PWP and PWN.

5. Adjust PWP and PWN to position the eye crosspoint

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods of time can adversely affect device reliability. Unless otherwise specified, maximum ratings apply to both die and packaged product.

Table 4. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	Tstg	–40	125	°C
Supply Voltage	Vss	–5.5	0	V
Supply Current	Iss	—	400	mA
Input Voltage	V_{DATAP}, V_{DATAN}	–2.0	0.5	V
Output Voltage	V_{DOUTP}, V_{DOUTN}	–4.1	0.5	V
Modulation Control Voltage	V_{MOD}	Vss – 0.5	Vss + 1.5	V
Offset Control Voltage	V_{BIAS}	Vss – 0.5	Vss + 2.5	V
Pulse Width Control Voltage	V_{PWP}, V_{PWN}	Vss – 0.5	Vss + 2.5	V
Modulation Current	I_{VMOD}	–3	3	mA

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Agere Systems Inc. employs a human-body model (HBM) and a charged device module (CDM) for ESD susceptibility testing and protection design evaluation. Our method complies with the EOS/ESD association standard for ESD sensitivity testing for CDM.

Device	Voltage
TCMD0110G	TBD

Recommended Operating Conditions

Table 5. Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data Rate	—	NRZ	—	—	10.7	Gbits/s
Supply Voltage	V_{SS}	—	–5.5	—	–5.0	V
Operating Case Temperature	T_{CASE}	—	0	—	85	°C
Data Input Signal	V_{DATAP}, V_{DATAN}	ac coupled, single-ended	0.5	—	1.0	Vp-p
		ac coupled, differential	0.5	—	1.0	Vp-p
		dc coupled, single-ended	0.5	—	1.0	Vp-p
		dc coupled, differential	0.5	—	1.0	Vp-p
Clock Input Signal	V_{CLKP}, V_{CLKN}	ac coupled, single-ended	0.5	—	1.0	Vp-p
		ac coupled, differential	0.5	—	1.0	Vp-p
		dc coupled, single-ended	0.5	—	1.0	Vp-p
		dc coupled, differential	0.5	—	1.0	Vp-p
Input Data to Clock Setup and Hold Time	t_S, t_H	See Figure 8	—	TBD	—	ps
Modulation Current Control Voltage	V_{MOD}	V_{MOD} referenced V_{SS}	Vss	—	Vss + 1.0	V
Offset Level Control Voltage	V_{BIAS}	V_{BIAS} referenced Vss	Vss	—	Vss + 2.0	V
Pulse Width Control Voltage	V_{PWP}, V_{PWN}	PWP and PWN referenced to Vss	Vss + 1.0	—	Vss + 2.0	V
Clock Select Signal	V_{CSEL}	CSEL referenced to Vss	Vss	—	Vss + TBD	V

Electrical Characteristics

Table 6. Electrical Characteristics

$T_{AMBIENT}$ = 25 °C, R_L = 50 Ω, V_{SS} = –5.2 V, V_{IN} = 600 mVp-p, clock enabled, V_{CLK} = 600 mVp-p, both data and clock single-ended ac coupled. Bit rate = 9.95328 Gbits/s NRZ and the data pattern = $2^{31} - 1$ PRBS. Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluation. Typical values are for information purposes only and are not part of the testing requirements.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Maximum Output Signal Amplitude	V_{AMP}	R_L = 50 Ω, V_{BIAS} = Vss	3.0	—	—	V
Maximum Output Signal Amplitude with dc Offset	V_{AMP}	R_L = 50 Ω, V Offset = –1.0 V	2.5	—	—	V
Minimum Output Signal Amplitude	V_{AMP}	R_L = 50 Ω, V_{BIAS} = Vss, V_{MOD} = Vss	—	—	1.5	V
Data Output High	$V_{DOUT, H}$	R_L = 50 Ω, V_{BIAS} = Vss	–600	—	0.0	mV
Output Offset Voltage Minimum†	V_{OFFSET}	R_L = 50 Ω, V_{BIAS} = V_{SS} + 2.0 V	—	—	–1.5	V
MOD Rise/Fall Time	T_R/T_F	20—80%; R_L = 50 Ω, V_{AMP} = 3.0 Vp-p, V_{BIAS} = Vss	—	—	35	ps
Maximum Pulse Width	PW	—	120	—	—	ps
Minimum Pulse Width	PW	—	—	—	80	ps
Pulse Width Control Input	PWP	80 ps pulse width for mark at V_{SS} + 1.0; 120 ps at V_{SS} + 2.0	V_{SS} + 1.0	—	V_{SS} + 2.0	V
Output Voltage Overshoot	V_{OSLOW} V_{OSHIGH}	V_{AMP} > 2.0 V	–10	—	+10	%
Phase Margin	—	—	—	TBD	—	Deg
Jitter (RMS)*	—	Clock enabled mode	—	—	3	ps
		Clock disabled mode	—	—	5	ps
Supply Current	I_{SS}	Output amp = 2.5 Vp-p Output offset = –1.0 V	—	—	300	mA

* $J_{RMS} = \sqrt{(J_{RMS, DUT})^2 - (J_{RMS, SYSTEM})^2}$

† See Figure 7.

Electrical Characteristics (continued)

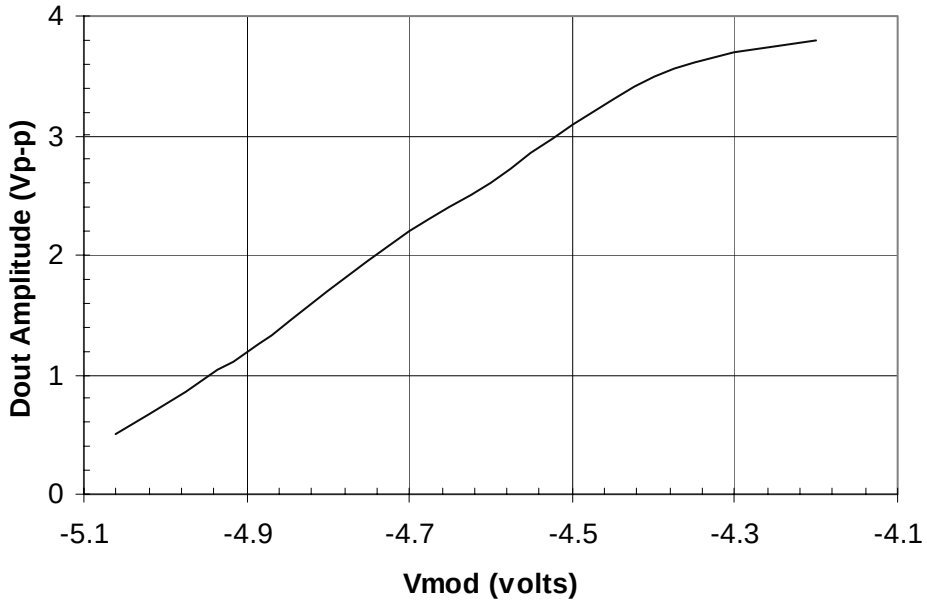


Figure 4. VMOD Vs. DOUT

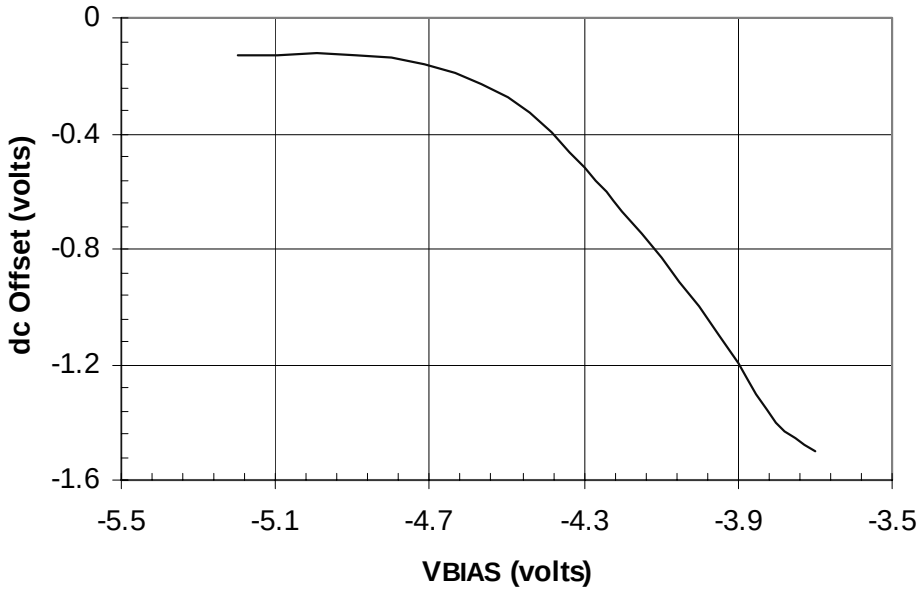


Figure 5. Offset Vs. VBIAS

Electrical Characteristics (continued)

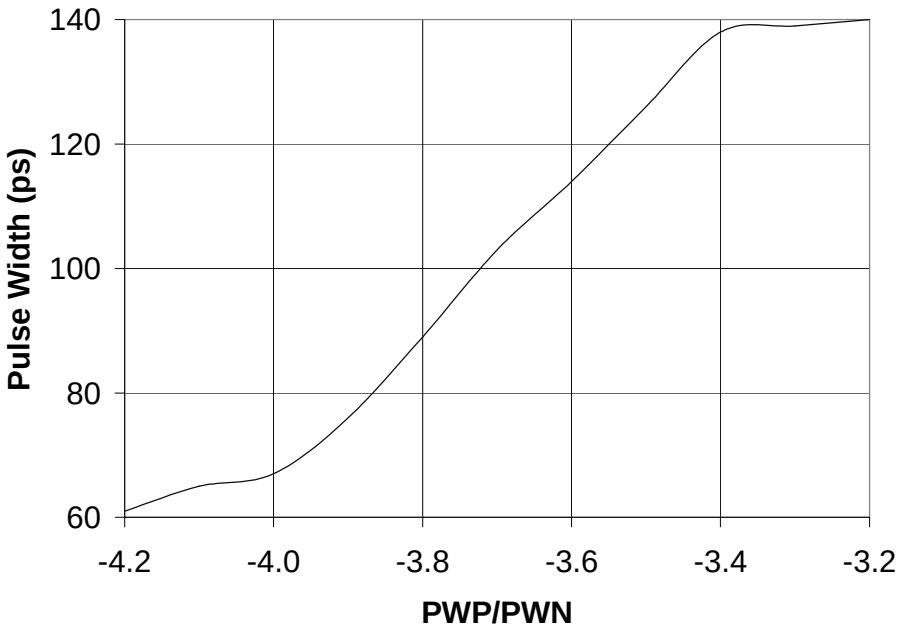


Figure 6. PWP/PWN Vs. Pulse Width

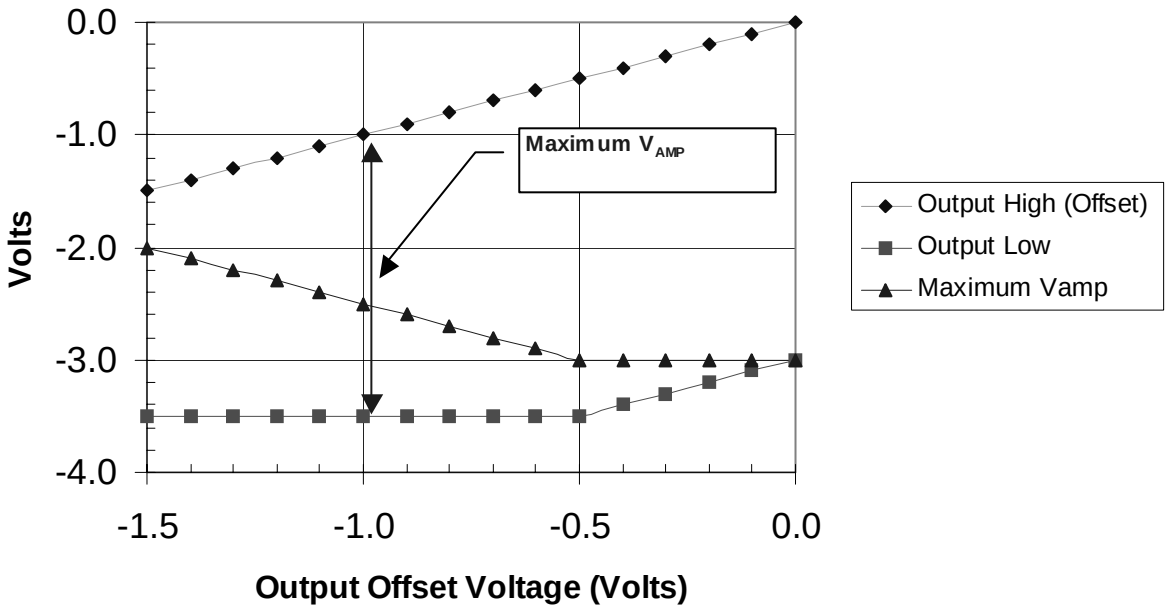
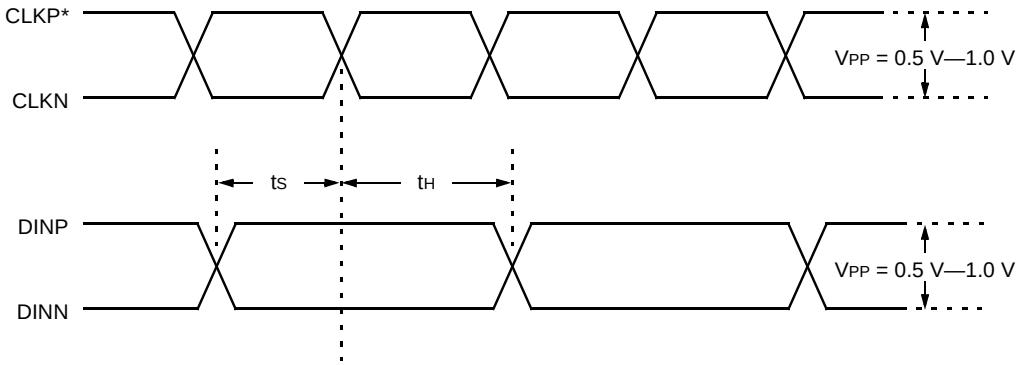


Figure 7. Available Output Amplitude as a Function of Offset Voltage

Timing Requirements



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* The active edge will be the rising edge of the CLKP

Figure 8. Input Data to Clock Setup and Hold Time

Chip Visual Inspection Criteria

At 100x the chips will be visually free of the following defects:

- Scratches in the metallization (including air-bridges) that leave less than 50% of the original width undisturbed and distort the outline of the metal feature.
- Voids or missing metallization that leave less than 50% of the original width undisturbed.
- Extra metals that bridge adjacent same-layer metal features. This includes bond pads damaged from probing.
- Cracks or chips out that extend into the active area of the device.
- Damaged air-bridges that have been distorted or torn off.
- Particles on the surface of the chip that are large enough to bridge between bond pads.
- Stains larger than the size of a bond pad.
- Lifted or blistered metallization.
- Missing nitride that occurs over or under an active feature.
- Defects to bond pad area:
  — Stains larger than 25% of bond pads.
  — Extra nitride on the bond pad that reduces the open area by more than 25%.
  — Probe damage that removes more than 25% of the bond pad.
  — Probe damage that causes cracks in the surrounding nitride substrate.

On Wafer Results

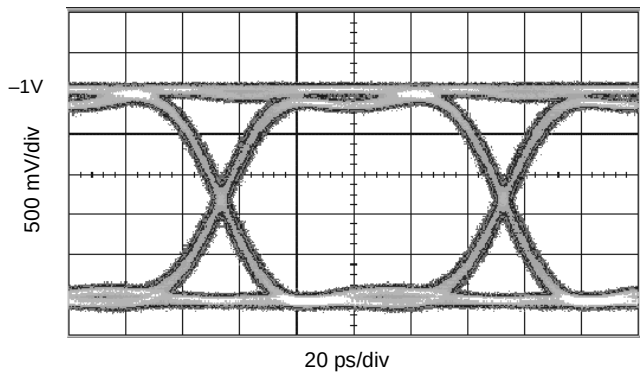


Figure 9. Electrical Eye Diagram of Clocked (CKSEL = –5.2 V) TCMD0110G Output with a –1 V Offset and 2.5 V Amplitude

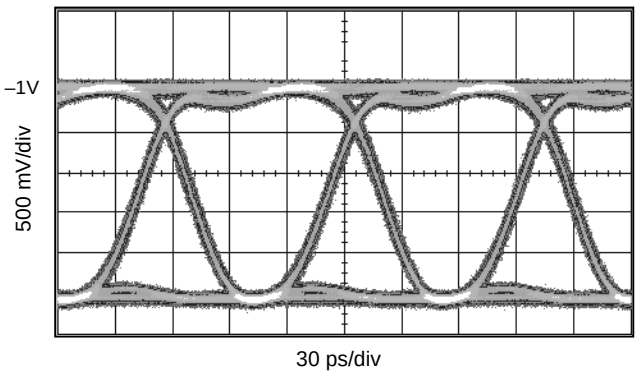


Figure 10. Electrical Eye Diagram with Pulse Adjusted for Greater than 120 ps Pulse Width (PWP = Vss + 2 V)

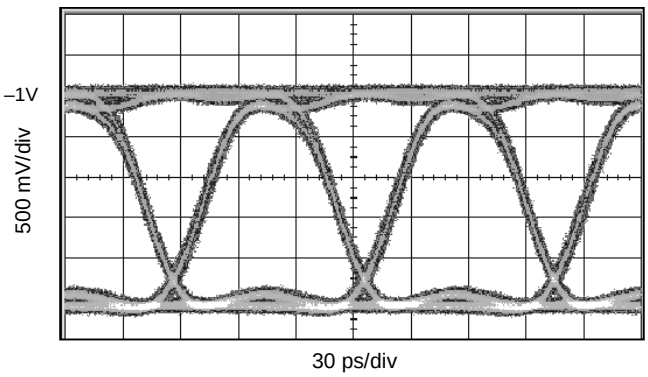


Figure 11. Electrical Eye Diagram with Pulse Width Adjusted for Less than 80 ps Pulse Width (PWP = Vss + 1 V)

Results of TCMD0110G Driving an Agere E2580 Type Electroabsorption Modulated Laser (EML)

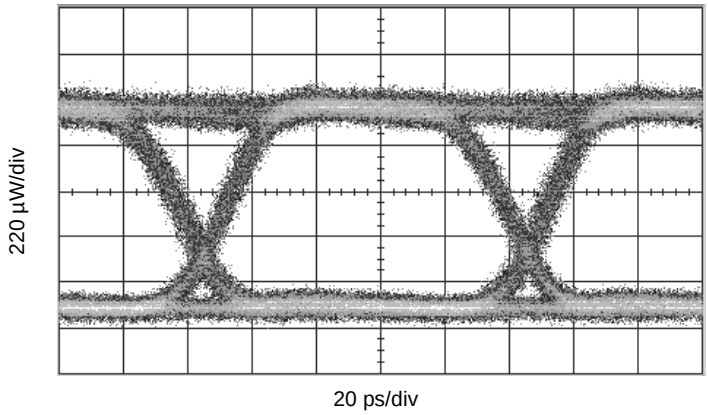


Figure 12. Optical Eye Diagram with 1.0 V Input to TCMD0110G

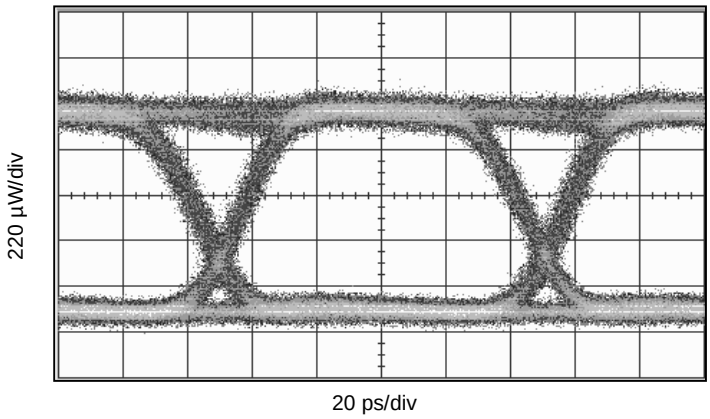


Figure 13. Optical Eye Diagram with 0.5 V Input to TCMD0110G

Agere Bonding Parameters

Parameters in Table 7 have been provided as a reference for die applications. They represent parameters used at Agere Systems and some or all may be process and bonder dependent. They are not intended to indicate universal settings that should be used for every process and/or bonder.

Table 7. Bonding Parameters Used at Agere Systems

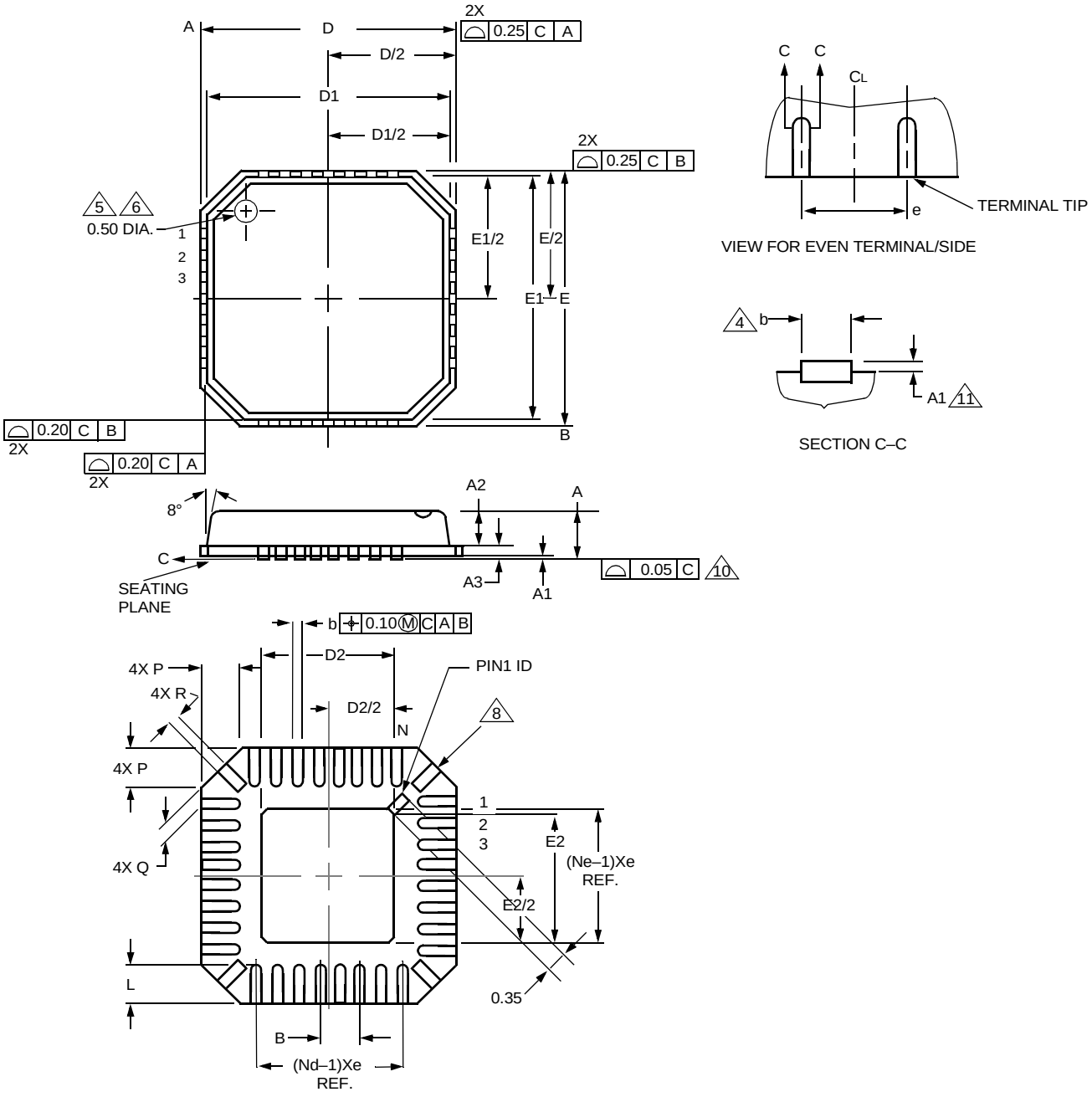
Parameter	Specifications
Wire bonder	ESEC 3018
Bondsite temperature	150 °C ± 10 °C
Bond wire	99.99% Gold, .001 in diameter, 3-6% elongation
Capillary	UTS-38EE-CM-1/16-XL (from SPT), hole size = 38 µm (1.5 mils), tip diameter = 130 µm (5.1 mils), chamfer diameter = 58 µm (2.3 mils)
Ball bond parameters	Force = 450 mN, US time = 12 ms, US power = 20%
Wedge bond parameters	Force = 550 mN, US time = 15 ms, US power = 25%
EFO parameters	FAB size = 60 µm (1.3 ms spark time, 34.04 uA current)
Wire pull strength	Range = 7.0—12.0 gf, Agere spec = min 5.0 gf
Ball sheer	Range = 45—65 gf, Agere spec = 35 gf

Mounting and Connections

The TCMD0110G package is a 32-pin *Micro*LeadFrame™ (MLF) package. The package is a near CSP (chip scale package) plastic encapsulated with a copper leadframe substrate. This package is leadless and electrical contacts are made by soldering lands on the bottom surface to the printed-circuit board (PCB). Since the package does not include traditional formed gull-wing leads, a soldering iron cannot be used to solder the package to the PCB. Instead, solder paste must be printed onto the PCB and then reflowed after component placement. The temperature during solder re-flow should not exceed 220 °C and the time above liquids should be less than 75 seconds. There is a die attach paddle on the bottom that facilitates heat dissipation from the die to the PCB. For effective heat conduction, the PCB must have features to effectively conduct heat away from the package. This can be achieved by incorporating a thermal pad and thermal vias on the PCB. While a thermal pad will provide a solderable surface on the top of the PCB for better grounding, thermal vias are needed to provide a thermal path to inner and/or bottom layers of the PCB to remove the heat. Heat could further be transferred into the module case by including a thermal pad on the opposite side of the PCB, directly under the device, and building a pedestal into the case to make contact with the thermal pad. The die attached paddle is at ground potential.

Package Dimensions

32- Pin MLF Package



Package Dimensions (continued)

Table 8. Package Dimensions (in mm)

Symbol	Dimensions			Note
	Min	Nom	Max	
A	—	0.85	1	—
A1	0.00	0.01	0.05	1
A2	—	0.65	0.8	—
A3	0.20 REF.			—
D	5.00 BSC			4
D1	4.75 BSC			4
E	5.00 BSC			4
E1	4.75 BSC			4
q			12°	—
P	0.24	0.42	0.6	—
R	0.13	0.17	0.23	—
e	0.50 BSC			—
N	32			2
Nd	8			2
Ne	8			2
L	0.30	0.40	0.50	—
B	0.18	0.23	0.30	3
Q	0.00	0.20	0.45	—
D2	2.95	3.10	3.25	—
E2	2.95	3.10	3.25	—

Notes:
1. Applied only for terminals.
2. N is the number of terminals.
   Nd is the number of terminals in x-direction.
   Ne is the number of terminals in y-direction.
3. Dimension b applies to plated terminal snd is measured between 0.20 mm and 0.25 mm from terminal tip.
4. BSC is a basic dimension without tolerance.

*Micro*LeadFrame is a trademark of Amkor Technology, Inc.

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