



74LCX16245A

LOW VOLTAGE CMOS 16-BIT BUS TRANSCEIVER (3-STATE) WITH 5V TOLERANT INPUTS AND OUTPUTS

- 5V TOLERANT INPUTS AND OUTPUTS
- HIGH SPEED:
 $t_{PD} = 5.2 \text{ ns (MAX.) at } V_{CC} = 3.0\text{V}$
- POWER-DOWN PROTECTION ON INPUTS AND OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 24 \text{ mA (MIN)}$
- PCI BUS LEVELS GUARANTEED AT 24mA
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
 $V_{CC} \text{ (OPR)} = 2.0\text{V to } 3.6\text{V (1.5V Data Retention)}$
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 16245
- LATCH-UP PERFORMANCE EXCEEDS 500mA
- ESD PERFORMANCE:
 $\text{HBM} > 2000\text{V}; \text{MM} > 200\text{V}$

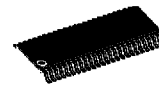
DESCRIPTION

The LCX16245A is a low voltage CMOS 16-BIT BUS TRANSCEIVER (3-STATE) fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology. It is ideal for low power and high speed 3.3V applications; it can be interfaced to 5V signal environment for both inputs and outputs.

This IC is intended for two-way asynchronous communication between data buses; the direction of data transmission is determined by DIR input. The two enable inputs \overline{nG} can be used to disable the device so that the buses are effectively isolated. It has better speed performance at 3.3V than 5V LSTTL family combined with the true CMOS low power consumption.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

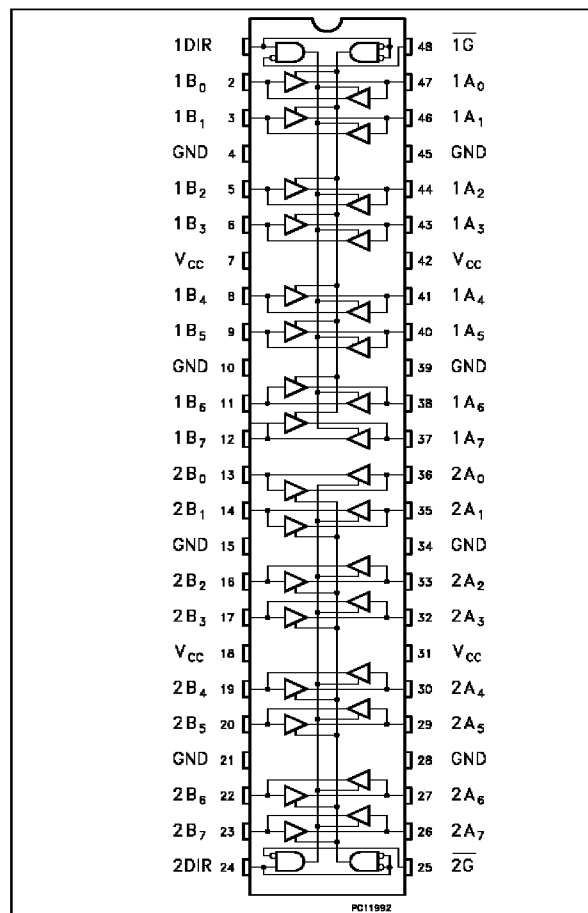
IT IS PROHIBITED TO APPLY A SIGNAL TO A TERMINAL WHEN IT IS IN OUTPUT MODE AND WHEN A BUS TERMINAL IS FLOATING (HIGH IMPEDANCE STATE) IT IS REQUESTED TO FIX THE INPUT LEVEL BY MEANS OF EXTERNAL PULL DOWN OR PULL UP RESISTOR.



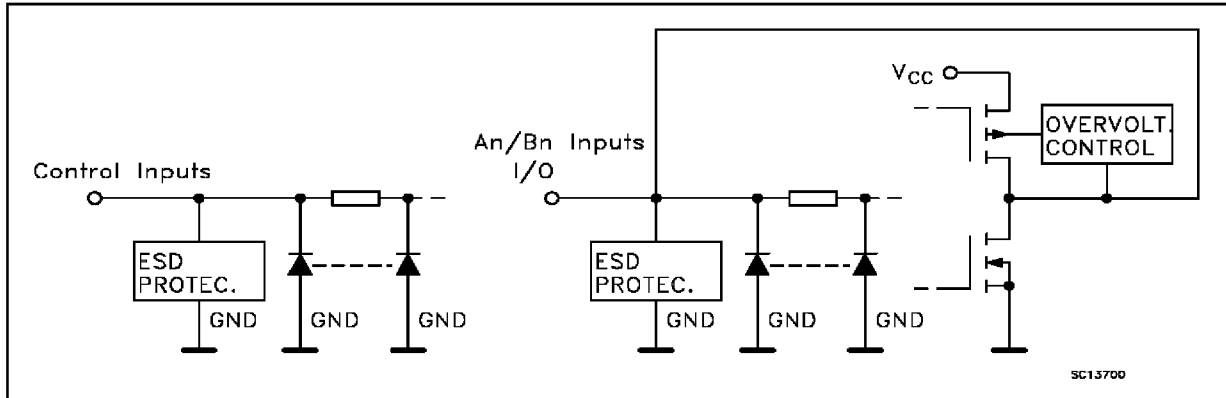
T
(TSSOP48 Package)

ORDER CODES :
74LCX16245AT

PIN CONNECTION



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

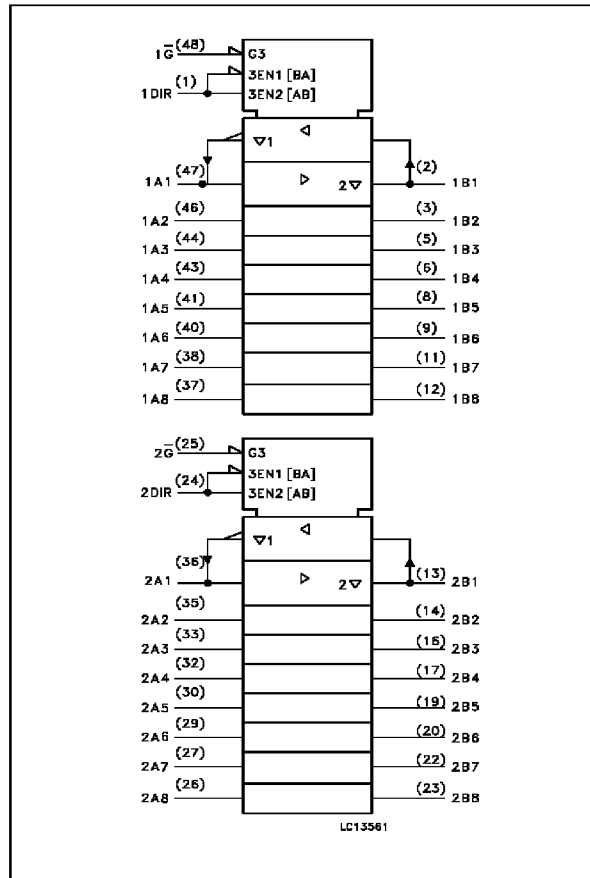
PIN No	SYMBOL	NAME AND FUNCTION
1	1DIR	Directional Control
2, 3, 5, 6, 8, 9, 11, 12	1B0 to 1B8	Data Inputs/Outputs
13, 14, 16, 17, 19, 20, 22, 23	2B0 to 2B8	Data Inputs/Outputs
24	2DIR	Directional Control
25	$\overline{2G}$	Output Enable Input
36, 35, 33, 32, 30, 29, 27, 26	2A0 to 2A8	Data Inputs/Outputs
47, 46, 44, 43, 41, 40, 38, 37	1A0 to 1A8	Data Inputs/Outputs
48	$\overline{1G}$	Output Enable Input
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V _{CC}	Positive Supply Voltage

TRUTH TABLE

INPUT		FUNCTION		OUTPUT
\overline{G}	DIR	A BUS	B BUS	
L	L	OUTPUT	INPUT	A = B
L	H	INPUT	OUTPUT	B = A
H	X	Z	Z	Z

X: "H" or "L"
Z: High impedance

IEC LOGIC SYMBOLS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to + 7.0	V
V_I	DC Input Voltage (DIR, \overline{G})	-0.5 to + 7.0	V
$V_{I/O}$	Bus I/O Voltage (OFF state)	-0.5 to + 7.0	V
$V_{I/O}$	Bus I/O Voltage (High or Low State) (note1)	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	- 50	mA
I_{OK}	DC Output Diode Current (note2)	± 50	mA
I_O	DC Output Source/Sink Current	± 50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current Per Supply Pin	± 100	mA
T_{stg}	Storage Temperature	-65 to +150	$^{\circ}C$
T_L	Lead Temperature (10 sec)	300	$^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

1) I_O absolute maximum rating must be observed

2) $V_O < GND$, $V_O > V_{CC}$

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	2.0 to 3.6	V
V_I	Input Voltage (DIR, \overline{G})	0 to 5.5	V
$V_{I/O}$	Bus I/O Voltage (OFF state)	0 to 5.5	V
$V_{I/O}$	Bus I/O Voltage (High or Low State)	0 to V_{CC}	V
I_{OH} , I_{OL}	High or Low Level Output Current ($V_{CC} = 3.0$ to $3.6V$)	± 24	mA
I_{OH} , I_{OL}	High or Low Level Output Current ($V_{CC} = 2.7$ to $3.0V$)	± 12	mA
T_{op}	Operating Temperature:	-40 to +85	$^{\circ}C$
dt/dv	Input Transition Rise or Fall Rate ($V_{CC} = 3.0V$) (note 2)	0 to 10	ns/V

1) Truth Table guaranteed: 1.5V to 3.6V

2) V_{IN} from 0.8V to 2.0V

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions		Value		Unit
		V _{CC} (V)		-40 to 85 °C		
				Min.	Max.	
V _{IH}	High Level Input Voltage	2.7 to 3.6		2.0		V
V _{IL}	Low Level Input Voltage				0.8	V
V _{OH}	High Level Output Voltage	2.7 to 3.6	V _I = V _{IH} or V _{IL}	I _O = -100 μA	V _{CC} - 0.2	V
		2.7		I _O = -12 mA	2.2	
		3.0		I _O = -18 mA	2.4	
				I _O = -24 mA	2.2	
V _{OL}	Low Level Output Voltage	2.7 to 3.6	V _I = V _{IH} or V _{IL}	I _O = 100 μA	0.2	V
		2.7		I _O = 12 mA	0.4	
		3.0		I _O = 16 mA	0.4	
		3.0		I _O = 24 mA	0.55	
I _I	Input Leakage Current	2.7 to 3.6	V _I = 0 to 5.5 V		±5	μA
I _{OZ}	3 State Output Leakage Current	2.7 to 3.6	V _I = V _{IH} or V _{IL} V _O = 0 to 5.5 V		±5	μA
I _{off}	Power Off Leakage Current	0	V _I or V _O = 5.5 V (per pin)		10	μA
I _{CC}	Quiescent Supply Current	2.7 to 3.6	V _I = V _{CC} or GND		20	μA
			V _I or V _O = 3.6 to 5.5 V		±20	
ΔI _{CC}	ICC incr. per input	2.7 to 3.6	V _{IH} = V _{CC} - 0.6 V		500	μA

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Conditions		Value			Unit
		V _{CC} (V)		T _A = 25 °C			
				Min.	Typ.	Max.	
V _{OLP}	Dynamic Low Voltage Quiet Output (note 1)	3.3	C _L = 50 pF V _{IL} = 0 V V _{IH} = 3.3 V		0.8		V
V _{OLV}					-0.8		

1) Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH to LOW or LOW to HIGH. The remaining output is measured in the LOW state.



AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, $R_L = 500 \Omega$, Input $t_r = t_f = 2.5 \text{ ns}$)

Symbol	Parameter	Test Condition		Value		Unit
		V _{CC} (V)	Waveform	-40 to 85 °C		
				Min.	Max.	
t _{PLH} t _{PHL}	Propagation Delay Time	2.7	1	1.5	6.2	ns
		3.0 to 3.6		1.5	5.2	
t _{PZL} t _{PZH}	Output Enable Time	2.7	2	1.5	7.5	ns
		3.0 to 3.6		1.5	6.5	
t _{PLZ} t _{PHZ}	Output Disable Time	2.7	2	1.5	7.0	ns
		3.0 to 3.6		1.5	6.0	
t _{OSLH} t _{OSHL}	Output to Output Skew Time (note 1, 2)	3.0 to 3.6			1.0	ns

1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW ($t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$)

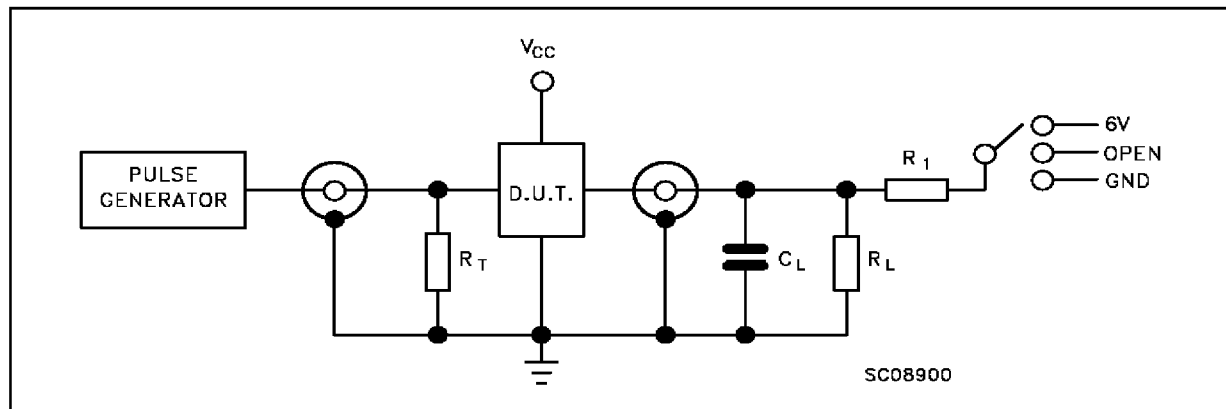
2) Parameter guaranteed by design

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions		Value			Unit
		V _{CC} (V)		T _A = 25 °C			
				Min.	Typ.	Max.	
C _{IN}	Input Capacitance	3.3	V _{IN} = 0 to V _{CC}		7		pF
C _{IO}	I/O Capacitance	3.3	V _{IN} = 0 to V _{CC}		8		pF
C _{PD}	Power Dissipation Capacitance (note 1)	3.3	f _{IN} = 10MHz V _{IN} = 0 or V _{CC}		20		pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the following equation. $I_{CC(oper)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/16$ (per circuit)

TEST CIRCUIT



TEST	SWITCH
t _{PLH} , t _{PHL}	Open
t _{PZL} , t _{PLZ}	6V
t _{PZH} , t _{PHZ}	GND

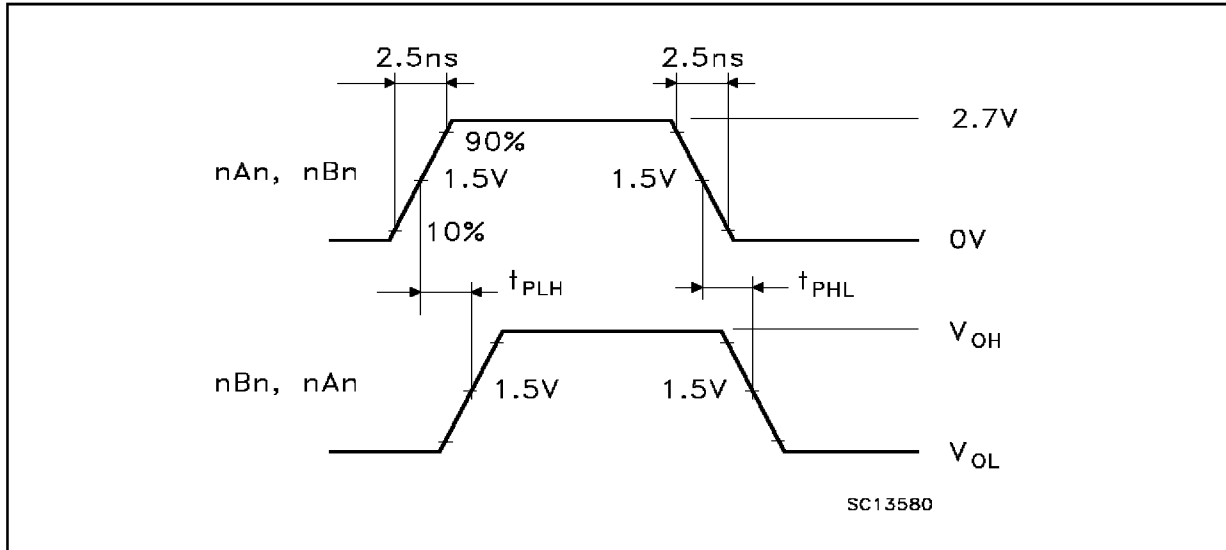
C_L = 50 pF or equivalent (includes jig and probe capacitance)

R_L = R₁ = 500Ω or equivalent

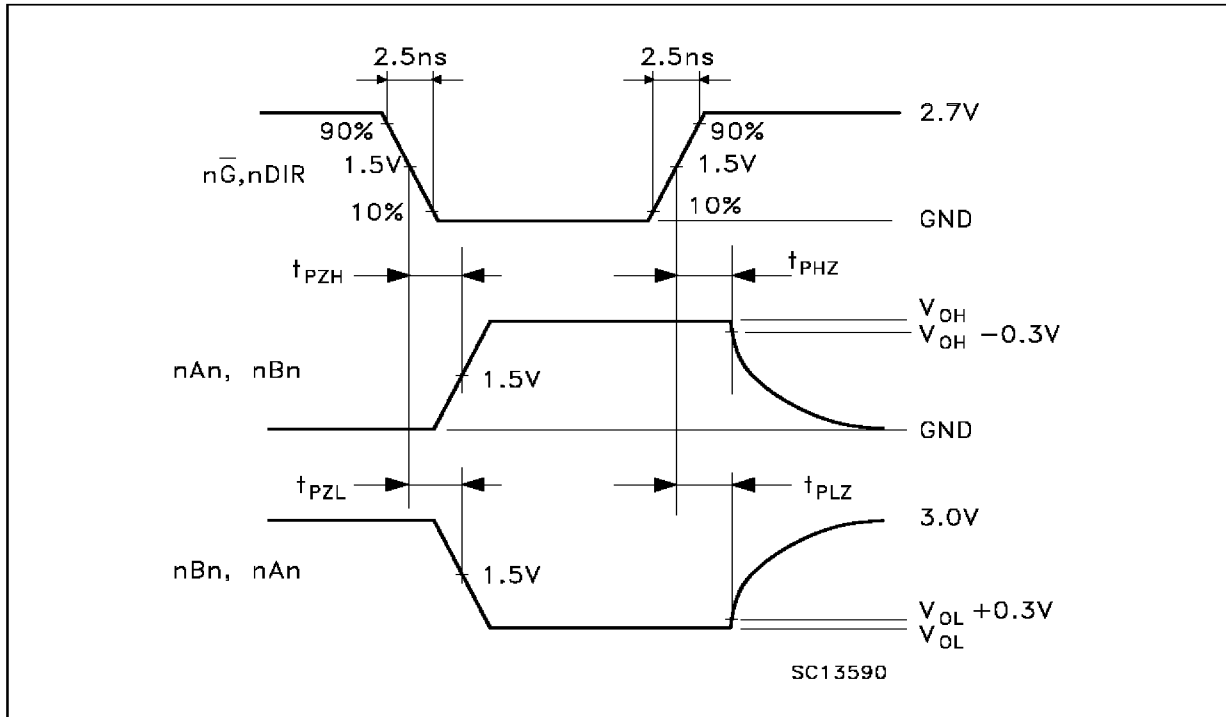
R_T = Z_{OUT} of pulse generator (typically 50Ω)



WAVEFORM 1: PROPAGATION DELAYS (f=1MHz; 50% duty cycle)



WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIME (f=1MHz; 50% duty cycle)



TSSOP48 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.433
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.85	0.9	0.95	0.335	0.354	0.374
b	0.17		0.27	0.0067		0.011
c	0.09		0.20	0.0035		0.0079
D	12.4	12.5	12.6	0.408	0.492	0.496
E	7.95	8.1	8.25	0.313	0.319	0.325
E1	6.0	6.1	6.2	0.236	0.240	0.244
e		0.5 BSC			0.0197 BSC	
K	0°	4°	8°	0°	4°	8°
L	0.50	0.60	0.70	0.020	0.024	0.028

