



## 3.3V CMOS 20-BIT BUFFER/ DRIVER WITH 3-STATE OUTPUTS AND BUS-HOLD

**IDT74ALVCH162827**

### FEATURES:

- 0.5 MICRON CMOS Technology
- Typical  $t_{sk(o)}$  (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{CC} = 3.3V \pm 0.3V$ , Normal Range
- $V_{CC} = 2.7V$  to  $3.6V$ , Extended Range
- $V_{CC} = 2.5V \pm 0.2V$
- CMOS power levels ( $0.4\mu W$  typ. static)
- Rail-to-Rail output swing for increased noise margin
- Available in SSOP, TSSOP, and TVSOP packages

### DRIVE FEATURES:

- Balanced Output Drivers:  $\pm 12mA$
- Low switching noise

### APPLICATIONS:

- 3.3V high speed systems
- 3.3V and lower voltage computing systems

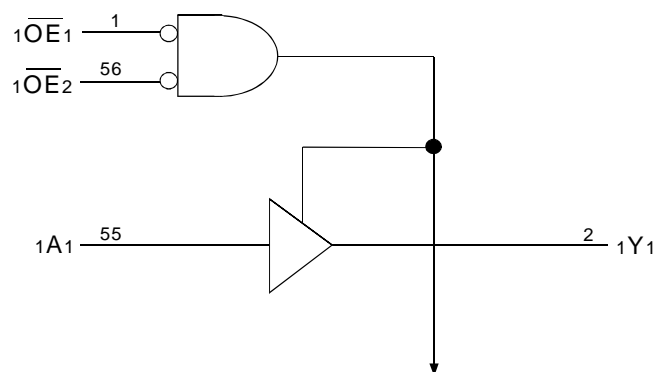
### DESCRIPTION:

This 20-bit buffer/driver is built using advanced dual metal CMOS technology. The ALVCH162827 device provides high-performance bus interface buffering for wide data/address paths or busses carrying parity. Two pairs of NAND-ed output enable controls offer maximum control flexibility and are organized to operate the device as two 10-bit buffers or one 20-bit buffer. Flow-through organization of signal pins facilitates ease of layout. All inputs are designed with hysteresis for improved noise margin.

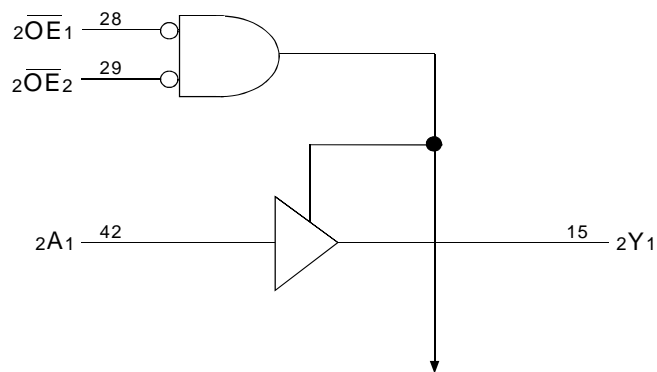
The ALVCH162827 has series resistors in the device output structure which will significantly reduce line noise when used with light loads. This driver has been designed to drive  $\pm 12mA$  at the designated threshold levels.

The ALVCH162827 has "bus-hold" which retains the inputs' last state whenever the input bus goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

## FUNCTIONAL BLOCK DIAGRAM

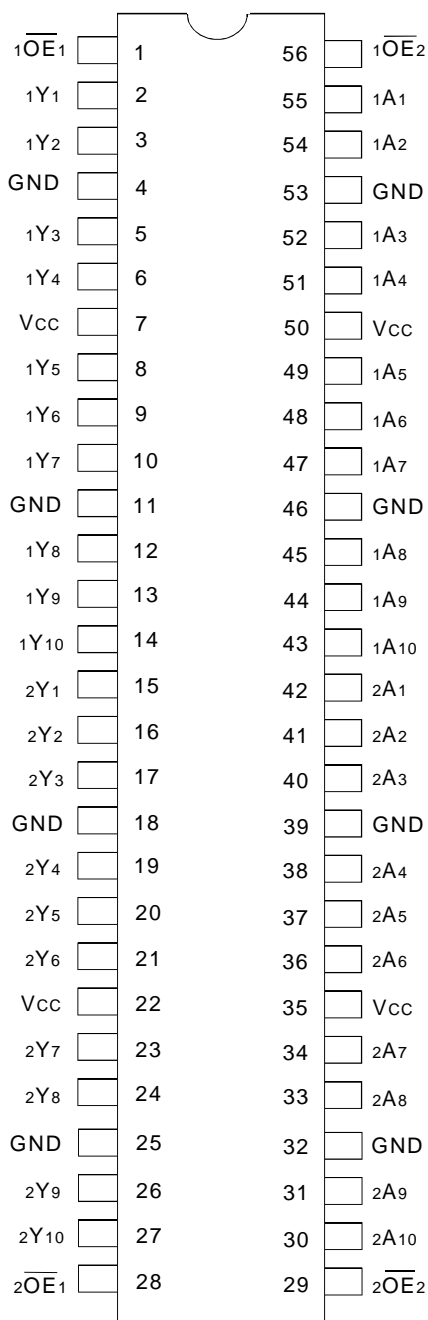


TO NINE OTHER CHANNELS



TO NINE OTHER CHANNELS

## PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
VTERM <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to VCC+0.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-50 to +50	mA
I <sub>IK</sub>	Continuous Clamp Current, V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub>	±50	mA
I <sub>OK</sub>	Continuous Clamp Current, V <sub>O</sub> < 0	-50	mA
I <sub>CC</sub> I <sub>SS</sub>	Continuous Current through each V <sub>CC</sub> or GND	±100	mA

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>CC</sub> terminals.
- All terminals except V<sub>CC</sub>.

## CAPACITANCE (T<sub>A</sub> = +25°C, F = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	5	7	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	7	9	pF
C <sub>OUT</sub>	I/O Port Capacitance	V <sub>IN</sub> = 0V	7	9	pF

### NOTE:

- As applicable to the device type.

## PIN DESCRIPTION

Pin Names	Description
$\overline{xOE}x$	Output Enable Inputs (Active LOW)
$xAx$	Data Inputs <sup>(1)</sup>
$xYx$	3-State Outputs

### NOTE:

- These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

## FUNCTION TABLE (EACH 10-BIT SECTION)<sup>(1)</sup>

Inputs			Output
$\overline{xOE}1$	$\overline{xOE}2$	$xAx$	$xYx$
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

### NOTE:

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
Z = High Impedance

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. <sup>(1)</sup>	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage Level	V <sub>CC</sub> = 2.3V to 2.7V		1.7	—	—	V
		V <sub>CC</sub> = 2.7V to 3.6V		2	—	—	
V <sub>IL</sub>	Input LOW Voltage Level	V <sub>CC</sub> = 2.3V to 2.7V		—	—	0.7	V
		V <sub>CC</sub> = 2.7V to 3.6V		—	—	0.8	
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = 3.6V	V <sub>I</sub> = V <sub>CC</sub>	—	—	±5	μA
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = 3.6V	V <sub>I</sub> = GND	—	—	±5	μA
I <sub>OZH</sub> I <sub>OZL</sub>	High Impedance Output Current (3-State Output pins)	V <sub>CC</sub> = 3.6V	V <sub>O</sub> = V <sub>CC</sub>	—	—	±10	μA
			V <sub>O</sub> = GND	—	—	±10	
V <sub>IK</sub>	Clamp Diode Voltage	V <sub>CC</sub> = 2.3V, I <sub>IN</sub> = -18mA		—	-0.7	-1.2	V
V <sub>H</sub>	Input Hysteresis	V <sub>CC</sub> = 3.3V		—	100	—	mV
I <sub>CC1</sub> I <sub>CC2</sub> I <sub>CC3</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = 3.6V V <sub>IN</sub> = GND or V <sub>CC</sub>		—	0.1	40	μA
ΔI <sub>CC</sub>	Quiescent Power Supply Current Variation	One input at V <sub>CC</sub> - 0.6V, other inputs at V <sub>CC</sub> or GND		—	—	750	μA

**NOTE:**

1. Typical values are at V<sub>CC</sub> = 3.3V, +25°C ambient.

## BUS-HOLD CHARACTERISTICS

Symbol	Parameter <sup>(1)</sup>	Test Conditions		Min.	Typ. <sup>(2)</sup>	Max.	Unit
I <sub>BHH</sub> I <sub>BHL</sub>	Bus-Hold Input Sustain Current	V <sub>CC</sub> = 3V	V <sub>I</sub> = 2V	-75	—	—	μA
			V <sub>I</sub> = 0.8V	75	—	—	
I <sub>BHH</sub> I <sub>BHL</sub>	Bus-Hold Input Sustain Current	V <sub>CC</sub> = 2.3V	V <sub>I</sub> = 1.7V	-45	—	—	μA
			V <sub>I</sub> = 0.7V	45	—	—	
I <sub>BHHO</sub> I <sub>BHLO</sub>	Bus-Hold Input Overdrive Current	V <sub>CC</sub> = 3.6V	V <sub>I</sub> = 0 to 3.6V	—	—	±500	μA

**NOTES:**

1. Pins with Bus-Hold are identified in the pin description.
2. Typical values are at V<sub>CC</sub> = 3.3V, +25°C ambient.

## OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	IOH = - 0.1mA	VCC - 0.2	—	V
		VCC = 2.3V	IOH = - 4mA	1.9	—	
			IOH = - 6mA	1.7	—	
		VCC = 2.7V	IOH = - 4mA	2.2	—	
			IOH = - 8mA	2	—	
		VCC = 3V	IOH = - 6mA	2.4	—	
IOH = - 12mA	2		—			
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	IOL = 0.1mA	—	0.2	V
		VCC = 2.3V	IOL = 4mA	—	0.4	
			IOL = 6mA	—	0.55	
		VCC = 2.7V	IOL = 4mA	—	0.4	
			IOL = 8mA	—	0.6	
		VCC = 3V	IOL = 6mA	—	0.55	
IOL = 12mA	—		0.8			

- NOTE:**  
 1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range. TA = - 40°C to + 85°C.

## OPERATING CHARACTERISTICS, TA = 25°C

Symbol	Parameter	Test Conditions	VCC = 2.5V ± 0.2V	VCC = 3.3V ± 0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance Outputs enabled	CL = 0pF, f = 10Mhz	16	18	pF
CPD	Power Dissipation Capacitance Outputs disabled		4	6	

SWITCHING CHARACTERISTICS<sup>(1)</sup>

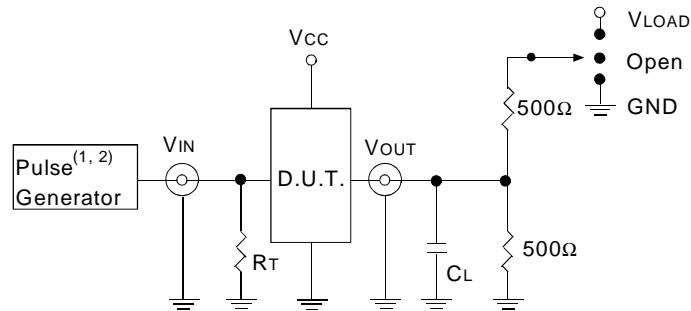
Symbol	Parameter	VCC = 2.5V ± 0.2V		VCC = 2.7V		VCC = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
tPLH	Propagation Delay	1	4.4	—	4.4	1.5	3.8	ns
tPHL	xAx to xYx							
tPZH	Output Enable Time	1.4	6.3	—	6.2	1.6	5.1	ns
tPZL	$\overline{xOEx}$ to xYx							
tPHZ	Output Disable Time	1.7	5.9	—	5.2	1.8	4.7	ns
tPLZ	$\overline{xOEx}$ to xYx							
tSK(O)	Output Skew <sup>(2)</sup>	—	—	—	—	—	500	ps

- NOTES:**  
 1. See TEST CIRCUITS AND WAVEFORMS. TA = - 40°C to + 85°C.  
 2. Skew between any two outputs of the same package and switching in the same direction.

## TEST CIRCUITS AND WAVEFORMS

### TEST CONDITIONS

Symbol	V <sub>CC</sub> <sup>(1)</sup> = 3.3V ± 0.3V	V <sub>CC</sub> <sup>(1)</sup> = 2.7V	V <sub>CC</sub> <sup>(2)</sup> = 2.5V ± 0.2V	Unit
V <sub>LOAD</sub>	6	6	2 x V <sub>CC</sub>	V
V <sub>IH</sub>	2.7	2.7	V <sub>CC</sub>	V
V <sub>T</sub>	1.5	1.5	V <sub>CC</sub> / 2	V
V <sub>LZ</sub>	300	300	150	mV
V <sub>HZ</sub>	300	300	150	mV
C <sub>L</sub>	50	50	30	pF



Test Circuit for All Outputs

#### DEFINITIONS:

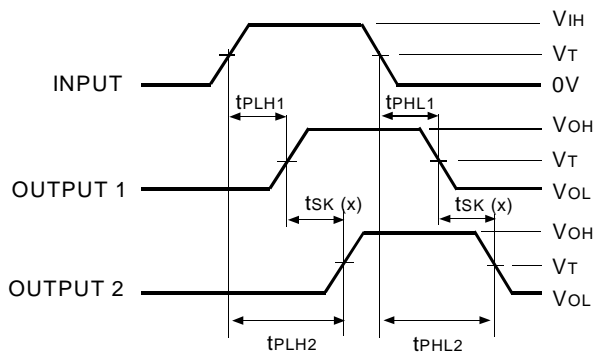
C<sub>L</sub> = Load capacitance: includes jig and probe capacitance.  
R<sub>T</sub> = Termination resistance: should be equal to Z<sub>OUT</sub> of the Pulse Generator.

#### NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t<sub>r</sub> ≤ 2.5ns; t<sub>r</sub> ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t<sub>r</sub> ≤ 2ns; t<sub>r</sub> ≤ 2ns.

### SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V <sub>LOAD</sub>
Disable High Enable High	GND
All Other Tests	Open

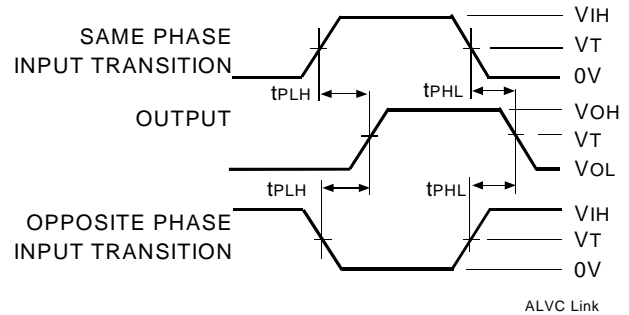


$$tsk(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

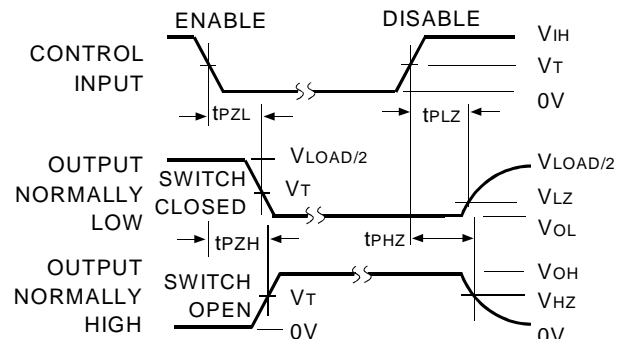
Output Skew - tsk(x)

#### NOTES:

1. For tsk(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For tsk(b) OUTPUT1 and OUTPUT2 are in the same bank.



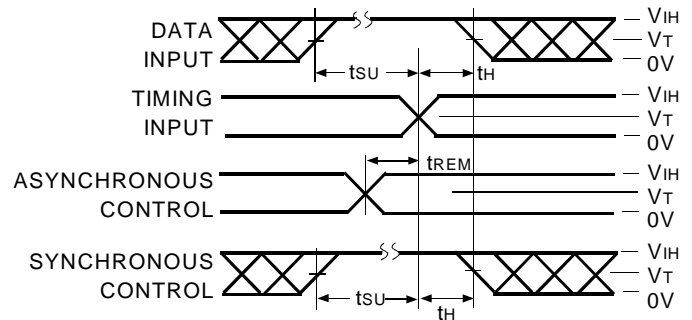
Propagation Delay



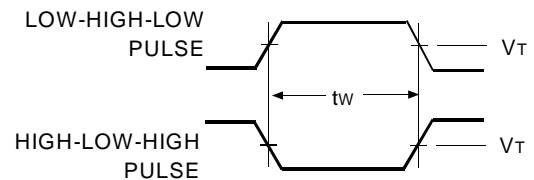
Enable and Disable Times

#### NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

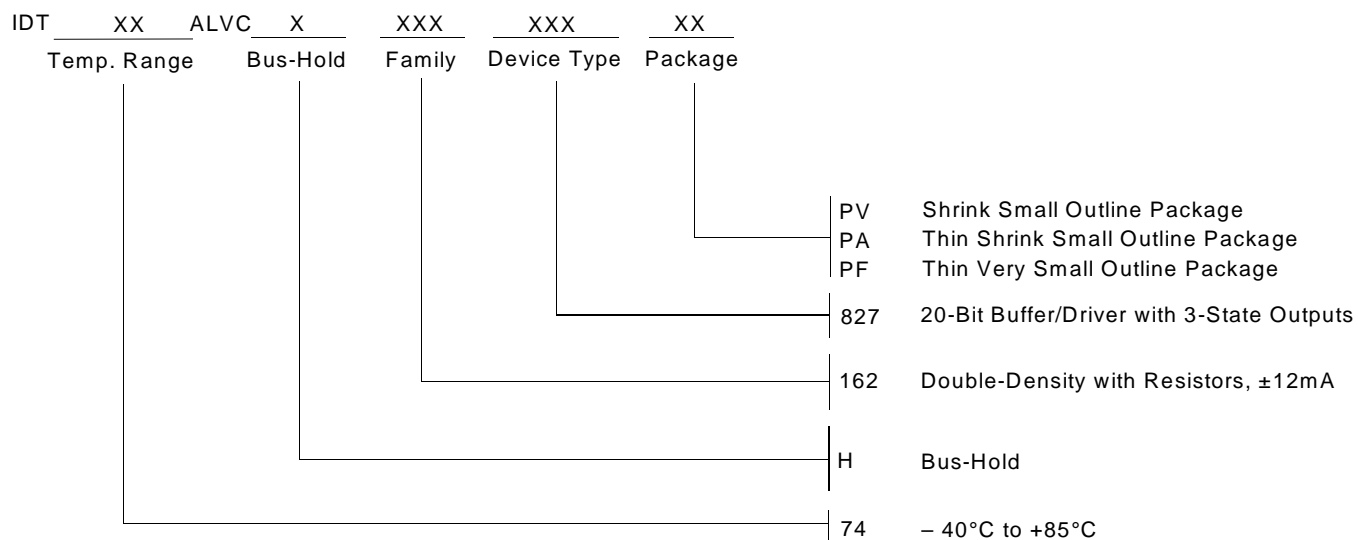


Set-up, Hold, and Release Times



Pulse Width

## ORDERING INFORMATION



**CORPORATE HEADQUARTERS**  
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