SIEMENS

Mini IOM-2 Controller
MICO
PEF 2015 Version 1.1

Addendum 03.98 to the Data Sheet 12.97

Bus Interface Timing

For proper operation of the MICO the timings in figures 19a and 20 (Data Sheet 12.97) are depicted more detailed concerning the $\overline{RD}$, $\overline{WR}$, $\overline{CS}$ signals (Siemens/Intel mode) and the R/$\overline{W}$, $\overline{DS}$ signals (Motorola mode), respectively.

Between two read (write) accesses in Intel mode the according control signal $\overline{RD}$ ($\overline{WR}$) has to be deactivated. Thus a read/write cycle control by only asserting and deasserting $\overline{CS}$ is not possible.

The same applies to the $\overline{DS}$ signal in Motorola mode.

Bus Interface Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
R or $\overline{W}$ set-up to $\overline{DS}$	t_{DSD}	0		ns
R or $\overline{W}$ hold time from $\overline{DS}$	t_{RWh}		10	ns
$\overline{RD}$-pulse width	t_{RR}	80		ns
$\overline{RD}$-control interval	t_{RI}	40		ns
Data output delay from $\overline{RD}$**x$\overline{CS}$**,$\overline{DS}$**x$\overline{CS}$**	t_{RD}		80	ns
Data float delay from $\overline{RD}$**x$\overline{CS}$**, $\overline{DS}$**x$\overline{CS}$**	t_{DF}		25	ns
$\overline{WR}$-pulse width	t_{WW}	45		ns
$\overline{WR}$-control interval	t_{WI}	40		ns
Data set-up time to $\overline{WR}$x$\overline{CS}$, $\overline{DS}$x$\overline{CS}$	t_{DW}	0		ns
Data hold time from $\overline{WR}$x$\overline{CS}$, $\overline{DS}$x$\overline{CS}$	t_{WD}	15		ns

Revision History: Previous Version:
Major Changes:

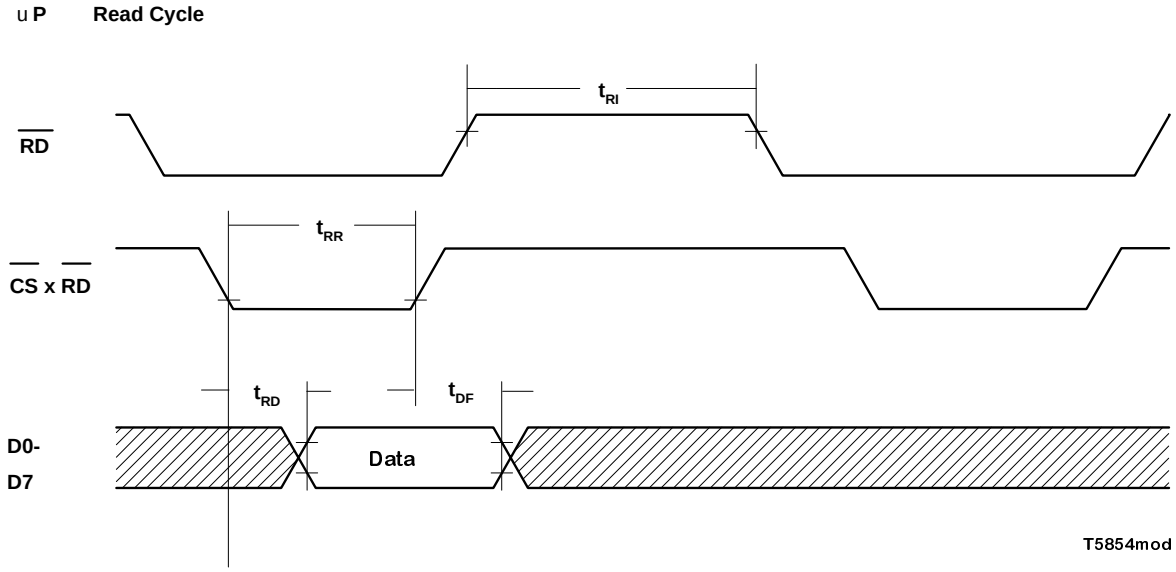

Figure 1 Siemens/Intel Bus Mode

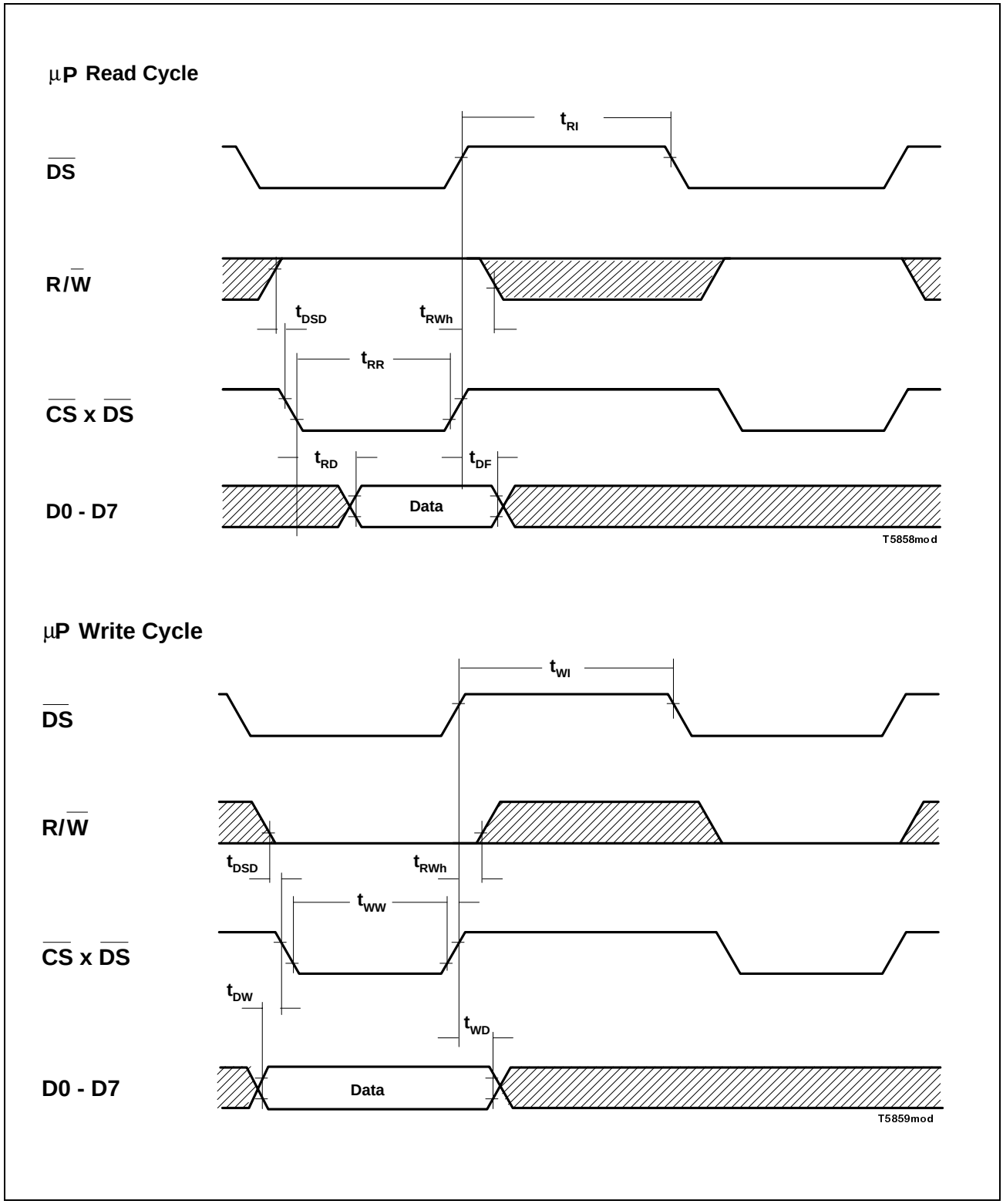

Figure 2 Motorola Mode