Low Power, Low Noise and Distortion, Rail-to-Rail Output Amplifier

ADA4841-1

FEATURES

Low power: 1.1 mA supply current
Low wideband noise
- **2 nV/√Hz**
- **1.4 pA/√Hz**

Low 1/F noise
- **6 nV/√Hz @ 10 Hz**
- **13 pA/√Hz @ 10 Hz**

Low distortion
- **−111 dBc @ 100 kHz, V_O = 2 V p-p**

High speed
- **80 MHz, −3 dB bandwidth (G = +1)**
- **12 V/μs slew rate**
- **175 ns settling time to 0.1%**

Low offset voltage 0.29 mV max
Rail-to-rail output
Power down
Wide supply range: 2.7 V to 12 V

APPLICATIONS

Low power, low noise signal processing
Battery-powered instrumentation
16-bit PulSAR® ADC drivers

CONNECTION DIAGRAM (TOP VIEW)

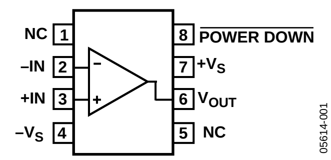

Figure 1. 8-Lead SOIC (R)

GENERAL DESCRIPTION

The ADA4841-1 is a unity gain stable, low noise and distortion, rail-to-rail output amplifier that has a quiescent current of 1.4 mA maximum. Despite its low power consumption, this amplifier offers low wideband voltage noise performance of 2 nV/√Hz and 1.4 pA/√Hz current noise, along with excellent spurious-free dynamic range (SFDR) of −110 dBc at 100 kHz. To maintain a low noise environment at lower frequencies, the amplifier has low 1/F noise of 6 nV/√Hz and 13 pA/√Hz at 10 Hz.

The ADA4841-1 has a wide supply voltage range from 2.7 V to 12 V and an output that swings within less than 100 mV of either rail. The input common-mode voltage range extends down to the negative supply. The ADA4841-1 can drive up to 20 pF of capacitive load with minimal peaking.

The ADA4841-1 provides the performance required to efficiently support emerging 16-bit to 18-bit ADCs and is ideal for portable instrumentation, high channel count, industrial measurement, and medical applications. The ADA4841-1 is an ideal match for driving Analog Devices, Inc. AD7685/AD7686 16-bit PulSAR ADCs.

The ADA4841-1 is a SOIC package, with Pb-free lead finish. This amplifier is rated to work over the industrial temperature range (−40°C to +125°C).

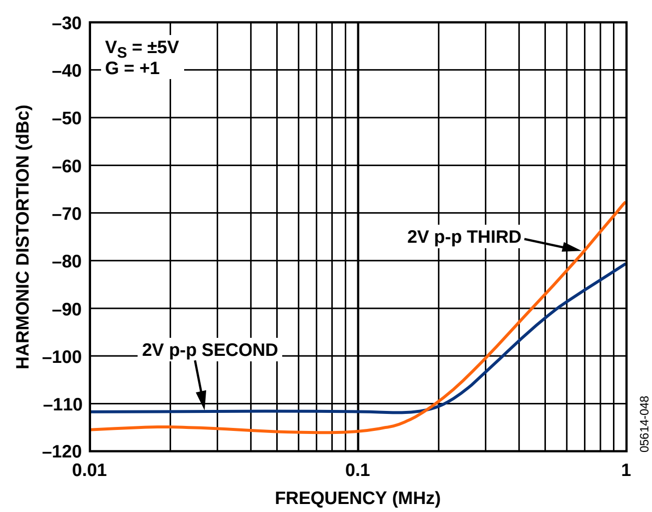

Figure 2. Harmonic Distortion

Rev. A

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TABLE OF CONTENTS

REVISION HISTORY

9/05—Rev. 0 to Rev. A

Changes to Features ... 1
Changes to Figure 2 ... 1
Changes to Figure 12 ... 8
Changes to Figure 40 ... 14
Changes to Headroom Considerations Section ... 15

7/05—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, V_S = ±5 V, R_L = 1 kΩ, Gain = +1, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_O = 0.02 V p-p	58	80		MHz
	V_O = 2 V p-p		3		MHz
Slew Rate	G = +1, V_O = 9 V step, R_L = 1 kΩ	12	13		V/μs
Settling Time to 0.1%	G = +1, V_O = 8 V step		650		ns
Settling Time to 0.01%	G = +1, V_O = 8 V step		1000		ns
NOISE/HARMONIC PERFORMANCE					
Harmonic Distortion HD2/HD3	f_C = 100 kHz, V_O = 2 V p-p, G = +1		−111/−115		dBc
	f_C = 1 MHz, V_O = 2 V p-p		−80/−67		dBc
Input Voltage Noise	f = 100 kHz		2		nV/√Hz
Input Current Noise	f = 100 kHz		1.3		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage			60	290	μV
Input Offset Voltage Drift			1		μV/°C
Input Bias Current			3.4	5.3	μA
Input Offset Current			0.1	0.4	μA
Open-Loop Gain	V_O = ±4 V	103	114		dB
INPUT CHARACTERISTICS					
Input Resistance, Common Mode			90		MΩ
Input Resistance, Differential Mode			25		kΩ
Input Capacitance, Common Mode			1		pF
Input Capacitance, Differential Mode			3		pF
Input Common-Mode Voltage Range		−5.1		+4	V
Common-Mode Rejection Ratio (CMRR)	V_{CM} = −2 V to +2 V	95	114		dB
POWER DOWN					
Input Voltage					
Power Down			3.3		V
Input Bias Current					
Enable	Power down = +5 V		1	2	μA
Power Down	Power down = −5 V		−13	−30	μA
Switching Speed					
Enable			1		μs
Power Down			40		μs
OUTPUT CHARACTERISTICS					
Output Voltage Swing		±4.90	±4.955		V
Output Current	Sourcing		30		mA
	Sinking		60		mA
Capacitive Load Drive	30% overshoot		15		pF
POWER SUPPLY					
Operating Range		2.7		12	V
Quiescent Current			1.1	1.5	mA
	Disable = Low		40	90	μA
Positive Power Supply Rejection Ratio	$+V_S$ = 5 V to 6 V, $-V_S$ = −5 V	96	110		dB
Negative Power Supply Rejection Ratio	$+V_S$ = 5 V, $-V_S$ = −5 V to +6 V	97	120		dB

$T_A = 25°C$, $V_S = 5$ V, $R_L = 1$ kΩ, Gain = +1, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_O = 0.02 V p-p	54	80		MHz
	V_O = 2 V p-p		3		MHz
Slew Rate	G = +1, V_O = 4 V step, R_L = 1 kΩ	10	12		V/μs
Settling Time to 0.1%	G = +1, V_O = 2 V step		175		ns
Settling Time to 0.01%	G = +1, V_O = 2 V step		550		ns
NOISE/HARMONIC PERFORMANCE					
Harmonic Distortion HD2/HD3	f_C = 100 kHz, V_O = 2 V p-p		−109/−114		dBc
	f_C = 1 MHz, V_O = 2 V p-p		−78/−66		dBc
Input Voltage Noise	f = 100 kHz		2		nV/√Hz
Input Current Noise	f = 100 kHz		1.3		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage			60	290	μV
Input Offset Voltage Drift			1		μV/°C
Input Bias Current			3.4	5.3	μA
Input Offset Current			0.1	0.4	μA
Open-Loop Gain	V_O = 0.5 V to 4.5 V	103	124		dB
INPUT CHARACTERISTICS					
Input Resistance, Common Mode			90		MΩ
Input Resistance, Differential Mode			25		kΩ
Input Capacitance, Common Mode			1		pF
Input Capacitance, Differential Mode			3		pF
Input Common-Mode Voltage Range		−0.1		+4	V
Common-Mode Rejection Ratio (CMRR)	V_{CM} = 0 V to1.5 V	88	120		dB
Power Down					
Input Voltage					
Power Down			3.3		V
Input Bias Current					
Enable	Power down = 5 V		1	2	μA
Power Down	Power down = 0 V		−13	−30	μA
Switching Speed					
Enable			1		μs
Power Down			40		μs
OUTPUT CHARACTERISTICS					
Output Voltage Swing		0.065 to 4.920	0.029 to 4.974		V
Output Current	Sourcing		30		mA
	Sinking		60		mA
Capacitive Load Drive	30% overshoot		15		pF
POWER SUPPLY					
Operating Range		2.7		5.5	V
Quiescent Current			1.1	1.4	mA
	Power down = 0 V		35	70	μA
Positive Power Supply Rejection Ratio	$+V_S$ = 5 V to 6 V, $−V_S$ = 0 V	95	110		dB
Negative Power Supply Rejection Ratio	$+V_S$ = 5 V, $−V_S$ = 0 V to −1 V	96	120		dB

T_A = 25°C, V_S = 3 V, R_L = 1 kΩ, Gain =+1, unless otherwise noted.

Table 3.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_O = 0.02 V p-p	52	80		MHz
Slew Rate	G = +1, V_O = 2 V step, R_L = 1 kΩ	10	12		V/μs
Settling Time to 0.1%	G = +1, V_O = 1 V step		120		ns
Settling Time to 0.01%	G = +1, V_O = 1 V step		250		ns
NOISE/HARMONIC PERFORMANCE					
Harmonic Distortion HD2/HD3	f_C = 100 kHz, V_O = 1 V p-p		−97/−100		dBc
	f_C = 1 MHz, V_O = 1 V p-p		−79/−80		dBc
Input Voltage Noise	f = 100 kHz		2		nV/√Hz
Input Current Noise	f = 100 kHz		1.3		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage			60	295	μV
Input Offset Voltage Drift			1		μV/°C
Input Bias Current			3.4	5.3	μA
Input Offset Current			0.1	0.4	μA
Open-Loop Gain	V_O = 0.5 V to 4.5 V	101	123		dB
INPUT CHARACTERISTICS					
Input Resistance, Common Mode			90		MΩ
Input Resistance, Differential Mode			25		kΩ
Input Capacitance, Common Mode			1		pF
Input Capacitance, Differential Mode			3		pF
Input Common-Mode Voltage Range		−0.1		+2	V
Common-Mode Rejection Ratio (CMRR)	V_{CM} = 0 V to 0.4 V	86	120		dB
Power Down					
Input Voltage					
Power Down			1.3		V
Input Bias Current					
Enable	Power down = 3 V		1	2	μA
Power Down	Power down = 0 V		−10	−30	μA
Switching Speed					
Enable			1		μs
Power Down			40		μs
OUTPUT CHARACTERISTICS					
Output Voltage Swing		0.045 to 2.955	0.023 to 2.988		V
Output Current	Sourcing		30		mA
	Sinking		60		mA
Capacitive Load Drive	30% overshoot		30		pF
POWER SUPPLY					
Operating Range		2.7		3.5	V
Quiescent Current			1.1	1.3	mA
	Power down = 0 V		25	60	μA
Positive Power Supply Rejection Ratio	$+V_S$ = 3 V to 4 V, $-V_S$ = 0 V	95	110		dB
Negative Power Supply Rejection Ratio	$+V_S$ = 3 V, $-V_S$ = 0 V to −1 V	96	120		dB

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	12.6 V
Power Dissipation	See Figure 3
Common-Mode Input Voltage	$-V_S - 0.5$ V to $+V_S + 0.5$ V
Differential Input Voltage	±1.8 V
Storage Temperature	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature	JEDEC J-STD-20
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for device soldered in circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	Unit
8-lead SOIC	125	°C/W

Maximum Power Dissipation

The maximum safe power dissipation for the ADA4841-1 is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the amplifiers. Exceeding a junction temperature of 150°C for an extended period can result in changes in silicon devices, potentially causing degradation or loss of functionality.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the die due to the amplifier's drive at the output. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S).

$$P_D = \textit{Quiescent Power} + (\textit{Total Drive Power} - \textit{Load Power})$$

$$P_D = (V_S \times I_S) + \left(\frac{V_S}{2} \times \frac{V_{OUT}}{R_L}\right) - \frac{{V_{OUT}}^2}{R_L}$$

RMS output voltages should be considered. If R_L is referenced to $-V_S$, as in single-supply operation, the total drive power is $V_S \times I_{OUT}$. If the rms signal levels are indeterminate, consider the worst case, when $V_{OUT} = V_S/4$ for R_L to midsupply.

$$P_D = (V_S \times I_S) + \frac{(V_S/4)^2}{R_L}$$

In single-supply operation with R_L referenced to $-V_S$, worst case is $V_{OUT} = V_S/2$.

Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, more metal directly in contact with the package leads and through holes under the device reduces θ_{JA}.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 8-lead SOIC (125°C/W) on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

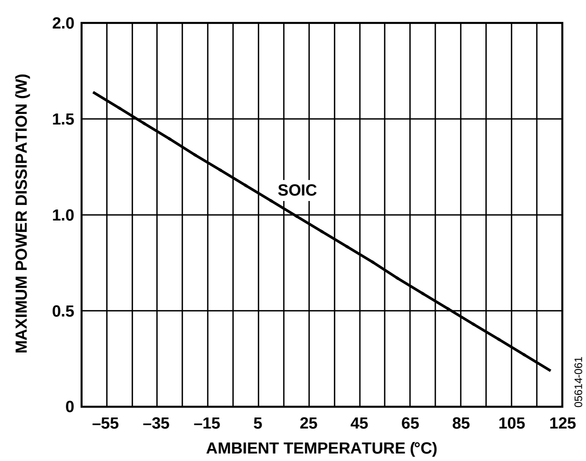

Figure 3. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

WARNING!
ESD SENSITIVE DEVICE

TYPICAL PERFORMANCE CHARACTERISTICS

R_L = 1 kΩ, unless otherwise noted.

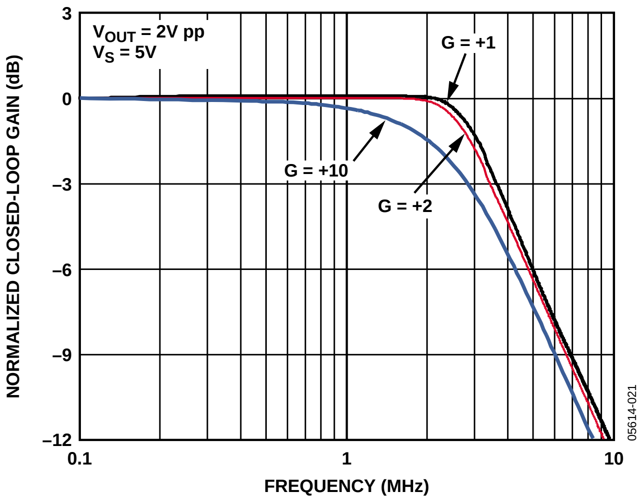

Figure 4. Large Signal Frequency Response vs. Gain

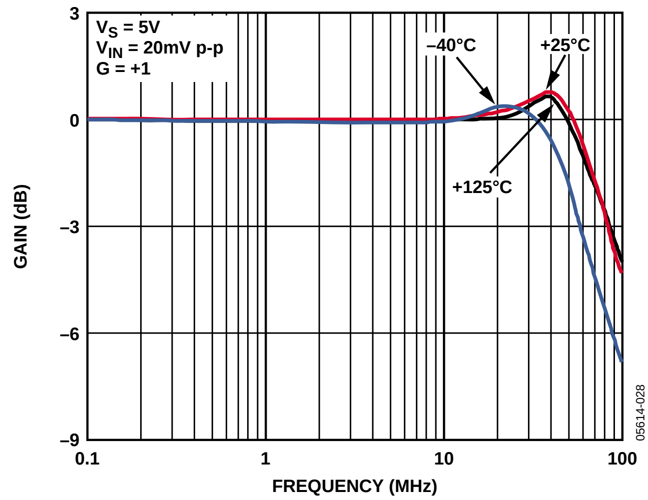

Figure 7. Small Signal Frequency Response vs. Temperature

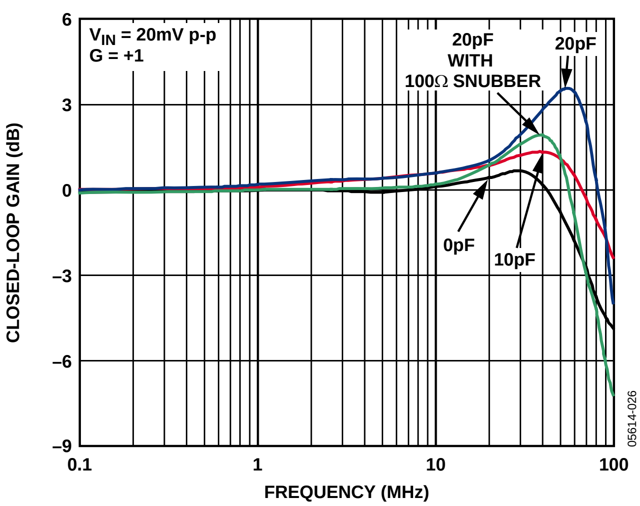

Figure 5. Small Signal Frequency Response vs. Capacitive Load

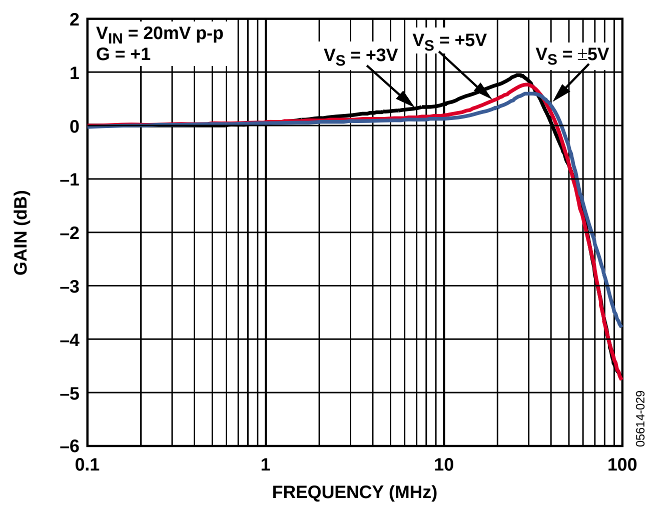

Figure 8. Small Signal Frequency Response vs. Supply Voltage

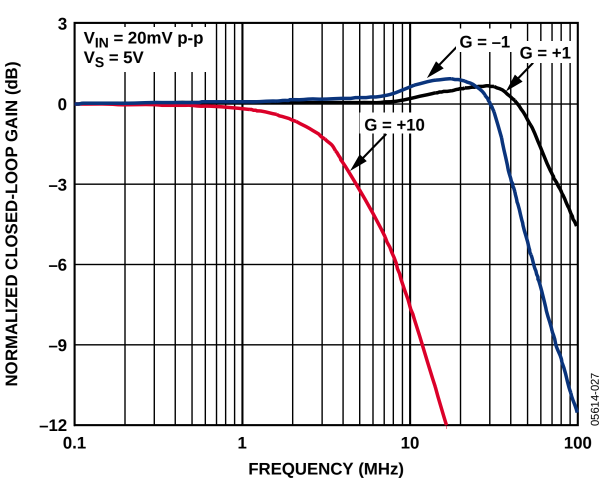

Figure 6. Small Signal Frequency Response vs. Gain

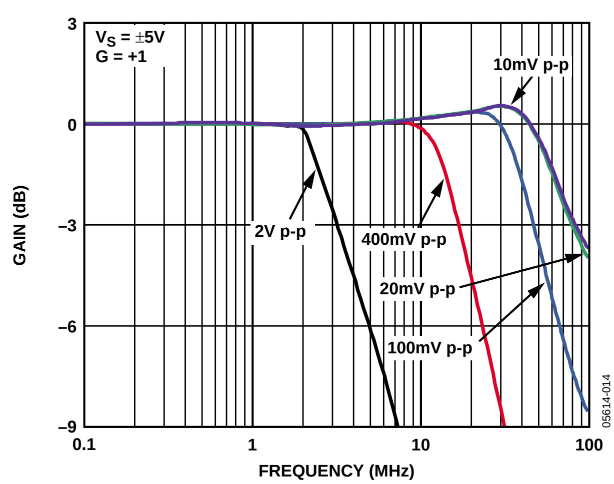

Figure 9. Frequency Response for Various V_{OUT}

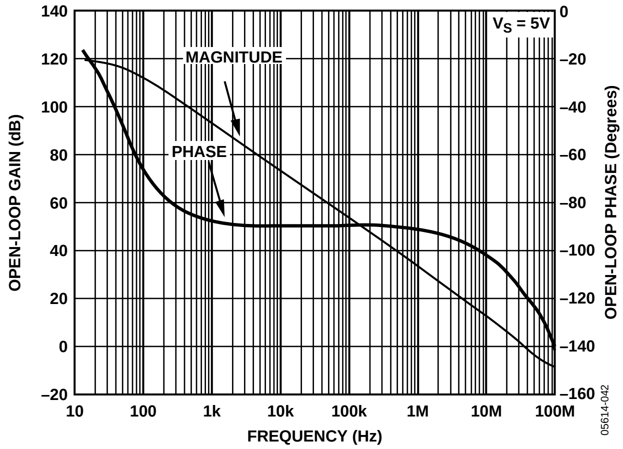

Figure 10. Open-Loop Gain and Phase vs. Frequency

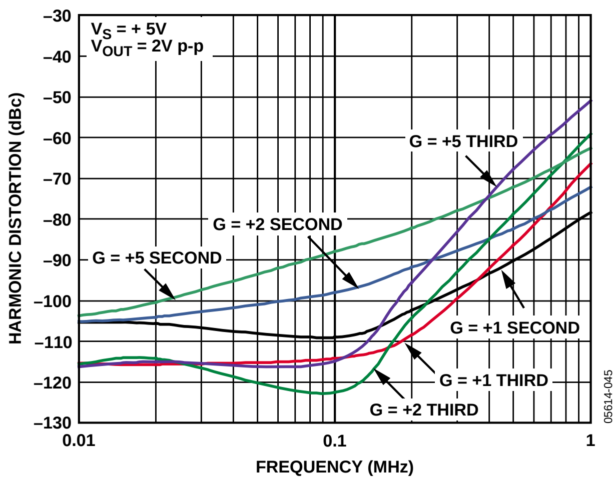

Figure 11. Harmonic Distortion vs. Frequency for Various Gains

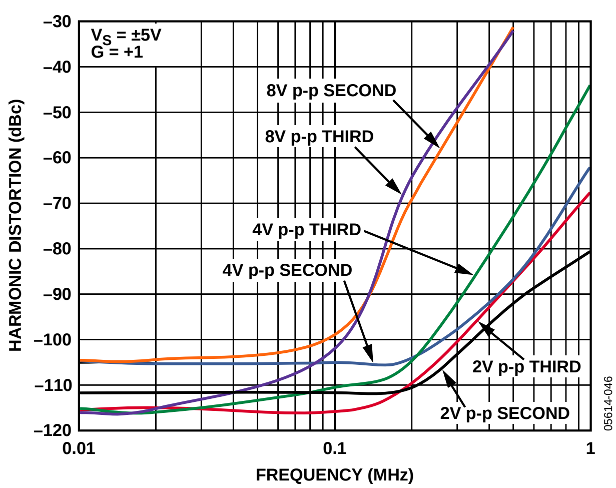

Figure 12. Harmonic Distortion vs. Frequency for Various Output Voltages

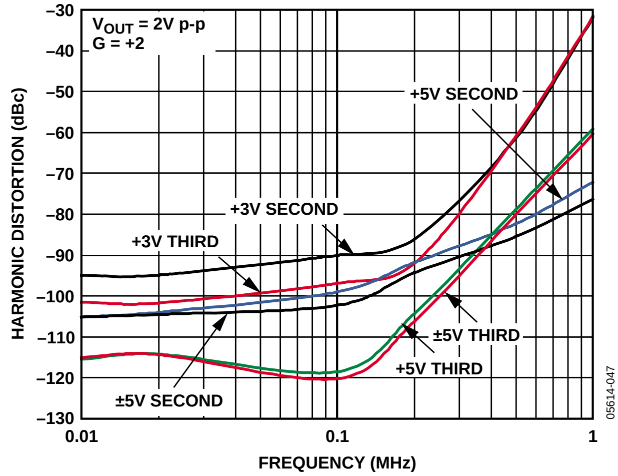

Figure 13. Harmonic Distortion vs. Frequency for Various Supplies

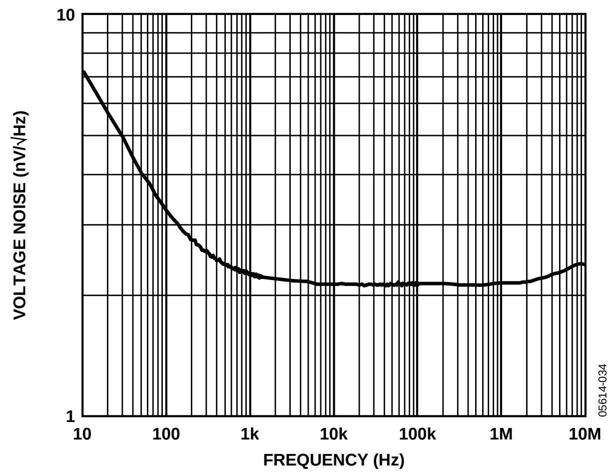

Figure 14. Voltage Noise vs. Frequency

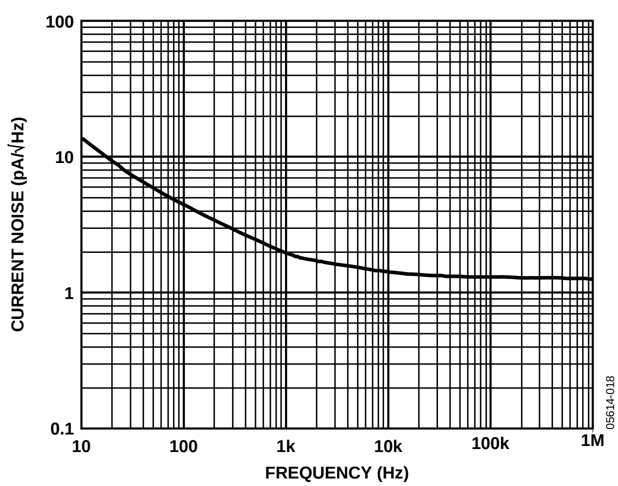

Figure 15. Current Noise vs. Frequency

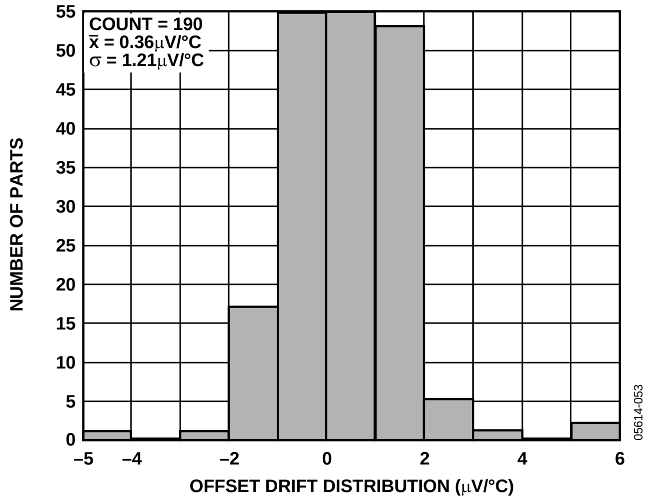

Figure 16. Input Offset Voltage Distribution

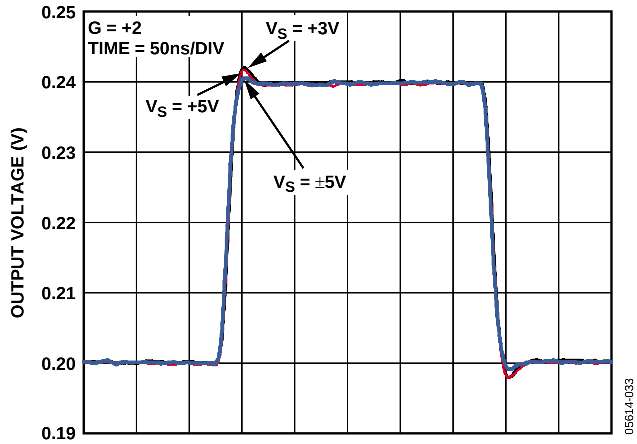

Figure 19. Small Signal Transient Response for Various Supplies

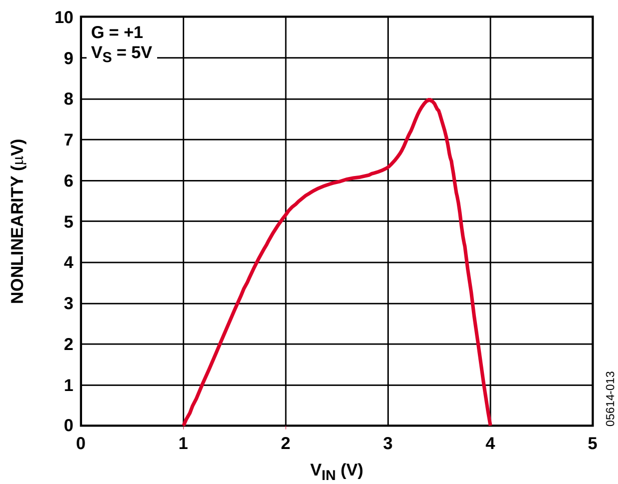

Figure 17. Nonlinearity vs. V_{IN}

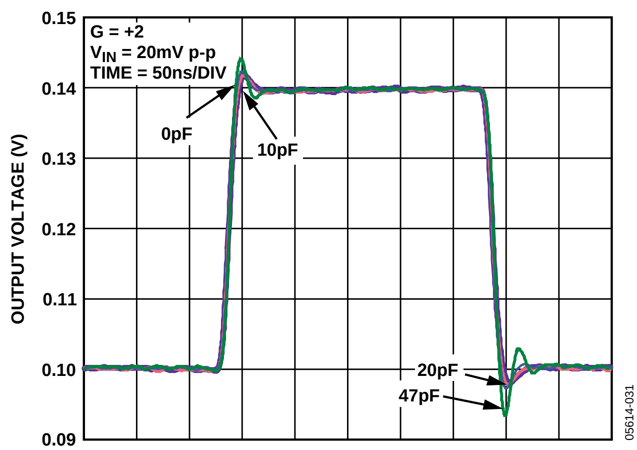

Figure 20. Small Signal Transient Response for Various Capacitive Loads

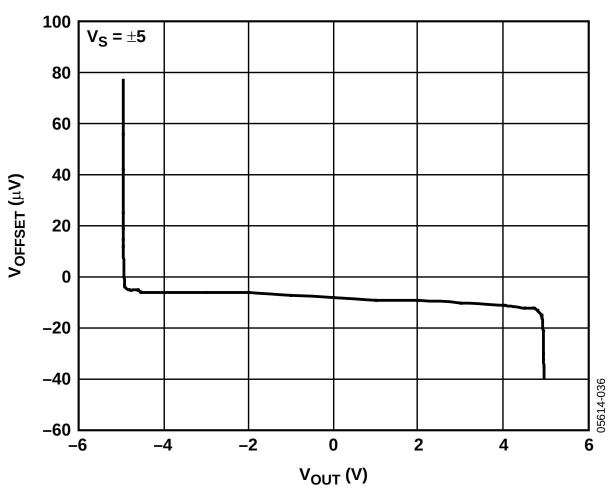

Figure 18. Input Error Voltage vs. Output Voltage

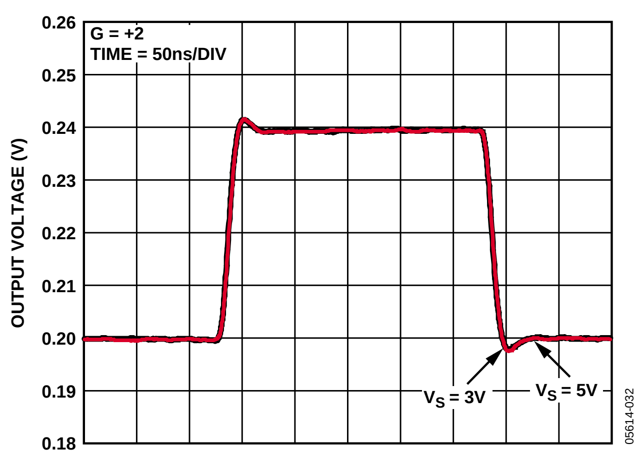

Figure 21. Small Signal Transient Response for Various Supplies

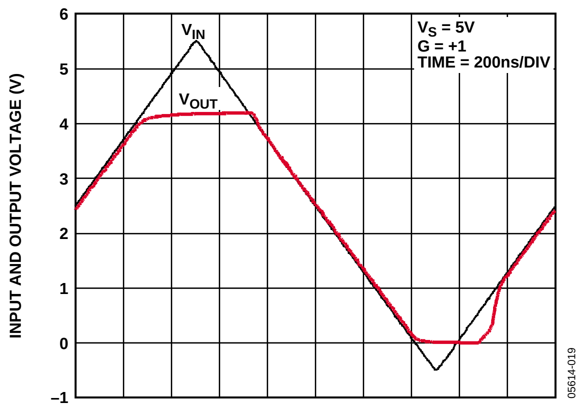

Figure 22. Input Overdrive Recovery

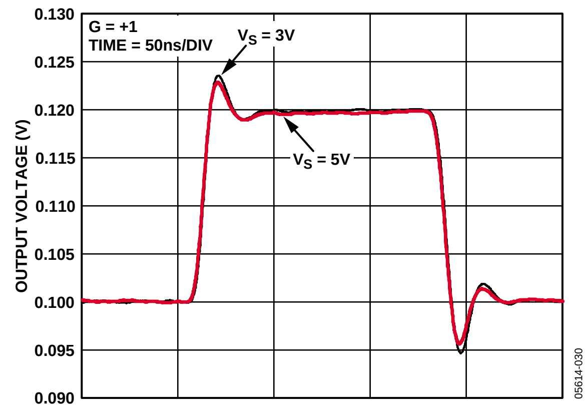

Figure 25. Small Signal Transient Response for Various Supplies

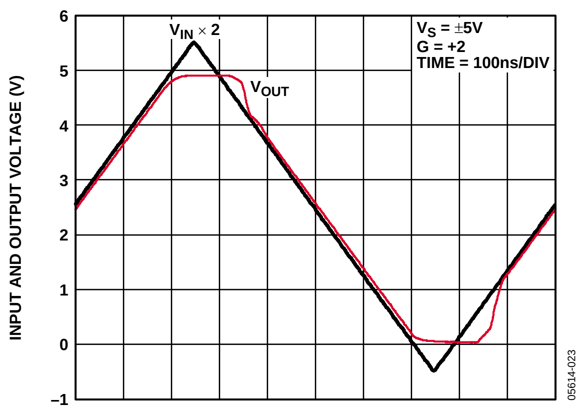

Figure 23. Output Overdrive Recovery

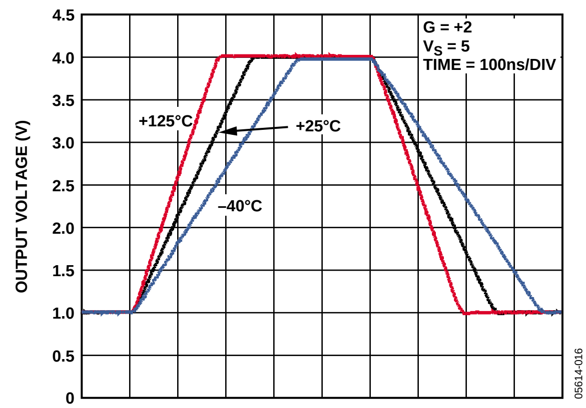

Figure 26. Output Voltage vs. Temperature

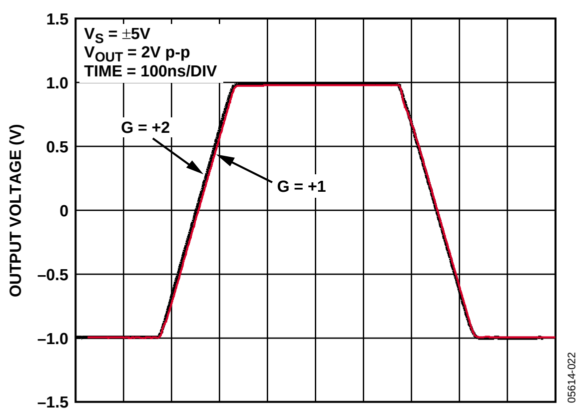

Figure 24. Large Signal Transient Response for Various Gains

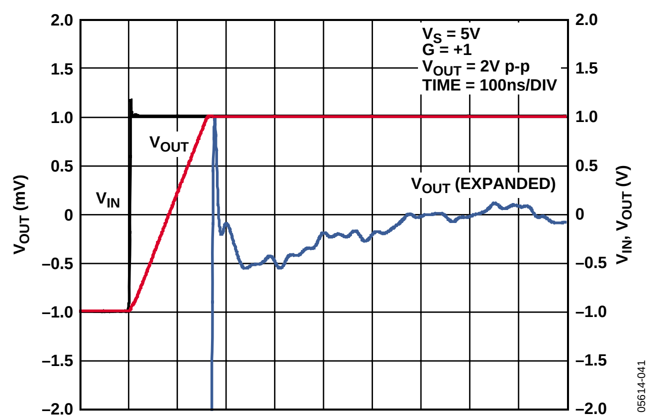

Figure 27. Settling Time

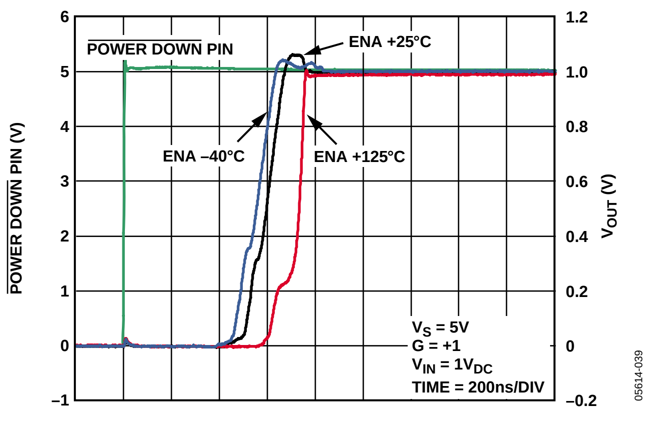

Figure 28. Power-Up Time vs. Temperature

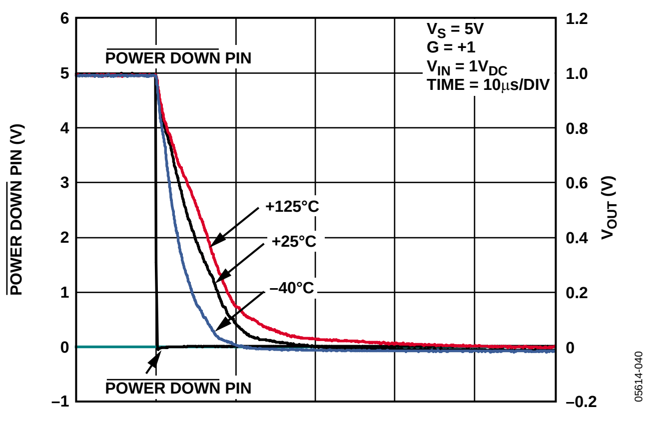

Figure 29. Power-Down Time vs. Temperature

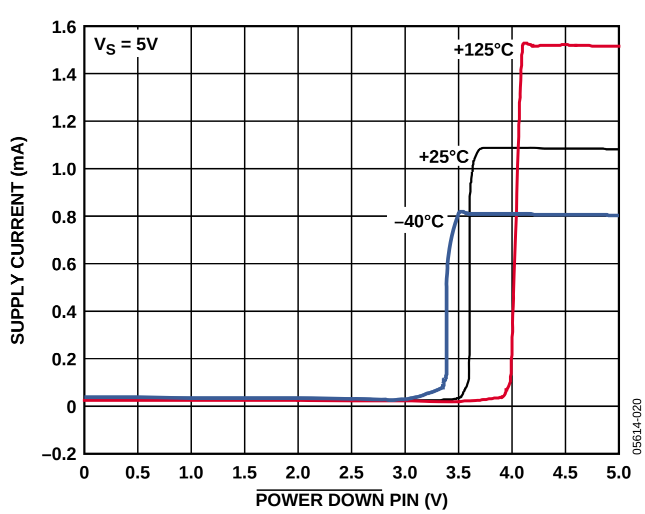

Figure 30. Supply Current vs. POWER DOWN Pin Voltage

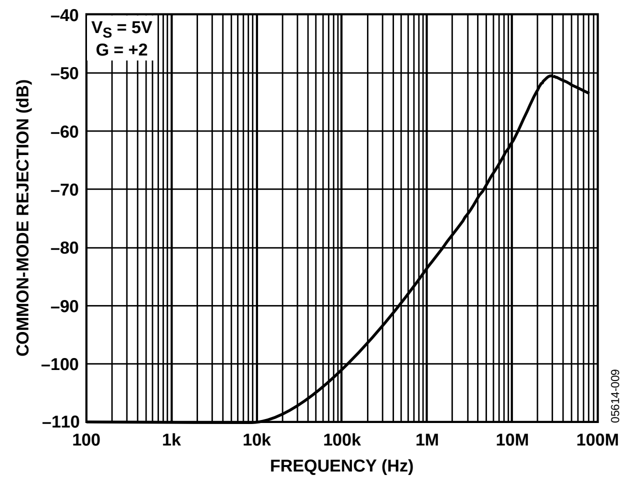

Figure 31. CMRR vs. Frequency

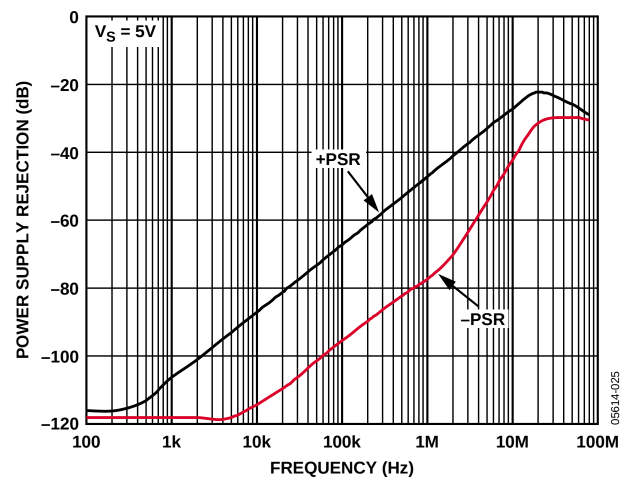

Figure 32. PSRR vs. Frequency

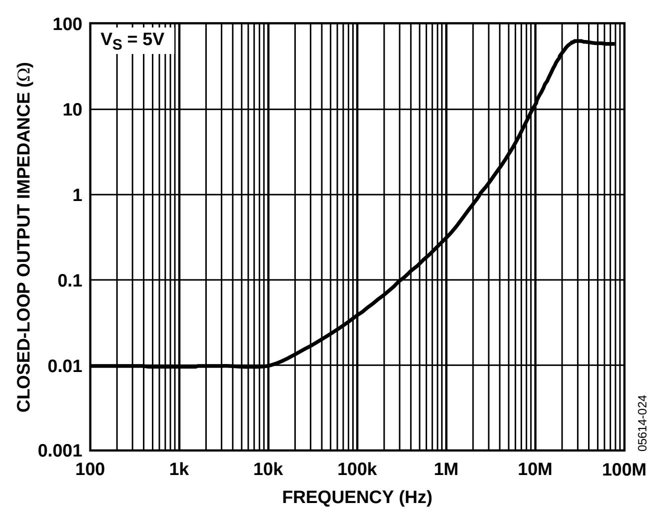

Figure 33. Output Impedance vs. Frequency

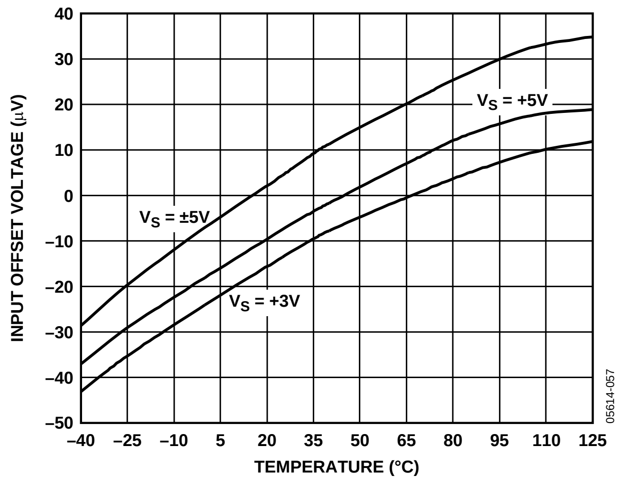

Figure 34. Input Offset Voltage vs. Temperature for Various Supplies

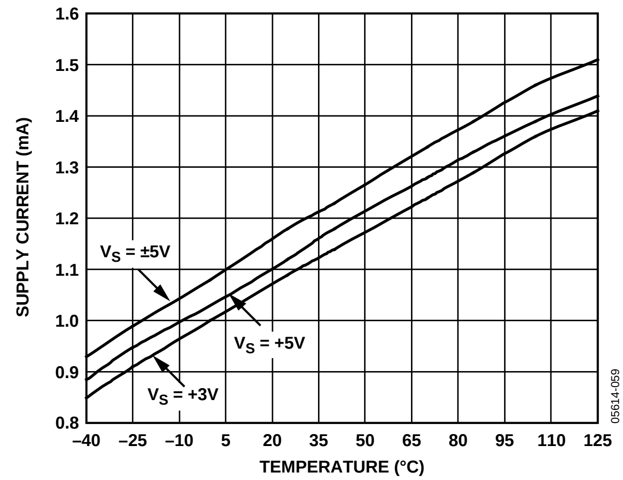

Figure 36. Supply Current vs. Temperature for Various Supplies

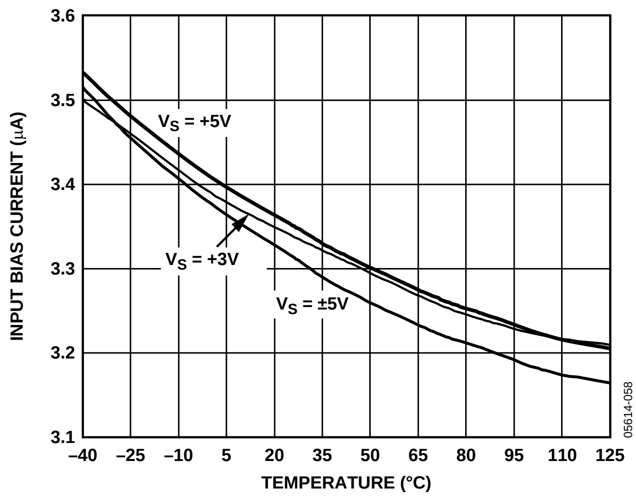

Figure 35. Input Bias Current vs. Temperature for Various Supplies

THEORY OF OPERATION

AMPLIFIER DESCRIPTION

The ADA4841-1 is a low power, low noise, precision voltage-feedback op amp for single or dual voltage supply operation. The ADA4841-1 is fabricated on ADI's second generation XFCB process and features a trimmed supply current and an offset voltage. The 2 nV/√Hz voltage noise (very low for a 1.1 mA supply current amplifier), 60 μV offset voltage, and sub 1 μV/°C offset drift is accomplished with an input stage made of an undegenerated PNP input pair driving a symmetrical folded cascode. A rail-to-rail output stage provides the maximum linear signal range possible on low voltage supplies and has the current drive capability needed for the relatively low resistance feedback networks required for low noise operation. CMRR, PSRR, and open-loop gain are all well above 100 dB, preserving the precision performance in a variety of configurations. Gain bandwidth is kept high for this power level to preserve the outstanding linearity performance to frequencies up to 100 kHz. The ADA4841-1 has a power-down function to further reduce power consumption. All this results in a low noise, power efficient, precision amplifier that is well suited for high resolution and precision applications.

DC PERFORMANCE CONSIDERATIONS

Figure 37 shows a typical connection diagram and the major dc error sources. The ideal transfer function (all error sources set to 0 and infinite dc gain) can be written as

$$V_{OUT} = \left(1+\frac{R_F}{R_G}\right)\times V_{IP} - \left(\frac{R_F}{R_G}\right)\times V_{IN} \tag{1}$$

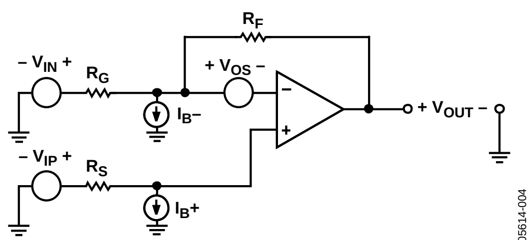

Figure 37. Typical Connection Diagram and DC Error Sources

This reduces to the familiar forms for inverting and noninverting op amp gain expressions:

$$V_{OUT} = \left(1+\frac{R_F}{R_G}\right)\times V_{IP} \tag{2}$$

(Noninverting gain, V_{IN} = 0 V)

$$V_{OUT} = \left(\frac{-R_F}{R_G}\right)\times V_{IN} \tag{3}$$

(Inverting gain, V_{IP} = 0 V)

The total output voltage error is the sum of errors due to the amplifier's offset voltage and input currents. The output error due to the offset voltage can be estimated as

$$V_{OUT_{ERROR}} = \left(V_{OFFSET_{NOM}} + \frac{VCM}{CMRR} + \frac{V_P - V_{PNOM}}{PSRR} + \frac{V_{OUT}}{A}\right)\times\left(1+\frac{R_F}{R_G}\right) \tag{4}$$

where:

$V_{OFFSET_{NOM}}$ is the offset voltage at the specified supply voltage. This is measured with the input and output at midsupply.

VCM is the common-mode voltage.

V_P is the power supply voltage.

$V_{P_{NOM}}$ is the specified power supply voltage.

CMRR is the common-mode rejection ratio.

PSRR is the power supply rejection ratio.

A is the dc open-loop gain.

The output error due to the input currents can be estimated as

$$V_{OUT_{ERROR}} = (R_F \,||\, R_G)\times\left(1+\frac{R_F}{R_G}\right)I_{B-} - R_S\times\left(1+\frac{R_F}{R_G}\right)\times I_{B+} \tag{5}$$

Note that setting R_S equal to $R_F||R_G$ compensates for the voltage error due to the input bias current.

NOISE CONSIDERATIONS

Figure 38 illustrates the primary noise contributors for the typical gain configurations. The total rms output noise is the root-mean-square of all the contributions.

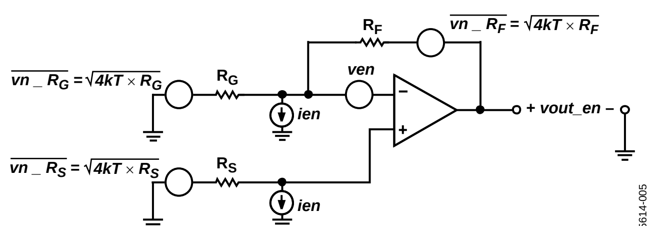

Figure 38. Noise Sources in Typical Connection

The output noise spectral density can be calculated by

$$\overline{vout\_en} = \sqrt{4kTRf + \left(1+\frac{R_F}{R_G}\right)^2 \left[4kTRs + \overline{ien}^2 R_S{}^2 + \overline{ven}^2\right] + \left(\frac{R_F}{R_G}\right)^2 4kTRg + \overline{ien}^2 R_F{}^2} \tag{6}$$

where:

k is Boltzmann's Constant.

T is the absolute temperature, degrees Kelvin.

ien is the amplifier input current noise spectral density, pA/√Hz.

ven is the amplifier input voltage spectral density, nV/√Hz.

R_S is the source resistance as shown in Figure 38.

R_F and R_G are the feedback network resistances, as shown in Figure 38.

Source resistance noise, amplifier voltage noise ($\overline{\text{ven}}$), and the voltage noise from the amplifier's current noise ($\overline{\text{ien}} \times R_S$) are all subject to the noise gain term ($1 + R_F/R_G$). Note that with a 2 nV/√Hz input voltage noise and 1 pA/√Hz input current, the noise contributions of the amplifier are relatively small for source resistances between approximately 200 Ω and 30 kΩ. Figure 39 shows the total RTI noise due to the amplifier vs. the source resistance. In addition, the value of the feedback resistors used impacts the noise. It is recommended to keep the value of feedback resistors between 250 Ω and 1 kΩ to keep the total noise low.

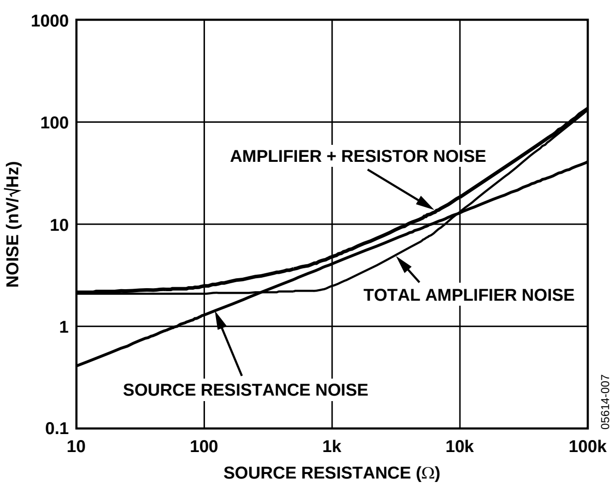

Figure 39. RTI Noise vs. Source Resistance

HEADROOM CONSIDERATIONS

The ADA4841-1 is designed to provide maximum input and output signal ranges with 16-bit to 18-bit dc linearity. As the input or output headroom limits are reached, the signal's linearity degrades.

The input stage positive limit is almost exactly a volt below the positive supply at room temperature. Input voltages above that start to show clipping behavior. The positive input voltage limit increases with temperature with a coefficient of about 2 mV/°C. The lower supply limit is nominally below the minus supply; therefore, in a standard gain configuration, the output stage limits the signal headroom on the negative supply side. Figure 40 and Figure 41 show the nominal CMRR behavior at the limits of the input headroom for three temperatures—this is generated using the subtractor topology shown in Figure 42, which avoids the output stage limitation.

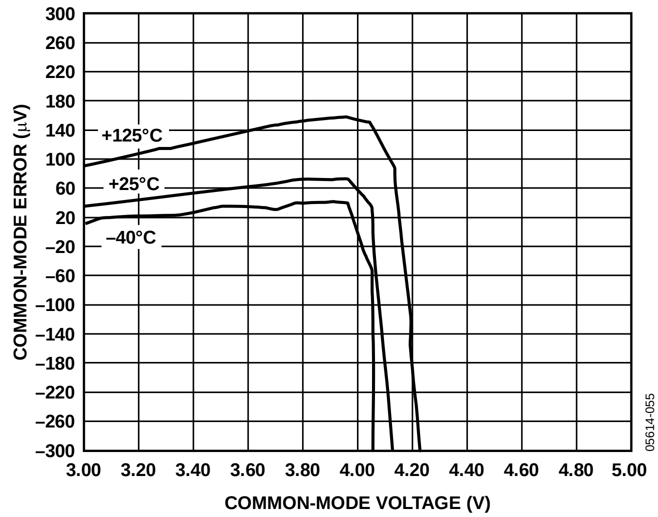

Figure 40. V_{OS} vs. +CMP vs. Common-Mode Error

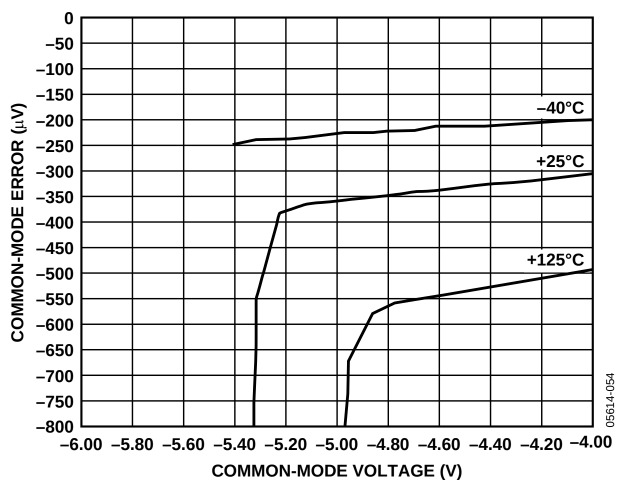

Figure 41. V_{OS} vs. –CMP vs. Common-Mode Error

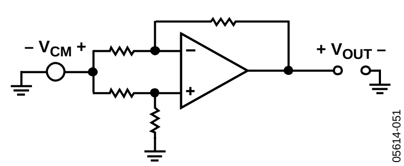

Figure 42. Common-Range Subtractor

Figure 43 shows the amplifier's frequency response as a G = −1 inverter with the input and output stage biased near the negative supply rail.

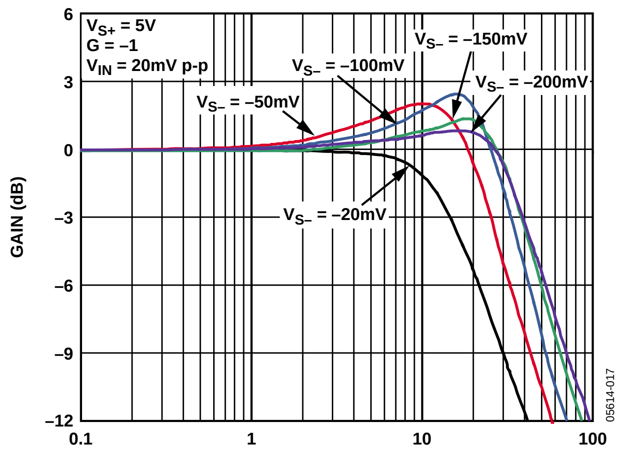

Figure 43. Small Signal Frequency Response vs. Negative Supply Bias

The input voltage (V_{IN}) and reference voltage (V_{IP}) are both at 0 V, see Figure 37. $+V_S$ is biased at +5 V, and $-V_S$ is swept from −200 mV to −20 mV. With the input and output voltages biased 200 mV from the bottom rail, the G = −1 inverter frequency response is not much different from what is seen with the input and output voltages biased near midsupply. At 150 mV bias, the frequency response starts to decrease and at 20 mV, the inverter band-width is less than half its nominal value.

CAPACITANCE DRIVE

Capacitance at the output of an amplifier creates a delay within the feedback path that, if within the bandwidth of the loop, can create excessive ringing and oscillation. The G = +1 follower topology has the highest loop bandwidth of any typical configuration and therefore is the most vulnerable to the effects of capacitance load.

A small resistor in series with the amplifier's output and the capacitive load mitigates the problem. Figure 44 plots the recommended series resistance vs. the capacitance for gains of +1, +2, and +5.

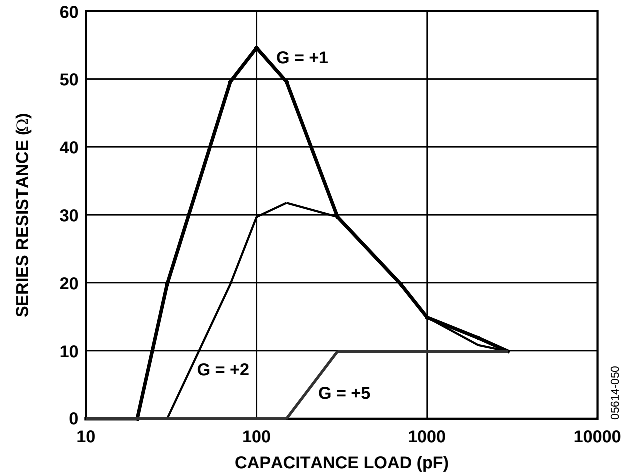

Figure 44. Series Resistance vs. Capacitive Load

INPUT PROTECTION

The ADA4841-1 is fully protected from ESD events, withstanding ESD events of 2.5 keV with no measured performance degradation. The precision input is protected with an ESD network between the power supplies and diode clamps across the input device pair, as shown in Figure 45.

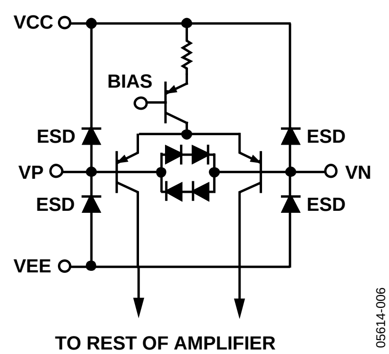

Figure 45. Input Stage and Protection Diodes

For differential voltages above approximately 1.4 V, the diode clamps start to conduct. Too much current can cause damage due to excessive heating. If large differential voltages need to be sustained across the input terminals, it is recommended that the current through the input clamps be limited to below 150 mA. Series input resistors sized appropriately for the expected differential overvoltage provide the needed protection.

The ESD clamps start to conduct for input voltages more than 0.7 V above the positive supply and input voltages more than 0.7 V below the negative supply. It is recommended that the fault current be limited to less than 150 mA if an overvoltage condition is expected.

POWER-DOWN OPERATION

Figure 46 shows the ADA4841-1 power-down circuitry. If the $\overline{\text{POWER DOWN}}$ pin is left unconnected, the base of Qx is pulled high by resistor Y and the part is turned on. Pulling the power-down pin approximately 1.7 V below the positive supply turns the part off, reducing the supply current to approximately 40 μA.

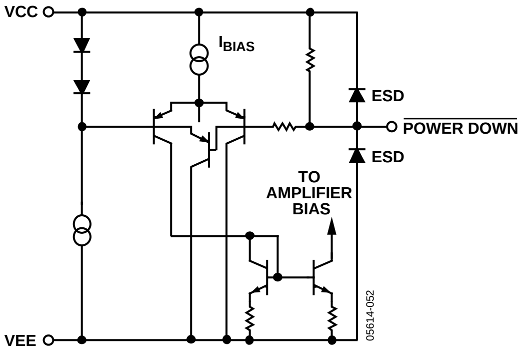

Figure 46. Power-Down Circuit

The $\overline{\text{POWER DOWN}}$ pin is protected with ESD clamps, as shown in Figure 46. Voltages beyond the power supplies cause these diodes to conduct. The guidelines for limiting the overload current in the input protection section should also be followed for the $\overline{\text{POWER DOWN}}$ pin.

APPLICATIONS

TYPICAL PERFORMANCE VALUES

To reduce design time and eliminate uncertainty Table 6 provides a convenient reference for typical gains, component values, and performance parameters.

16-BIT ADC DRIVER

The combination of low noise, low power, and high speed make the ADA4841-1 the perfect driver solution for low power, 16-bit ADCs, such as the AD7685. Figure 47 shows a typical 16-bit single-supply application. There are different challenges to do a single-supply, high resolution design, and the ADA4841-1 addresses these nicely. In a single-supply system, one of the main challenges is to use the amplifier in buffer mode to have the lowest output noise and still preserve linearity compatible with the ADC. Rail-to-rail input amplifiers are usually higher noise than the ADA4841-1 and cannot be used in this mode because of the nonlinear region around the crossover point of their input stages. The ADA4841-1, which has no crossover region but has a wide linear input range from 100 mV below ground to 1 V below positive rail, solves this problem, as shown in Figure 47. It can accept the 0 V to 4.096 V input range with a supply as low as 5.2 V. This supply also allows the use of a small, low dropout, low temperature drift ADR364 reference voltage. Note that at the low end of the input range close to ground, the ADA4841-1 can exhibit some nonlinearity, such as any rail-to-rail output amplifier. The ADA4841-1 drives a one-pole, low-pass filter. This filter limits the already very low noise contribution from the amplifier to the AD7685.

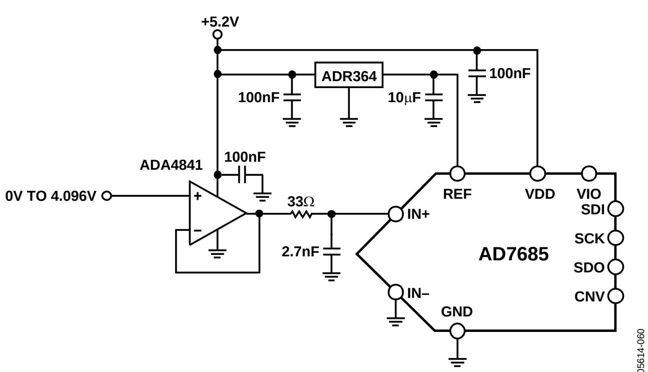

Figure 47. ADC Driver Schematic

RECONSTRUCTION FILTER

The ADA4841-1 can also be used as a reconstruction filter at the output of DACs for suppression of the sampling frequency. The filter shown in Figure 48 is a two-pole, 500 KHz Sallen-Key LPF with a fixed gain of G = +1.6.

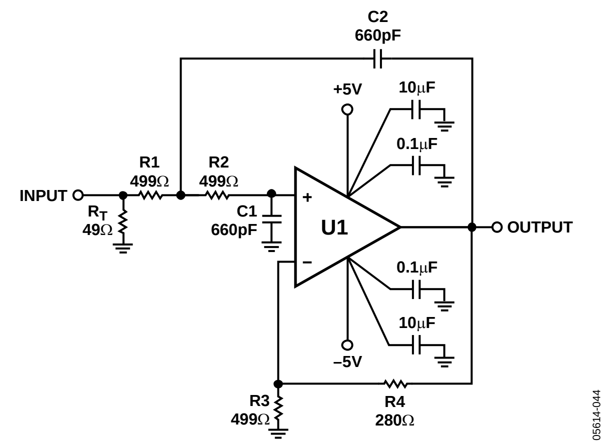

Figure 48. Two-Pole 500 kHz Reconstruction Filter Schematic

Setting the resistors and capacitors equal to each other greatly simplifies the design equations for the Sallen-Key filter. The corner frequency, or −3 dB frequency, can be described by the equation

$$f_C = \frac{1}{2\pi R1C1}$$

The quality factor, or *Q*, is shown in the equation

$$Q = \frac{1}{3 - K}$$

For minimum peaking, set Q equal to 0.707.

The gain, or *K*, of the amplifier is

$$K = \frac{R4}{R3} + 1$$

Resistor values are kept low for minimal noise contribution, offset voltage, and optimal frequency response.

Table 6. Recommended Values and Typical Performance

Gain	R_F (Ω)	R_G (Ω)	−3 dB BW (MHz)	Slew Rate (V/µs)	Peaking (dB)	Output Noise ADA4841-1 Only (nV/√Hz)	Total Output Noise Including Resistors (nV/√Hz)
+1	0	N/A	77	12.5	0.9	2	2
+2	499	499	34	12.5	0.3	4	5.73
−1	499	499	38	12.5	0.4	4	5.73
+5	499	124	11	12	0	10	11.9
+10	499	54.9	5	12	0	20	21.1
+20	499	26.1	2.3	11.2	0	40	42.2

Capacitor selection is critical for optimal filter performance. Capacitors with low temperature coefficients, such as NPO ceramic capacitors, are good choices for filter elements. Figure 49 shows the filter response.

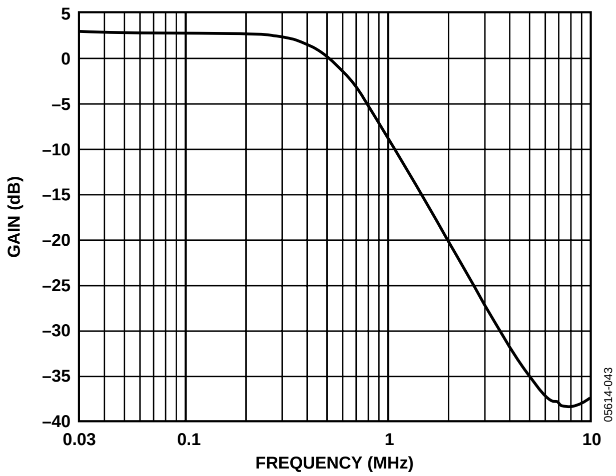

Figure 49. Filter Frequency Response

LAYOUT CONSIDERATIONS

To ensure optimal performance, careful and deliberate attention must be paid to the board layout, signal routing, power supply bypassing, and grounding.

GROUND PLANE

It is important to avoid ground in the areas under and around the input and output of the ADA4841-1. Stray capacitance created between the ground plane and the input and output pads of a device are detrimental to a high speed amplifier's performance. Stray capacitance at the inverting input, along with the amplifier's input capacitance, lowers the phase margin and can cause instability. Stray capacitance at the output creates a pole in the feedback loop. This can reduce phase margin and can cause the circuit to become unstable.

POWER SUPPLY BYPASSING

Power supply bypassing is a critical aspect in the performance of the ADA4841-1. A parallel connection of capacitors from each of the power supply pins to ground works best. A typical connection is shown in Figure 48. Smaller value capacitors offer better high frequency response where larger value electrolytics offer better low frequency performance. Paralleling different values and sizes of capacitors helps to ensure that the power supply pins are provided a low ac impedance across a wide band of frequencies. This is important for minimizing the coupling of noise into the amplifier. This can be especially important when the amplifier PSR is starting to roll off—the bypass capacitors can help lessen the degradation in PSR performance.

Starting directly at the ADA4841-1 power supply pins, the smallest value capacitor should be placed on the same side of the board as the amplifier, and as close as possible to the amplifier power supply pin. The ground end of the capacitor should be connected directly to the ground plane. Keeping the capacitors' distance short but equal from the load is important and can improve distortion performance. This process should be repeated for the next largest value capacitor.

It is recommended that a 0.01 µF ceramic 0508 case be used. The 0508 case size offers low series inductance and excellent high frequency performance. A 10 µF electrolytic capacitor should be placed in parallel with the 0.01 µF capacitor. Depending on the circuit parameters, some enhancement to performance can be realized by adding additional capacitors. Each circuit is different and should be individually analyzed for optimal performance.

OUTLINE DIMENSIONS

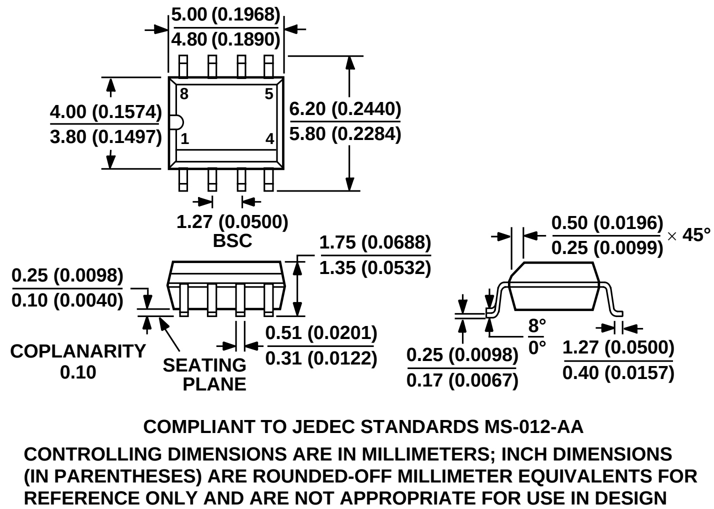

Figure 50. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Ordering Quantity
ADA4841-1YRZ[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	1
ADA4841-1YRZ-R7[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	1,000
ADA4841-1YRZ-RL[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	2,500

[1] Z = Pb-free part.

NOTES

D05614–0–9/05(A)