

No. 1778B

**DM1620****SANYO**

**LIQUID CRYSTAL  
DOT MATRIX DISPLAY MODULE  
16 characters x 2 lines**

**General Description**

The DM1620 is a liquid crystal dot matrix display module that consists of LCD panel LCD-5021, LCD control driver HD44780, driver LC7930 and is capable of providing (16 characters x 2 lines) display. It contains a controller, a data RAM, and a character generator ROM required for providing display. Data interfacing is in 8-bit parallel or 4-bit parallel and data can be written in or read from a microprocessor.

**General Specifications**

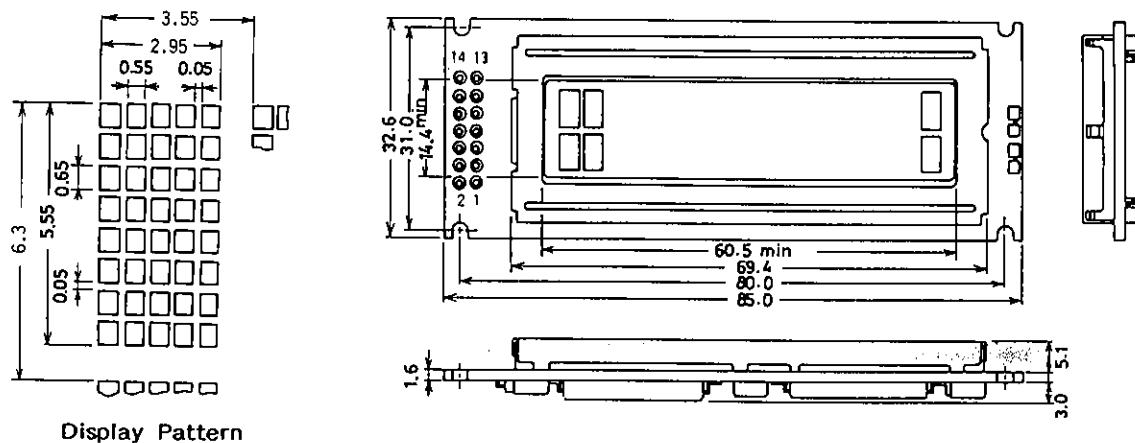
1. Display stem	1/5bias 1/16duty
2. Display content	16 character x 2 lines
3. Dots organizing 1 character	5 x 7 dots/character + cursor
4. Display data RAM	80 x 8 bits
5. Character generator ROM	160-character JIS font set + 32-character special font set Refer to Table 1.
6. Character generator RAM	64 x 8 bits    5 x 7 dots    8 characters
7. Instruction function	Refer to Table 2.
8. Circuit diagram	Refer to Fig. 3

**Outline**

1. Module outline	32.6(W) x 85.0(L) x 10(T) (mm)
2. View area	60.5 x 14.4 (mm)
3. Dot size	0.55 x 0.65 (mm)
4. Dot pitch	0.60 x 0.70 (mm)
5. Character size (5 x 8 dots)	2.95 x 5.55 (mm)

**Absolute Maximum Ratings/Ta=25 °C**

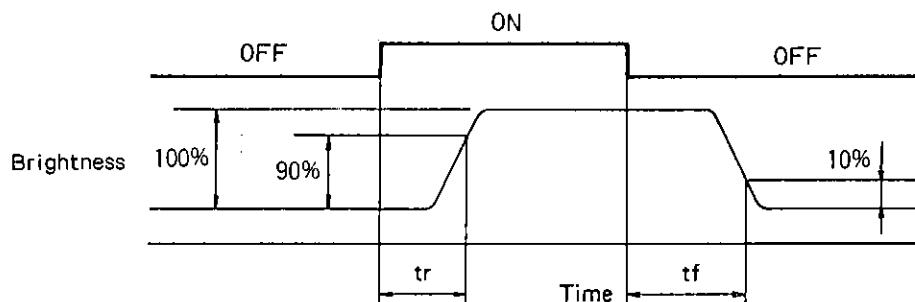
		unit
Supply Voltage	VDD-VSS	-0.3 to +7
Input Voltage	VI	V
Drive Voltage	VDD-VO	-0.3 to VDD+0.3
Operating Temperature	Topr	-0.3 to +9
Storage Temperature	Tstg	0 to +50 °C
		-20 to +70 °C

**Module Dimensions 5000A  
(unit: mm)**

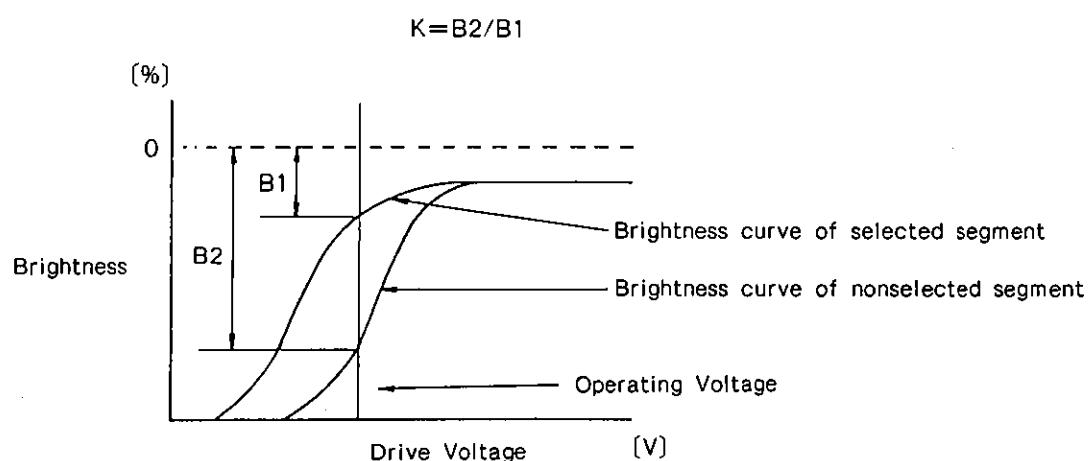
**SANYO Electric Co., Ltd. Semiconductor Business Headquarters**  
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

Electrooptical Characteristics/V<sub>DD</sub>-V<sub>SS</sub>=5.0V, Ta=25°C unless otherwise specified

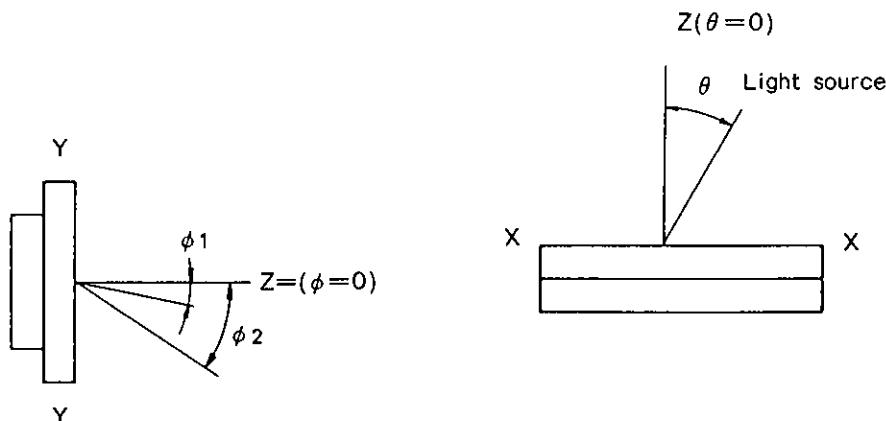
			min	typ	max	unit
Input "High" Voltage	V <sub>IH</sub>		2.2		5.0	V
Input "LOW" Voltage	V <sub>IL</sub>		0		0.5	V
Output "High" Voltage	V <sub>OH</sub>	DB0 to DB7, -I <sub>OH</sub> =0.2mA	2.4			V
Output "Low" Voltage	V <sub>OL</sub>	DB0 to DB7, -I <sub>OL</sub> =1.2mA			0.4	V
Input Current	I <sub>P</sub>	Pull-up MOS V <sub>DD</sub> =5V	50	125	250	μA
Current Dissipation	I <sub>DD</sub>	No input/output current included		(1.2)	2.5	mA
Oscillation Frequency	F <sub>OSC</sub>		190	270	350	kHz
Viewing Angle	θ <sub>2</sub> - θ <sub>1</sub>	K=1.4 θ=0°	20			degree
Contrast Ratio	K	θ=20° θ=0°	3.0			
Rise Time	t <sub>r</sub>	θ=20° θ=0°		150	250	ms
Fall Time	t <sub>f</sub>	θ=20° θ=0°		150	250	ms
LCD Drive Voltage (Recommend Value)	V <sub>DD</sub> -V <sub>O</sub>	Ta=0 °C θ=20°, θ=0°, K≥3	4.4	4.5	4.6	V
	V <sub>DD</sub> -V <sub>O</sub>	Ta=25 °C " " "	4.0	4.1	4.2	V
1/16 duty	V <sub>DD</sub> -V <sub>O</sub>	Ta=50 °C " " "	3.4	3.5	3.6	V

(1) Test Condition for Response Time (t<sub>r</sub>, t<sub>f</sub>)

## (2) Definition of Contrast (K)



## (3) Contrast Ratio Measuring Method



Angles  $\phi$  and  $\theta$  are defined shown above.

The light source is placed in the  $\theta$  direction at an angle of 30° and the sensor is placed in the  $\phi$  direction to measure the contrast.

## Pin Description

No.	Pin Name	Function
1	VSS	(-) power supply pin 0V
2	VDD	(+) power supply pin +5V
3	VO	Pin for applying LCD drive voltage
4	RS	Input pin HI=Data LOW=Instruction
5	R/W	Input pin HI=Read LOW=Write
6	E	Input pin Enable signal
7	DB0	
8	DB1	
9	DB2	
10	DB3	
11	DB4	
12	DB5	
13	DB6	
14	DB7	
Data bus line		

Note 1. The LCD drive voltage can be varied from 3V to 5V by a variable resistor of 5kohm connected across VSS and VO.

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**Timing Characteristics**

			min	typ	max	unit
Enable Cycle Time		$t_{cycE}$	1000			ns
Enable Pulse Width	High level	$PWEH$	450			ns
Enable Rise/Fall time		$t_{Er}, t_{Ef}$			25	ns
Set Up Time	RS/RW-E	$t_{AS}$	140			ns
Address Hold Time		$t_{AH}$	10			ns
Data Delay time		$t_{DDR}$			320	ns
Data Set Up Time		$t_{DSW}$			195	ns
Data Hold Time		$t_H(t_{DHR})$	10 (20)			ns

Figs. 1,2

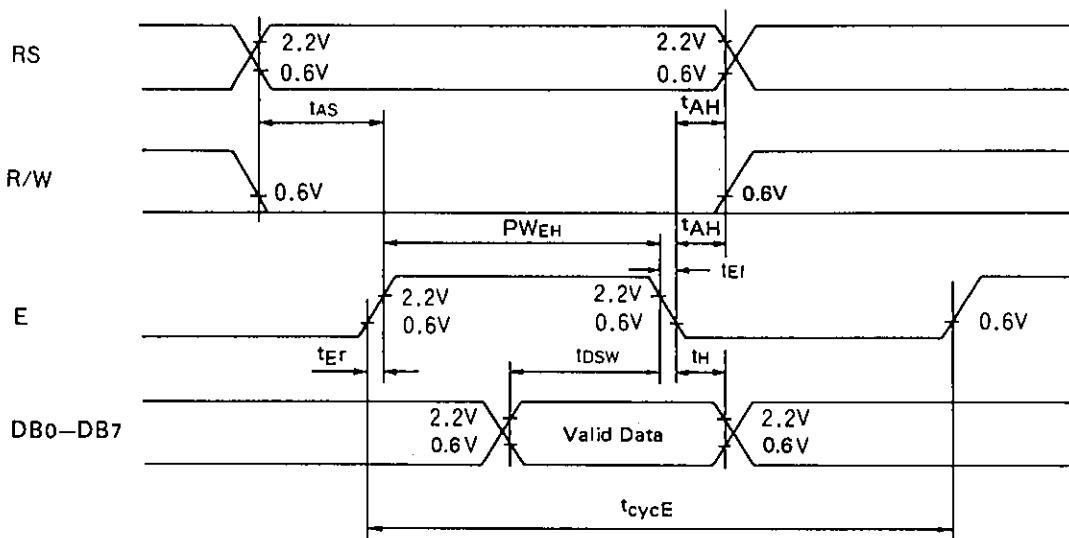
**Write Operation**

Fig. 1 Interface Timing (Data Write)

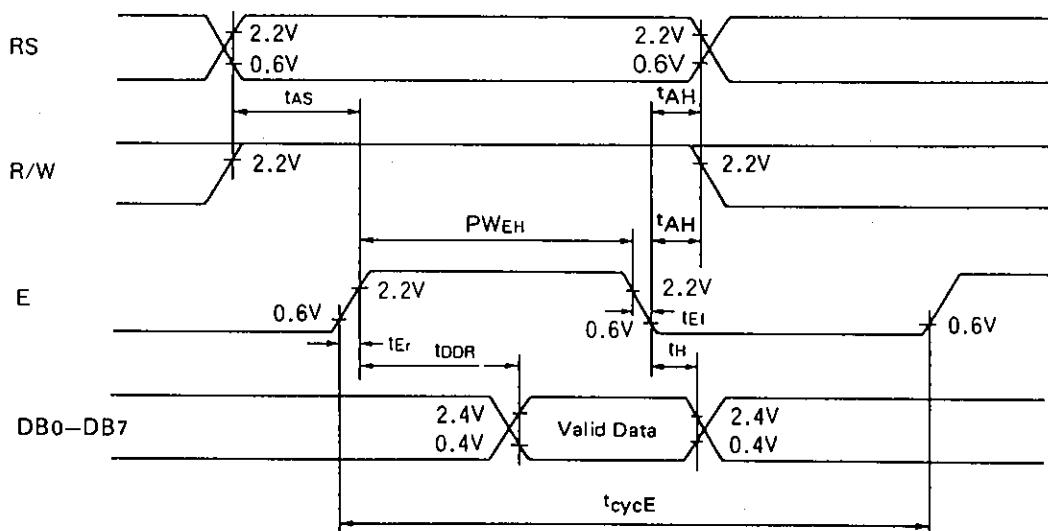
**Read Operation**

Fig. 2 Interface Timing (Data Read)

Table 1 Character code

Low-order 4-bit Hi-order 4-bit	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)		Q	A	P	~	P		~	Q	E	C	P
xxxx0001	(2)	!	I	A	Q	a	g	a	?	F	A	q	q
xxxx0010	(3)	H	2	B	R	b	r	F	Y	Y	Z	P	B
xxxx0011	(4)	#	3	C	S	c	s	J	T	T	E	C	~
xxxx0100	(5)	\$	4	D	T	d	t	X	I	H	H	M	Q
xxxx0101	(6)	Z	5	E	U	e	u	*	A	A	J	S	U
xxxx0110	(7)	R	6	F	U	f	v	P	H	H	Z	P	Z
xxxx0111	(8)	?	7	G	W	g	w	Z	F	Z	S	Q	X
xxxx1000	(1)	C	8	H	X	h	x	4	O	X	Y	J	X
xxxx1001	(2)	O	9	I	Y	i	y	6	T	J	J	V	Y
xxxx1010	(3)	*	:	J	Z	j	z	3	O	N	V	J	F
xxxx1011	(4)	+	;	K	E	k	e	2	T	O	0	X	R
xxxx1100	(5)	,	<	L	Y	l	y	1	P	S	S	V	A
xxxx1101	(6)	---	=	M	O	m	o	>	Z	N	0	t	+
xxxx1110	(7)	,	>	N	^	n	^	+	a	T	t	~	H
xxxx1111	(8)	/	?	O	0	o	0	+	e	Y	?	6	■

(Note) The CG RAM is a character generator RAM used to store the character patterns that can be programmed, as desired, by the user.

Table 2 Instruction function

Instruction	Code											Contents	Execution Time (fOSC=250kHz)															
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0																		
Display clear	0	0	0	0	0	0	0	0	0	1	Clears all display and returns the cursor to the home position (address 0).											82μs to 1.64ms						
Cursor home	0	0	0	0	0	0	0	0	1	*	Returns the cursor to the home position (address 0). Also returns the display being shifted to the original position. The DD RAM contents remain unaffected.											40 μs to 1.6ms						
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets the cursor move direction and specified whether to or not to shift the display. These operations are performed during data write and read.											40μs						
Display ON/OFF control	0	0	0	0	0	0	1	D	C	B	Sets all display ON/OFF(D), cursor ON/OFF(C), cursor position character blink(B).											40μs						
Cursor/display shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves the cursor and shifts the display without affecting the DD RAM contents.											40μs						
Function set	0	0	0	0	1	DL	N	F	*	*	Sets the interface data length (DL), number of display lines (L), and character font (F).											40μs						
CG RAM address set	0	0	0	1	ACG							Sets the CG RAM address. RAM data is sent/received after this setting.											40μs					
DD RAM address set	0	0	1	ADD							Sets the DD RAM address. DD RAM data is sent/received after this setting.											40μs						
Busy flag/address read	0	1	BF	AC							Reads the contents of busy flag (BF) indicating internal operation is in progress and reads the contents of address counter.											1μs						
CG RAM DD RAM data write	1	0	Write Data							Writes data into the DD RAM or CG RAM.											40μs							
CG RAM/ DD RAM data read	1	1	Read Data							Reads data from the DD RAM or CG RAM.											40μs							
	I/D = 1: Increment (+) I/D = 0: Decrement (-) S = 1: Accompanied by display shift S/C = 1: Display shift S/C = 0: Cursor move R/L = 1: Right-shift R/L = 0: Left-shift DL = 1: 8 bits                            DL = 0: 4 bits N = 1: 2 lines                            N = 0: 1 line F = 1: 5 x 10 dots                      F = 0: 5 x 7 dots BF = 1: Internally operating BF = 0: Possible to accept instruction											DD RAM:Display data RAM CG RAM:Character generator RAM ACG: CG RAM address ADD: DD RAM address Corresponds to cursor address. AC: Address counter used for both DD RAM and CG RAM.			The change in the frequency (fOSC) also causes the execution time to be changed. (Example) When fOSC=270kHz, 40μs x 250/270 =37μs.													

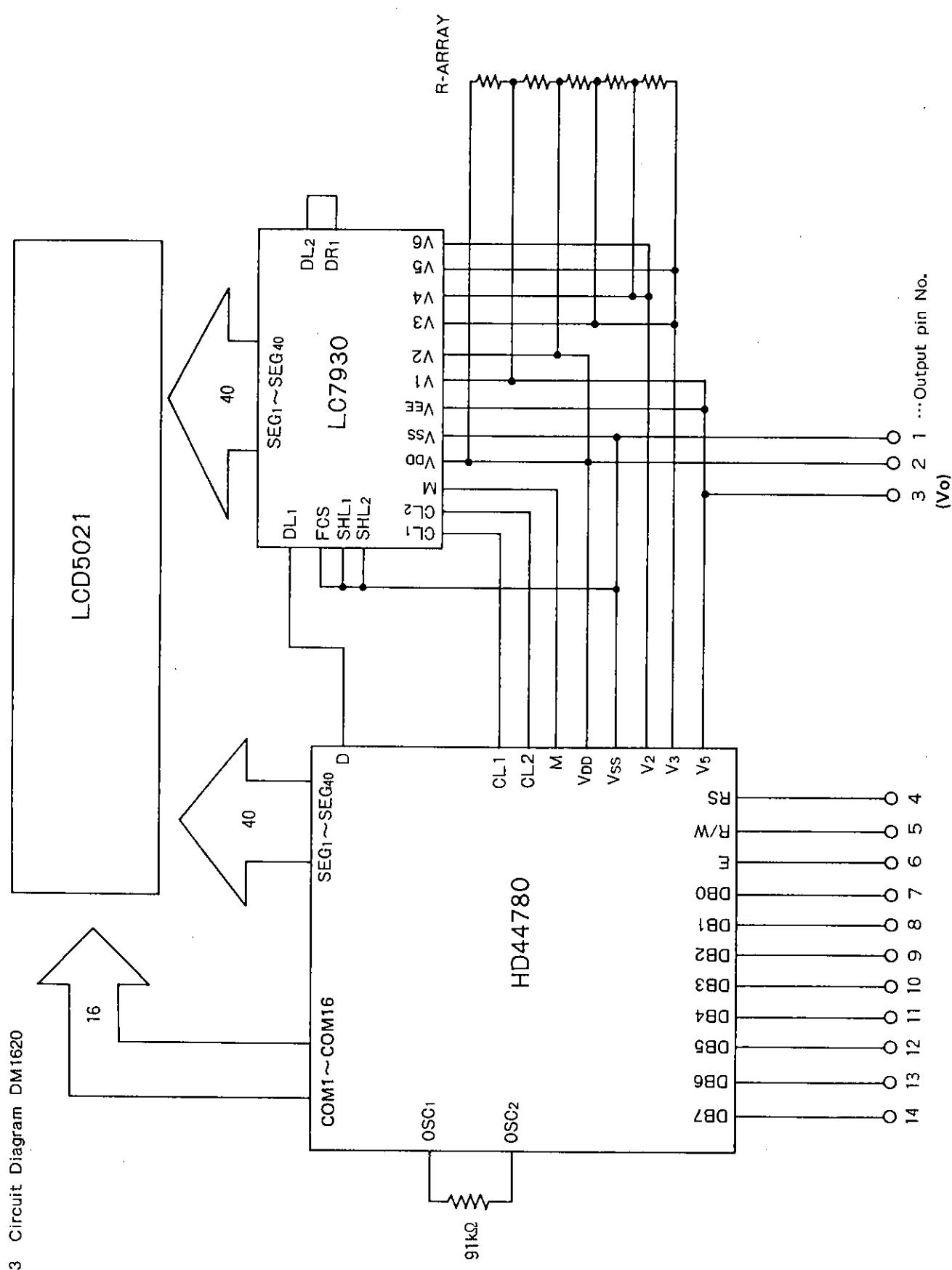


Fig. 3 Circuit Diagram DM1620