

To all our customers

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Renesas Technology Corp.  
Customer Support Dept.  
April 1, 2003

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# HM62V8100I Series

Wide Temperature Range Version  
8 M SRAM (1024-kword × 8-bit)



ADE-203-1278B (Z)  
Rev. 1.0  
Mar. 12, 2002

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## Description

The Hitachi HM62V8100I Series is 8-Mbit static RAM organized 1,048,576-word × 8-bit. HM62V8100I Series has realized higher density, higher performance and low power consumption by employing Hi-CMOS process technology. It offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It is packaged in 48 bumps chip size package with 0.75 mm bump pitch or standard 44-pin TSOP II for high density surface mounting.

## Features

- Single 3.0 V supply: 2.7 V to 3.6 V
- Fast access time: 55 ns (Max)
- Power dissipation:
  - Active: 6.0 mW/MHz (Typ)
  - Standby: 1.5  $\mu$ W (Typ)
- Completely static memory.
  - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output.
  - Three state output
- Battery backup operation.
  - 2 chip selection for battery backup
- Temperature range: -40 to +85°C

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## HM62V8100I Series

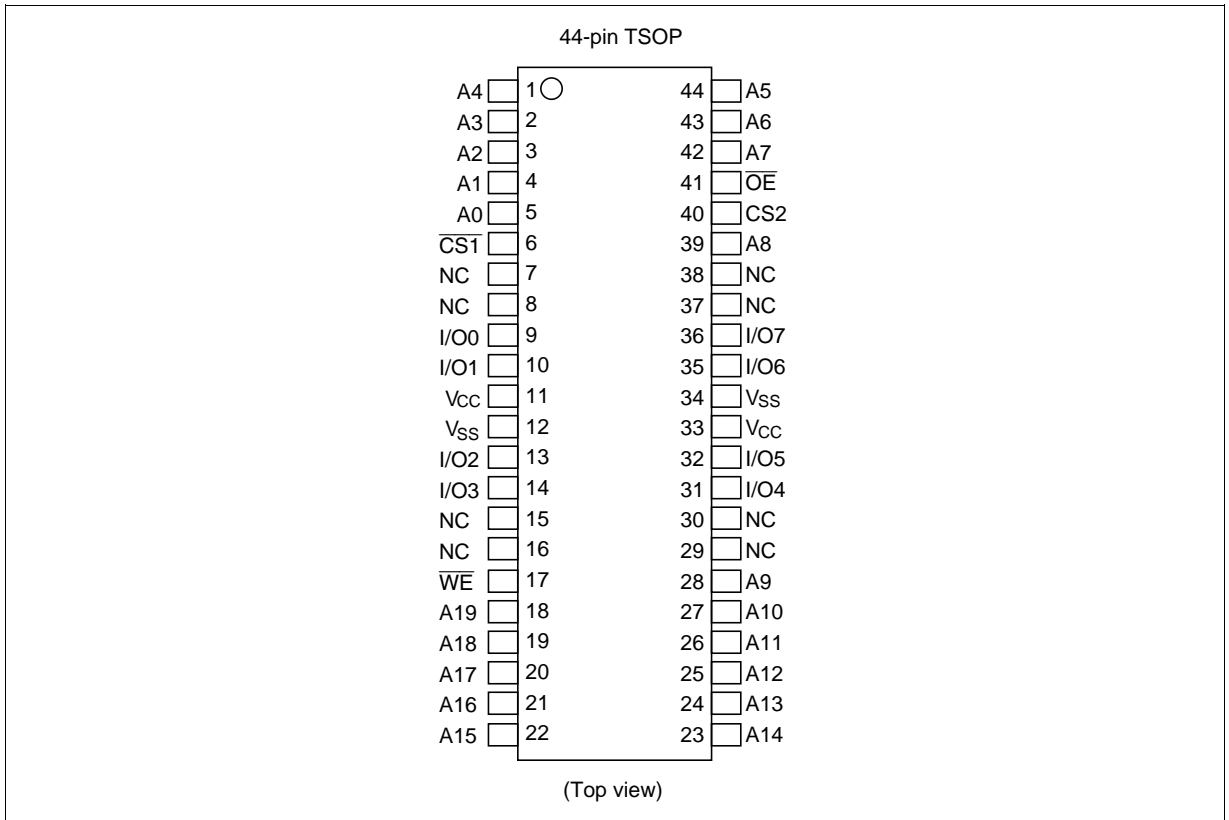
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### Ordering Information

Type No.	Access time	Package
HM62V8100LTTI-5	55 ns	400-mil 44pin plastic TSOP II (normal-bend type) (TTP-44DE)
HM62V8100LTTI-5SL	55 ns	
HM62V8100LBPI-5	55 ns	48-bumps CSP with 0.75 mm bump pitch (TBP-48A)
HM62V8100LBPI-5SL	55 ns	

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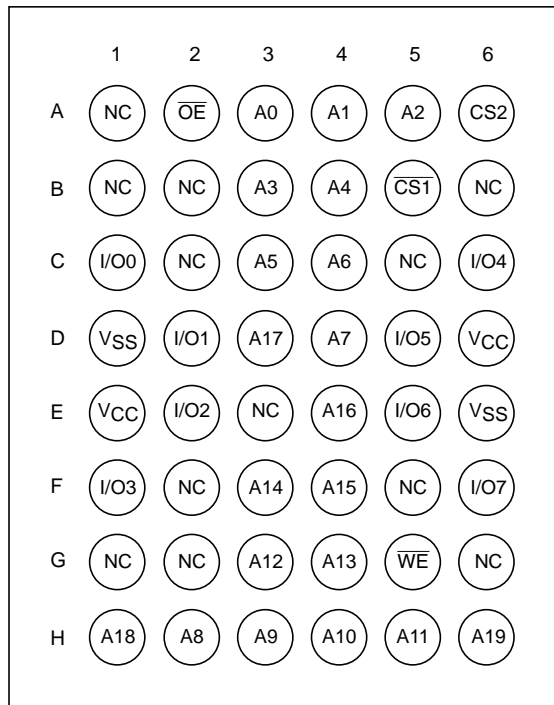
Pin Arrangement



Pin Description (TSOP)

Pin name	Function
A0 to A19	Address input
I/O0 to I/O7	Data input/output
$\overline{CS1}$	Chip select 1
CS2	Chip select 2
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
V <sub>cc</sub>	Power supply
V <sub>ss</sub>	Ground
NC	No connection

48-bumps CSP

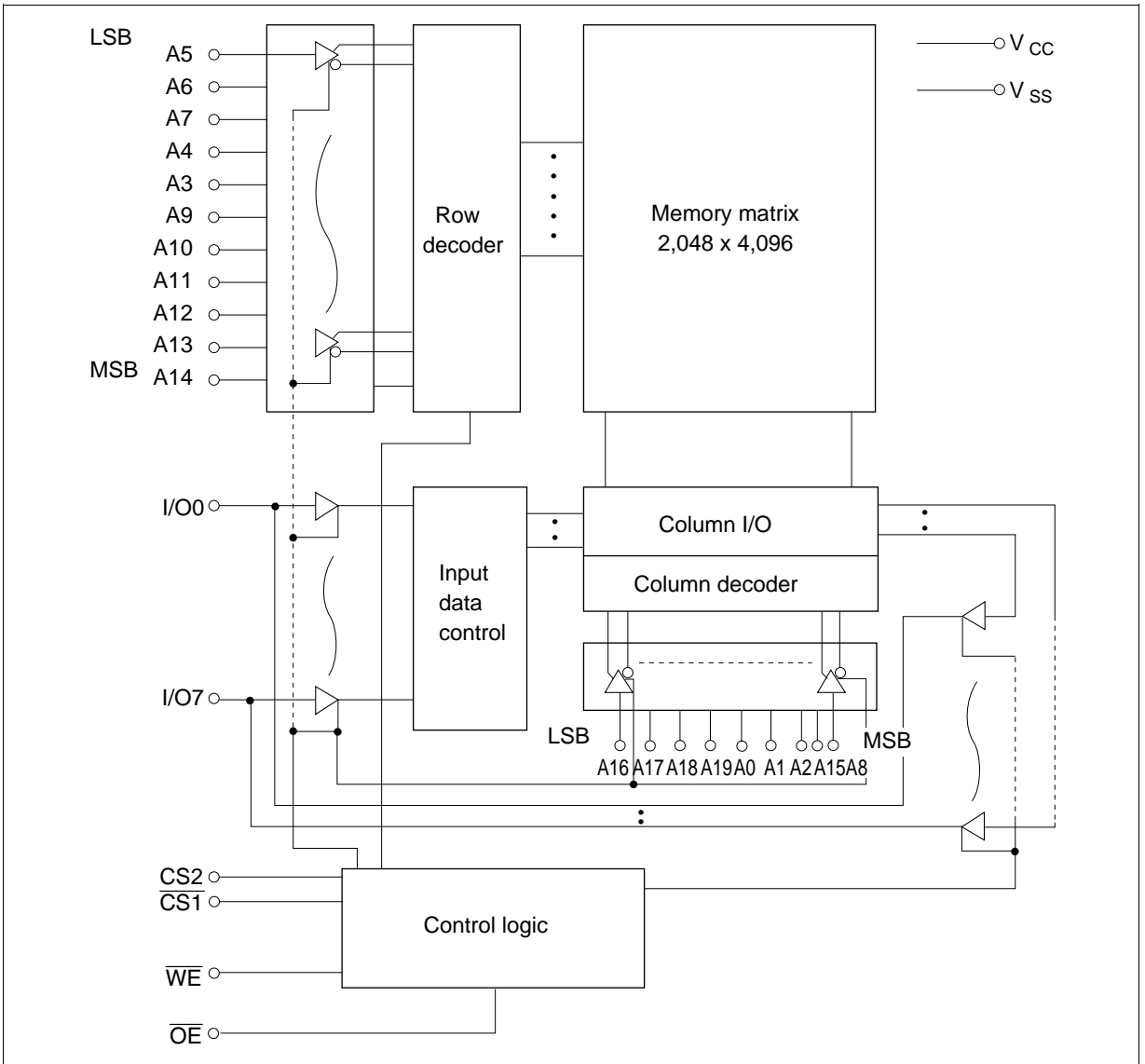


(Top view)

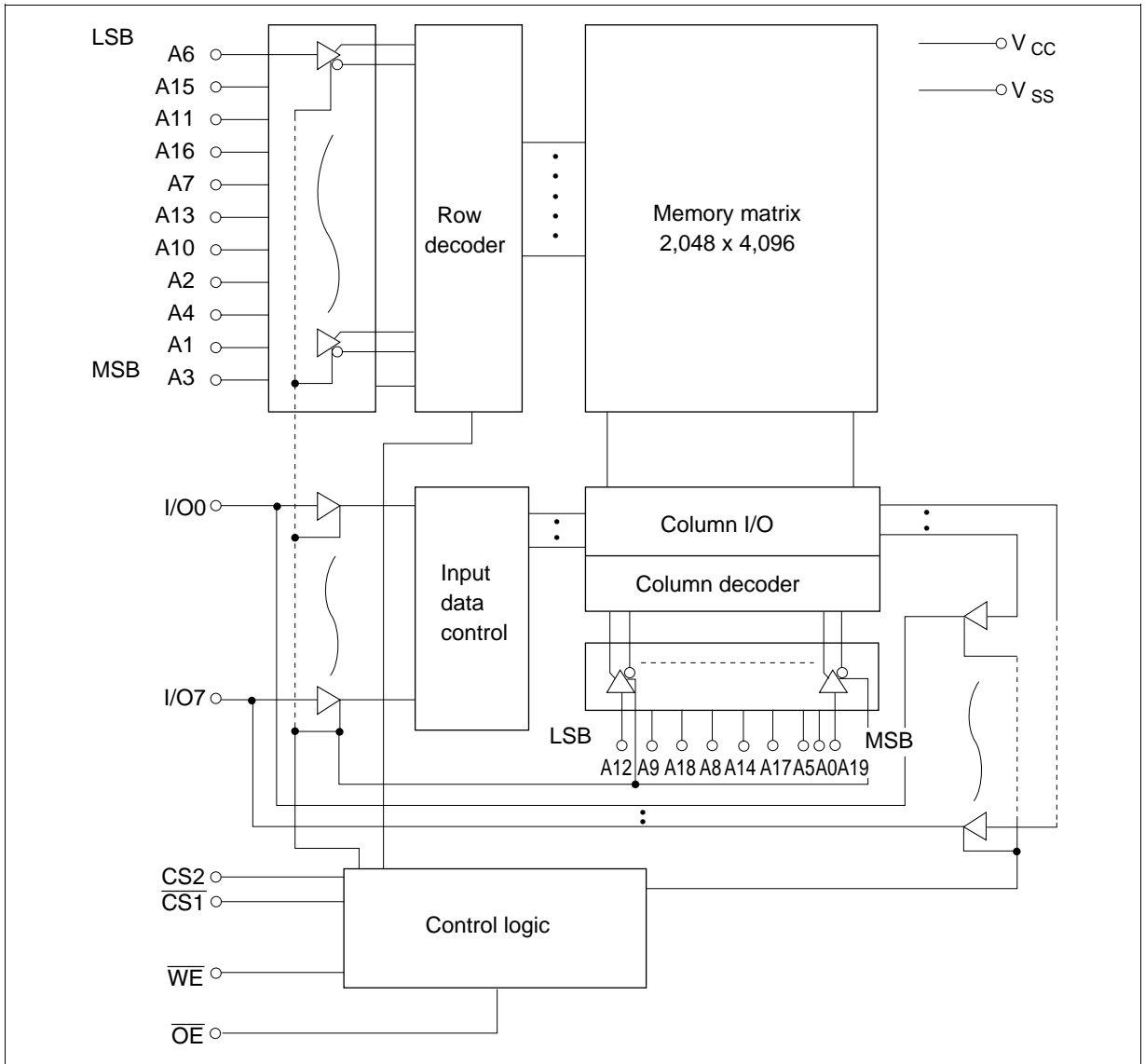
## Pin Description (CSP)

Pin name	Function
A0 to A19	Address input
I/O0 to I/O7	Data input/output
$\overline{CS1}$	Chip select 1
CS2	Chip select 2
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
V <sub>CC</sub>	Power supply
V <sub>SS</sub>	Ground
NC	No connection

Block Diagram (TSOP)



## Block Diagram (CSP)





**Operation Table**

$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	I/O0 to I/O7	Operation
H	x	x	x	High-Z	Standby
x	L	x	x	High-Z	Standby
L	H	H	L	Dout	Read
L	H	L	x	Din	Write
L	H	H	H	High-Z	Output disable

Note: H:  $V_{IH}$ , L:  $V_{IL}$ , x:  $V_{IH}$  or  $V_{IL}$

**Absolute Maximum Ratings**

Parameter	Symbol	Value	Unit
Power supply voltage relative to $V_{SS}$	$V_{CC}$	-0.5 to + 4.6	V
Terminal voltage on any pin relative to $V_{SS}$	$V_T$	-0.5 <sup>*1</sup> to $V_{CC} + 0.3$ <sup>*2</sup>	V
Power dissipation	$P_T$	1.0	W
Storage temperature range	Tstg	-55 to +125	°C
Storage temperature range under bias	Tbias	-40 to +85	°C

Notes: 1.  $V_T$  min: -3.0 V for pulse half-width  $\leq$  30 ns.  
 2. Maximum voltage is +4.6 V.

**DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	$V_{CC}$	2.7	3.0	3.6	V	
	$V_{SS}$	0	0	0	V	
Input high voltage	$V_{IH}$	2.2	—	$V_{CC} + 0.3$	V	
Input low voltage	$V_{IL}$	-0.3	—	0.6	V	1
Ambient temperature range	Ta	-40	—	85	°C	

Note: 1.  $V_{IL}$  min: -3.0 V for pulse half-width  $\leq$  30 ns.

# HM62V8100I Series

## DC Characteristics

Parameter	Symbol	Min	Typ* <sup>1</sup>	Max	Unit	Test conditions
Input leakage current	$ I_{LI} $	—	—	1	$\mu\text{A}$	$V_{in} = V_{SS}$ to $V_{CC}$
Output leakage current	$ I_{LO} $	—	—	1	$\mu\text{A}$	$\overline{CS1} = V_{IH}$ or $CS2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ , or $V_{IO} = V_{SS}$ to $V_{CC}$
Operating current	$I_{CC}$	—	—	20	mA	$\overline{CS1} = V_{IL}$ , $CS2 = V_{IH}$ , Others = $V_{IH}/V_{IL}$ , $I_{IO} = 0$ mA
Average operating current	$I_{CC1}$	—	14	25	mA	Min. cycle, duty = 100%, $I_{IO} = 0$ mA, $\overline{CS1} = V_{IL}$ , $CS2 = V_{IH}$ , Others = $V_{IH}/V_{IL}$
	$I_{CC2}$	—	2	4	mA	Cycle time = 1 $\mu\text{s}$ , duty = 100%, $I_{IO} = 0$ mA, $\overline{CS1} \leq 0.2$ V, $CS2 \geq V_{CC} - 0.2$ V $V_{IH} \geq V_{CC} - 0.2$ V, $V_{IL} \leq 0.2$ V
Standby current	$I_{SB}$	—	0.1	0.3	mA	$CS2 = V_{IL}$
Standby current	$I_{SB1}^{*2}$	—	0.5	25	$\mu\text{A}$	$0 \text{ V} \leq V_{in}$ (1) $0 \text{ V} \leq CS2 \leq 0.2 \text{ V}$ or (2) $\overline{CS1} \geq V_{CC} - 0.2 \text{ V}$ , $CS2 \geq V_{CC} - 0.2 \text{ V}$
	$I_{SB1}^{*3}$	—	0.5	10	$\mu\text{A}$	
Output high voltage	$V_{OH}$	2.2	—	—	V	$I_{OH} = -1$ mA
Output low voltage	$V_{OL}$	—	—	0.4	V	$I_{OL} = 2$ mA

Note: 1. Typical values are at  $V_{CC} = 3.0$  V,  $T_a = +25^\circ\text{C}$  and not guaranteed.

2. This characteristic is guaranteed only for L version.

3. This characteristic is guaranteed only for L-SL version.

## Capacitance ( $T_a = +25^\circ\text{C}$ , $f = 1.0$ MHz)

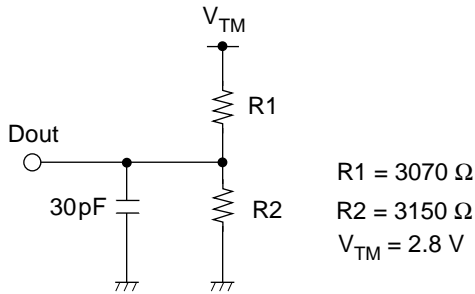
Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Input capacitance	$C_{in}$	—	—	8	pF	$V_{in} = 0$ V	1
Input/output capacitance	$C_{IO}$	—	—	10	pF	$V_{IO} = 0$ V	1

Note: 1. This parameter is sampled and not 100% tested.

**AC Characteristics** ( $T_a = -40$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 2.7$  V to 3.6 V, unless otherwise noted.)

**Test Conditions**

- Input pulse levels:  $V_{IL} = 0.4$  V,  $V_{IH} = 2.2$  V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures (Including scope and jig)



# HM62V8100I Series

## Read Cycle

Parameter	Symbol	HM62V8100I		Unit	Notes
		-5			
		Min	Max		
Read cycle time	$t_{RC}$	55	—	ns	
Address access time	$t_{AA}$	—	55	ns	
Chip select access time	$t_{ACS1}$	—	55	ns	
	$t_{ACS2}$	—	55	ns	
Output enable to output valid	$t_{OE}$	—	35	ns	
Output hold from address change	$t_{OH}$	10	—	ns	
Chip select to output in low-Z	$t_{CLZ1}$	10	—	ns	2, 3
	$t_{CLZ2}$	10	—	ns	2, 3
Output enable to output in low-Z	$t_{OLZ}$	5	—	ns	2, 3
Chip deselect to output in high-Z	$t_{CHZ1}$	0	20	ns	1, 2, 3
	$t_{CHZ2}$	0	20	ns	1, 2, 3
Output disable to output in high-Z	$t_{OHZ}$	0	20	ns	1, 2, 3

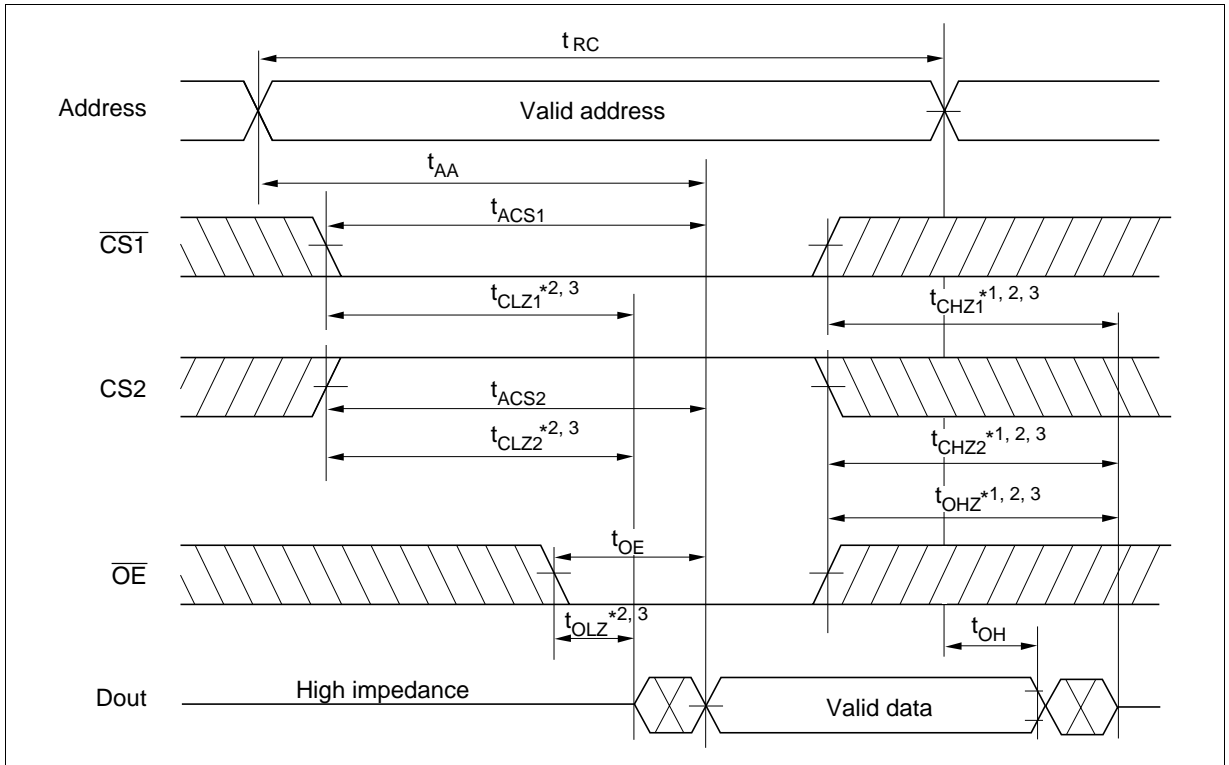
Write Cycle

Parameter	Symbol	HM62V8100I		Unit	Notes
		-5			
		Min	Max		
Write cycle time	$t_{WC}$	55	—	ns	
Address valid to end of write	$t_{AW}$	50	—	ns	
Chip selection to end of write	$t_{CW}$	50	—	ns	5
Write pulse width	$t_{WP}$	40	—	ns	4
Address setup time	$t_{AS}$	0	—	ns	6
Write recovery time	$t_{WR}$	0	—	ns	7
Data to write time overlap	$t_{DW}$	25	—	ns	
Data hold from write time	$t_{DH}$	0	—	ns	
Output active from end of write	$t_{OW}$	5	—	ns	2
Output disable to output in High-Z	$t_{OHZ}$	0	20	ns	1, 2
Write to output in high-Z	$t_{WHZ}$	0	20	ns	1, 2

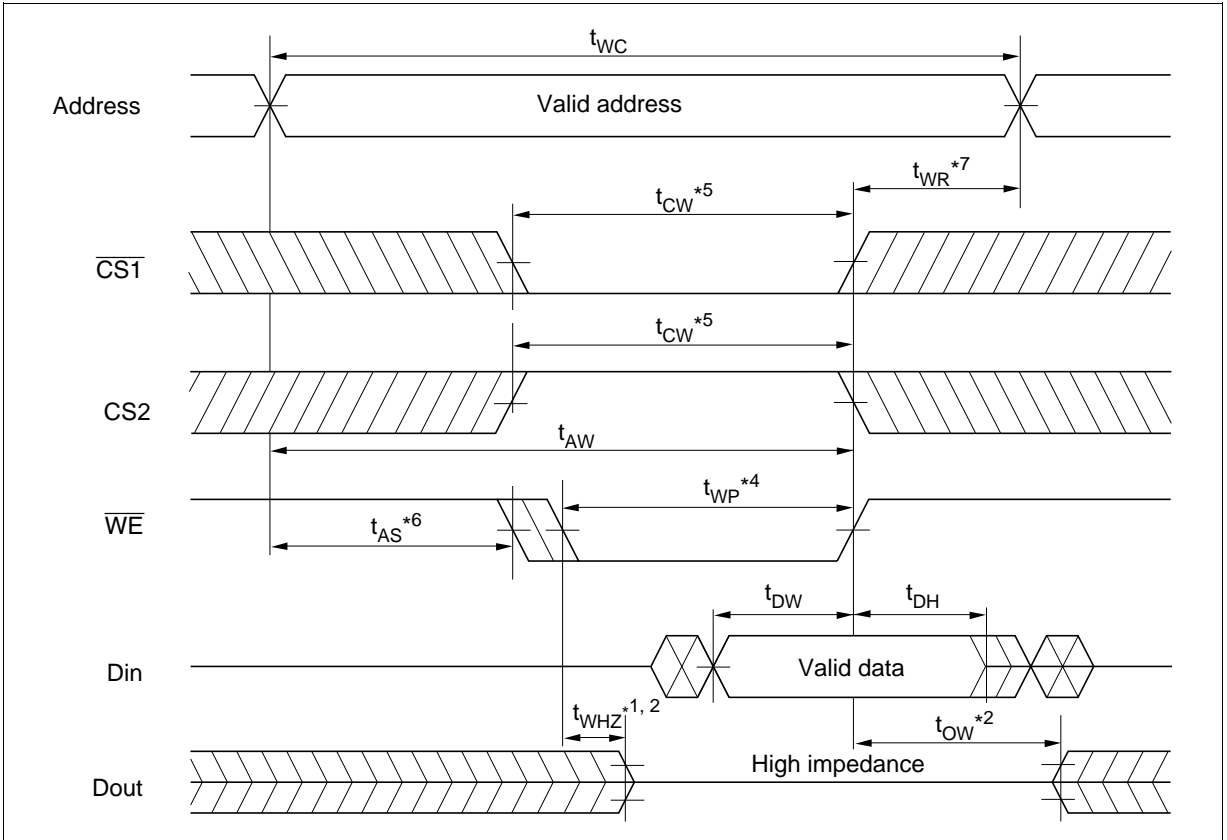
- Notes:
- $t_{CHZ}$ ,  $t_{OHZ}$  and  $t_{WHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
  - This parameter is sampled and not 100% tested.
  - At any given temperature and voltage condition,  $t_{HZ}$  max is less than  $t_{LZ}$  min both for a given device and from device to device.
  - A write occurs during the overlap of a low  $\overline{CS1}$ , a high CS2, a low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS1}$  going low, CS2 going high,  $\overline{WE}$  going low. A write ends at the earliest transition among  $\overline{CS1}$  going high, CS2 going low,  $\overline{WE}$  going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
  - $t_{CW}$  is measured from the later of  $\overline{CS1}$  going low or CS2 going high to the end of write.
  - $t_{AS}$  is measured from the address valid to the beginning of write.
  - $t_{WR}$  is measured from the earliest of  $\overline{CS1}$  or  $\overline{WE}$  going high or CS2 going low to the end of write cycle.

## Timing Waveform

### Read Cycle

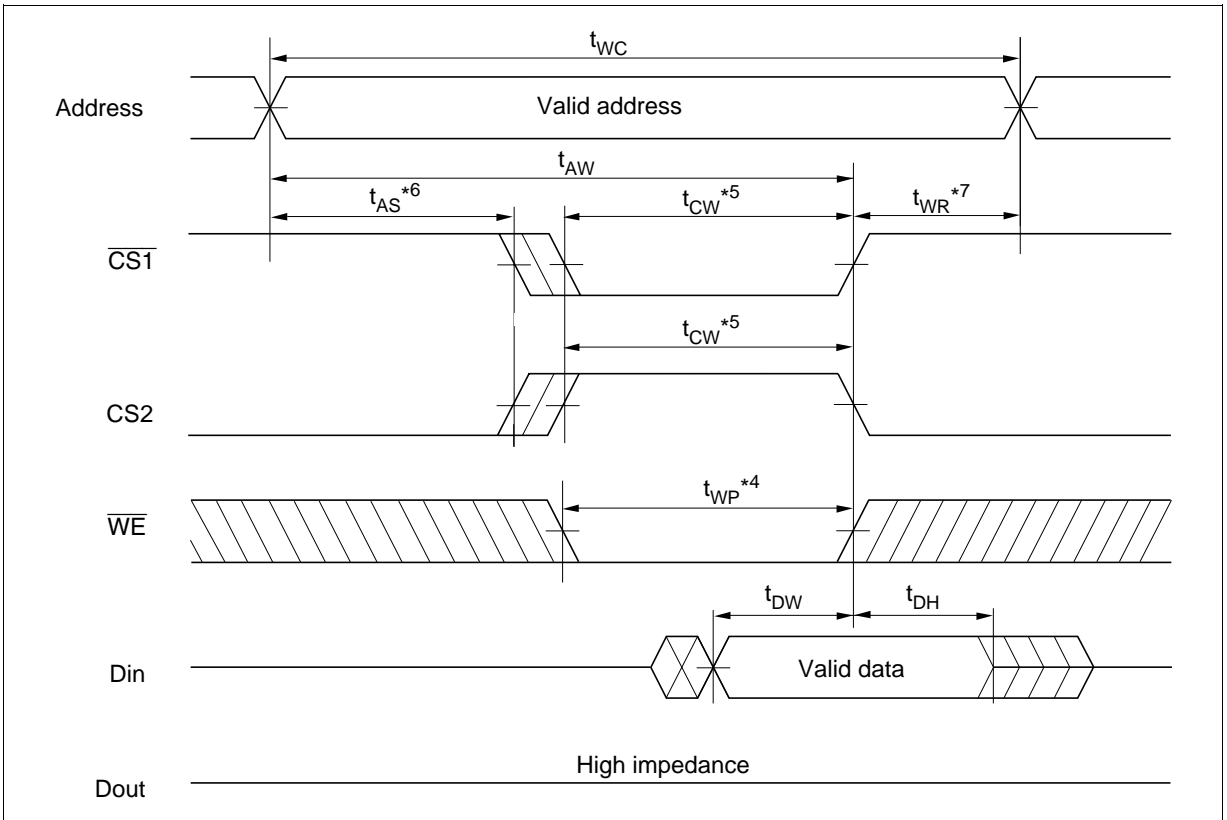


Write Cycle (1) ( $\overline{\text{WE}}$  Clock)



# HM62V8100I Series

Write Cycle (2) ( $\overline{CS}$  Clock,  $\overline{OE} = V_{IH}$ )



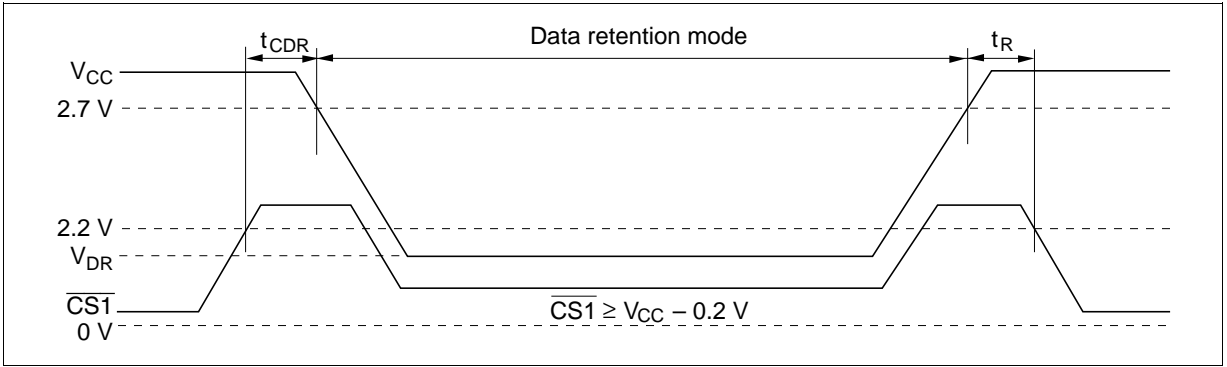


Low  $V_{CC}$  Data Retention Characteristics ( $T_a = -40$  to  $+85^\circ\text{C}$ )

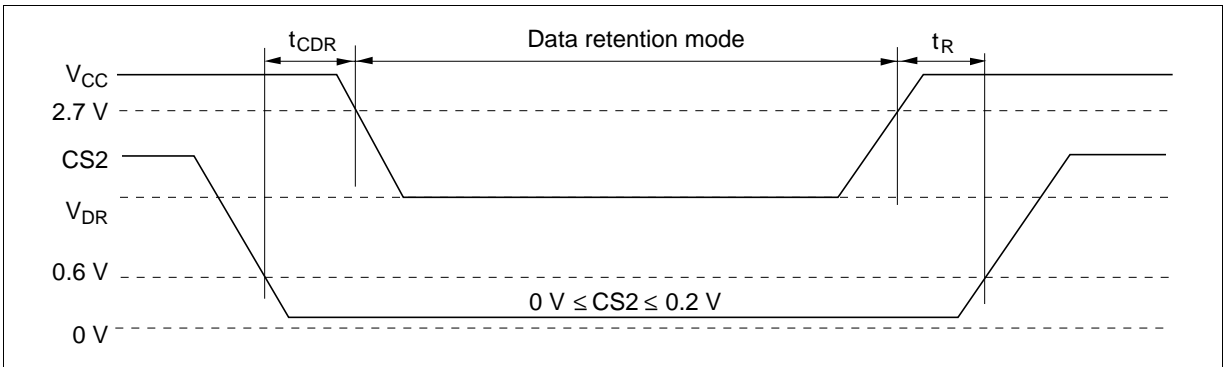
Parameter	Symbol	Min	Typ <sup>*4</sup>	Max	Unit	Test conditions <sup>*3</sup>
$V_{CC}$ for data retention	$V_{DR}$	2.0	—	3.6	V	$V_{in} \geq 0V$ (1) $0V \leq CS2 \leq 0.2V$ or (2) $CS2 \geq V_{CC} - 0.2V$ $\overline{CS1} \geq V_{CC} - 0.2V$
Data retention current	$I_{CCDR}^{*1}$	—	0.5	25	$\mu\text{A}$	$V_{CC} = 3.0V, V_{in} \geq 0V$ (1) $0V \leq CS2 \leq 0.2V$ or (2) $CS2 \geq V_{CC} - 0.2V,$ $\overline{CS1} \geq V_{CC} - 0.2V$
	$I_{CCDR}^{*2}$	—	0.5	10	$\mu\text{A}$	
Chip deselect to data retention time	$t_{CDR}$	0	—	—	ns	See retention waveform
Operation recovery time	$t_R$	$t_{RC}^{*5}$	—	—	ns	

- Notes:
1. This characteristic is guaranteed only for L version.
  2. This characteristic is guaranteed only for L-SL version.
  3. CS2 controls address buffer,  $\overline{WE}$  buffer,  $\overline{CS1}$  buffer,  $\overline{OE}$  buffer and Din buffer. If CS2 controls data retention mode,  $V_{in}$  levels (address,  $\overline{WE}$ ,  $\overline{OE}$ ,  $\overline{CS1}$ , I/O) can be in the high impedance state. If  $\overline{CS1}$  controls data retention mode, CS2 must be  $CS2 \geq V_{CC} - 0.2V$  or  $0V \leq CS2 \leq 0.2V$ . The other input levels (address,  $\overline{WE}$ ,  $\overline{OE}$ , I/O) can be in the high impedance state.
  4. Typical values are at  $V_{CC} = 3.0V, T_a = +25^\circ\text{C}$  and not guaranteed.
  5.  $t_{RC}$  = read cycle time.

## Low $V_{CC}$ Data Retention Timing Waveform (1) ( $\overline{CS1}$ Controlled)



## Low $V_{CC}$ Data Retention Timing Waveform (2) (CS2 Controlled)

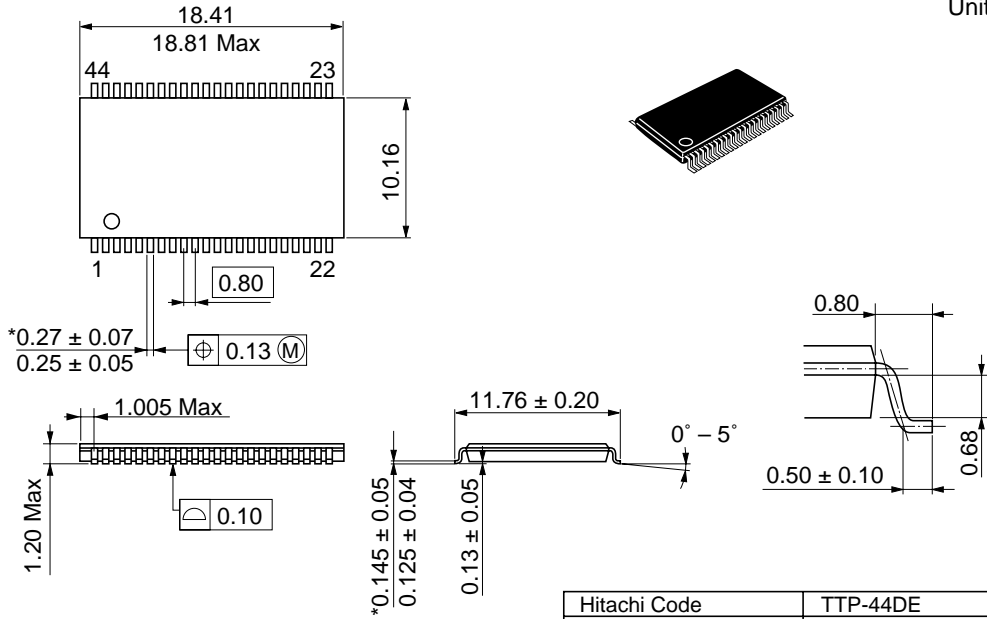


Package Dimensions

HM62V8100LTTI Series (TTP-44DE)

As of July, 2001

Unit: mm



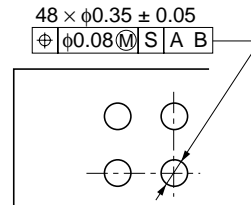
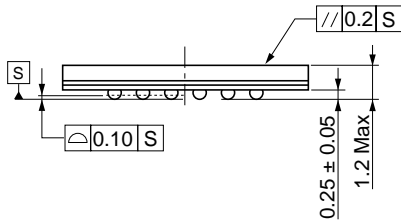
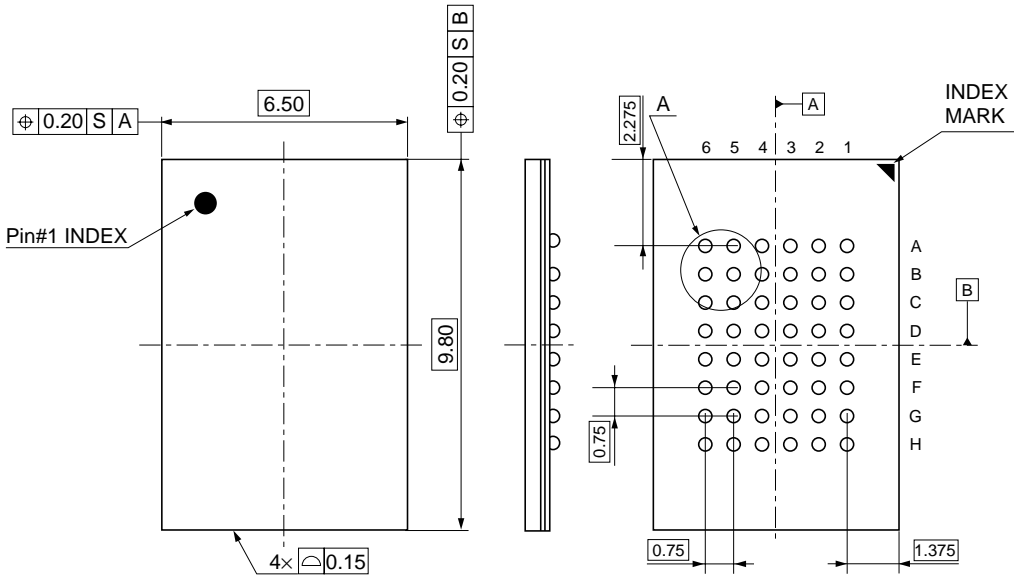
\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	TTP-44DE
JEDEC	—
JEITA	—
Mass (reference value)	0.43 g

# HM62V8100I Series

## HM62V8100LBPI Series (TBP-48A)

As of July, 2001  
Unit: mm



Details of the part A

Hitachi Code	TBP-48A
JEDEC	-
JEITA	-
Mass (reference value)	0.13 g

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**Hitachi, Ltd.**

Semiconductor & Integrated Circuits  
 Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan  
 Tel: (03) 3270-2111 Fax: (03) 3270-5109

URL <http://www.hitachisemiconductor.com/>

**For further information write to:**

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