LT1113

Dual Low Noise, Precision, JFET Input Op Amps

FEATURES

- 100% Tested Low Voltage Noise: $6nV/\sqrt{Hz}$ Max
- SO-8 Package Standard Pinout
- Voltage Gain: 1.2 Million Min
- Offset Voltage: 1.5mV Max
- Offset Voltage Drift: 15μV/°C Max
- Input Bias Current, Warmed Up: 450pA Max
- Gain Bandwidth Product: 5.6MHz Typ
- Guaranteed Specifications with ±5V Supplies
- Guaranteed Matching Specifications

APPLICATIONS

- Photocurrent Amplifiers
- Hydrophone Amplifiers
- High Sensitivity Piezoelectric Accelerometers
- Low Voltage and Current Noise Instrumentation Amplifier Front Ends
- Two and Three Op Amp Instrumentation Amplifiers
- Active Filters

DESCRIPTION

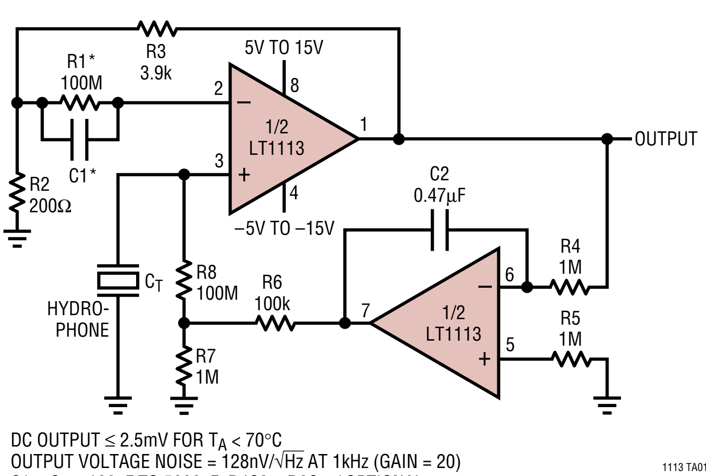
The LT®1113 achieves a new standard of excellence in noise performance for a dual JFET op amp. The $4.5nV/\sqrt{Hz}$ 1kHz noise combined with low current noise and picoampere bias currents makes the LT1113 an ideal choice for amplifying low level signals from high impedance capacitive transducers.

The LT1113 is unconditionally stable for gains of 1 or more, even with load capacitances up to 1000pF. Other key features are 0.4mV V_{OS} and a voltage gain of 4 million. Each individual amplifier is 100% tested for voltage noise, slew rate and gain bandwidth.

The design of the LT1113 has been optimized to achieve true precision performance with an industry standard pinout in the S0-8 package. A set of specifications are provided for ±5V supplies and a full set of matching specifications are provided to facilitate the use of the LT1113 in matching dependent applications such as instrumentation amplifier front ends.

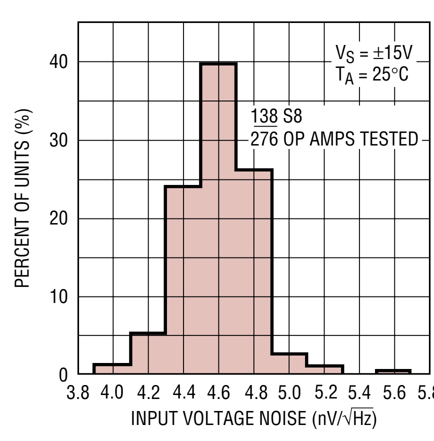
TYPICAL APPLICATION

Low Noise Hydrophone Amplifier with DC Servo



DC OUTPUT ≤ 2.5mV FOR T_A < 70°C
OUTPUT VOLTAGE NOISE = $128nV/\sqrt{Hz}$ AT 1kHz (GAIN = 20)
C1 ≈ C_T ≈ 100pF TO 5000pF; R4C2 > R8C_T; *OPTIONAL

1kHz Input Noise Voltage Distribution



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage
- –55°C to 105°C .... ±20V
- 105°C to 125°C .... ±16V

Differential Input Voltage .... ±40V
Input Voltage (Equal to Supply Voltage) .... ±20V
Output Short Circuit Duration .... 1 Minute
Storage Temperature Range .... –65°C to 150°C

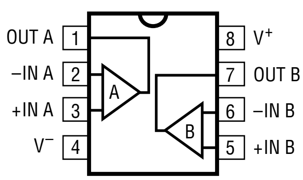
Operating Temperature Range
- LT1113AC/LT1113C (Note 2) .... –40°C to 85°C
- LT1113AM/LT1113M .... –55°C to 125°C

Specified Temperature Range
- LT1113AC/LT1113C (Note 3) .... –40°C to 85°C
- LT1113AM/LT1113M .... –55°C to 125°C

Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW



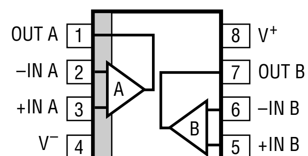
J8 PACKAGE 8-LEAD CERDIP　N8 PACKAGE 8-LEAD PDIP

T_{JMAX} = 160°C, θ_{JA} = 100°C/W (J8)
T_{JMAX} = 150°C, θ_{JA} = 130°C/W (N8)

ORDER PART NUMBER

LT1113AMJ8
LT1113MJ8
LT1113ACN8
LT1113CN8

TOP VIEW



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 190°C/W

ORDER PART NUMBER

LT1113CS8

S8 PART MARKING

1113

Consult factory for Industrial grade parts.

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $V_{CM} = 0V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 4)	LT1113AM/AC MIN	TYP	MAX	LT1113M/C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage			0.40	1.5		0.50	1.8	mV
		$V_S = \pm5V$		0.45	1.7		0.55	2.0	mV
I_{OS}	Input Offset Current	Warmed Up (Note 5)		30	100		35	150	pA
I_B	Input Bias Current	Warmed Up (Note 5)		300	450		320	480	pA
e_n	Input Noise Voltage	0.1Hz to 10Hz		2.4			2.4		μV_{P-P}
	Input Noise Voltage Density	f_O = 10Hz		17			17		$nV/\sqrt{Hz}$
		f_O = 1000Hz		4.5	6.0		4.5	6.0	$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f_O = 10Hz, f_O = 1000Hz (Note 6)		10			10		$fA/\sqrt{Hz}$
R_{IN}	Input Resistance								
	Differential Mode			10^{11}			10^{11}		Ω
	Common Mode	V_{CM} = –10V to 8V		10^{11}			10^{11}		Ω
		V_{CM} = 8V to 11V		10^{10}			10^{10}		Ω
C_{IN}	Input Capacitance			14			14		pF
		$V_S = \pm5V$		27			27		pF
V_{CM}	Input Voltage Range (Note 7)		13.0	13.5		13.0	13.5		V
			–10.5	–11.0		–10.5	–11.0		V
CMRR	Common Mode Rejection Ratio	V_{CM} = –10V to 13V	85	98		82	95		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm4.5V$ to $\pm20V$	86	100		83	98		dB
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm12V$, R_L = 10k	1200	4800		1000	4500		V/mV
		$V_O = \pm10V$, R_L = 1k	600	4000		500	3000		V/mV

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $V_{CM} = 0V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1113AM/AC MIN	LT1113AM/AC TYP	LT1113AM/AC MAX	LT1113M/C MIN	LT1113M/C TYP	LT1113M/C MAX	UNITS
V_{OUT}	Output Voltage Swing	$R_L = 10k$ $R_L = 1k$	±13.5 ±12.0	±13.8 ±13.0		±13.0 ±11.5	±13.8 ±13.0		V V
SR	Slew Rate	$R_L \geq 2k$ (Note 9)	2.3	3.9		2.3	3.9		V/µs
GBW	Gain Bandwidth Product	$f_O = 100kHz$	4.0	5.6		4.0	5.6		MHz
t_S	Settling Time	0.01%, $A_V = +1$, $R_L = 1k$, $C_L \leq 1000pF$, 10V Step		4.2			4.2		µs
	Channel Separation	$f_O = 10Hz$, $V_O = \pm10V$, $R_L = 1k$		130			126		dB
I_S	Supply Current per Amplifier	 $V_S = \pm5V$		5.3 5.3	6.25 6.20		5.3 5.3	6.50 6.45	mA mA
ΔV_{OS}	Offset Voltage Match			0.8	2.5		0.8	3.3	mV
ΔI_B^+	Noninverting Bias Current Match	Warmed Up (Note 5)		10	80		10	120	pA
ΔCMRR	Common Mode Rejection Match	(Note 11)	81	94		78	94		dB
ΔPSRR	Power Supply Rejection Match	(Note 11)	82	95		80	95		dB

The ● denotes specifications which apply over the temperature range $0°C \leq T_A \leq 70°C$. $V_S = \pm15V$, $V_{CM} = 0V$, unless otherwise noted. (Note 12)

SYMBOL	PARAMETER	CONDITIONS (Note 4)		LT1113AC MIN	LT1113AC TYP	LT1113AC MAX	LT1113C MIN	LT1113C TYP	LT1113C MAX	UNITS
V_{OS}	Input Offset Voltage	 $V_S = \pm5V$	● ●		0.6 0.7	2.1 2.3		0.7 0.8	2.5 2.7	mV mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift	(Note 8)	●		7	15		8	20	µV/°C
I_{OS}	Input Offset Current		●		50	350		55	450	pA
I_B	Input Bias Current		●		600	1200		700	1600	pA
V_{CM}	Input Voltage Range		● ●	12.9 −10.0	13.4 −10.8		12.9 −10.0	13.4 −10.8		V V
CMRR	Common Mode Rejection Ratio	$V_{CM} = -10V$ to 12.9V	●	81	97		79	94		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm4.5V$ to $\pm20V$	●	83	99		81	97		dB
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm12V$, $R_L = 10k$ $V_O = \pm10V$, $R_L = 1k$	● ●	900 500	3600 2600		800 400	3400 2400		V/mV V/mV
V_{OUT}	Output Voltage Swing	$R_L = 10k$ $R_L = 1k$	● ●	±13.2 ±11.7	±13.5 ±12.7		±12.7 ±11.3	±13.5 ±12.7		V V
SR	Slew Rate	$R_L \geq 2k$ (Note 9)	●	2.1	3.7		1.7	3.7		V/µs
GBW	Gain Bandwidth Product	$f_O = 100kHz$	●	3.2	4.5		3.2	4.5		MHz
I_S	Supply Current per Amplifier	 $V_S = \pm5V$	● ●		5.3 5.3	6.35 6.30		5.3 5.3	6.55 6.50	mA mA
ΔV_{OS}	Offset Voltage Match		●		0.9	3.5		0.9	4.5	mV
ΔI_B^+	Noninverting Bias Current Match		●		30	300		35	400	pA
ΔCMRR	Common Mode Rejection Match	(Note 11)	●	76	93		74	93		dB
ΔPSRR	Power Supply Rejection Match	(Note 11)	●	79	93		77	93		dB

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the temperature range $-40°C \le T_A \le 85°C$. $V_S = \pm15V$, $V_{CM} = 0V$, unless otherwise noted. (Note 10)

SYMBOL	PARAMETER	CONDITIONS (Note 4)		LT1113AC MIN	LT1113AC TYP	LT1113AC MAX	LT1113C MIN	LT1113C TYP	LT1113C MAX	UNITS
V_{OS}	Input Offset Voltage		●		0.7	2.4		0.8	2.8	mV
		$V_S = \pm5V$	●		0.8	2.6		0.9	3.0	mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift		●		7	15		8	20	µV/°C
I_{OS}	Input Offset Current		●		80	700		90	1000	pA
I_B	Input Bias Current		●		1750	3000		1800	5000	pA
V_{CM}	Input Voltage Range		●	12.6	13.0		12.6	13.0		V
			●	−10.0	−10.5		−10.0	−10.5		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = -10V$ to $12.6V$	●	80	96		78	93		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm4.5V$ to $\pm20V$	●	81	98		79	96		dB
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm12V$, $R_L = 10k$	●	850	3300		750	3000		V/mV
		$V_O = \pm10V$, $R_L = 1k$	●	400	2200		300	2000		V/mV
V_{OUT}	Output Voltage Swing	$R_L = 10k$	●	±13.0	±12.5		±12.5	±12.5		V
		$R_L = 1k$	●	±11.5	±12.0		±11.0	±12.0		V
SR	Slew Rate	$R_L \ge 2k$	●	2.0	3.5		1.6	3.5		V/µs
GBW	Gain Bandwidth Product	$f_O = 100kHz$	●	2.9	4.3		2.9	4.3		MHz
I_S	Supply Current per Amplifier		●		5.30	6.35		5.30	6.55	mA
		$V_S = \pm5V$	●		5.25	6.30		5.25	6.50	mA
ΔV_{OS}	Offset Voltage Match		●		1.0	4.4		1.0	5.1	mV
ΔI_B^+	Noninverting Bias Current Match		●		50	600		55	900	pA
ΔCMRR	Common Mode Rejection Match	(Note 11)	●	76	93		73	93		dB
ΔPSRR	Power Supply Rejection Match	(Note 11)	●	77	92		75	92		dB

The ● denotes specifications which apply over the temperature range $-55°C \le T_A \le 125°C$. $V_S = \pm15V$, $V_{CM} = 0V$, unless otherwise noted. (Note 12)

SYMBOL	PARAMETER	CONDITIONS (Note 4)		LT1113AM MIN	LT1113AM TYP	LT1113AM MAX	LT1113M MIN	LT1113M TYP	LT1113M MAX	UNITS
V_{OS}	Input Offset Voltage		●		0.8	2.7		0.9	3.3	mV
		$V_S = \pm5V$	●		0.8	2.8		0.9	3.4	mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift	(Note 8)	●		5	12		8	15	µV/°C
I_{OS}	Input Offset Current		●		0.8	15		1.0	25	nA
I_B	Input Bias Current		●		25	50		27	70	nA
V_{CM}	Input Voltage Range		●	12.6	13.0		12.6	13.0		V
			●	−10.0	−10.4		−10.0	−10.4		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = -10V$ to $12.6V$	●	79	95		77	92		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm4.5V$ to $\pm20V$	●	80	97		78	95		dB

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the temperature range $-55°C \le T_A \le 125°C$. $V_S = \pm15V$, $V_{CM} = 0V$, unless otherwise noted. (Note 12)

SYMBOL	PARAMETER	CONDITIONS (Note 4)		LT1113AM MIN	LT1113AM TYP	LT1113AM MAX	LT1113M MIN	LT1113M TYP	LT1113M MAX	UNITS
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm12V$, $R_L = 10k$	●	800	2700		700	2500		V/mV
		$V_O = \pm10V$, $R_L = 1k$	●	400	1500		300	1000		V/mV
V_{OUT}	Output Voltage Swing	$R_L = 10k$	●	±13.0	±12.5		±12.5	±12.5		V
		$R_L = 1k$	●	±11.5	±12.0		±11.0	±12.0		V
SR	Slew Rate	$R_L \ge 2k$ (Note 9)	●	1.9	3.3		1.6	3.3		V/µs
GBW	Gain Bandwidth Product	$f_O = 100kHz$	●	2.2	3.4		2.2	3.4		MHz
I_S	Supply Current Per Amplifier		●		5.30	6.35		5.30	6.55	mA
		$V_S = \pm5V$	●		5.25	6.30		5.25	6.50	mA
ΔV_{OS}	Offset Voltage Match		●		1.0	5.0		1.0	5.5	mV
ΔI_B^+	Noninverting Bias Current Match		●		1.8	12		2.0	20	nA
ΔCMRR	Common Mode Rejection Match	(Note 11)	●	75	92		73	92		dB
ΔPSRR	Power Supply Rejection Match	(Note 11)	●	76	91		74	91		dB

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: The LT1113C is guaranteed functional over the Operating Temperature Range of –40°C to 85°C. The LT1113M is guaranteed functional over the Operating Temperature Range of –55°C to 125°C.

Note 3: The LT1113C is guaranteed to meet specified performance from 0°C to 70°C. The LT1113C is designed, characterized and expected to meet specified performance from –40°C to 85°C but is not tested or QA sampled at these temperatures. For guaranteed I grade parts, consult the factory. The LT1113M is guaranteed to meet specified performance from –55°C to 125°C.

Note 4: Typical parameters are defined as the 60% yield of parameter distributions of individual amplifiers, i.e., out of 100 LT1113s (200 op amps) typically 120 op amps will be better than the indicated specification.

Note 5: Warmed-up I_B and I_{OS} readings are extrapolated to a chip temperature of 50°C from 25°C measurements and 50°C characterization data.

Note 6: Current noise is calculated from the formula:

$$i_n = (2qI_B)^{1/2}$$

where $q = 1.6 \cdot 10^{-19}$ coulomb. The noise of source resistors up to 200M swamps the contribution of current noise.

Note 7: Input voltage range functionality is assured by testing offset voltage at the input voltage range limits to a maximum of 2.3mV (A grade) to 2.8mV (C grade).

Note 8: This parameter is not 100% tested.

Note 9: Slew rate is measured in $A_V = -1$; input signal is ±7.5V, output measured at ±2.5V.

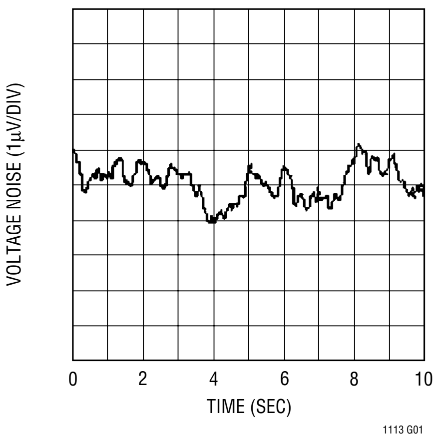
Note 10: The LT1113 is designed, characterized and expected to meet these extended temperature limits, but is not tested at –40°C and 85°C. Guaranteed I grade parts are available. Consult factory.

Note 11: ΔCMRR and ΔPSRR are defined as follows:
(1) CMRR and PSRR are measured in µV/V on the individual amplifiers.
(2) The difference is calculated between the matching sides in µV/V.
(3) The result is converted to dB.

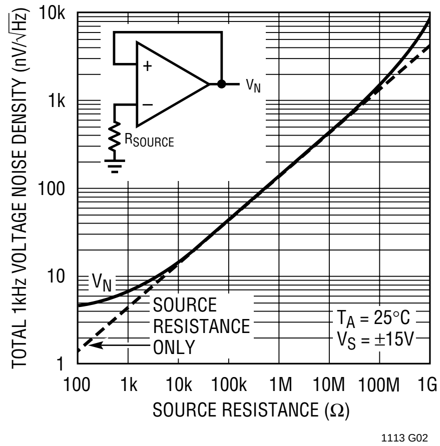
Note 12: The LT1113 is measured in an automated tester in less than one second after application of power. Depending on the package used, power dissipation, heat sinking, and air flow conditions, the fully warmed-up chip temperature can be 10°C to 50°C higher than the ambient temperature.

TYPICAL PERFORMANCE CHARACTERISTICS

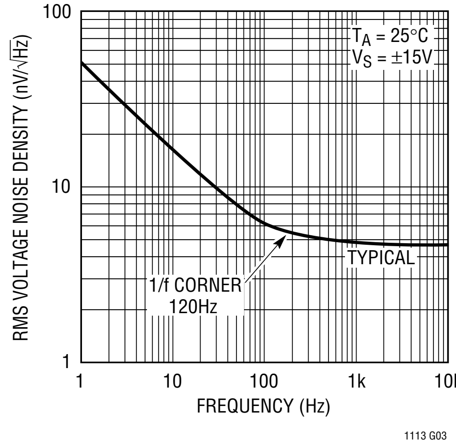
0.1Hz to 10Hz Voltage Noise



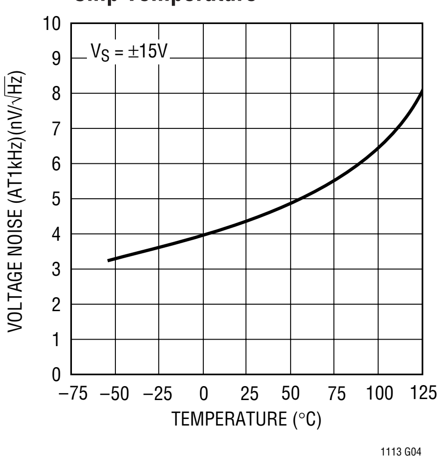
1kHz Output Voltage Noise Density vs Source Resistance



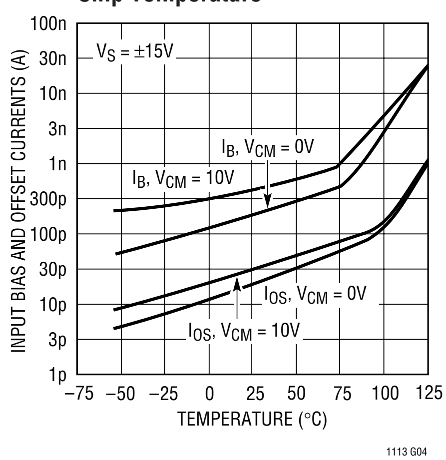
Voltage Noise vs Frequency



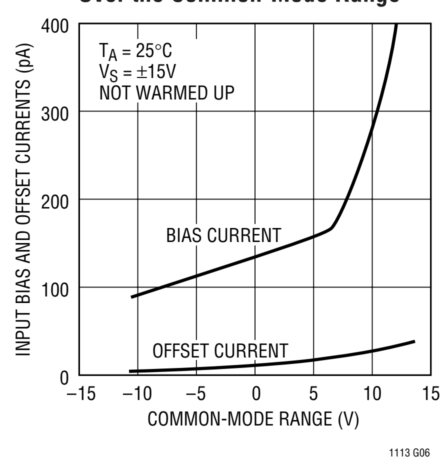
Voltage Noise vs Chip Temperature



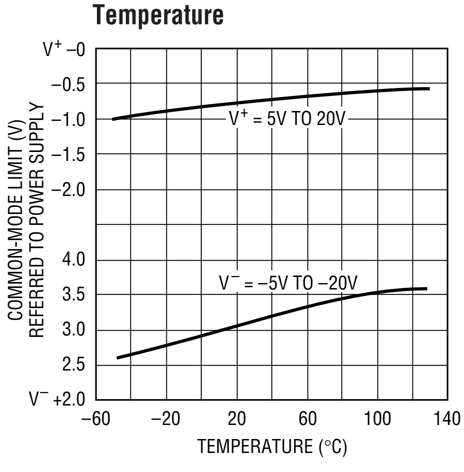
Input Bias and Offset Currents vs Chip Temperature



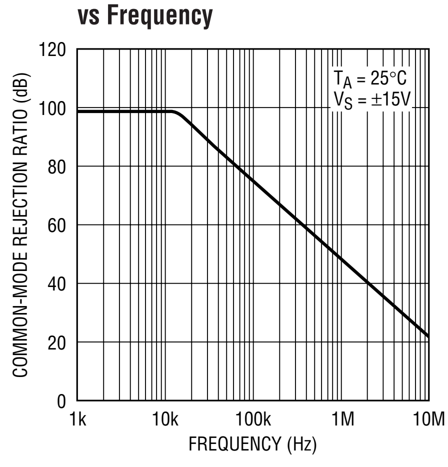
Input Bias and Offset Currents Over the Common-Mode Range



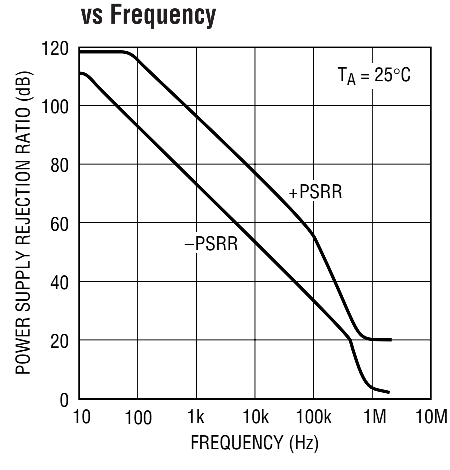
Common-Mode Limit vs Temperature



Common-Mode Rejection Ratio vs Frequency

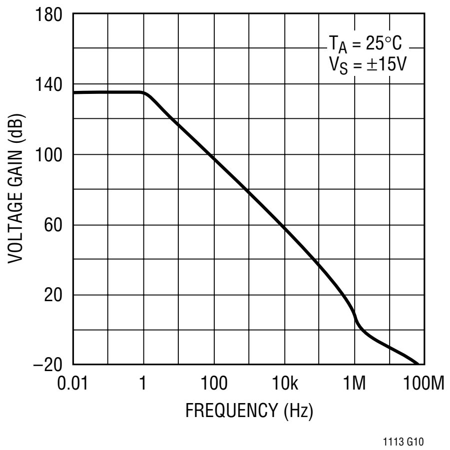


Power Supply Rejection Ratio vs Frequency

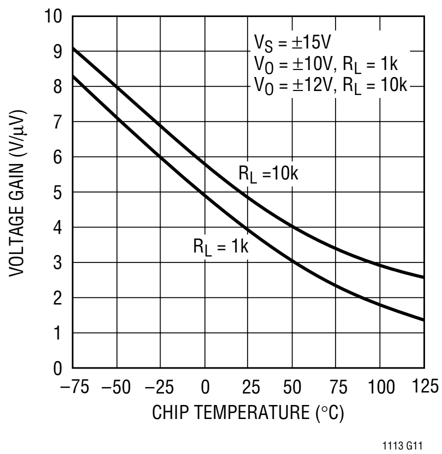


TYPICAL PERFORMANCE CHARACTERISTICS

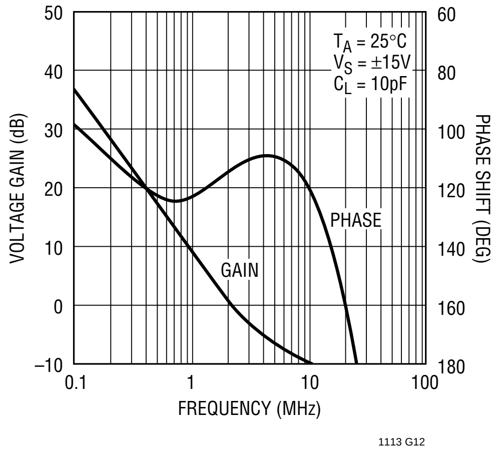
Voltage Gain vs Frequency



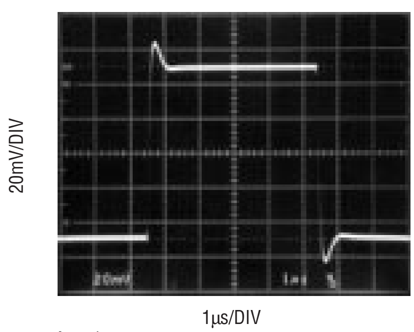
Voltage Gain vs Chip Temperature



Gain and Phase Shift vs Frequency



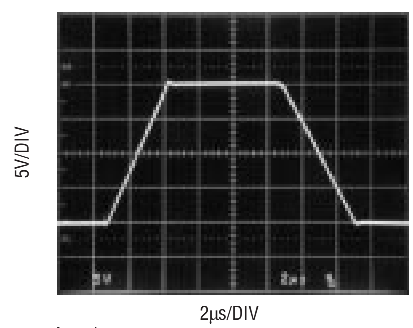
Small-Signal Transient Response



A_V = 1
C_L = 10pF
V_S = ±15V, ±5V

1113 G13

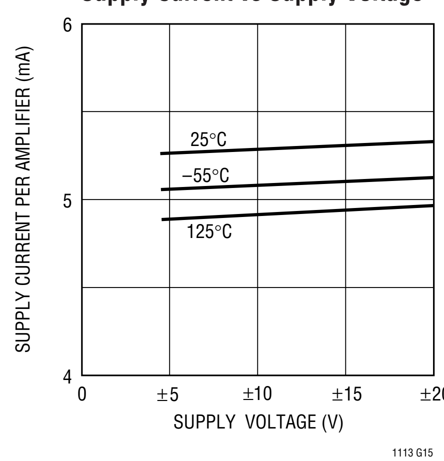
Large-Signal Transient Response



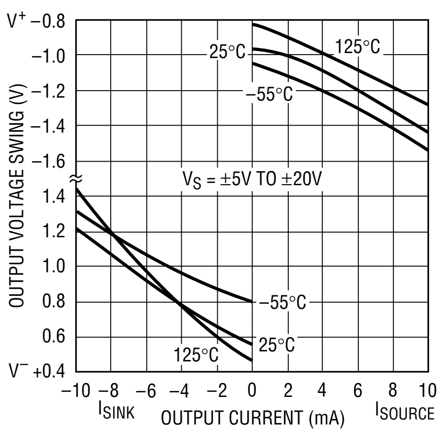
A_V = 1
C_L = 10pF
V_S = ±15V

1113 G14

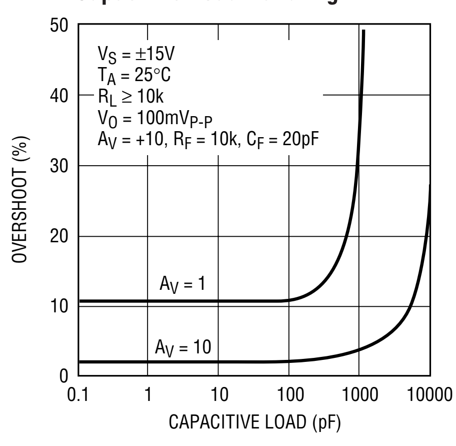
Supply Current vs Supply Voltage



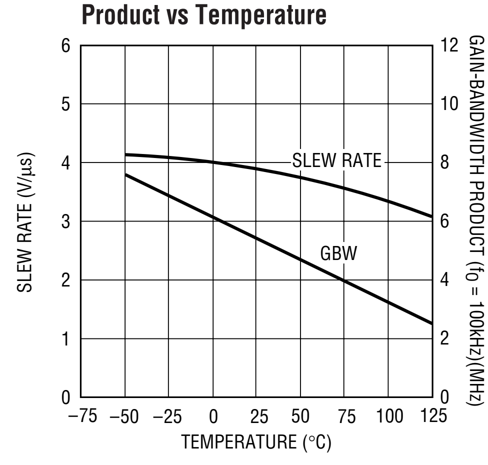
Output Voltage Swing vs Load Current



Capacitive Load Handling

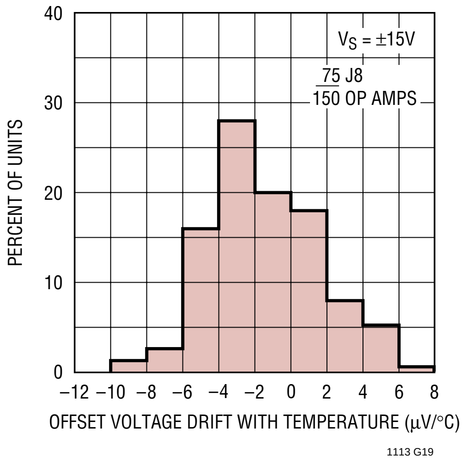


Slew Rate and Gain-Bandwidth Product vs Temperature

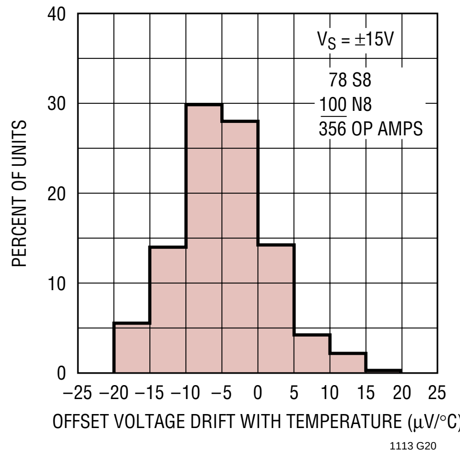


TYPICAL PERFORMANCE CHARACTERISTICS

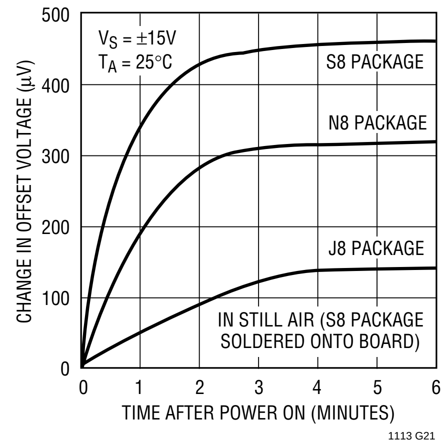
Distribution of Offset Voltage Drift with Temperature (J8)



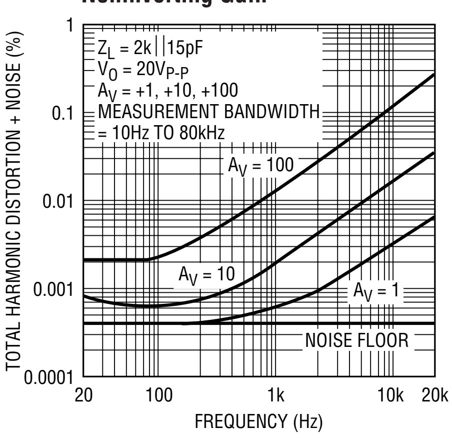
Distribution of Offset Voltage Drift with Temperature (N8, S8)



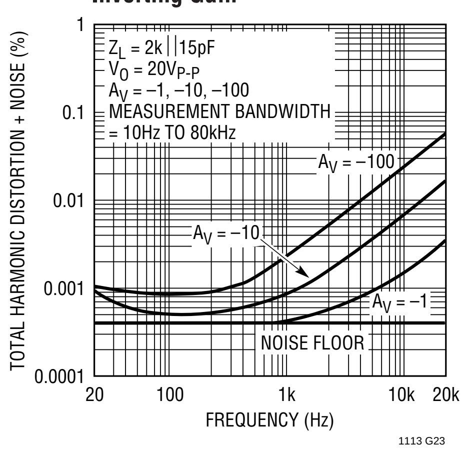
Warm-Up Drift



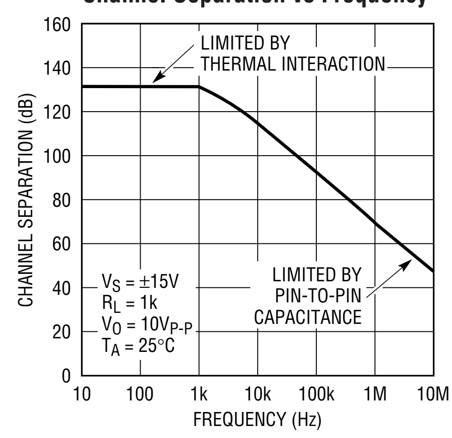
THD and Noise vs Frequency for Noninverting Gain



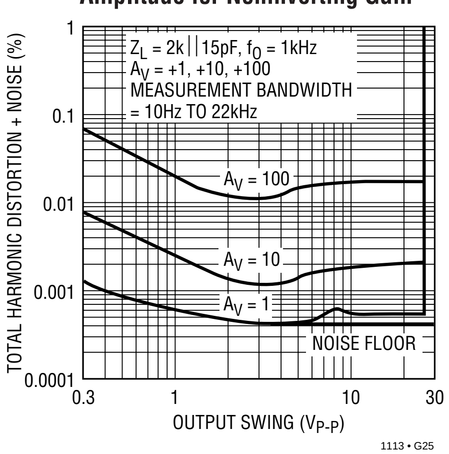
THD and Noise vs Frequency for Inverting Gain



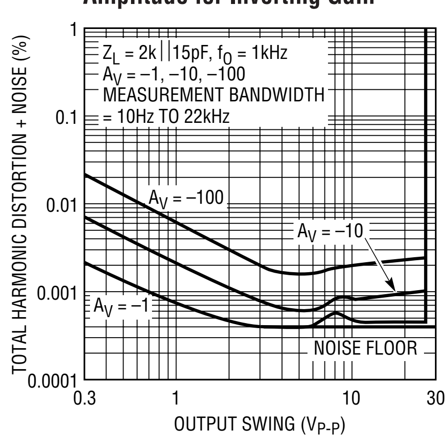
Channel Separation vs Frequency



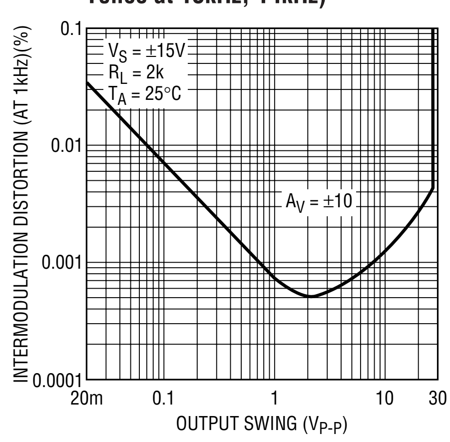
THD and Noise vs Output Amplitude for Noninverting Gain



THD and Noise vs Output Amplitude for Inverting Gain



CCIF IMD Test (Equal Amplitude Tones at 13kHz, 14kHz)*



* See LT1115 data sheet for definition of CCIF testing.

APPLICATIONS INFORMATION

The LT1113 dual in the plastic and ceramic DIP packages are pin compatible with and directly replace such JFET op amps as the OPA2111 and OPA2604 with improved noise performance. Being the lowest noise dual JFET op amp available to date, the LT1113 can replace many bipolar op amps that are used in amplifying low level signals from high impedance transducers. The best bipolar op amps will eventually loose out to the LT1113 when transducer impedance increases due to higher current noise. The low voltage noise of the LT1113 allows it to surpass every dual and most single JFET op amps available. For the best performance versus area available anywhere, the LT1113 is offered in the narrow SO-8 surface mount package with standard pinout and no degradation in performance.

The low voltage and current noise offered by the LT1113 makes it useful in a wide range of applications, especially where high impedance, capacitive transducers are used such as hydrophones, precision accelerometers and photo diodes. The total output noise in such a system is the gain times the RMS sum of the op amp input referred voltage noise, the thermal noise of the transducer, and the op amp bias current noise times the transducer impedance. Figure 1 shows total input voltage noise versus source resistance. In a low source resistance (<5k) application the op amp voltage noise will dominate the total noise. This means the LT1113 will beat out any dual JFET op amp, only the lowest noise bipolar op amps have the edge (at low source resistances). As the source resistance increases from 5k to 50k, the LT1113 will match the best bipolar op amps for noise performance, since the thermal noise of the transducer (4kTR) begins to dominate the total noise. A further increase in source resistance, above 50k, is where the op amp's current noise component ($2qI_B R_{TRANS}$) will eventually dominate the total noise. At these high source resistances, the LT1113 will out perform the lowest noise bipolar op amp due to the inherently low current noise of FET input op amps. Clearly, the LT1113 will extend the range of high impedance transducers that can be used for high signal to noise ratios. This makes the LT1113 the best choice for high impedance, capacitive transducers.

The high input impedance JFET front end makes the LT1113 suitable in applications where very high charge sensitivity is required. Figure 2 illustrates the LT1113 in its inverting and noninverting modes of operation. A charge amplifier is shown in the inverting mode example; here the gain depends on the principal of charge conservation at the input of the LT1113. The charge across the transducer capacitance, C_S, is transferred to the feedback capacitor C_F, resulting in a change in voltage, dV, equal to dQ/C_F.

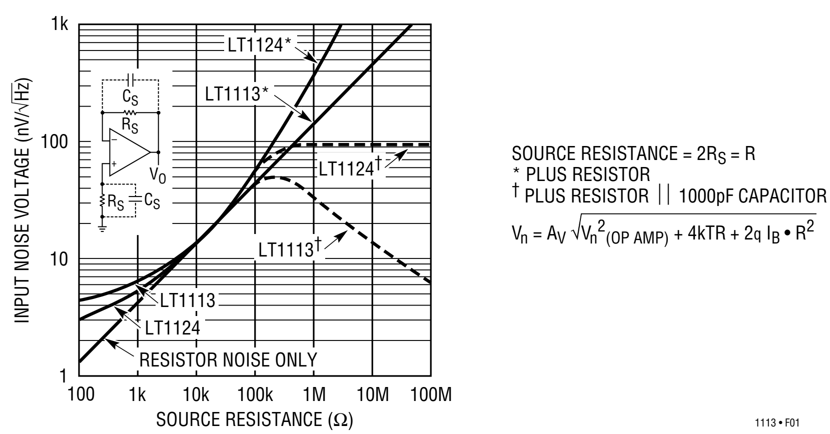


Figure 1. Comparison of LT1113 and LT1124 Total Output 1kHz Voltage Noise Versus Source Resistance

APPLICATIONS INFORMATION

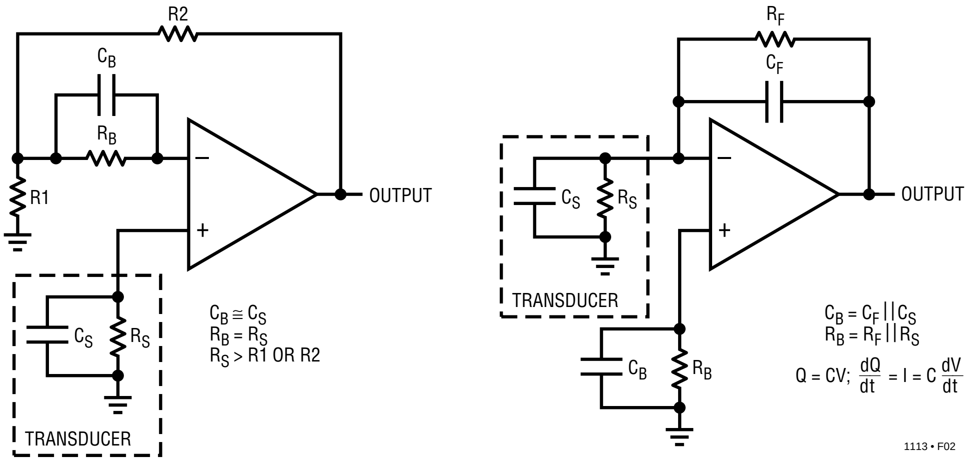


Figure 2. Noninverting and Inverting Gain Configurations

The gain therefore is 1 + C_F/C_S. For unity gain, C_F should equal the transducer capacitance plus the input capacitance of the LT1113 and R_F should equal R_S. In the noninverting mode example, the transducer current is converted to a change in voltage by the transducer capacitance; this voltage is then buffered by the LT1113 with a gain of 1 + R1/R2. A DC path is provided by R_S, which is either the transducer impedance or an external resistor. Since R_S is usually several orders of magnitude greater than the parallel combination of R1 and R2, R_B is added to balance the DC offset caused by the noninverting input bias current and R_S. The input bias currents, although small at room temperature, can create significant errors over increasing temperature, especially with transducer resistances of up to 100M or more. The optimum value for R_B is determined by equating the thermal noise ($4kTR_S$) to the current noise ($2qI_B$) times R_S^2. Solving for R_S results in $R_B = R_S = 2V_T/I_B$

$$\left(V_T = \frac{kT}{q} = 26\text{mV at } 25°\text{C}\right).$$

A parallel capacitor, C_B, is used to cancel the phase shift caused by the op amp input capacitance and R_B.

Reduced Power Supply Operation

The LT1113 can be operated from ±5V supplies for lower power dissipation resulting in lower I_B and noise at the expense of reduced dynamic range. To illustrate this benefit, let's look at the following example:

An LT1113CS8 operates at an ambient temperature of 25°C with ±15V supplies, dissipating 318mW of power (typical supply current = 10.6mA for the dual). The SO-8 package has a θ_{JA} of 190°C/W, which results in a die temperature increase of 60.4°C or a room temperature die operating temperature of 85.4°C. At ±5V supplies, the die temperature increases by only one third of the previous amount or 20.1°C resulting in a typical die operating temperature of only 45.1°C. A 40 degree reduction of die temperature is achieved at the expense of a 20V reduction in dynamic range. If no DC correction resistor is used at the input, the input referred offset will be the input bias current at the operating die temperature times the transducer resistance (refer to Input Bias and Offset Currents vs Chip Temperature graph in Typical Performance Characteristics section). A 100mV input V_{OS} is the result of a 1nA I_B (at 85°C) dropped across a 100M transducer resistance; at ±5V supplies, the input offset is only 28mV (I_B at 45°C is 280pA). Careful selection of a DC correction

APPLICATIONS INFORMATION

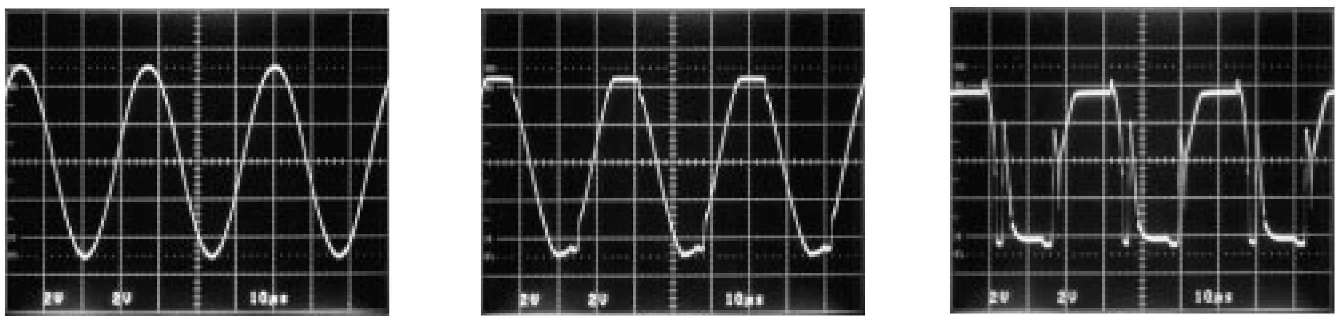


Figure 3. Voltage Follower with Input Exceeding the Common-Mode Range ($V_S = \pm 5V$)

resistor (R_B) will reduce the IR errors due to I_B by an order of magnitude. A further reduction of IR errors can be achieved by using a DC servo circuit shown in the applications section of this data sheet. The DC servo has the advantage of reducing a wide range of IR errors to the millivolt level over a wide temperature variation. The preservation of dynamic range is especially important when reduced supplies are used, since input bias currents can exceed the nanoamp level for die temperatures over 85°C.

To take full advantage of a wide input common mode range, the LT1113 was designed to eliminate phase reversal. Referring to the photographs shown in Figure 3, the LT1113 is shown operating in the follower mode ($A_V = +1$) at ±5V supplies with the input swinging ±5.2V. The output of the LT1113 clips cleanly and recovers with no phase reversal, unlike the competition as shown by the last photograph. This has the benefit of preventing lock-up in servo systems and minimizing distortion components. The effect of input and output overdrive on one amplifier has no effect on the other, as each amplifier is biased independently.

Advantages of Matched Dual Op Amps

In many applications the performance of a system depends on the matching between two operational amplifiers rather than the individual characteristics of the two op amps. Two or three op amp instrumentation amplifiers, tracking voltage references and low drift active filters are some of the circuits requiring matching between two op amps.

The well-known triple op amp configuration in Figure 4 illustrates these concepts. Output offset is a function of the difference between the two halves of the LT1113. This error cancellation principle holds for a considerable number of input referred parameters in addition to offset voltage and bias current. Input bias current will be the average of the two noninverting input currents (I_B+). The difference between these two currents (ΔI_B+) is the offset current of the instrumentation amplifier. Common mode and power supply rejections will be dependent only on the match between the two amplifiers (assuming perfect resistor matching).

APPLICATIONS INFORMATION

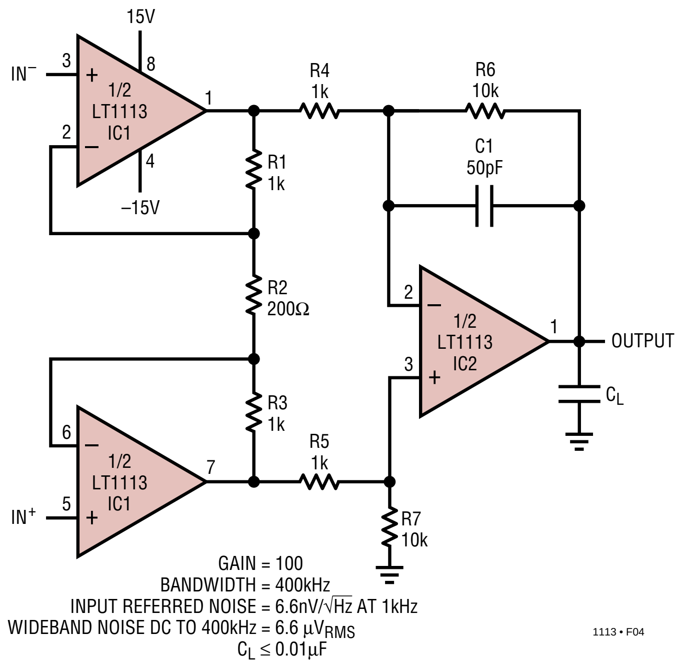


Figure 4. Three Op Amp Instrumentation Amplifier

The concepts of common mode and power supply rejection ratio match (ΔCMRR and ΔPSRR) are best demonstrated with a numerical example:

Assume $CMRR_A$ = +50µV/V or 86dB,

and $CMRR_B$ = + 39µV/V or 88dB,

then ΔCMRR = 11µV/V or 99dB;

if $CMRR_B$ = -39µV/V which is still 88dB,

then ΔCMRR = 89µV/V or 81dB

Clearly the LT1113, by specifying and guaranteeing all of these matching parameters, can significantly improve the performance of matching-dependent circuits.

Typical performance of the instrumentation amplifier:

Input offset voltage = 0.8mV

Input bias current = 320pA

Input offset current = 10pA

Input resistance = $10^{11}\Omega$

Input noise = 3.4µV_{P-P}

High Speed Operation

The low noise performance of the LT1113 was achieved by making the input JFET differential pair large to maximize the first stage gain. Increasing the JFET geometry also increases the parasitic gate capacitance, which if left unchecked, can result in increased overshoot and ringing. When the feedback around the op amp is resistive (R_F), a pole will be created with R_F, the source resistance and capacitance (R_S,C_S), and the amplifier input capacitance (C_{IN} = 27pF). In closed loop gain configurations and with R_S and R_F in the kilohm range (Figure 5), this pole can create excess phase shift and even oscillation. A small capacitor (C_F) in parallel with R_F eliminates this problem. With $R_S(C_S + C_{IN}) = R_FC_F$, the effect of the feedback pole is completely removed.

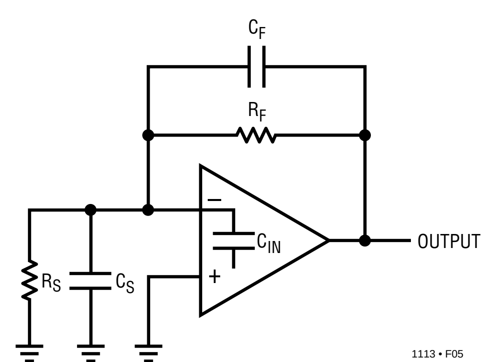
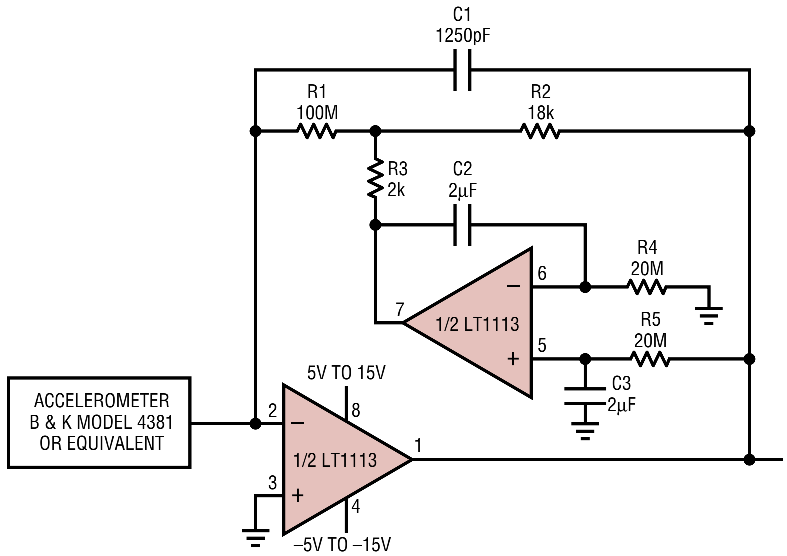


Figure 5.

TYPICAL APPLICATIONS

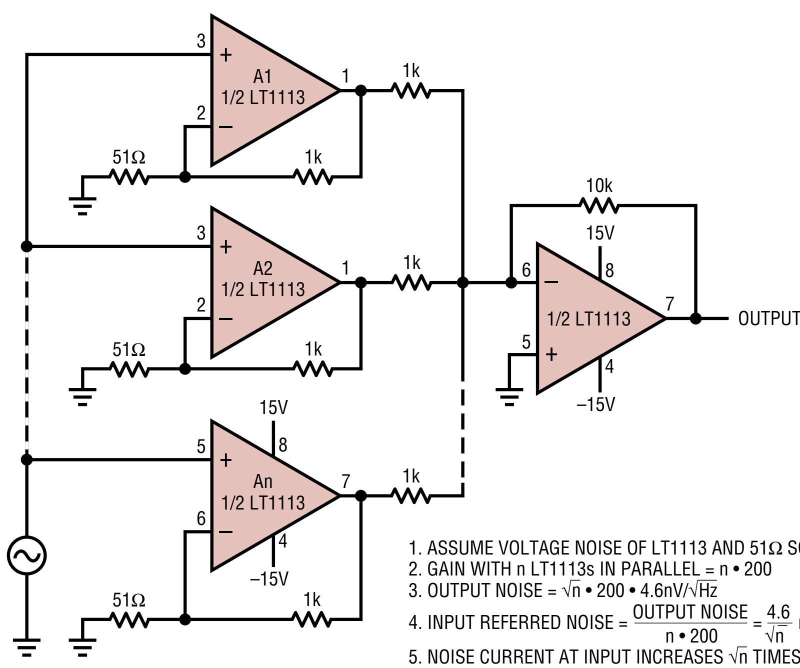
Accelerometer Amplifier with DC Servo



R4C2 = R5C3 > R1 (1 + R2/R3) C1
OUTPUT = 0.8mV/pC* = 8.0mV/g**
DC OUTPUT $\leq$ 2.7mV
OUTPUT NOISE = 6nV/$\sqrt{\text{Hz}}$ AT 1kHz

*PICOCOULOMBS
**g = EARTH'S GRAVITATIONAL CONSTANT

Paralleling Amplifiers to Reduce Voltage Noise

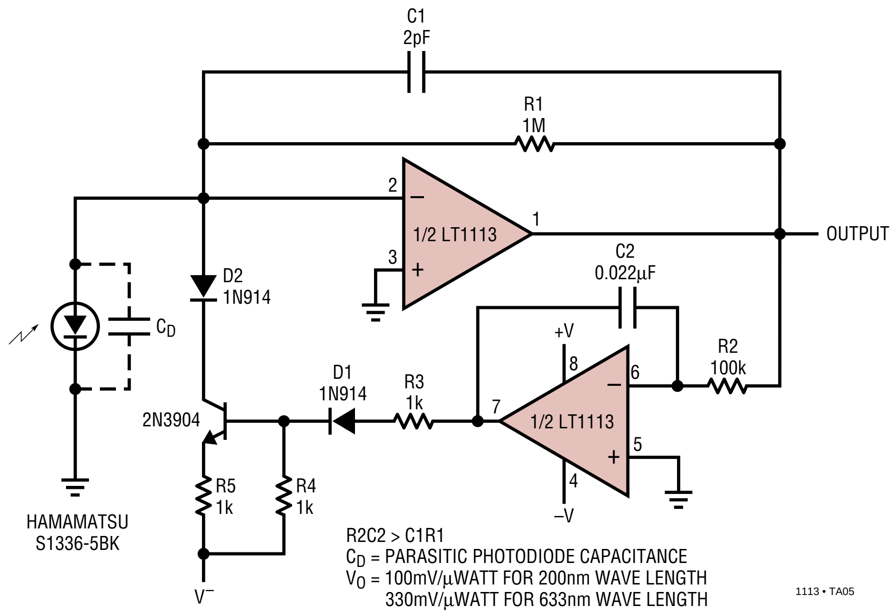


1. ASSUME VOLTAGE NOISE OF LT1113 AND 51Ω SOURCE RESISTOR = 4.6nV/$\sqrt{\text{Hz}}$
2. GAIN WITH n LT1113s IN PARALLEL = n • 200
3. OUTPUT NOISE = $\sqrt{n}$ • 200 • 4.6nV/$\sqrt{\text{Hz}}$
4. INPUT REFERRED NOISE = $\frac{\text{OUTPUT NOISE}}{n \cdot 200} = \frac{4.6}{\sqrt{n}}$ nV/$\sqrt{\text{Hz}}$
5. NOISE CURRENT AT INPUT INCREASES $\sqrt{n}$ TIMES
6. IF n = 5, GAIN = 1000, BANDWIDTH = 1MHz, RMS NOISE, DC TO 1MHz = $\frac{9\mu V}{\sqrt{5}}$ = 4µV

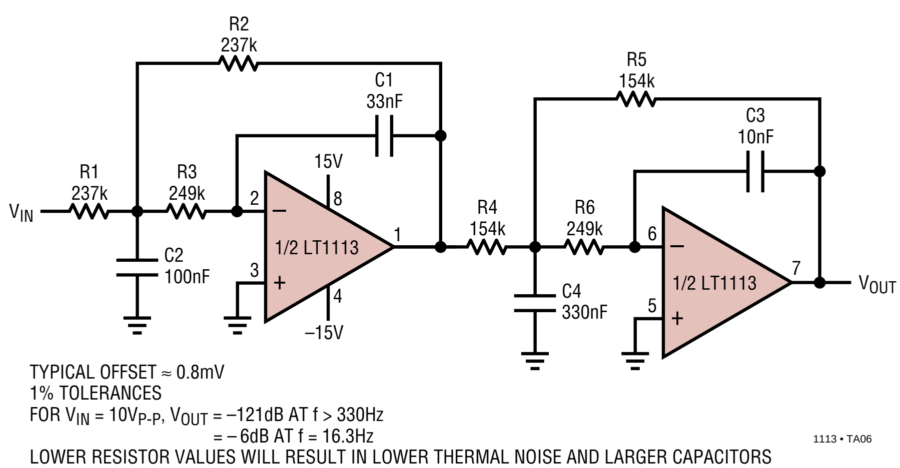
1113 • TA04

TYPICAL APPLICATIONS

Low Noise Light Sensor with DC Servo



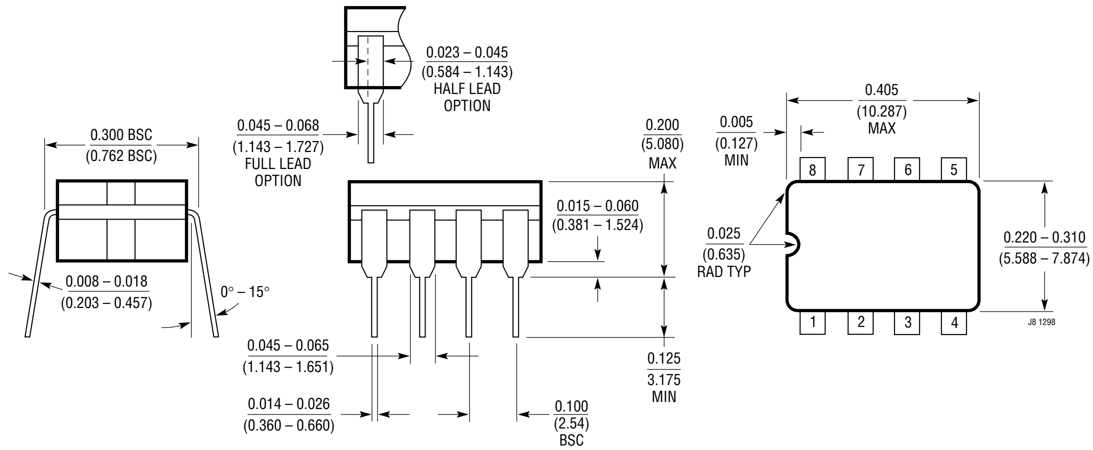
10Hz Fourth Order Chebyshev Lowpass Filter (0.01dB Ripple)



PACKAGE DESCRIPTION

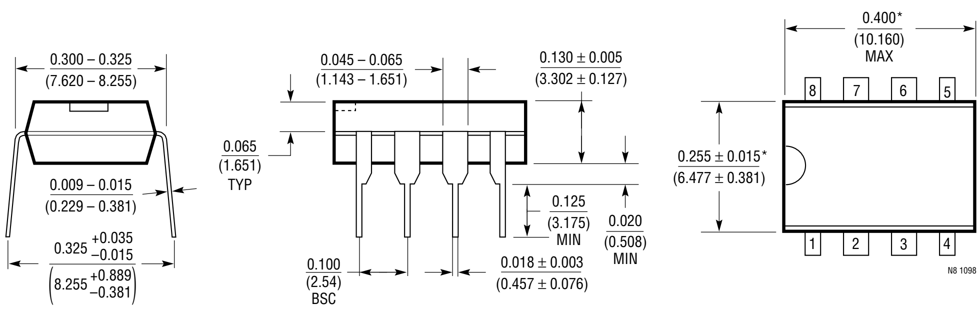
Dimensions in inches (millimeters) unless otherwise noted.

J8 Package
8-Lead CERDIP (Narrow 0.300, Hermetic)
(LTC DWG # 05-08-1110)



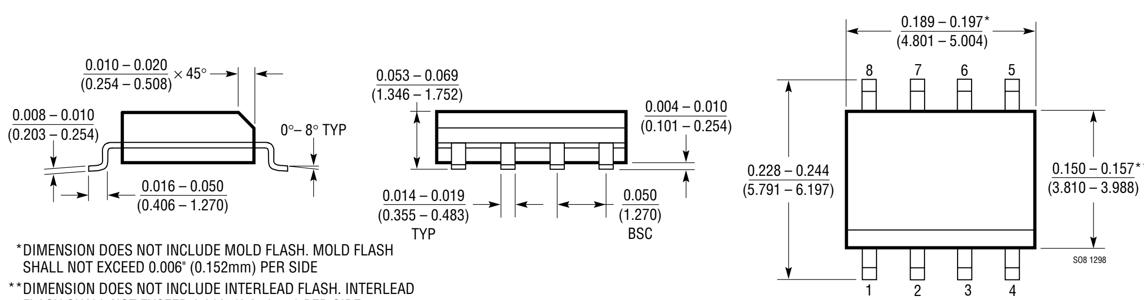
NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE OR TIN PLATE LEADS

N8 Package
8-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

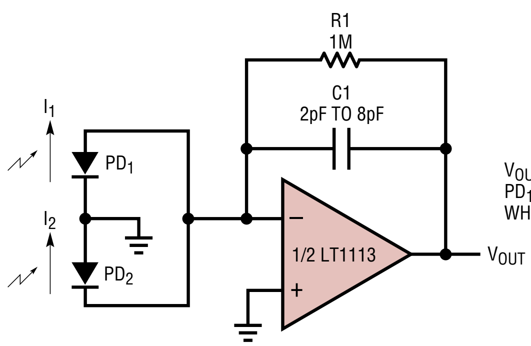
S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

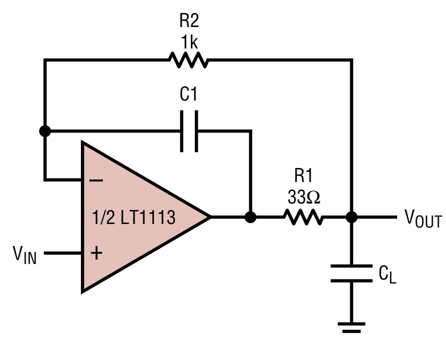
TYPICAL APPLICATIONS

Light Balance Detection Circuit



$V_{OUT} = 1M \bullet (I_1 – I_2)$
PD_1, PD_2 = HAMAMATSU S1336-5BK
WHEN EQUAL LIGHT ENTERS PHOTODIODES, $V_{OUT} < 3mV$.

Unity Gain Buffer with Extended Load Capacitance Drive Capability



$C1 = C_L \le 0.1\mu F$
OUTPUT SHORT-CIRCUIT CURRENT
(~30mA) WILL LIMIT THE RATE AT WHICH THE
VOLTAGE CAN CHANGE ACROSS LARGE CAPACITORS
$(I = C\frac{dV}{dt})$

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1028	Single Low Noise Precision Op Amp	$V_{NOISE} = 1.1nV/\sqrt{Hz}$ Max
LT1124	Dual Low Noise Precision Op Amp	$V_{NOISE} = 4.2nV/\sqrt{Hz}$ Max
LT1169	Dual Low Noise Precision JFET Op Amp	10pA I_B
LT1462	Dual Picoamp I_B C-Load™ Op Amp	I_B = 2pA Max, 10000pF C-Load, $I_S = 45\mu A$
LT1464	Dual Picoamp I_B C-Load Op Amp	I_B = 2pA Max, 10000pF C-Load, $I_S = 200\mu A$
LT1792	Single Low Noise Precision Op Amp	Single LT1113
LT1793	Single Low Noise Precision Op Amp	Single LT1169

C-Load is a trademark of Linear Technology Corporation.

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