

M66850J/FP, M66851J/FP M66852J/FP, M66853J/FP

SRAM TYPE FIFO MEMORY

DESCRIPTION

M66850/851/852/853 are very high-speed and clock synchronous FIFO(First-In,First-Out) memories fabricated by high-speed CMOS technology.

These FIFOs are applicable for a data buffer as networks and communications.

The write operation is controlled by a write clock pin(WCLK) and two write enable pins(WEN1,WEN2).

Data present at the data input pins(D0-D8) is written into the Synchronous FIFO on every rising write clock edge when the device is enabled for writing.

The read operation is controlled by a read clock pin(RCLK) and two read enable pins(REN1,REN2).

Data is read from the Synchronous FIFO on every rising read clock edge when the device is enabled for reading. An output enable pin(OE) controls the states of the data output pins(Q0-Q8).

MITSUBISHI FIFOs have four flags (EF,FF,PAE,PAF). The empty flag EF and the full flag FF are fixed flags. The almost empty flag PAE and the almost full flag PAF are programmable flags. The programmable flag offset is initiated by the load pin(LD).

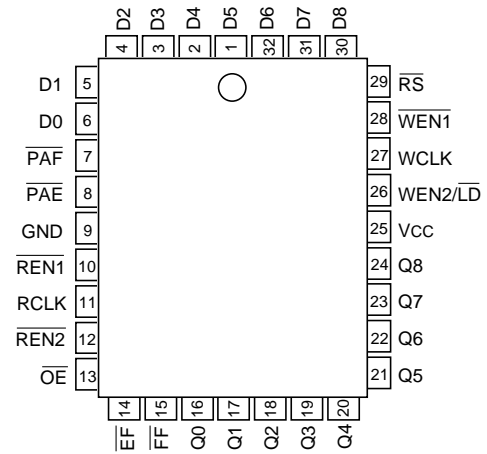
FEATURES

- Memory configuration
 - 64words x 9bits (M66850J/FP)
 - 256words x 9bits (M66851J/FP)
 - 512words x 9bits (M66852J/FP)
 - 1024words x 9bits (M66853J/FP)
- Write and Read Clocks can be independent
- Advanced CMOS technology
- Programmable Almost-Empty and Almost-Full flags
- High-speed : 25ns cycle time
- Package Available :
 - 32-pin Pastic Leded Chip Carrier(PLCC)
 - 32-pin Low profile Quad Flat Package(LQFP)

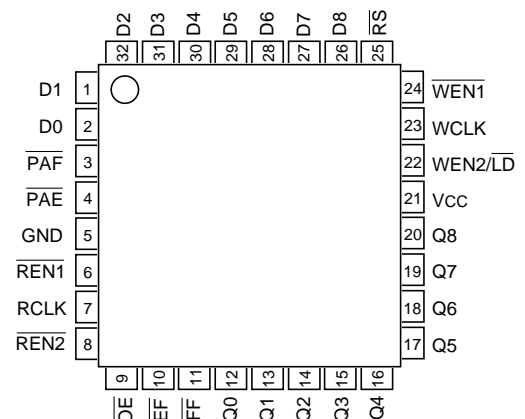
APPLICATION

- Data Buffer for networks communications.

PIN CONFIGURATION (TOP VIEW)

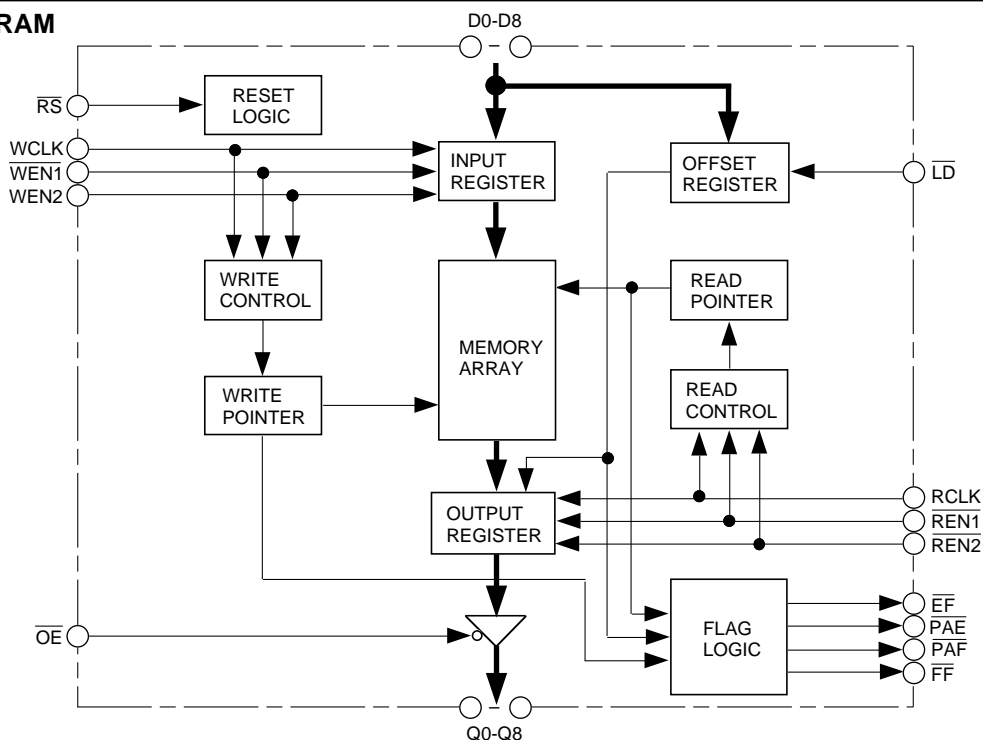


Outline 32P0(M66850 – 853J)



Outline 32P6B(M66850 – 853FP)

BLOCK DIAGRAM



M66850J/FP, M66851J/FP M66852J/FP, M66853J/FP

SRAM TYPE FIFO MEMORY

PIN and SIGNAL DESCRIPTIONS

- Vcc
One +5 volt power supply pin.
- GND
One 0 volt ground pin.
- \overline{RS} : Reset(INPUT)
When \overline{RS} is set LOW, internal read and write pointers are set to the first physical location, the output register is initialized to LOW, FF and PAF are set HIGH, \overline{EF} and PAE are set LOW.
A reset is required after power-up before a write operation.
- WCLK : Write Clock(INPUT)
Data present on D0-D8 is written into the FIFO on the rising edge of WCLK when the FIFO is enabled for writing.
- RCLK : Read Clock(INPUT)
Data is read from the FIFO on the rising edge of RCLK when the FIFO is enabled for reading.
- $\overline{WEN1}$: Write Enable1(INPUT)
If the FIFO is configured to allow loading of the offset registers, $\overline{WEN1}$ is the only the write enable. When $\overline{WEN1}$ is LOW, data on D0-D8 is written to the FIFO on the rising edge of WCLK.
If the FIFO is configured to have two write enables, data on D0-D8 is written to the FIFO on the rising edge of WCLK when $\overline{WEN1}$ is LOW and WEN2 is High. But if the FF is LOW, data on D0-D8 will not be written to the FIFO.
- WEN2/ \overline{LD} : Write Enable2/ \overline{Load} (INPUT)
The function of this signal is defined at reset.
If WEN2/ \overline{LD} is HIGH at reset, this signal functions as a second write enable(WEN2). If WEN2/ \overline{LD} is LOW at reset, this signal functions as a control to load and read the offset register.
If the FIFO is configured to have two write enables, data on D0-D8 is written to the FIFO on the rising edge of WCLK when $\overline{WEN1}$ is LOW and WEN2 is High. But if the FF is LOW, data on D0-D8 will not be written to the FIFO.
If the FIFO is configured to have programmable flags, it is possible to write and read from the offset registers. There are four 9-bit offset registers. Two are used to control the programmable Almost-Empty Flag and two are used to control the programmable Almost-Full Flag.
Data on D0-D8 is written to an offset register on the rising edge of WCLK when WEN1 is LOW and LD is LOW. Data on D0 – D8 is written to the offset registers in the following order :
PAE LSB, PAE MSB, PAF LSB, PAF MSB.
- $\overline{REN1}$, $\overline{REN2}$: Read Enable(INPUT)
Data is read from the FIFO and presented Q0-8 on the rising edge of RCLK, when $\overline{REN1}$ and $\overline{REN2}$ are LOW and output port is enabled.
If either Read Enable is HIGH, the output register holds the previous data.
When the FIFO is empty, the Read Enable signals are ignored.
- \overline{OE} : Output Enable(INPUT)
When \overline{OE} is LOW, the output port Q0-8 is enabled for output.
When \overline{OE} is HIGH, the output port Q0-8 is placed in a high impedance state.
- D0-8 : Data Input(INPUT)
D0-8 is the 9-bit data input port.
- Q0-8 : Data Output(OUTPUT)
Q0-8 is the 9-bit data Output port.
- \overline{EF} : Empty Flag(OUTPUT)
The Empty flag goes LOW when the read pointer is equal to the write pointer.
When \overline{EF} is LOW, the FIFO is empty and further data reads from the data output are inhibited.
 \overline{EF} is synchronized to the rising edge of RCLK.
- \overline{PAE} : Programmable Almost-Empty Flag(OUTPUT)
When \overline{PAE} is LOW, the FIFO is almost empty based on the offset. The default offset is Empty+7. PAE is synchronized to the rising edge of RCLK.
- \overline{FF} : Full Flag(OUTPUT)
When \overline{FF} is LOW, the FIFO is full and further data writes into the data input are inhibited.
The Full Flag goes LOW when the FIFO is full of data.
 \overline{FF} is synchronized to the rising edge of WCLK.
- \overline{PAF} : Programmable Almost-Full Flag(OUTPUT)
When \overline{PAF} is LOW, the FIFO is almost full based on the offset. The default offset is Full-7. PAF is synchronized to the rising edge of WCLK.

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OFFSET FLAG

$\overline{\text{LD}}$	$\overline{\text{WEN1}}$	WCLK	SELECTION
0	0		Empty Offset (LSB) Empty Offset (MSB) Full Offset (LSB) Full Offset (MSB)
0	1		No Operation
1	0		Write into FIFO
1	1		No Operation

Figure 1. Write Offset Register

$\overline{\text{LD}}$	$\overline{\text{REN1}}$	$\overline{\text{REN2}}$	RCLK	SELECTION
0	0	0		Empty Offset (LSB) Empty Offset (MSB) Full Offset (LSB) Full Offset (MSB)
0	0	1		No Operation
	1	0		
	1	1		Read from FIFO
1	1	0		No Operation
	0	1		
	1	0		
1	1	1		No Operation

Figure 2. Read Offset Register

M66850J(64X9-bit) OFFSET REGISTERS									
	8	7	6	5	4	3	2	1	0
PAE LSB	X	X	X	E5	E4	E3	E2	E1	E0
	Default Value 007H								
PAE MSB	X	X	X	X	X	X	X	X	X
PAF LSB	X	X	X	F5	F4	F3	F2	F1	F0
	Default Value 007H								
PAF MSB	X	X	X	X	X	X	X	X	X

M66852J(512X9-bit) OFFSET REGISTERS									
	8	7	6	5	4	3	2	1	0
PAE LSB	X	E7	E6	E5	E4	E3	E2	E1	E0
	Default Value 007H								
PAE MSB	X	X	X	X	X	X	X	X	E8
	Default Value 0								
PAF LSB	X	F7	F6	F5	F4	F3	F2	F1	F0
	Default Value 007H								
PAF MSB	X	X	X	X	X	X	X	X	F8
	Default Value 0								

M66851J(256X9-bit) OFFSET REGISTERS									
	8	7	6	5	4	3	2	1	0
PAE LSB	X	E7	E6	E5	E4	E3	E2	E1	E0
	Default Value 007H								
PAE MSB	X	X	X	X	X	X	X	X	X
PAF LSB	X	F7	F6	F5	F4	F3	F2	F1	F0
	Default Value 007H								
PAF MSB	X	X	X	X	X	X	X	X	X

M66853J(1024X9-bit) OFFSET REGISTERS									
	8	7	6	5	4	3	2	1	0
PAE LSB	X	E7	E6	E5	E4	E3	E2	E1	E0
	Default Value 007H								
PAE MSB	X	X	X	X	X	X	X	E9	E8
	Default Value 0 0								
PAF LSB	X	F7	F6	F5	F4	F3	F2	F1	F0
	Default Value 007H								
PAF MSB	X	X	X	X	X	X	X	F9	F8
	Default Value 0 0								

E0/F0 are the least significant bits.
 X=Don't Care.

Figure 3. Offset Register Location

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{cc}	Supply voltage	A value based on GND pin	-0.5 – +7.0	V
V _i	Input voltage		-0.3 – V _{cc} +0.5	V
V _o	Output voltage		-0.3 – V _{cc} +0.5	V
P _d	Maximum power dissipation	T _a =70°C	Note	mW
T _{stg}	Storage temperature		-65 – 150	°C

Note : 450mW(32P6B), 550mW(32P0)

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V _{cc}	Supply voltage	4.5	5	5.5	V
GND	Supply voltage		0		V
T _{opr}	Operating ambient temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (T_a=0 – 70°C, V_{cc}=5V±10%, GND=0V)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V _{IH}	"H"input voltage		2.0			V
V _{IL}	"L"input voltage				0.8	V
V _{OH}	"H"output voltage	I _{oH} = -1mA	2.4			V
V _{OL}	"L"output voltage	I _{oL} = 8mA			0.4	V
I _{IH}	"H"input current	V _i = V _{cc} , Any input			1.0	μA
I _{IL}	"L"input current	V _i = GND, Any input			-1.0	μA
I _{oZH}	Off state "H"output current	V _o = V _{cc}			5.0	μA
I _{oZL}	Off state "L"output current	V _o = GND			-5.0	μA
I _{cc1}	Operating power supply current	V _i = V _{cc} or GND, f = 40MHz, Outputs are open			70	mA
I _{cc2}	Power supply current (Static)	V _i = V _{cc} or GND, Outputs are open			500	μA
C _i	Input capacitance	f = 1MHz			10	pF
C _o	Off state output capacitance	f = 1MHz			15	pF

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SWITCHING CHARACTERISTICS ($T_a=0 - 70^\circ\text{C}$, $V_{cc}=5V\pm 10\%$, $GND=0V$)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tAC	Data Access Time	3		15	ns
twFF	Write Clock to Full Flag			15	ns
tREF	Read Clock to Empty Flag			15	ns
tPAF	Write Clock to Almost-Full Flag			15	ns
tPAE	Read Clock to Almost-Empty Flag			15	ns
toE	Output Enable to Output Valid	3		13	ns
toLZ	Output Enable to Output in Low-Z	0			ns
toHZ	Output Enable to Output in High-Z	3		13	ns
trSF	Reset to Flag and Output Valid time			25	ns

TIMING CONDITIONS ($T_a=0 - 70^\circ\text{C}$, $V_{cc}=5V\pm 10\%$, $GND=0V$)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tCLK	Clock Cycle Time	25			ns
tCLKH	Clock Pulse Width HIGH	10			ns
tCLKL	Clock Pulse Width LOW	10			ns
tDS	Data Setup Time	6			ns
tDH	Data Hold Time	1			ns
tENS	Enable Setup Time	6			ns
tENH	Enable Hold Time	1			ns
tRS	Reset Pulse Width	25			ns
tRSS	Reset Setup Time	25			ns
tRSR	Reset Recovery Time	25			ns
tSKEW1	Skew time between Read Clock and Write Clock for Empty Flag and Full Flag	10			ns
tSKEW2	Skew time between Read Clock and Write Clock for Almost-Empty Flag and Almost-Full Flag	40			ns

AC TEST CONDITIONS

In Pulse Levels	GND – 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 4

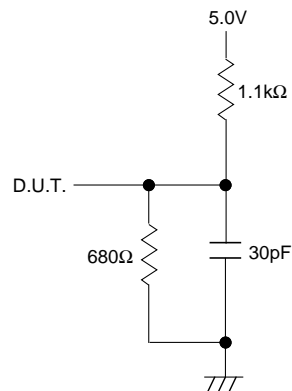
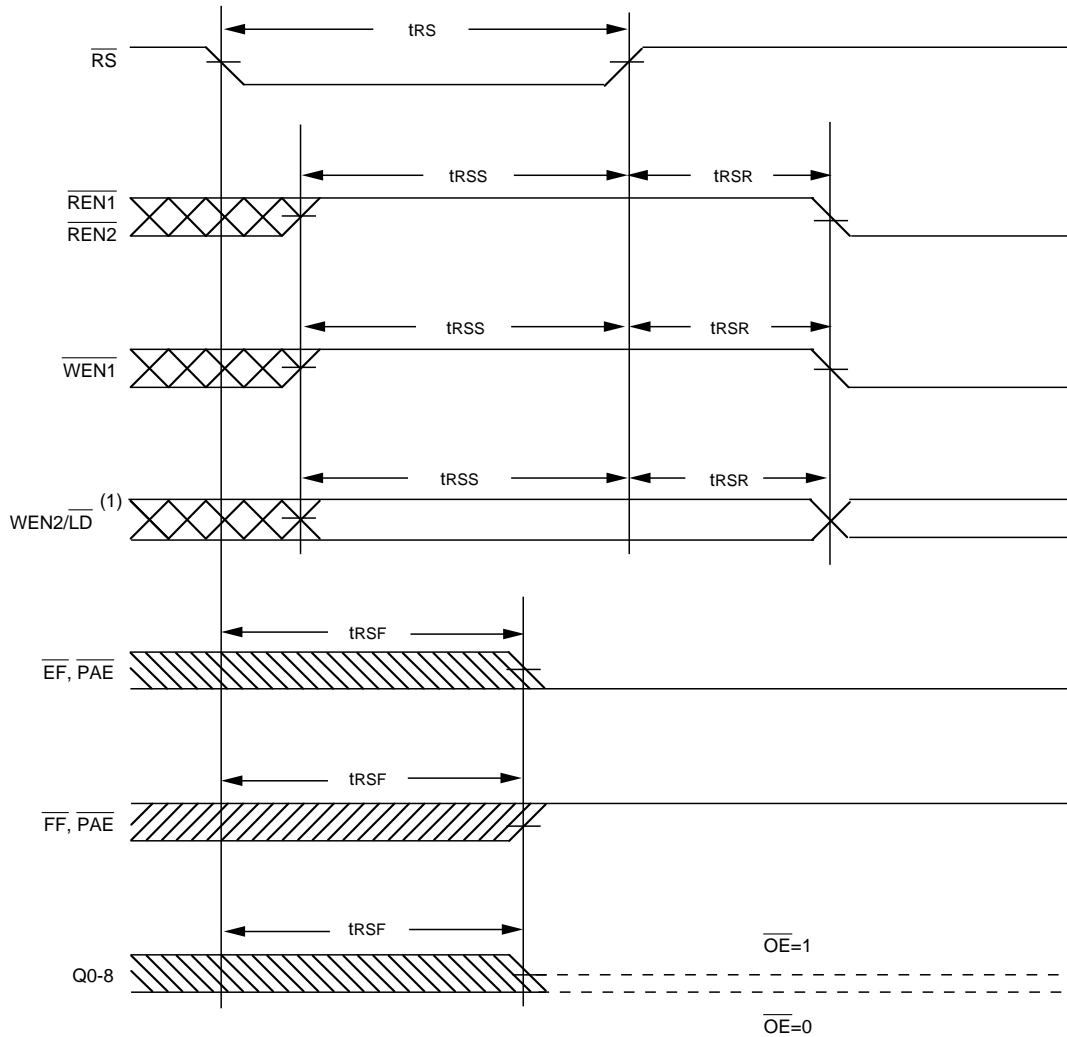


Figure 4. Output Load
Including Test board and scope capacitances.

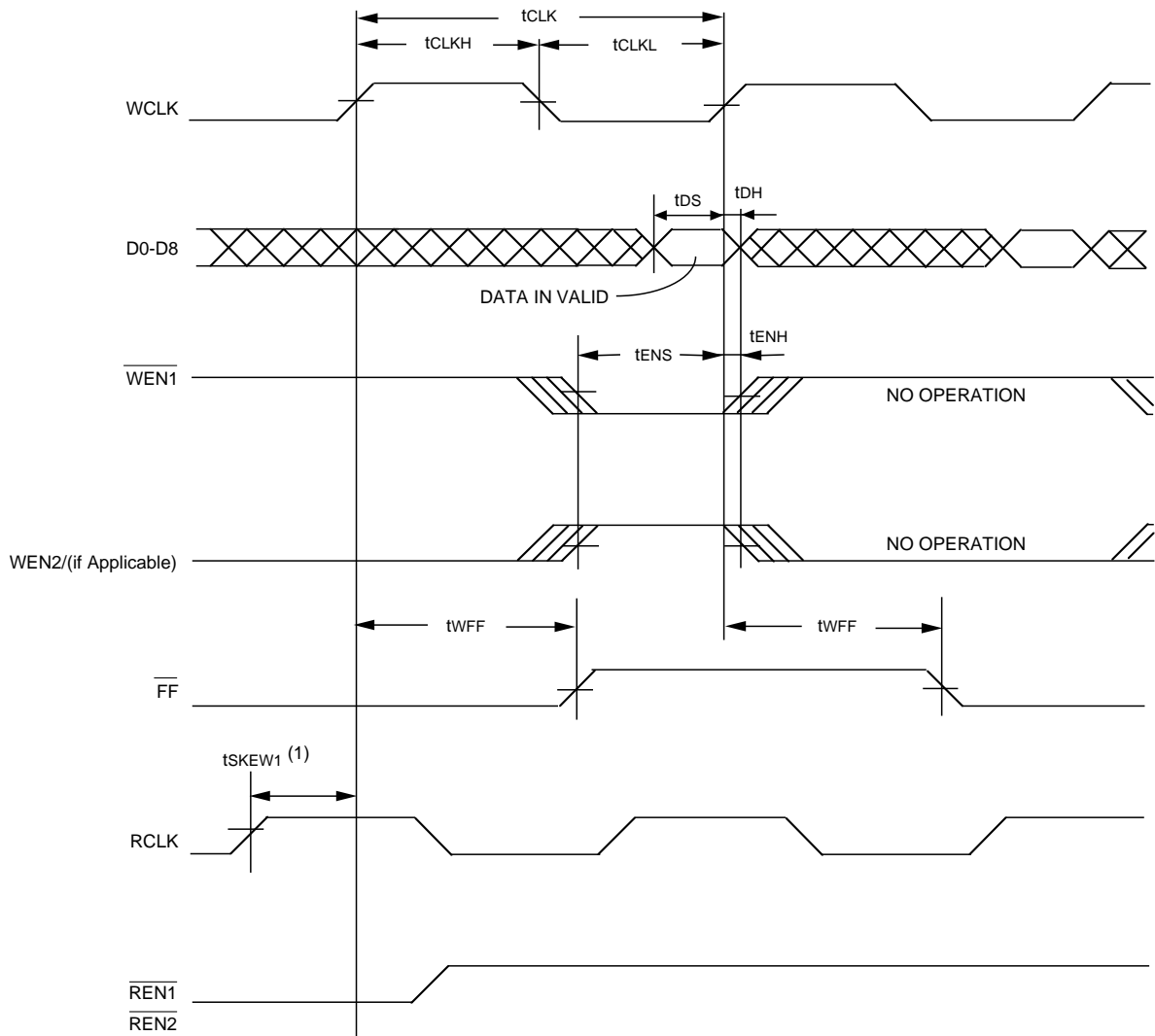
• Reset Timing



NOTE :

1. If during reset $\overline{WEN2/LD}$ is HIGH, this signal functions as a second enable (WEN2).
 If during reset $\overline{WEN2/LD}$ is LOW, this signal functions as an offset register.

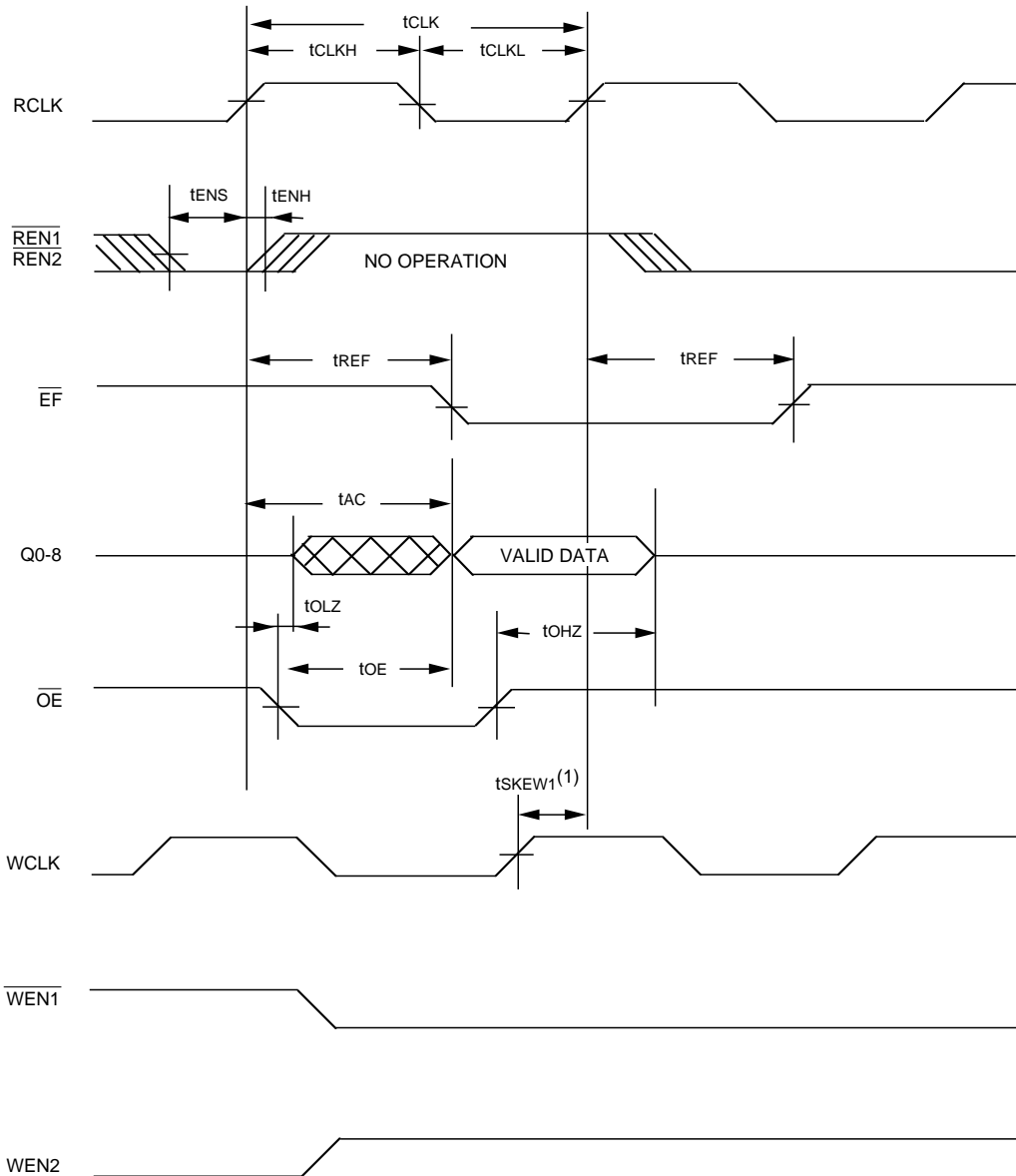
• Write Cycle Timing



NOTE :

1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge for \overline{FF} to change during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1} , then \overline{FF} may not change state until the next WCLK edge.

• Read Cycle Timing

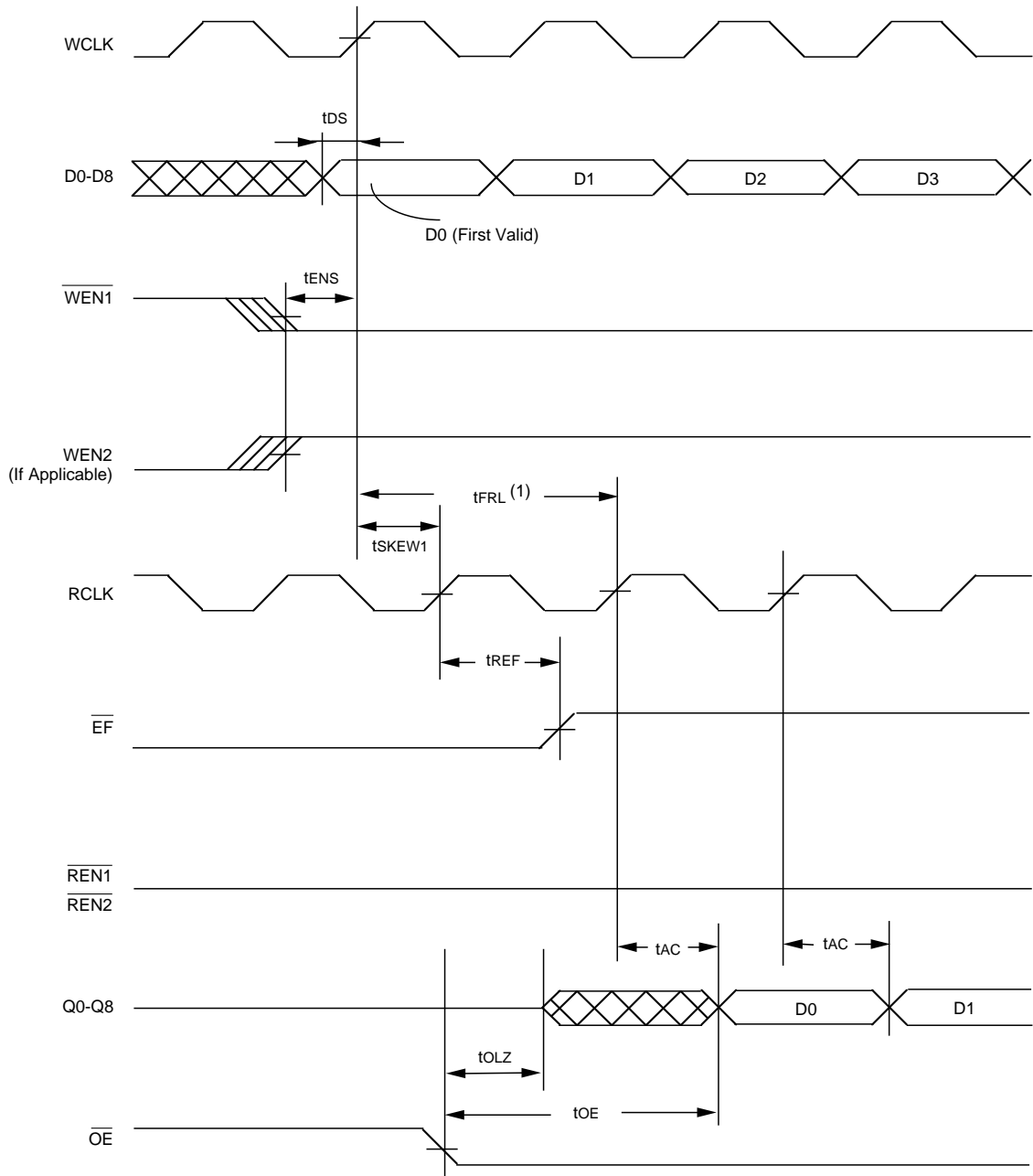


NOTE :

1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge for \overline{EF} to change during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1} , then \overline{EF} may not change state until the next RCLK edge.

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• First Data Word Latency Timing

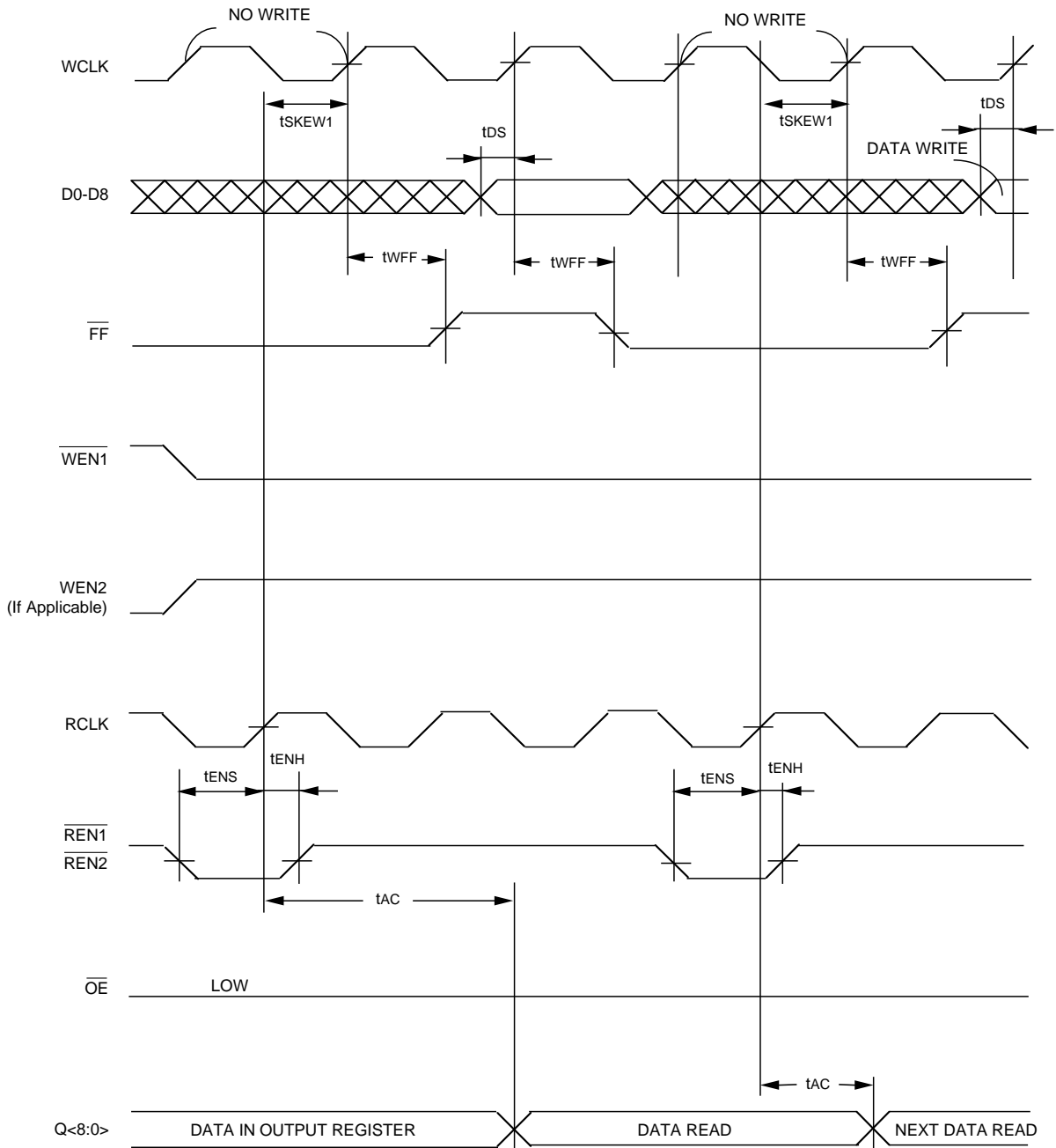


NOTE :

- When $t_{SKEW1} \geq$ minimum specification, $t_{FRL \text{ maximum}} = t_{CLK} + t_{SKEW1}$.
 When $t_{SKEW1} \leq$ minimum specification, $t_{FRL \text{ maximum}} = 2t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$.

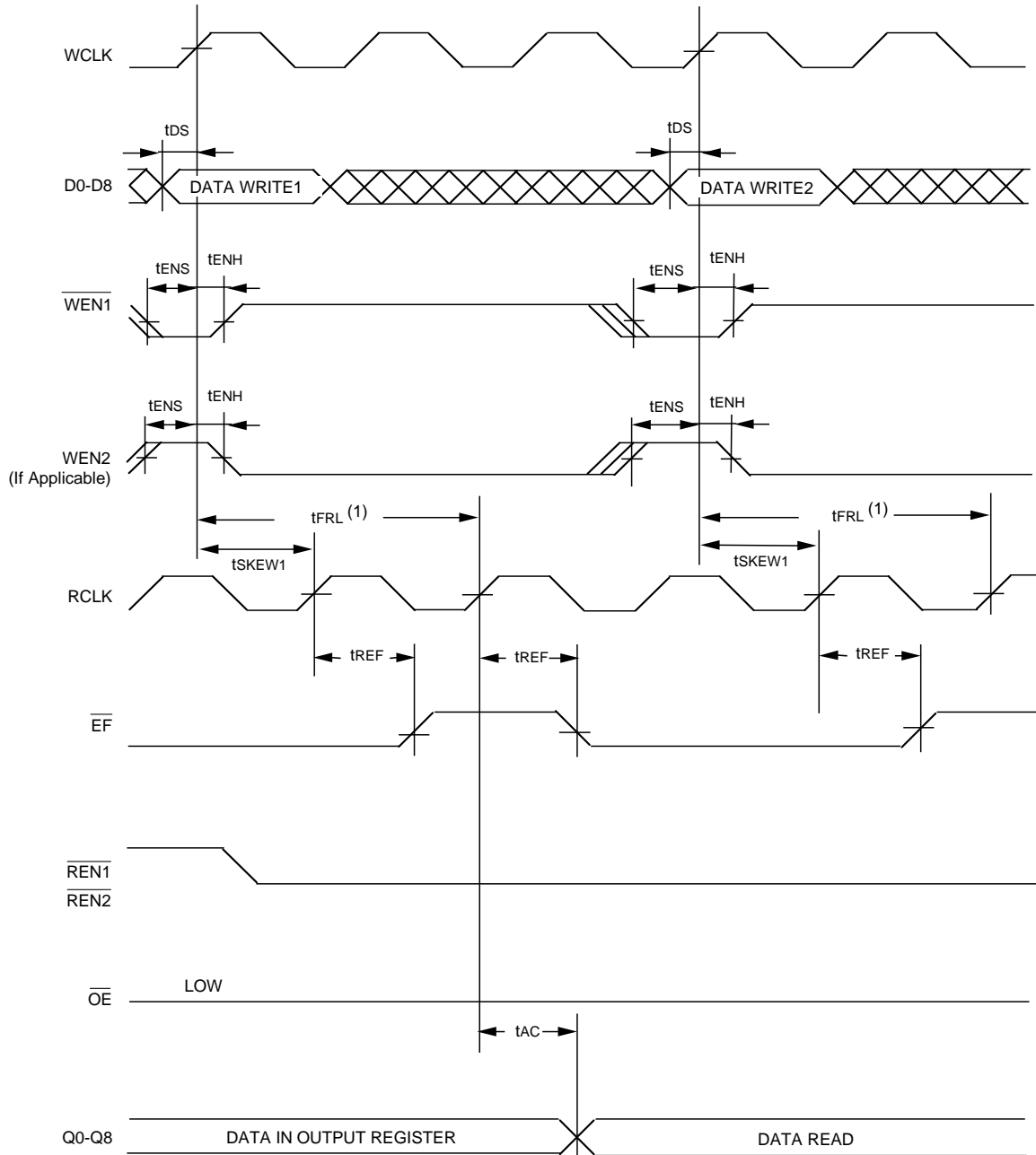
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• Full Flag Timing



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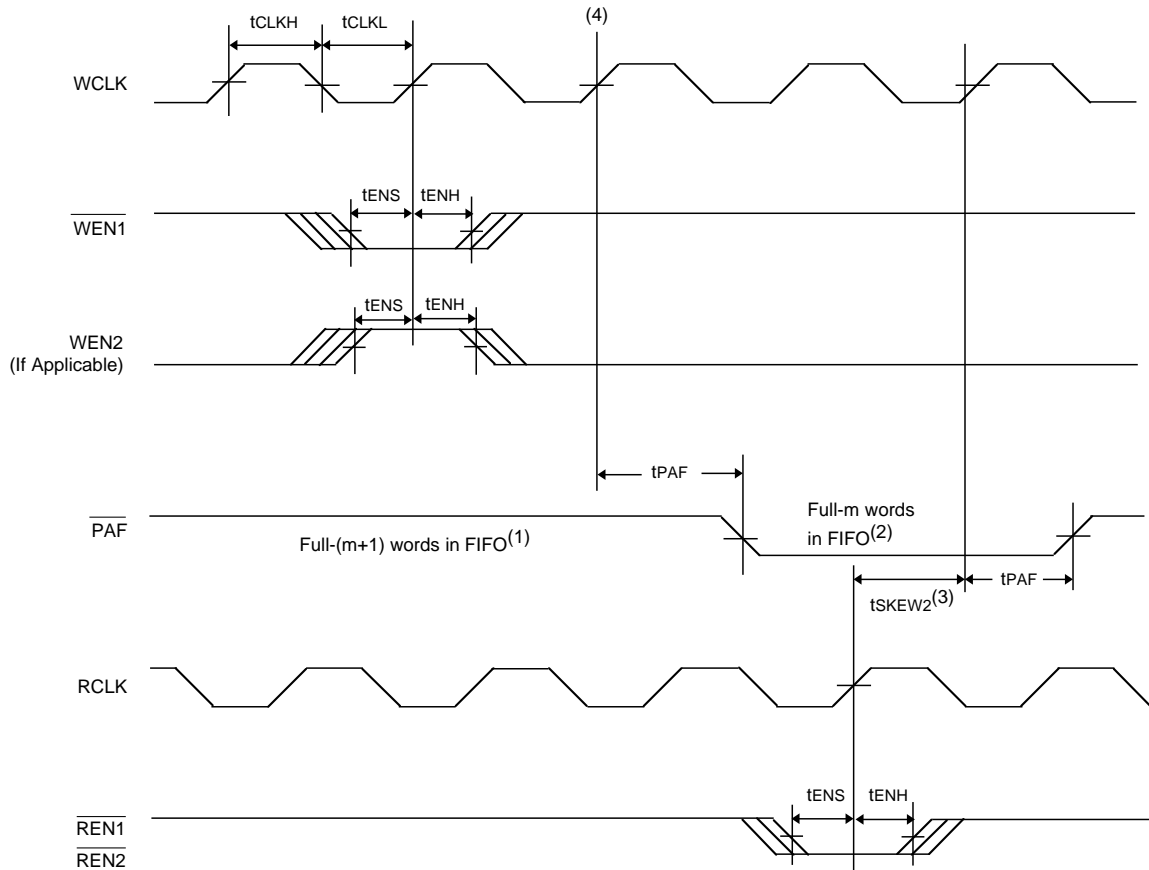
• Empty Flag Timing



NOTE :

- When $t_{SKEW1} \geq$ minimum specification, $t_{FRL} \text{ maximum} = t_{CLK} + t_{SKEW1}$.
 When $t_{SKEW1} \leq$ minimum specification, $t_{FRL} \text{ maximum} = 2t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$.

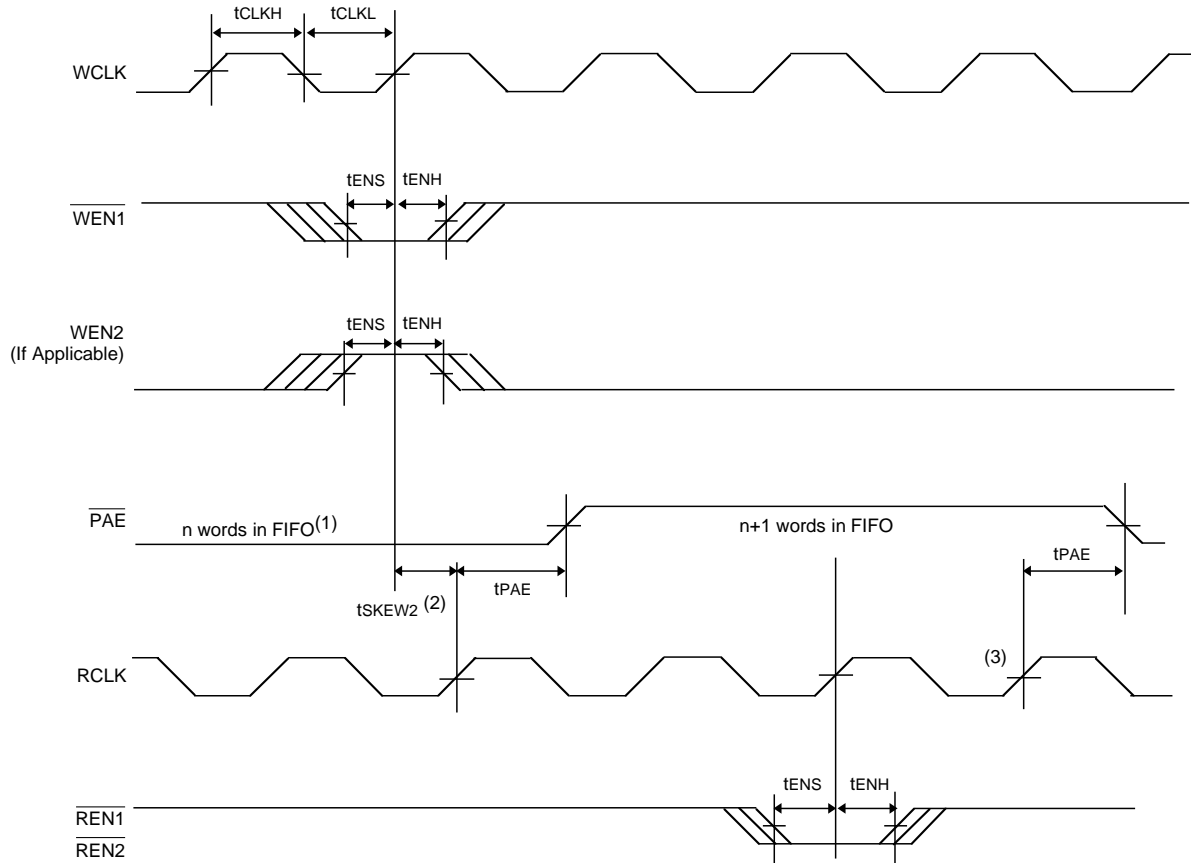
• Programmable Full Flag Timing



NOTES :

1. \overline{PAF} offset= m .
2. 64- m words in for M66850, 256- m words in for M66851, 512- m words in for M66852, 1024- m words in for M66853.
3. t_{SKEW2} is the minimum time between a rising RCLK edge and a rising WCLK edge for \overline{PAF} to change during that clock cycle.
 If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW2} , then \overline{PAF} may not change state until the next rising edge of WCLK.
4. If a write is performed on this rising edge of the write clock, there will be Full- $(m-1)$ words in the FIFO when \overline{PAF} goes LOW.

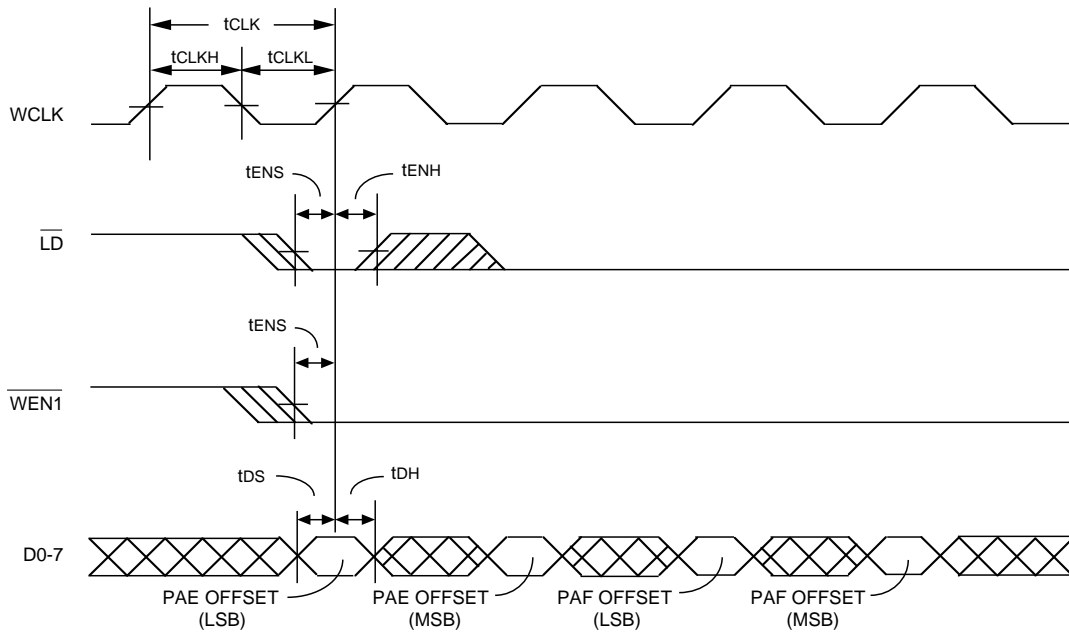
• Programmable Empty Flag Timing



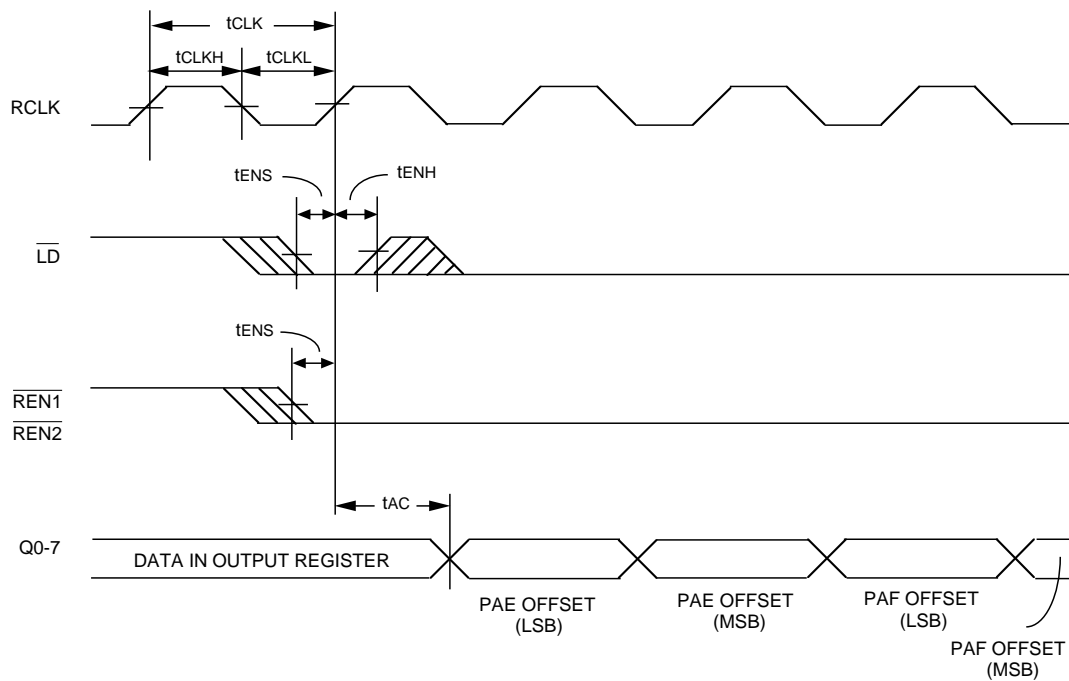
NOTES :

1. \overline{PAE} offset = m.
2. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge for \overline{PAE} to change during that clock cycle.
If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2} , then \overline{PAE} may not change state until the next rising edge of RCLK.
3. If a read is performed on this rising edge of the read clock, there will be Empty+(n-1) words in the FIFO when \overline{PAE} goes LOW.

• Write Offset Registers Timing

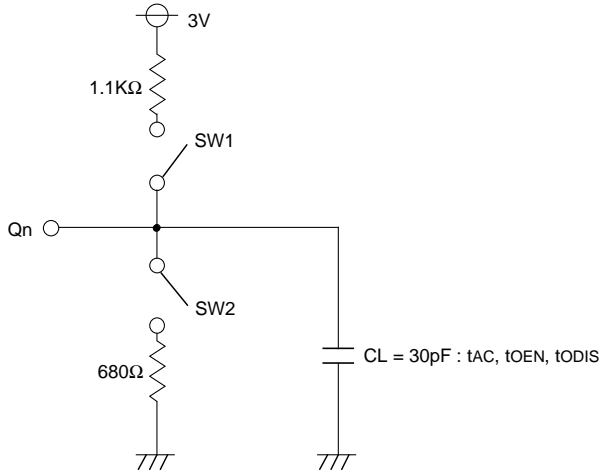


• Read Offset Registers Timing



NOTE :
 A read and write should not be performed simultaneously to the offset registers.

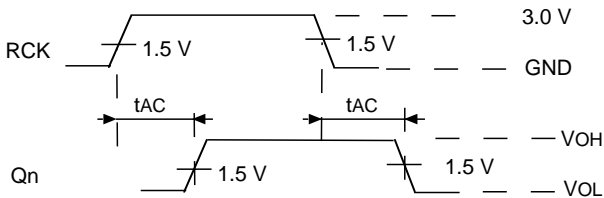
PARAMETER MEASUREMENT INFORMATION



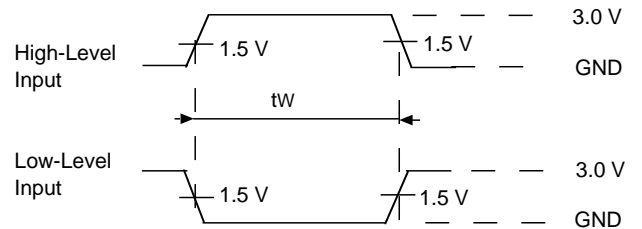
Item	SW1	SW2
tAC	Close	Close
tPLZ	Close	Open
tPHZ	Open	Close
tPZL	Close	Open
tPZH	Open	Close

Input Pulus Level : 0 – 3V
 Input Pulus Rising time and Falling time : 3 ns
 Threshold voltage of Input / Output : 1.5V
 But tPLZ is decided at 10% of output pulse. tPHZ is decided at 90% of output pulse.
 Output Load : Including Test board and scope capacitances.

VOLTAGE WAVEFORM PROPAGATION DELAY TIMES



VOLTAGE WAVEFORM PULSE DURATION TIMES



VOLTAGE WAVEFORM ENABLE AND DISABLE TIMES

