Bookly Micro

4 Megabit (512 K x 8/256 K x 16) Flash Memory PA29LV400T/B

3.0 Volt-Only Boot Block

DEVICE FEATURES

- **Single Power Supply**
  - Voltage Range: 3.0 to 3.6 volt for both read and write operations
- **Sector Architecture**
  - Byte Mode (512K x 8): One 16-Kbyte, two 8-Kbyte, one 32-Kbyte, and seven 64-Kbyte sectors
  - Word Mode (256K x 16): One 8-Kword, two 4-Kword, one 16-Kword, and seven 32-Kword sectors
- **Top or Bottom Boot Block Configuration**
- **Read Access Time**
  - Access time: 55, 70, 90 and 120 ns
- **Power Consumption**
  - Automatic sleep mode current: 200 nA
  - Standby mode current: 200 nA
  - Read current: 7 mA
  - Program/Erase current: 30 mA
- **Erase Features**
  - Chip Erase Capability
  - Sector Protection: Using hardware method to lock a sector and prevent any program or erase operations within that sector. Sectors can be locked in-system or via programming equipment. Temporary Sector Unprotect feature allows code changes in previously locked sectors.
- **Erase Suspend/Erase Resume**
  - Suspends an erase operation to read data from, or program data to a sector that is not being erased, then resumes the erase operation
- **Unlock Bypass Program**
  - Reduce overall programming time when issuing multiple program command sequences
- **Embedded Algorithms**
  - Embedded erase algorithm automatically preprograms and erases the entire chip or any combination of designated sectors
  - Embedded program algorithm automatically writes and verifies data at specified addresses
- **End-of-Program or End-of-Erase Software Detection**
  - Data# Polling
  - Toggle Bit
- **End-of-Program or End-of-Erase Hardware Detection**
  - Ready/Busy# Pin (RY/BY#)
- **Hardware Reset (RESET#)**
  - Hardware method to reset the device to reading array data
- **JEDEC Standard**
  - Pin-out and software compatible with single-power supply Flash memory
- **High Reliability:**
  - Endurance cycles: **1K** (Typical)
  - Data retention at 125ºC: **10-year**
- **Package Option**
  - 48- pin TSOP
  - 44- pin SO

PRODUCT DESCRIPTION

The PA29LV400B/T is a 4 Mbit, 3.0 volt-only Flash memory organized in 524,288 bytes or 262,144 words. The word-wide data (x16) appears on DQ15–DQ0 and the byte-wide data (x8) appears on DQ7–DQ0. This device can be programmed in-system using 3.0-volt single V_{CC} supply. No V_{PP} is required for write or erase operation. The device can also be programmed in standard EPROM programmers.

The device offers access times of 55, 70, 90 and 120 ns. The device has separate control signals, chip enable (CE#), write enable (WE#) and output enable (OE#), to eliminate bus contention. The device requires a 3.0-volt single power supply for both read and write operations. Both the program and erase operations are performed using the internally generated high voltages.

The device has command set that is compatible with the JEDEC single-power-supply Flash standard. The write cycles latch addresses and data needed for programming and erase operations. To read data from the device is similar to reading from other Flash or EPROM devices.

The programming operation occurs by executing the program command sequence. This initiates the Embedded Program Algorithm, which is an internal algorithm that automatically times the program pulse widths and verifies the proper cell margin. The Unlock Bypass Mode facilitates a faster programming time by issuing two write cycles (instead of four write cycles) to program data.

The erase operation occurs by executing the erase command sequence. This initiates the Embedded Erase Algorithm, which is an internal algorithm that automatically pre-programs the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies the proper cell margin.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, or by reading the DQ7 (Data# Polling) and DQ6 (Toggle Bit) status bits. After a program or erase cycle has been completed, the device is ready to read array data or to accept another command.

The sector erase architecture allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. Hardware data protection feature includes a low V_{CC} detector that automatically inhibits write operation during power transition. The hardware sector protection feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved during in-system operation or via programming equipment.

The Erase Suspend feature allows the user to put erase on hold for any period of time to read data from, or program data to any sector that is not selected for erasure.

The hardware RESET# pin will terminate any operation in progress and reset the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device in this case.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the automatic sleep mode. The system can also place the device into the standby mode. Both modes reduce greatly the power consumption.

The device is offered in package types of 44-pin SO and 48-pin TSOP.

ORDERING INFORMATION
Standard Products

The order number is defined by a combination of the following elements.

PA29LV400 B -70R E C

Temperature Range
C = Commercial (0°C to 70°C)
I = Industrial (-40°C to +85°C)
E = Extended (-55°C to +125°C)

Package Type
E = 48-Pin Thin Small Outline Package (TSOP), Standard Pin-out (TS048)
F = 48-Pin Thin Small Outline Package (TSOP), Reverse Pin-out (TSR048)
S = 44-Pin Small Outline Package (SO044)
KGD = Known Good Die

Speed Option
55R = 55ns
70R = 70ns
90R = 90ns
12R = 120ns

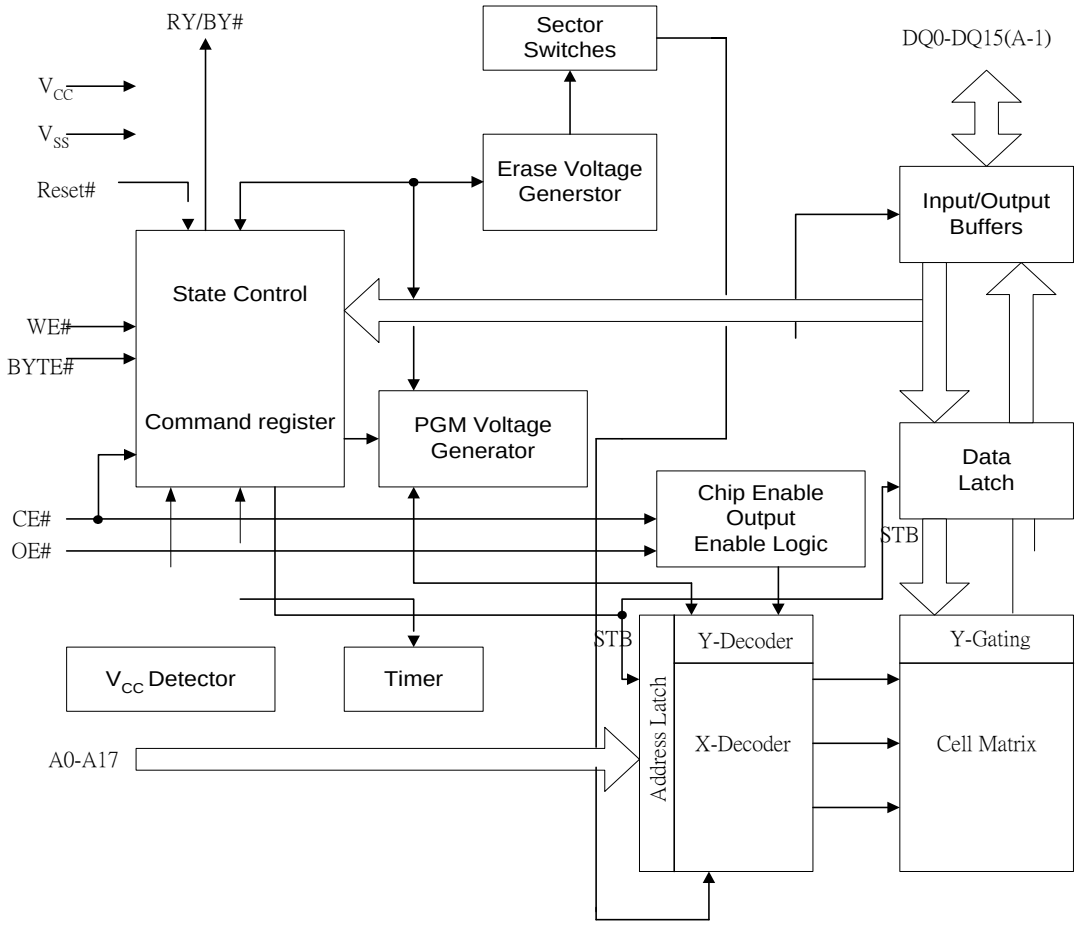
Boot Code Sector Architecture
T = Top Sector
B = Bottom Sector

Device Number/Description
PA29LV400
4 Megabit (512K x 8-Bit /256K x 16-Bit) Flash Memory
3.0-Volt only Read, Program and Erase

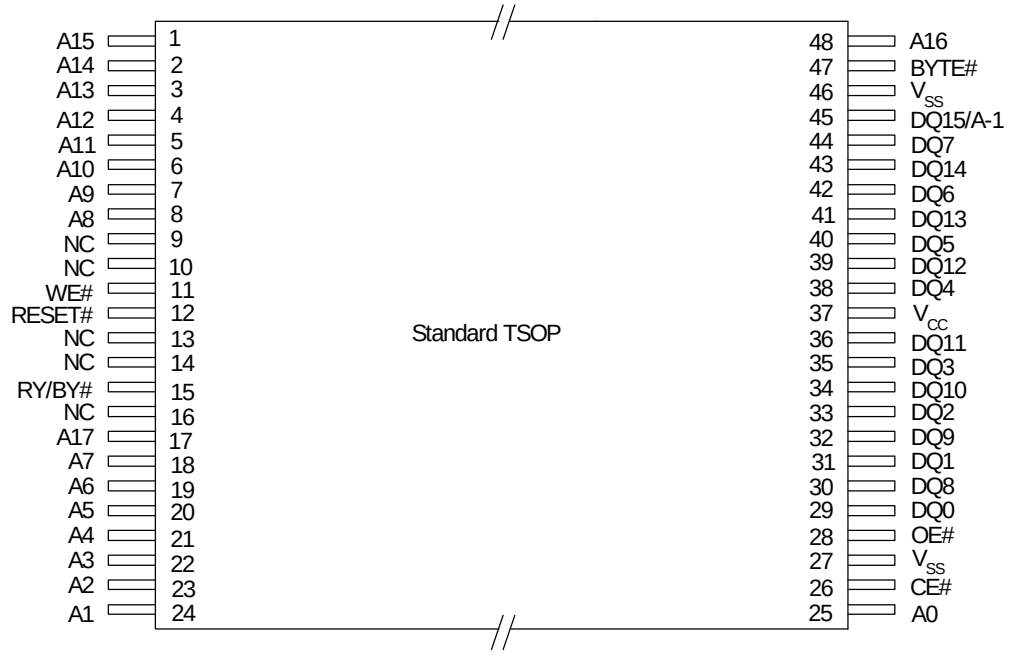
Valid Combinations for TSOP and SO Packages	
PA29LV400T-55R PA29LV400B-55R	EC, EI, EE, FC, FI, FE, SC, SI, SE
PA29LV400T-70R PA29LV400B-70R	
PA29LV400T-90R PA29LV400B-90R	
PA29LV400T-12R PA29LV400B-12R	

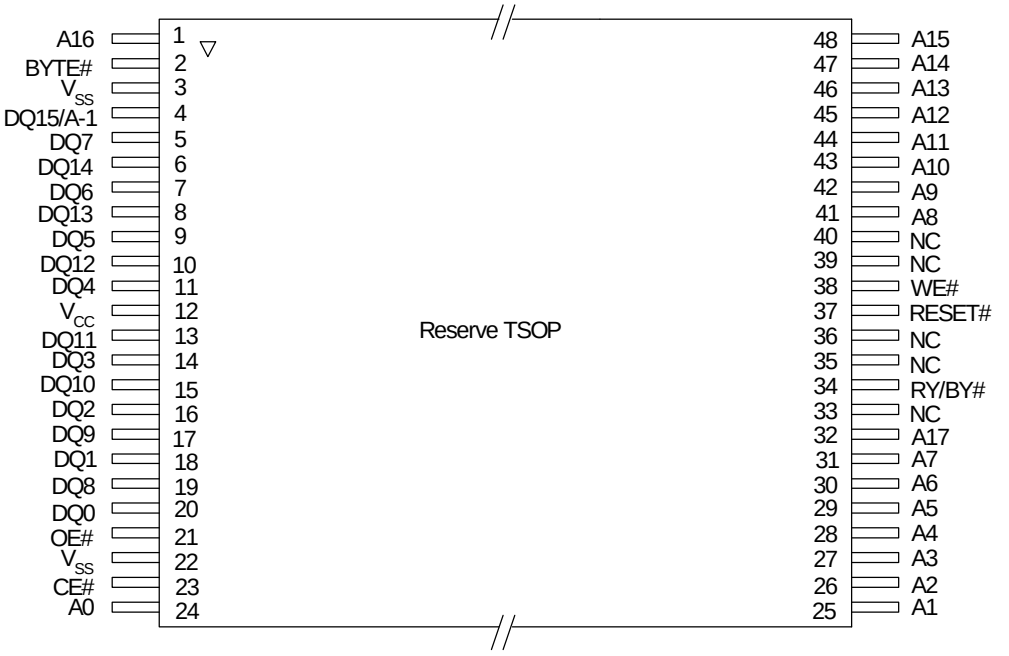
Valid Combinations: Valid Combinations list the configurations that are supported in volume for this device.

Functional Block Diagram

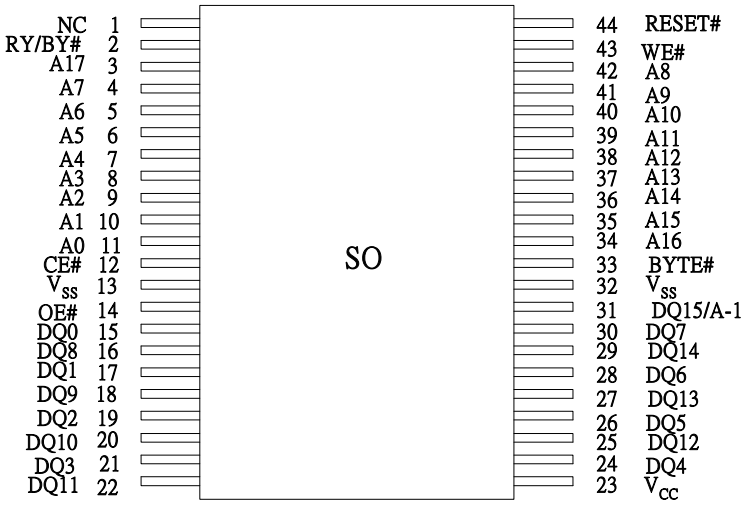


Pin Assignments





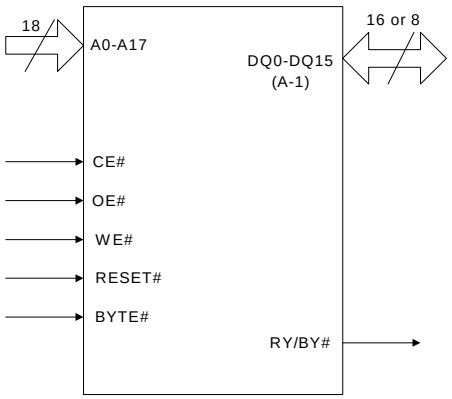
Pin Assignments



PIN DESCRIPTION

A0–A17 = 18 addresses
DQ0–DQ14 = 15 data inputs/outputs
DQ15/A-1 = DQ15 (data input/output, word mode), A-1 (LSB address input, byte mode)
BYTE# = Select 8-bit or 16-bit mode
CE# = Chip enable
OE# = Output enable
WE# = Write enable
RESET# = Hardware reset pin, active low
RY/BY# = Ready/Busy# output
VCC = 3.0-volt single power supply
VSS = Device ground
NC = Pin not connected internally

Logic Symbol



DEVICE OPERATION

The device operations are initiated through internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, and the address and data information that is needed to execute the command. The contents of the register serve as inputs to the internal state machine. The outputs of state machine dictate the function of the device. Table 1 lists the device operations, the inputs and control levels they require, and the resulting output.

Word/Byte Configuration

The BYTE# pin controls the device data I/O pins DQ15–DQ0 to operate either in byte or word configuration. If the BYTE# pin is set at logic '1', the device is in word configuration, and DQ15–DQ0 are active and controlled by CE# and OE#. If the BYTE# pin is set at logic '0', the device is in byte configuration, and only data I/O pins DQ0–DQ7 are active and controlled by CE# and OE#. The data I/O pins DQ8–DQ14 are in tri-state, and the DQ15 pin is used as an input for the LSB (A-1) address function.

Read

To read array data from the outputs, the system must set the CE# and OE# pins to V_{IL}. CE# is the power control, which selects the device. OE# is the output control, which gates array data to the output pins. The WE# should remain at V_{IH}. The BYTE# pin determines whether the device outputs array data in words or bytes.

The internal state machine is set to read array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is required in this mode to obtain array data. The device remains enabled for read access until the command register contents are altered. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the

Table 1. PAC29LV400B/T Device Operation

Operation	CE#	OE#	WE#	Reset#	Addresses (Note)	DQ0-DQ7	DQ8-DQ15	
							Byte# $=V_{IH}$	Byte# $=V_{IL}$
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	A_{IN}	D_{OUT}	D_{OUT}	DQ8-DQ14 = High-Z, DQ15= A-1
Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	A_{IN}	D_{IN}	D_{IN}	
Standby	$V_{CC}\pm$ 0.3V	X	X	$V_{CC}\pm$ 0.3V	X	High-Z	High-Z	High-Z
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	High-Z	High-Z	High-Z
Reset	X	X	X	V_{IL}	X	High-Z	High-Z	High-Z
Sector Protect	V_{IL}	V_{IH}	V_{IL}	V_{ID}	Sector Address, A6=L, A1=H, A0=L	D_{IN}	X	X
Sector Unprotect	V_{IL}	V_{IH}	V_{IL}	V_{ID}	Sector Address, A6=H, A1=H, A0=L	D_{IN}	X	X
Temporary Sector Unprotect	X	X	X	V_{ID}	A_{IN}	D_{IN}	D_{IN}	High-Z

V_{ID} = 12.0 ± 0.5 V, X = Don't Care, A_{IN} = Addresses In, D_{IN} = Data In, D_{OUT} = Data Out

Notes: Addresses are A17:A0 in word mode (BYTE# = V_{IH}), and A17:A-1 in byte mode (BYTE# = V_{IL}).

standard read timings, except that if it reads an address that is within the erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See "Erase Suspend/Erase Resume" for more information about this mode.

The system must issue the reset command to re-enable the device for reading array data if DQ5 goes high, or while in the autoselect mode. See the "Reset" in next section.

The Read Operations table provides the read parameters, and Figure 11 shows the timing diagram. I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

Reset

Writing the reset command to the device resets the device to reading array data. The address bits are don't care for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasing begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to reading array data (also applies to autoselect during Erase Suspend).

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to reading array data (also applies during Erase Suspend).

Write Command/Command Sequence

Writing specific address and data commands or sequences into the command register initiates device operations. Table 2 defines the valid register command sequences. Writing incorrect address and data values or writing them in the improper sequence resets the device to reading array data.

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must set WE# and CE# to V_{IL}, and OE# to V_{IH}. All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to the appropriate timing diagrams in the "AC Characteristics" section.

I_{CC2} in the DC Characteristics table represents the active current specification for the write mode. The "AC Characteristics" section contains timing specification tables and timing diagrams for the write operations.

Word/Byte Program

The system may program the device by word or byte, depending on the state of the BYTE# pin. Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is not required to provide further controls or timings. The device automatically generates the program pulses and verifies the programmed cell margin. Table 2 shows the address and data requirements for the byte program command sequence. When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using DQ7, DQ6 or RY/BY#. See "Write Operation Status" for information on these status bits.

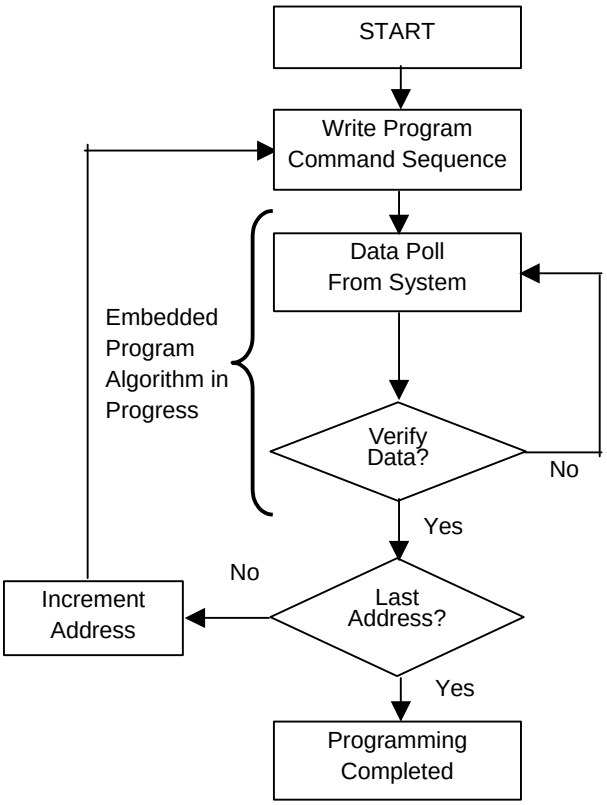
Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a hardware reset immediately terminates the programming operation. In order to ensure data integrity, the Byte Program command sequence should be reinitiated once the device has reset to reading array data. Programming is allowed in any sequence and across sector boundaries. A bit cannot be programmed from a "0" back to a "1". Attempting to do so may halt the operation and set DQ5 to "1", or cause the Data# Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still "0". Only erase operations can convert a "0" to a "1".

Unlock Bypass

The unlock bypass feature allows the system to program bytes or words to the device faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles, followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 2 shows the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the program address and the data 90h. The second cycle need only contain the data 00h. The device then returns to reading array data.

Figure 1 illustrates the algorithm for the program operation. See the Erase/Program Operations table in “AC Characteristics” for parameters, and to Figure 15 for timing diagrams.



Note: See Table 2 for program command sequence.

Figure 1. Program Operation

Chip Erase

Chip erase is a six-bus-cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Then, two additional unlock write cycles are issued, followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 2 shows the address and data requirements for the chip erase command sequence.

Any commands written to the chip during the Embedded Erase algorithm are ignored. Note that a hardware reset during the chip erase operation immediately terminates the operation. In order to ensure data integrity, the Chip Erase command sequence should be reinitiated once the device has returned to reading array data.

The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. See “Write Operation Status” for information about these status bits. When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

Figure 2 illustrates the algorithm for the erase operation. See the Erase/Program Operations tables in “AC Characteristics” for parameters, and Figure 16 for timing diagrams.

Sector Erase

Sector erase is a six-bus-cycle operation. The sector erase command sequence is initiated by

writing two unlock cycles, followed by a set-up command. Then, two additional unlock write cycles are issued, followed by the address of the sector to be erased, and the sector erase command. Table 2 shows the address and data requirements for the sector erase command sequence.

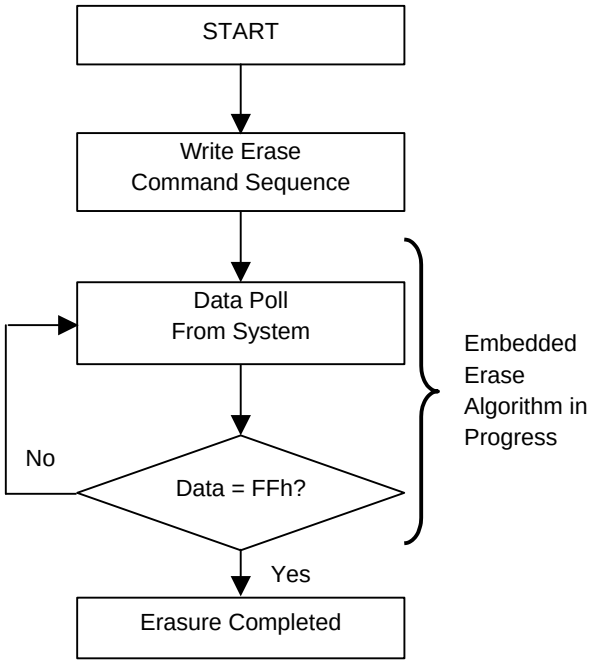
The device does not require the system to preprogram the memory prior to erase. The Embedded Erase algorithm automatically programs and verifies the sector with an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50 µs begins. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise the last address and command might not be accepted, and erasure may begin. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. If the time between additional sector erase commands can be assumed to be less than 50 µs, the system need not monitor DQ3. Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to reading array data. The system must rewrite the command sequence and any additional sector addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out. (See the "DQ3: Sector Erase Timer" section.) The time-out begins from the rising edge of the final WE# pulse in the command sequence. Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. Note that a hardware reset during the sector erase operation immediately terminates the operation. In order to ensure data integrity, the Sector Erase command sequence should be reinitiated once the device has returned to reading array data.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. (Refer to "Write Operation Status" for information on these status bits.)

Figure 2 illustrates the algorithm for the erase operation. Refer to the Erase/Program Operations tables in the "AC Characteristics" section for parameters, and the Figure 16 for timing diagrams.



Notes:

1. See Table 2 for erase command sequence.
2. See "DQ3: Sector Erase Timer" for more information.

Figure 2. Erase Operation

Erase Suspend/Erase Resume

The Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if it is written during the chip erase operation or Embedded Program algorithm. Writing the Erase Suspend command during the Sector Erase time-out immediately terminates the time-out period and suspends the erase operation. Addresses are "don't care" when writing the Erase Suspend command.

When the Erase Suspend command is written during a sector erase operation, the device

requires a maximum of 20 µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the system can read array data from, or program data to any sector not selected for erasure. (The device "erase suspends" all sectors selected for erasure.) Normal read and write timings and command definitions are applied to these read and program operations. Reading at any address within erase-suspended sectors produces status data on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. See "Write Operation Status" for information on these status bits.

After an erase-suspended program operation is complete, the system can once again read array data within non-suspended sectors. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See "Write Operation Status" for more information.

The system may also write the autoselect command sequence when the device is in the Erase Suspend mode. The device allows reading autoselect codes even at addresses within erasing sectors because the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation. See "Autoselect Mode" for more information.

The system must write the Erase Resume command (address bits are "don't care") to exit the erase suspend mode and continue the sector erase operation. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the device has resumed erasing.

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification through identifier codes appearing on outputs DQ7–DQ0. This mode is primarily used for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. Besides, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} (11.5 V to 12.5 V) on address pin A9. Address pins A6, A1, and A0 must be set as shown in Table 5. In addition, when verifying sector protection, the sector address must appear properly on the highest order address bits (see Tables 3 and 4). Table 5 shows the remaining address bits that are don't care. After setting all necessary bits as required, the programming equipment may then read the corresponding identifier code on DQ7–DQ0.

To access the autoselect codes in-system, the host system can also issue the autoselect command via the command register, as shown in Table 2. This method does not require V_{ID}.

The autoselect command sequence is initiated by writing two unlock cycles, followed by the autoselect command. The device then enters the autoselect mode, and the system may read at any address any number of times without initiating another command sequence. When device is in word-wide configuration, the read cycles at addresses XX00h, XX03h and XX02h retrieve the manufacturer code, and the read cycle at address XX01h returns the device identification code. When device is in byte-wide configuration, the read cycles at addresses XX00h, XX06h and XX04h retrieve the manufacturer code, and the read cycle at address XX02h returns the device identification code. A read cycle containing a sector address (SA) and the address XX40h in word mode (or XX80h in byte mode) returns 01h if that sector is protected, or 00h if it is unprotected. Refer to Tables 3 and 4 for valid sector addresses.

The system must write the reset command to exit the autoselect mode and return to reading array data.

Standby Mode

When the system is not reading from or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state and are independent of the OE# input. The device enters the CMOS standby mode when the CE# and RESET# pins are both held at V_{CC} ± 0.3V. Note that this is a more restricted voltage range than V_{IH}. If CE# and RESET# are held at V_{IH}, but not within V_{CC} ± 0.3V, the device will be in the standby mode, but the standby current will be greater. When in either of these standby modes, the device requires standard

access time (t_{CE}) for read access before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} in the DC Characteristics table represents the standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes device power consumption. The device enables automatically this mode when addresses are remain stable for t_{ACC} + 30ns. The automatic sleep mode is independent of the CE#, WE# and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. I_{CC5} in the DC Characteristics table represents the automatic sleep mode current specification.

Hardware Reset Pin (RESET#)

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, sets all output pins in tri-state, and ignores all read/write commands during the period of RESET# pulse.

The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated after the device is ready to accept another command sequence. This function is to ensure the data integrity.

Current is reduced during the period of RESET# pulse. When RESET# is held at V_{SS} ± 0.3 V, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within V_{SS} ± 0.3 V, the standby current will be larger.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains at “0” (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (i.e., the RY/BY# pin remains at “1”), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the RESET# pin returns to V_{IH}. Refer to the AC Characteristics tables for RESET# parameters and to Figure 12 for the timing diagram.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

Sector Protection/Unprotection

The hardware sector protection can disable both program and erase operations in any sector. The hardware sector unprotection can re-enable both program and erase operations in previously protected sectors. To alter sector protection requires V_{ID} on the RESET# pin, which can be implemented either in-system or via programming equipment. Figure 3 shows the algorithms and Figure 21 shows the timing diagram. For sector unprotect, all unprotected sectors must first be protected prior to the first sector unprotect write cycle. The device is shipped with all sectors unprotected.

Perfect Device Technology Ltd. offers the option of programming and protecting sectors at its factory prior to shipping the device.

Temporary Sector Unprotect

This feature allows temporary unprotection of previously protected sectors to change data in-system. The Sector Unprotect mode is activated by setting the RESET# pin to V_{ID}. During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once V_{ID} is removed from the RESET# pin, all the previously protected sectors are protected again. Figure 4 shows the algorithm, and Figure 20 shows the timing diagrams of this feature.

Hardware Data Protection

The command sequence with the requirement of unlock cycles for programming or erasure provides data protection against inadvertent writes (refer to Table 2 for command definitions).

In addition, the following hardware data protection features can prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system

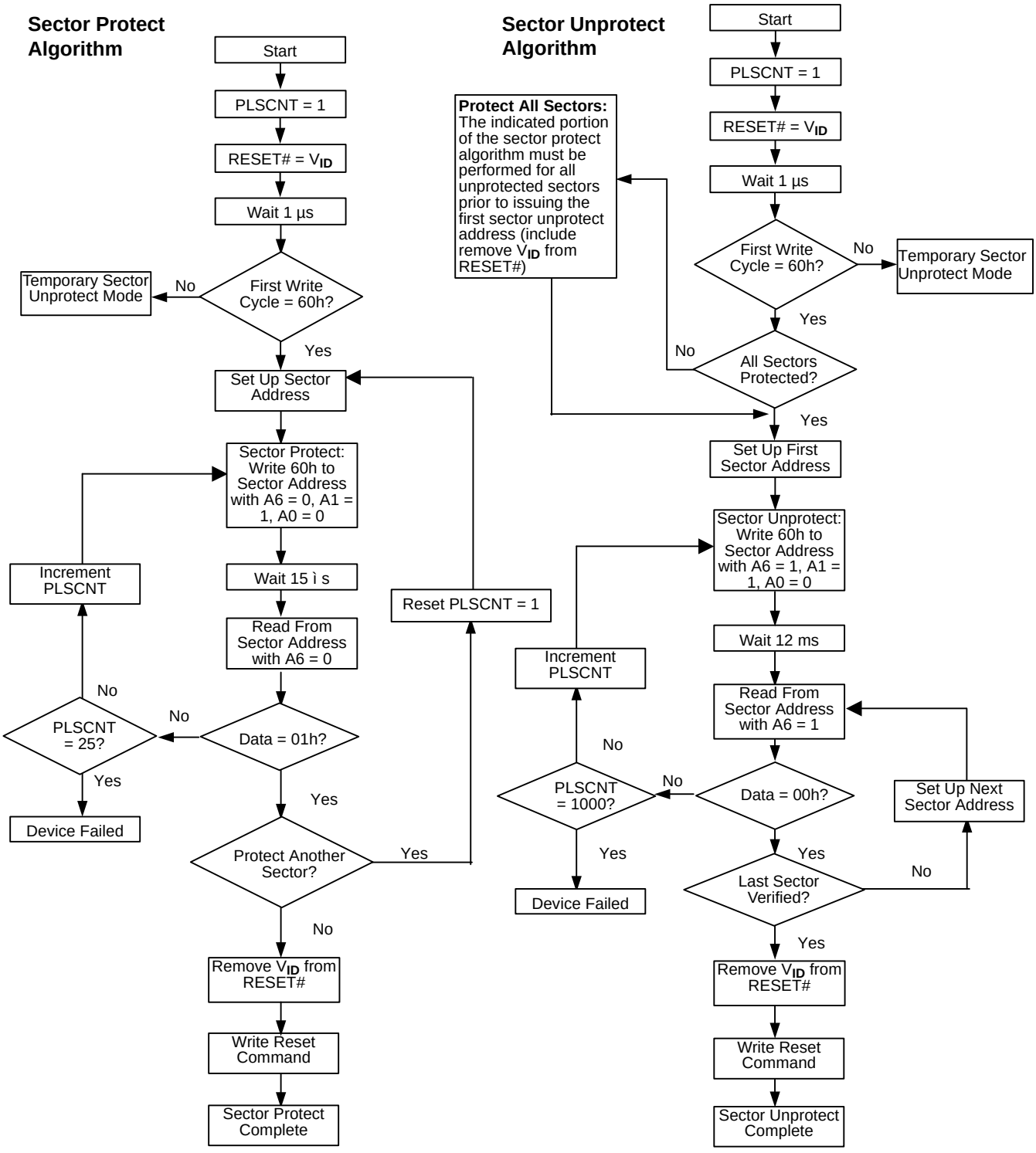
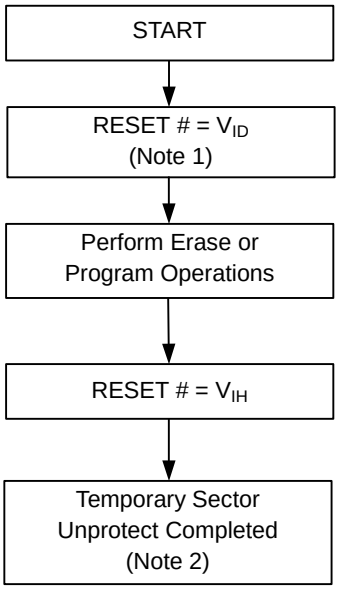


Figure 3. In-System Sector Protect/Unprotect



Notes:
1. All protected sectors unprotected.
3. All previously protected sectors are protected once again.

Figure 4. Temporary Sector Unprotect Operation

noise.

Noise/Glitch Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Write Inhibit Mode

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = $V_{IH,}$ or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to reading array data on power-up.

WRITE OPERATION STATUS

The device provides several bits to determine the status of a write operation: DQ2, DQ3, DQ5, DQ6, DQ7, and RY/BY#. Table 6 and the following subsections describe the functions of these bits. DQ7, RY/BY#, and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. These three bits are discussed first.

Data# Polling (DQ7)

The Data# Polling bit, DQ7, indicates whether an Embedded Algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the program or erase command sequence.

During the Embedded Program algorithm, the device output on DQ7 is complement to the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1µs, then the device returns to reading array data.

During the Embedded Erase algorithm, Data# Polling produces a “0” on DQ7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a “1” on DQ7. This is analogous to the complement/true datum output described for the Embedded Program algorithm: the erase function changes all the bits in a sector to “1”; prior to this, the device outputs the “complement”, or “0”. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 µs, then the device returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

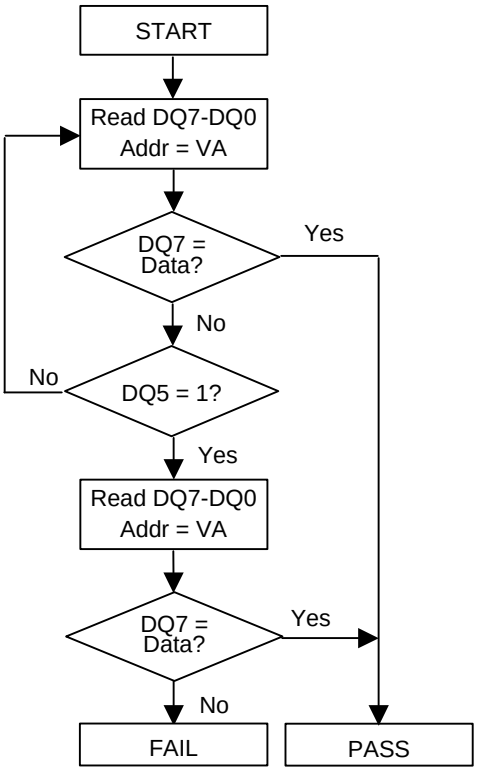
When the system detects DQ7 has changed from the complement to true data, it can read valid data at DQ7–DQ0 on the following read cycles. This is because DQ7 may change asynchronously with DQ0–DQ6 while Output Enable (OE#) is asserted low. Figure 17, Data# Polling Timings (During Embedded Algorithms) in the “AC Characteristics” section, illustrates this timing diagram.

Table 6 shows the outputs for Data# Polling

on DQ7. Figure 5 shows the Data# Polling algorithm.

Ready/Busy# (RY/BY#)

The RY/BY# is a dedicated, open-drain output pin that indicates whether an Embedded Algorithm is complete or in progress. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel and connect to V_{CC} with a pull-up resistor.



Notes:
1. VA = Valid address for programming. During a sector erase operation, a valid address is an address within any sector selected for erasure. During chip erase, a valid address is any non-protected sector address.
2. DQ7 should be rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.

Figure 5. Data# Polling Algorithm

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is ready to read array data (including during the Erase Suspend mode), or is in the standby mode. Table 6 shows the outputs for RY/BY#. Figures 14, 17 and 18 shows RY/BY# for reset, program, and erase operations, respectively.

Toggle Bit I (DQ6)

The "Toggle Bit I" on DQ6 indicates whether an Embedded Program or Erase algorithm is complete or in progress, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. The system may use either OE# or CE# to control the read cycles. When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (i.e., the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on DQ7: Data# Polling).

If a program address falls within a protected sector, DQ6 toggles for approximately 2 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspended program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 6 shows the outputs for Toggle Bit I on DQ6. Figure 6 shows the toggle bit algorithm. Figure 18 in the "AC Characteristics" section shows the toggle bit timing diagrams. Figure 19 shows the differences between DQ2 and DQ6 in graphical form. See also the subsection on DQ2: Toggle Bit II.

Toggle Bit II (DQ2)

When used with DQ6, the "Toggle Bit II" on DQ2 indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

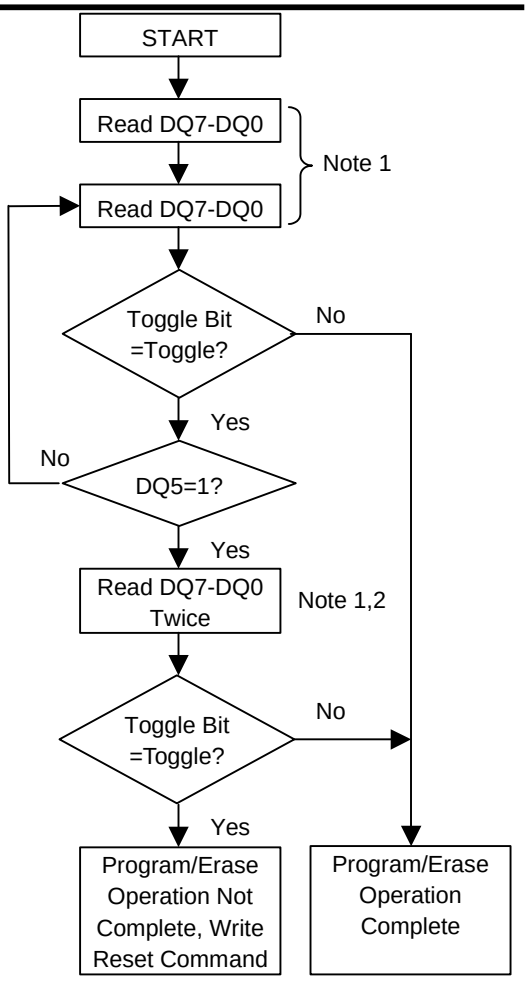
DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 6 to compare outputs for DQ2 and DQ6.

Figure 6 shows the toggle bit algorithm in flowchart form. See also the DQ6: Toggle Bit I subsection. Figure 18 shows the toggle bit timing diagram. Figure 19 shows the differences between DQ2 and DQ6 in graphical form.

Reading Toggle Bits DQ6/DQ2

Refer to Figure 6 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the



Notes:

1. Read toggle bit twice to determine whether or not it is toggling (see text).
2. Recheck toggle bit because it may stop toggling as DQ5 changes to "1" (see text).

Figure 6. Toggle Bit Algorithm

device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In

this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 6).

Exceeded Timing Limits (DQ5)

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under this condition, DQ5 produces a “1”, which indicates a failure condition that the program or erase cycle was not successfully completed.

In addition, the DQ5 failure condition may appear if the system tries to program a “1” to a location that is previously programmed to “0.” Only an erase operation can change a “0” back to a “1”. Under this condition, the device halts the operation, and when the operation has exceeded the timing limit, DQ5 produces a “1”.

Under above two conditions, the system must issue the reset command to return the device to reading array data.

Sector Erase Timer (DQ3)

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not an erase operation has begun. Note that the sector erase timer does not apply to the chip erase command. If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out is complete, DQ3 switches from “0” to “1”. If the time between additional sector erase commands from the system can be assumed to be less than 50 μs, the system need not monitor DQ3. See also the “Sector Erase” section.

After the sector erase command sequence is written, the system should read the status on DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to make sure the device has accepted the command sequence, and then read DQ3. If DQ3 is “1”, the internally controlled erase cycle has begun; all further commands (other than Erase Suspend) are ignored until the erase operation is complete. If DQ3 is “0”, the device will accept additional sector erase commands. To make sure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted. Table 6 shows the outputs for DQ3.

Table 2. PA29LV400T/B Command Definitions

Command Sequence (Note 1)			Cycles	Bus Cycles (Notes 2-5)											
				First		Second		Third		Fourth		Fifth		Sixth	
				Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 6)			1	RA	RD										
Reset (Note 7)			1	XXX	F0										
Autoselect (Note 8)	Manufacturer ID	Word	4	555	AA	2AA	55	555	90	X00	7F				
		Byte		AAA		555		AAA		X00					
		Word	4	555	AA	2AA	55	555	90	X03	7F				
		Byte		AAA		555		AAA		X06					
		Word	4	555	AA	2AA	55	555	90	X02	1F				
		Byte		AAA		555		AAA		X04					
	Device ID, Top Boot Block	Word	4	555	AA	2AA	55	555	90	X01	2202				
		Byte		AAA		555		AAA		X02	02				
	Device ID, Bottom Boot Block	Word	4	555	AA	2AA	55	555	90	X01	2203				
		Byte		AAA		555		AAA		X02	03				
	Sector Protect Verify (Note 9)	Word	4	555	AA	2AA	55	555	90	(SA) X40	XX00				
											XX01				
		Byte		AAA		555		AAA		(SA) X80	00				
											01				
Program		Word	4	555	AA	2AA	55	555	A0	PA	PD				
		Byte		AAA		555		AAA							
Unlock Bypass		Word	3	555	AA	2AA	55	555	20						
		Byte		AAA		555		AAA							
Unlock Bypass Program (Note 10)			2	XXX	A0	PA	PD								
Unlock Bypass Reset (Note 11)			2	XXX	90	XXX	00								
Chip Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
		Byte		AAA		555		AAA		AAA		555		AAA	
Sector Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
		Byte		AAA		555		AAA		AAA		555			
Erase Suspend (Note 12)			1	XXX	B0										
Erase Resume (Note 13)			1	XXX	30										

Legend:
X = Don't care
RA = Address of the memory location to be read.
RD = Data read from location RA during read operation.
PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.
PD = Data to be programmed at location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.
SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A17–A12 uniquely select any sector.

Notes:
1. See Table 1 for description of bus operations.
2. All values are in hexadecimal.
3. Except when reading array or autoselect data, all bus cycles are write operations.
4. Data bits DQ15–DQ8 are don't care for unlock and command cycles.
5. Address bits A17–A11 are don't care for unlock and command cycles, except when SA or PA required.
6. No unlock or command cycles required when reading array data.
7. The Reset command is required to return to reading array data when device is in the autoselect mode, or if DQ5 goes high (while the device is providing status data).
8. The fourth cycle of the autoselect command sequence is a read cycle.

9. The data is 00h for an unprotected sector and 01h for a protected sector. See “Autoselect Command Sequence” for more information.
10. The Unlock Bypass command is required prior to the Unlock Bypass Program command.
11. The Unlock Bypass Reset command is required to return to reading array data when the device is in the unlock bypass mode.
12. The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.
13. The Erase Resume command is valid only during the Erase Suspend mode.

Table 3. PA29LV400T Top Boot Block Sector Address Table

Sector	A17	A16	A15	A14	A13	A12	Sector Size (KBytes/ KWords)	Address Range (in hexadecimal)	
								(x 8) Address Range	(x 16) Address Range
SA0	0	0	0	X	X	X	64/32	00000h-0FFFFh	00000h-07FFFh
SA1	0	0	1	X	X	X	64/32	10000h-1FFFFh	08000h-0FFFFh
SA2	0	1	0	X	X	X	64/32	20000h-2FFFFh	10000h-17FFFh
SA3	0	1	1	X	X	X	64/32	30000h-3FFFFh	18000h-1FFFFh
SA4	1	0	0	X	X	X	64/32	40000h-4FFFFh	20000h-27FFFh
SA5	1	0	1	X	X	X	64/32	50000h-5FFFFh	28000h-2FFFFh
SA6	1	1	0	X	X	X	64/32	60000h-6FFFFh	30000h-37FFFh
SA7	1	1	1	0	X	X	32/16	70000h-77FFFh	38000h-3BFFFh
SA8	1	1	1	1	0	0	8/4	78000h-79FFFh	3C000h-3CFFFh
SA9	1	1	1	1	0	1	8/4	7A000h-7BFFFh	3D000h-3DFFFh
SA10	1	1	1	1	1	X	16/8	7C000h-7FFFFh	3E000h-3FFFFh

Table 4. PA29LV400B Bottom Boot Block Sector Address Table

Sector	A17	A16	A15	A14	A13	A12	Sector Size (KBytes/ KWords)	Address Range (in hexadecimal)	
								(x 8) Address Range	(x 16) Address Range
SA0	0	0	0	0	0	X	16/8	00000h-03FFFh	00000h-01FFFh
SA1	0	0	0	0	1	0	8/4	04000h-05FFFh	02000h-02FFFh
SA2	0	0	0	0	1	1	8/4	06000h-07FFFh	03000h-03FFFh
SA3	0	0	0	1	X	X	32/16	08000h-0FFFFh	04000h-07FFFh
SA4	0	0	1	X	X	X	64/32	10000h-1FFFFh	08000h-0FFFFh
SA5	0	1	0	X	X	X	64/32	20000h-2FFFFh	10000h-17FFFh
SA6	0	1	1	X	X	X	64/32	30000h-3FFFFh	18000h-1FFFFh
SA7	1	0	0	X	X	X	64/32	40000h-4FFFFh	20000h-27FFFh
SA8	1	0	1	X	X	X	64/32	50000h-5FFFFh	28000h-2FFFFh
SA9	1	1	0	X	X	X	64/32	60000h-6FFFFh	30000h-37FFFh
SA10	1	1	1	X	X	X	64/32	70000h-7FFFFh	38000h-3FFFFh

Notes for Tables 3 and 4: Address range is A17:A-1 in byte mode and A17:A0 in word mode.

Table 5. PA29LV400B/T Autoselect Codes (High Voltage Method)

Description	Mode	CE#	OE#	WE#	A17 to A12	A11 to A10	A9	A8 to A7	A6	A5 to A2	A1	A0	DQ8 to DQ15	DQ7 to DQ0
Manufacturer ID		V_{IL}	V_{IL}	V_{IH}	X	X	V_{ID}	X	V_{IL}	X	V_{IL}	V_{IL}	X	7Fh
											V_{IH}	V_{IH}	X	7Fh
											V_{IH}	V_{IL}	X	1Fh
Device ID: PA29LVF400T (Top Boot Block)	Word	V_{IL}	V_{IL}	V_{IH}	X	X	V_{ID}	X	V_{IL}	X	V_{IL}	V_{IH}	22h	02h
	Byte	V_{IL}	V_{IL}	V_{IH}									X	02h
Device ID: PA29LV400B (Bottom Boot Block)	Word	V_{IL}	V_{IL}	V_{IH}	X	X	V_{ID}	X	V_{IL}	X	V_{IL}	V_{IH}	22h	03h
	Byte	V_{IL}	V_{IL}	V_{IH}									X	03h
Sector Protection Verification		V_{IL}	V_{IL}	V_{IH}	SA	X	V_{ID}	X	V_{IH}	X	X	X	X	01h (Protected)
													X	00h (Unprotected)

Notes: SA = Sector Address, X = Don't Care

Table 6. Write Operation Status

Operation		DQ7 (Note2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)	RY/BY#
Standard Mode	Embedded Program Algorithm	DQ7#	Toggle	0	N/A	No Toggle	0
	Embedded Erase Algorithm	0	Toggle	0	1	Toggle	0
Erase Suspend Mode	Reading within Erase Suspended Sector	1	No Toggle	0	N/A	Toggle	1
	Reading within Non-Erase Suspended Sector	Data	Data	Data	Data	Data	1
	Erase-Suspended Program	DQ7#	Toggle	0	N/A	N/A	0

Notes:

1. DQ5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. See "DQ5: Exceeded Timing Limits" for more information.
2. DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature Plastic Packages ……. –65°C to 150°C

Ambient Temperature with Power Applied. ……..... –65°C to 125°C

Voltage with Respect to Ground V_{CC} (Note 1)…… –0.5 V to +4.0 V

A9, and RESET# (Note 2)…… –0.5 V to +12.5 V

All Other Pins (Note 1)…….. –0.5 V to V_{CC} +0.5 V

Output Short Circuit Current (Note 3)……... 200 mA

Note:

1. Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 7. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods up to 20 ns. See Figure 8.
2. Minimum DC input voltage on pins A9, and RESET# is –0.5 V. During voltage transitions, A9, and RESET# may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 7. Maximum DC input voltage on pin A9 is +12.5 V, which may overshoot to 14.0 V for periods up to 20 ns.
3. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended period may affect device reliability.

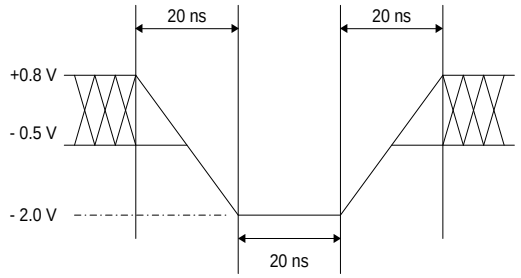


Figure 7. Maximum Negative Overshoot Waveform

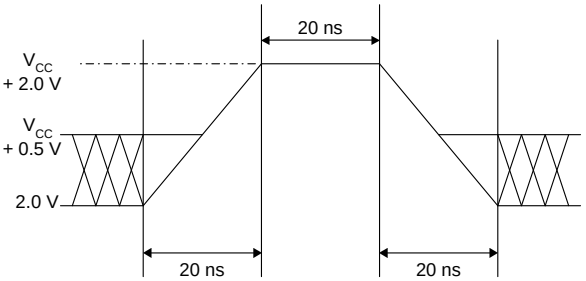


Figure 8. Maximum Positive Overshoot Waveform

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)…..……0°C to 70°C

Industrial (I) Devices

Ambient Temperature (T_A)……..…–40°C to 85°C

Extended (E) Devices

Ambient Temperature (T_A)…….–55°C to 125°C

V_{CC} Supply Voltages

V_{CC} for regulated voltage range….. 3.0 V to 3.6 V

V_{CC} for full voltage range…….. 2.7 V to 3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS
CMOS Compatible

Parameter	Description	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN}=V_{SS}$ to V_{CC}, $V_{CC}=V_{CC}$ max				±1.0	µA
I_{LIT}	A9 Input Load Current	$V_{CC}=V_{CC}$ max; A9=12.5V				35	µA
I_{LO}	Output Leakage Current	$V_{OUT}=V_{SS}$ to V_{CC}, $V_{CC}=V_{CC}$ max				±1.0	µA
I_{CC1}	V_{CC} Active Read Current (Note 1)	CE# = V_{IL}, OE# = V_{IH}, Byte Mode	5 MHz		7	12	mA
			1 MHz		2	4	mA
		CE# = V_{IL}, OE# = V_{IH}, Word Mode	5 MHz		7	12	mA
			1 MHz		2	4	mA
I_{CC2}	V_{CC} Active Write Current (Note 2, 3, 5)	CE#=V_{IL}, OE#=V_{IH}			30	50	mA
I_{CC3}	V_{CC} Standby Current (Note 2)	CE# and Reset#=V_{CC}±0.3V			0.2	5	µA
I_{CC4}	V_{CC} Reset Current (Note 2)	Reset#=V_{SS}±0.3V			0.2	5	µA
I_{CC5}	Automatic Sleep Mode (Notes 2, 4)	$V_{IH}=V_{CC}$±0.3V; $V_{IL}=V_{SS}$±0.3V			0.2	5	µA
V_{IL}	Input Low Voltage			-0.5		0.8	V
V_{IH}	Input High Voltage			0.7 x V_{CC}		V_{CC} + 0.3	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC}=3.3V		11.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL}=4.0mA, $V_{CC}=V_{CC}$ min				0.45	V
V_{OH1}	Output High Voltage	I_{OH}=-2.0mA, $V_{CC}=V_{CC}$ min		0.85V_{CC}			V
V_{OH2}		I_{OH}=-100µA, $V_{CC}=V_{CC}$ min		V_{CC}-0.4			V

Notes:

1. The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}. Typical V_{CC} is 3.0 V.
2. Maximum I_{CC} specifications are tested with V_{CC} = V_{CC} max.
3. I_{CC} active while Embedded Erase or Embedded Program is in progress.
4. Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30 ns.
5. Not 100% tested.

TEST CONDITIONS

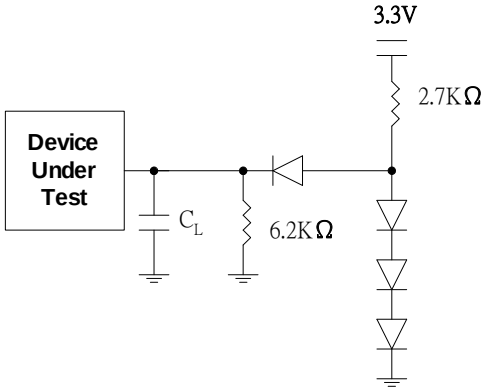


Table 7. Test Specifications

Test Condition	55 70	90, 120	Unit
Output Load	1TTL gate		
Output Load Capacitance, C_L (including jig capacitance)	30	100	pF
Input Rise and Fall Times	5		ns
Input Pulse Levels	0.0~3.0		V
Input Timing measurement reference levels	1.5		V
Output timing measurement reference levels	1.5		V

Note: Diodes are IN3064 or equivalent

Figure 9. Test Setup

KEY TO SWITCHING WAVEFORMS

Waveform	Inputs	Outputs
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is high Impedance State (High Z)

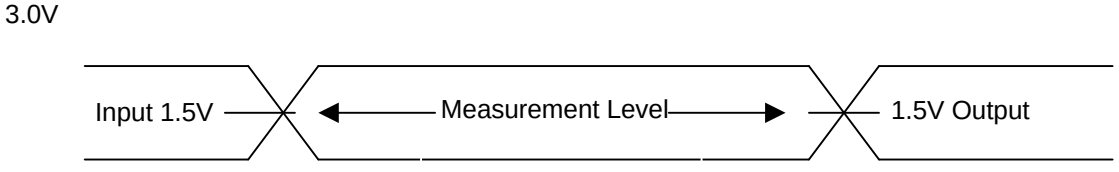


Figure 10. Input Waveforms and Measurement Levels

AC CHARACTERISTICS

Read Operations

Parameter		Description	Test Setup		Speed Options				Unit
JEDEC	Std				55	70	90	120	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)		Min	55	70	90	120	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	CE#=V_{IL} OE#=V_{IL}	Max	55	70	90	120	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	OE#=V_{IL}	Max	55	70	90	120	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay		Max	30	30	35	50	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Note 1)		Max	25	25	30	30	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Note 1)		Max	25	25	30	30	ns

Notes:

1. Not 100% tested.
2. See Figure 9 and Table 7 for test specifications.

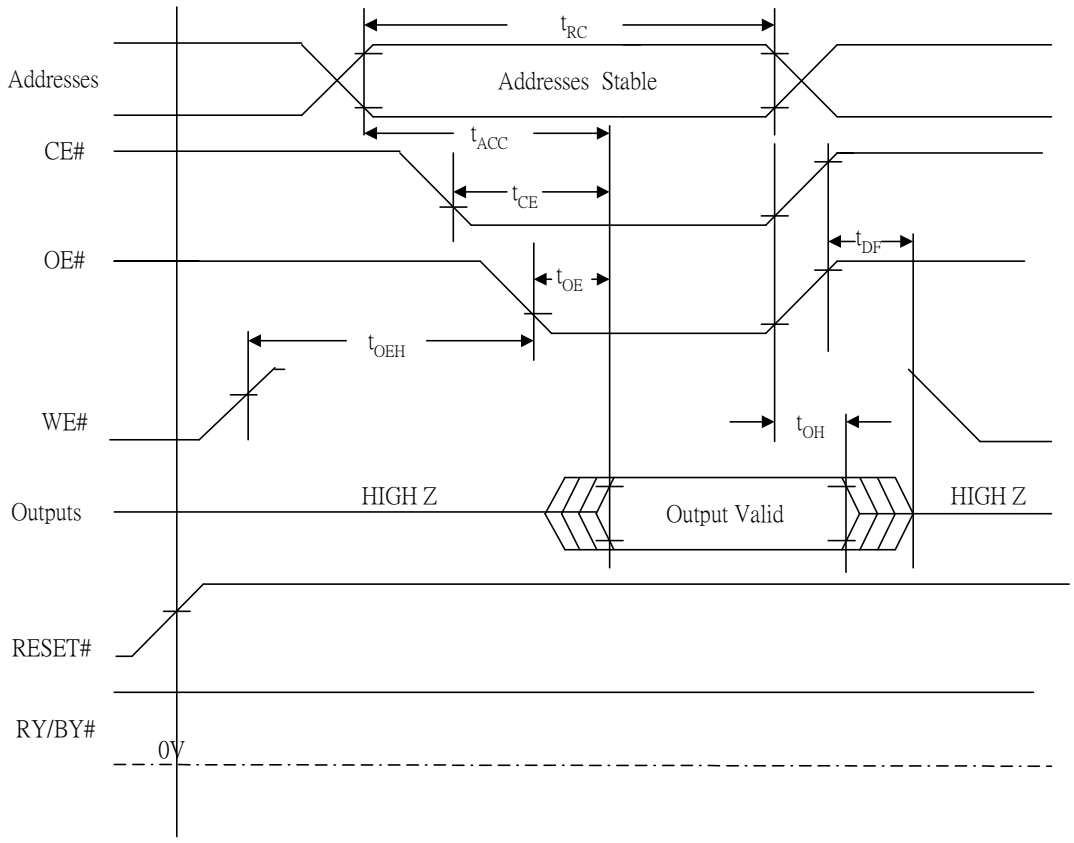


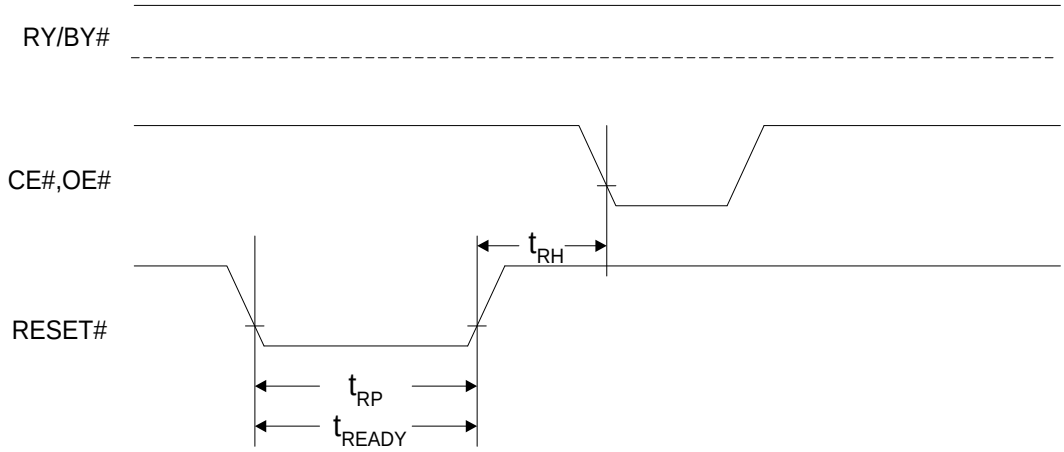
Figure 11. Read Timing

AC CHARACTERISTICS

Hardware Reset (Reset#)

Parameter		Description	Test Setup	All Speed Options	Unit
JEDEC	Std				
	t_{READY}	RESET# Pin Low (During Embedded Algorithms) to Read or Write (See Note)	Max	20	µs
	t_{READY}	RESET# Pin Low (NOT During Embedded Algorithms) to Read or Write (See Note)	Max	500	ns
	t_{RP}	RESET# Pulse Width	Min	500	ns
	t_{RH}	RESET# High Time Before Read (See Note)	Min	50	ns
	t_{RPD}	Reset# Low to Standby Mode	Min	20	µs
	t_{RB}	BY/BY# Recovery Time	Min	0	ns

Note: Not 100% tested.



Reset Timings NOT during Embedded Algorithms

Reset Timings during Embedded Algorithms

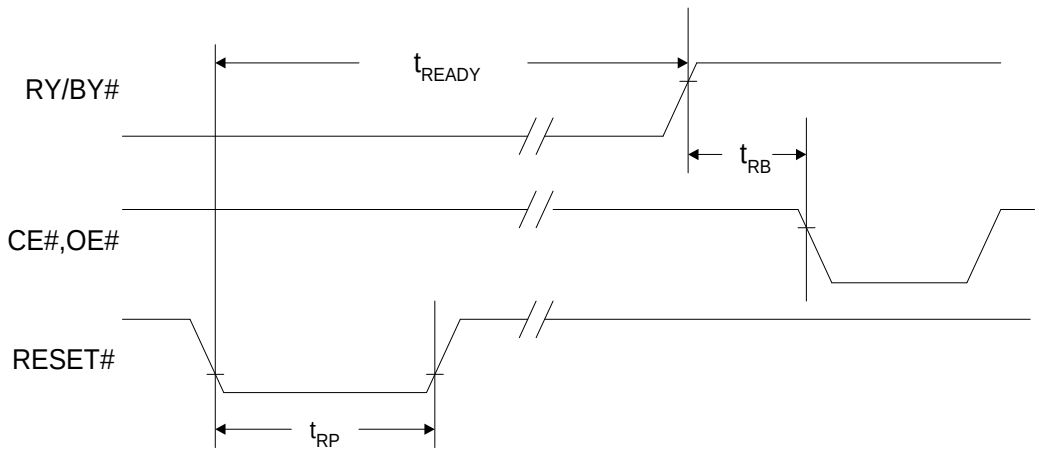


Figure 12. Reset# Timings

AC Characteristics

Word/Byte Configuration (Byte#)

Parameter		Description		Speed Options				Unit
JEDEC	Std			55	70	90	120	
	t_{ELFL} / t_{ELFH}	CE# to Byte# Switching Low or High	Max	5				ns
	t_{FLQZ}	Byte# Switching Low to Output High Z	Max	25	25	30	30	ns
	t_{FHQV}	Byte# Switching High to Output Active	Min	55	70	90	120	ns

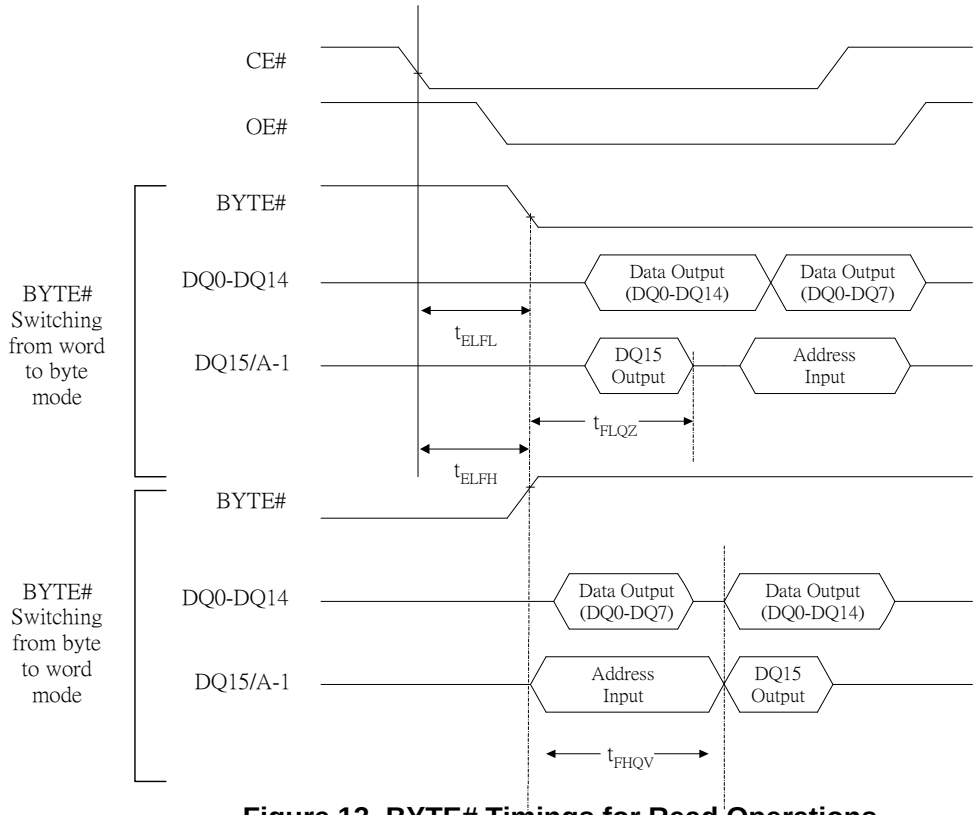
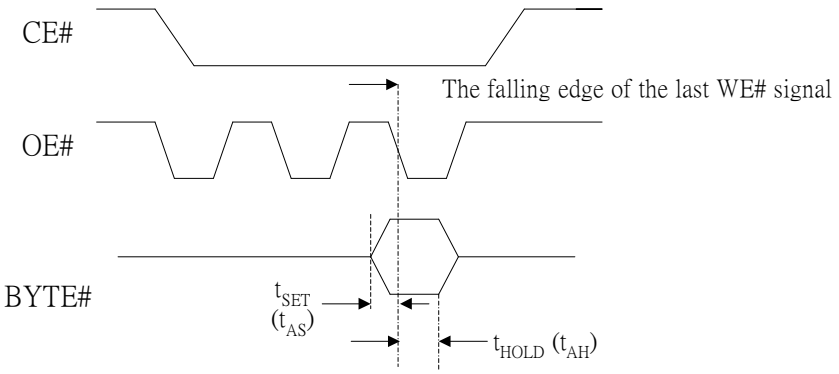


Figure 13. BYTE# Timings for Read Operations



Note: Refer to the Erase/Program Operations table for t_{AS} and t_{AH} specifications

Figure 14. BYTE# Timings for Write Operations

AC Characteristics

Erase/Program Operations

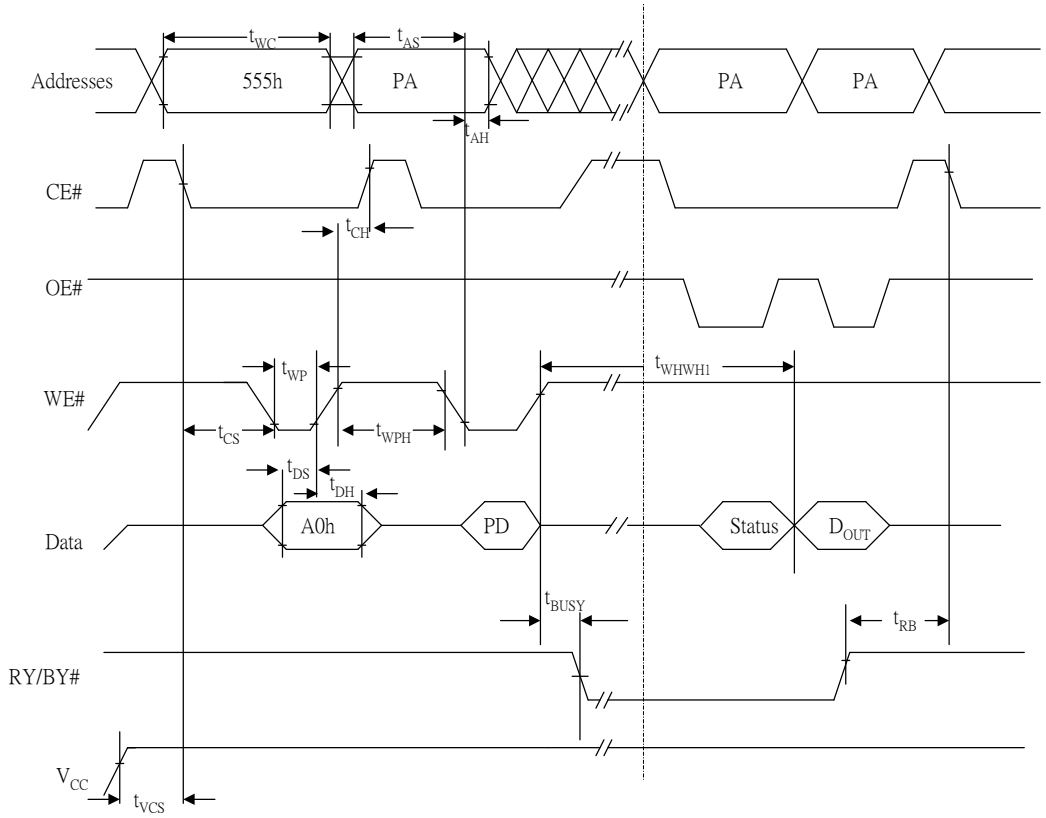
Parameter		Description			Speed Options				Unit
JEDEC	Std				55	70	90	120	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	55	70	90	120	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0				ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	45	45	45	50	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	35	35	45	50	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0				ns
	t_{OES}	Output Enable Setup Time		Min	0				ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0				ns
t_{ELWL}	t_{CS}	CE# Setup Time		Min	0				ns
t_{WHEH}	t_{CH}	CE# Hold Time		Min	0				ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	35	35	35	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		Min	30				ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Byte	Typ	13				µs
			Word	Typ	16				
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	0.7				sec
	t_{VCS}	V_{CC} Setup Time (Note 1)		Min	50				ns
	t_{RB}	Recovery Time from RY/BY#		Min	0				ns
	t_{BUSY}	Program/Erase Valid to RY/BY# Delay		Min	90				ns

Notes:

1. Not 100% tested.
2. See the “Erase and Programming Performance“ section for more information.

AC CHARACTERISTICS

Program Command Sequence (last two cycles) **Read Status Data (last two cycles)**

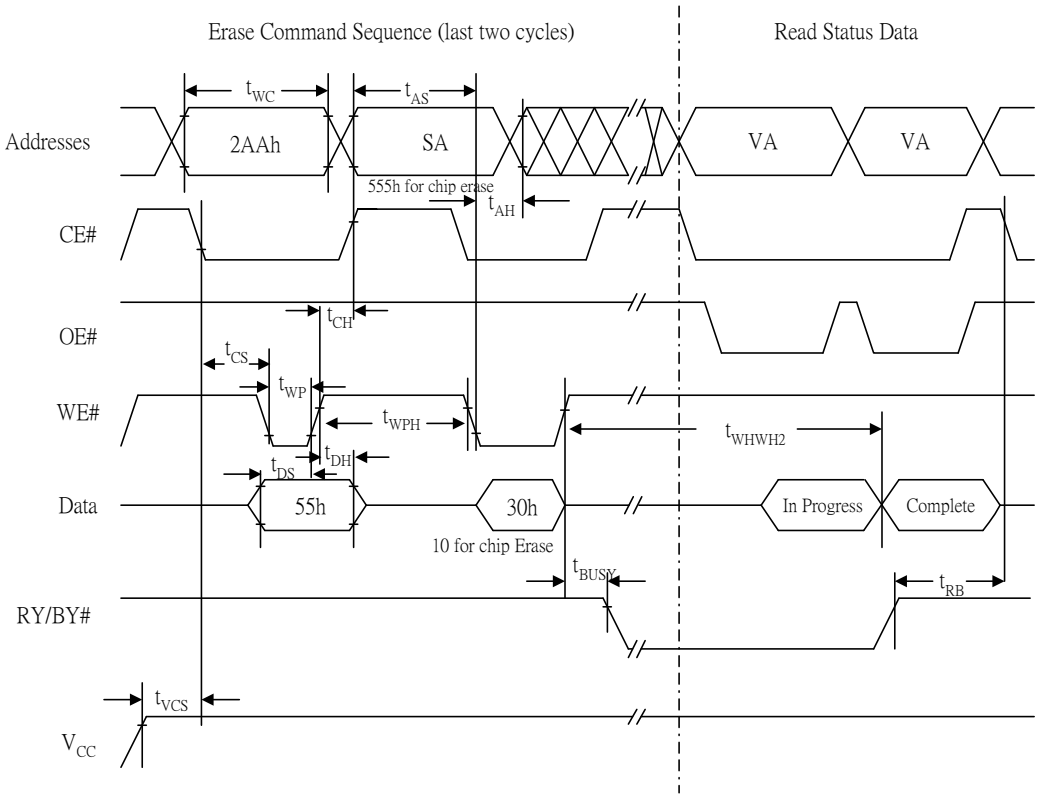


NOTES:

1. PA = program address, PD = program data, D_{OUT} is the true data at the program address.
2. Illustration shows device in word mode.

Figure 15. Program Operation Timings

AC CHARACTERISTICS

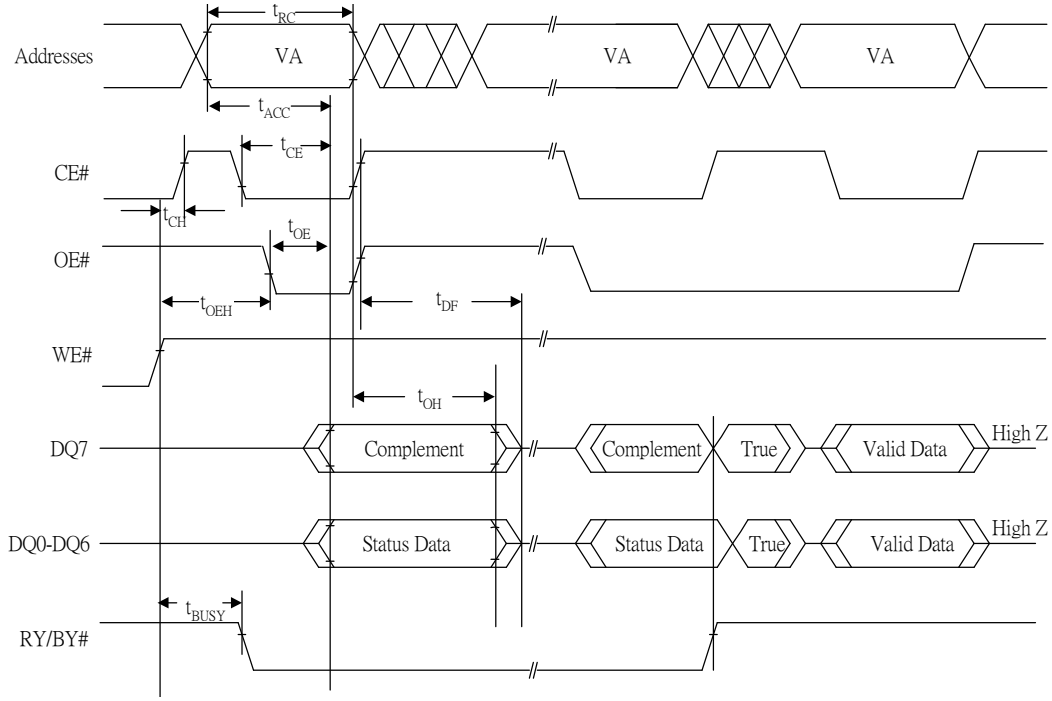


Notes:

1. SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see “Write Operation Status”)
2. Illustration shows device in word mode.

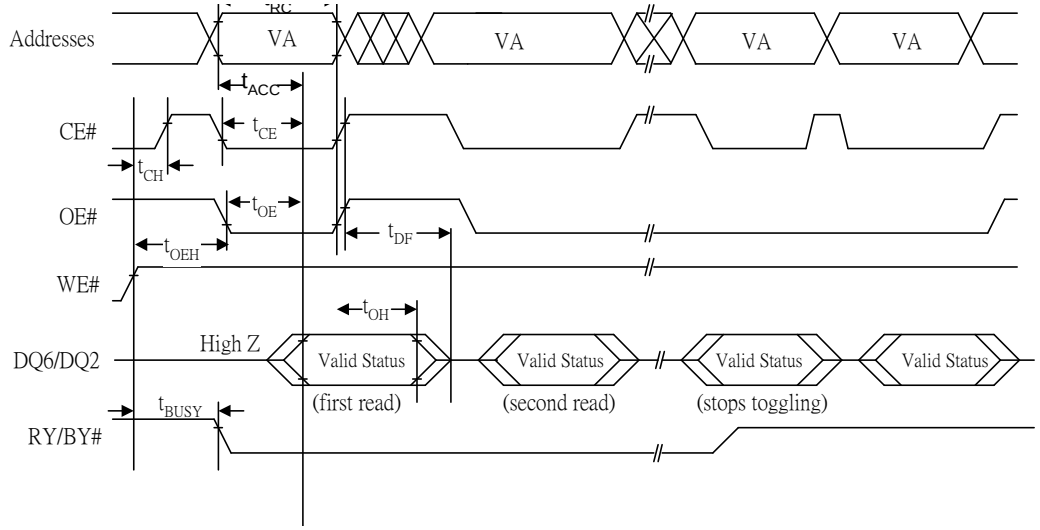
Figure 16. Chip/Sector Erase Operation Timings

AC CHARACTERISTICS



Note: VA=Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.

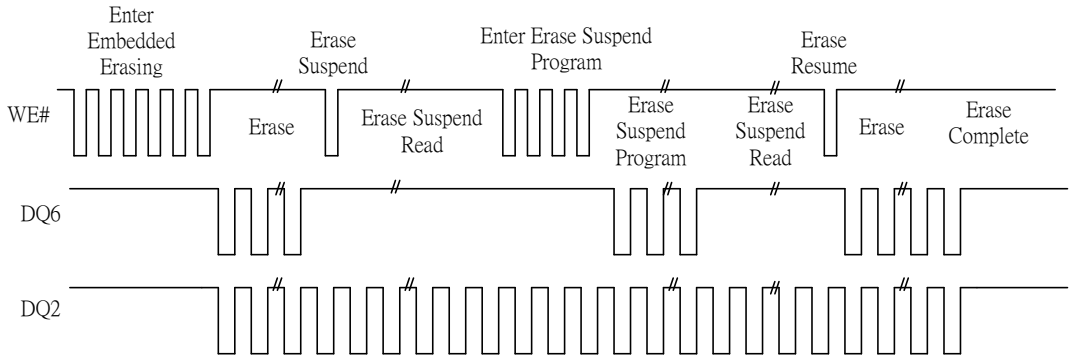
Figure 17. Data# Polling Timings (During Embedded Algorithms)



Note: VA=Valid address; not required for DQ6. Illustration shows first two status cycles after command sequence, last status read cycle and array data read cycle.

Figure 18. Toggle Bit Timings (During Embedded Algorithms)

AC CHARACTERISTICS



Note: The system may use OE# and CE# to toggle DQ2 and DQ6. DQ2 toggles only when read at an address within an erase-suspended sector.

Figure 19. DQ2 vs. DQ6

Temporary Sector Unprotect

Parameter		Description		All Speed Options	Unit
JEDEC	S				
	t_{VIDR}	V_{ID} Rise and Fall Time (See Note)	Min	500	ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4	µs

Note: Not 100% tested

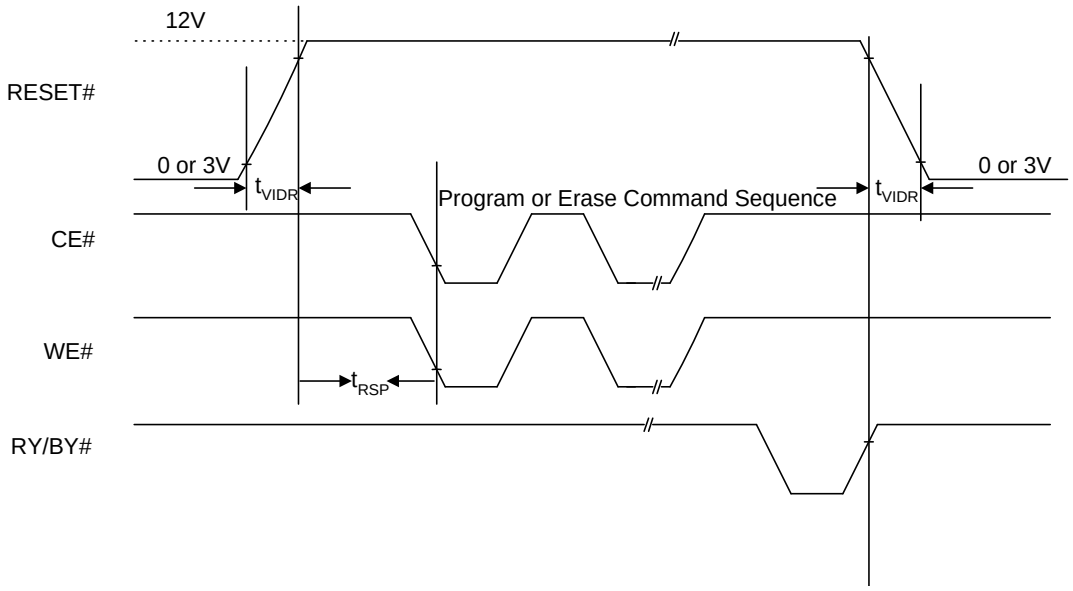
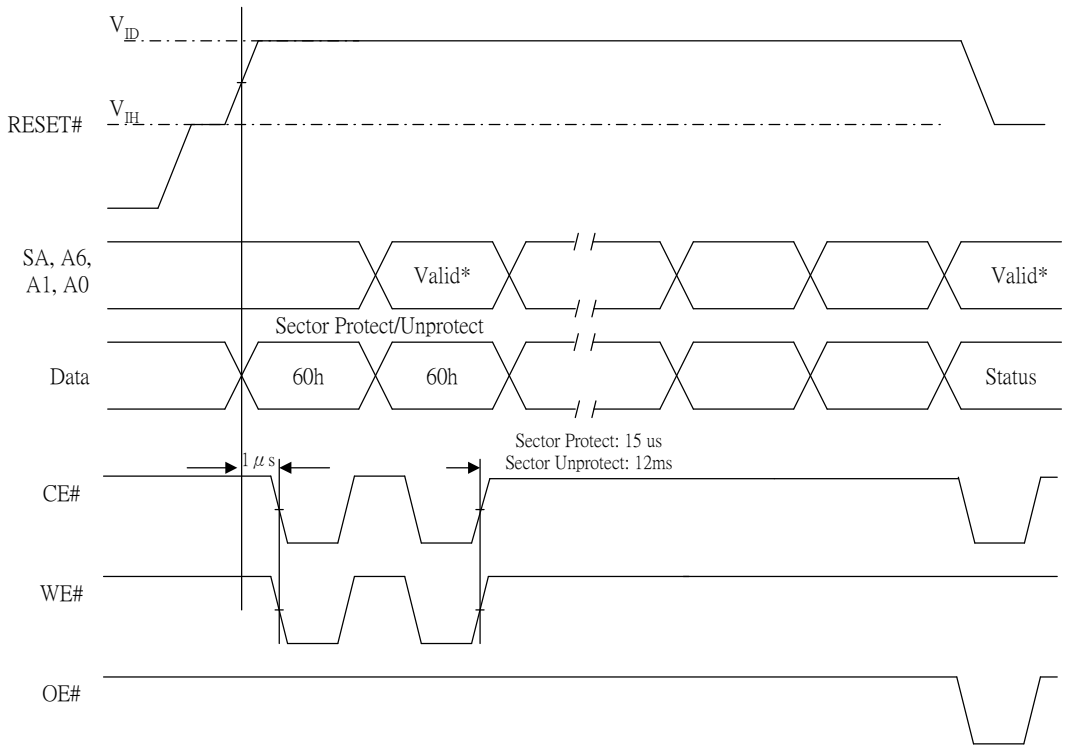


Figure 20. Temporary Sector Unprotect Timing Diagram

AC CHARACTERISTICS



* For sector protect, A6=0, A1=1, A0=0. For sector unprotect, A6=1, A1=1, A0=0.

Figure 21. Sector Protect/Unprotect Timing Diagram

AC CHARACTERISTICS

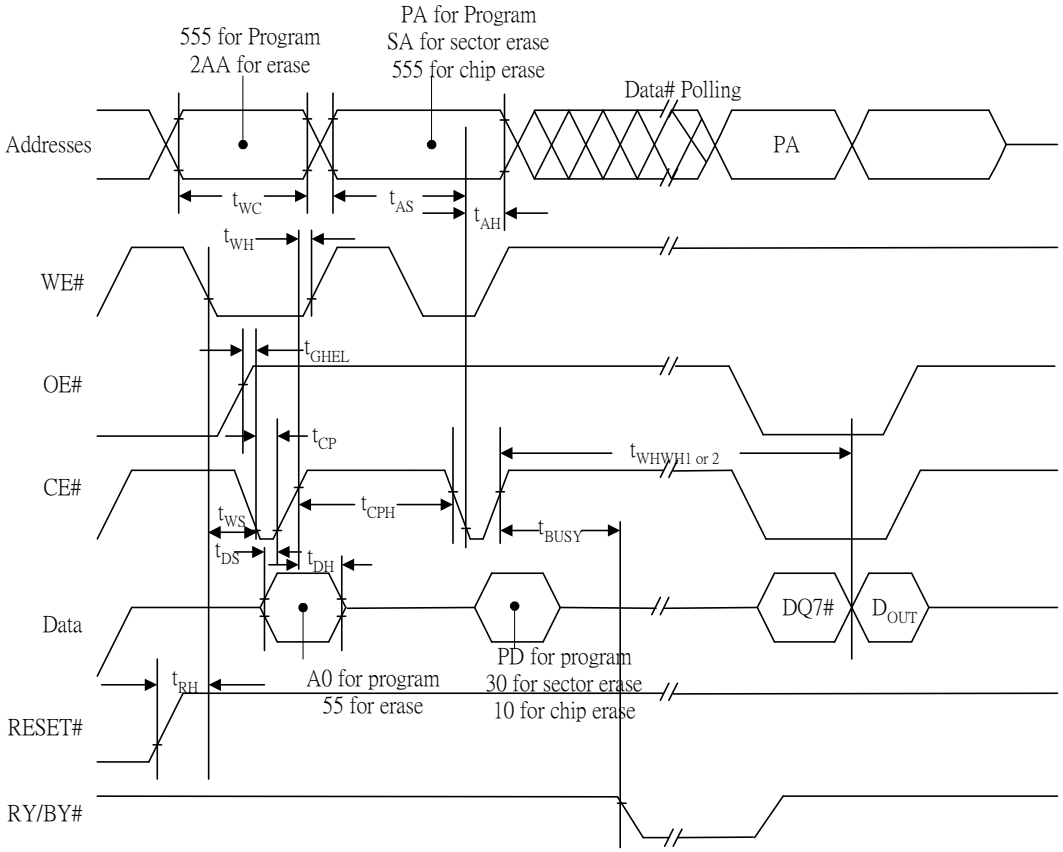
Alternate CE# Controlled Erase/Program Operations

Parameter		Description			Speed Options				Unit
JEDEC	Std				55	70	90	120	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	55	70	90	120	ns
t_{AVEL}	t_{AS}	Address Setup Time		Min	0				ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	45	45	45	50	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	35	35	45	50	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0				ns
	t_{OES}	Output Enable Setup Time		Min	0				ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0				ns
t_{WLEL}	t_{WS}	WE# Setup Time		Min	0				ns
t_{EHWH}	t_{WH}	WE# Hold Time		Min	0				ns
t_{ELEH}	t_{CP}	CE# Pulse Width		Min	35	35	35	50	ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High		Min	30				ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Byte	Typ	13				µs
			Word	Typ	16				
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	0.7				sec

Notes:

1. Not 100% tested.
2. See the “Erase and Programming Performance“ section for more information.

AC CHARACTERISTICS



Notes:

1. PA = program address, PD = program data, DQ7# = complement of the data written to the device, DOUT = data written to the device.
2. Figure indicates the last two bus cycles of the command sequence.
3. Word mode address used as an example.

Figure 22. Alternate CE# Controlled Write Operation Timings

Erase and Programming Performance

Parameter		Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time		0.7	15	s	Excludes 00h programming prior to erasure (Note 4)
Chip Erase Time		11		s	
Byte Programming Time		13	416	µs	Excludes system level Overhead (Note 5)
Word Programming Time		16	512	µs	
Chip Programming Time (Note 3)	Byte Mode	6.9	20.7	s	
	Word Mode	4.2	12.6	s	

Notes:

1. Typical program and erase times assume the following conditions: 25° C, 3.0 V V_{CC}. Additionally, typical programming assumes checkerboard pattern.
2. Under worst-case conditions of 90°C, V_{CC} = 2.7 V (3.0 V for regulated speed options).
3. The typical chip programming time is considerably less than the maximum chip programming time listed because most bytes programs are faster than the maximum program times listed.
4. In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.
5. System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 2 for further information on command definitions.

Latchup Characteristics

Description	Min	Max
Input voltage with respect to V_{SS} on all pins except I/O pins (Including A9, and RESET#)	-1.0V	12.5V
Input voltage with respect to V_{SS} on all I/O pins	-1.0V	V_{CC} + 1.0V
V_{CC} Current	-100mA	+100mA

Notes: Includes all pins except V_{CC} Test conditions: V_{CC} =3.0V, one pin at a time.

TSOP and SO Pin Capacitance

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN}=0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT}=0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN}=0	7.5	9	pF

Notes:

1. Sampled, not 100% tested.
2. Test conditions T_A = 25°C, f = 1.0MHz.