4-1/2 DIGIT ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **Low Roll-Over Error ..... ±1 Count Max**
- **Guaranteed Nonlinearity Error ..... ±1 Count Max**
- **Guaranteed Zero Reading for 0V Input**
- **True Polarity Indication at Zero for Null Detection**
- **Multiplexed BCD Data Output**
- **TTL-Compatible Outputs**
- **Differential Input**
- **Control Signals Permit Interface to UARTs and µProcessors**
- **Auto-Ranging Supported With Overrange and Underrange Signals**
- **Blinking Display Visually Indicates Overrange Condition**
- **Low Input Current ..... 1 pA**
- **Low Zero Reading Drift ..... 2 µV/°C**
- **Interfaces to TC7211A (LCD) and TC7212A (LED) Display Drivers**
- **Available in DIP and Surface-Mount Packages**

GENERAL DESCRIPTION

The TC7135 4-1/2 digit analog-to-digital converter (ADC) offers 50 ppm (1 part in 20,000) resolution with a maximum nonlinearity error of 1 count. An auto-zero cycle reduces zero error to below 10 µV and zero drift to 0.5 µV/°C. Source impedance errors are minimized by a 10 pA maximum input current. Roll-over error is limited to ±1 count.

By combining the TC7135 with a TC7211A (LCD) or TC7212A (LED) driver, a 4-1/2 digit display DVM or DPM can be constructed. Overrange and underrange signals support automatic range switching and special display blanking/flashing applications.

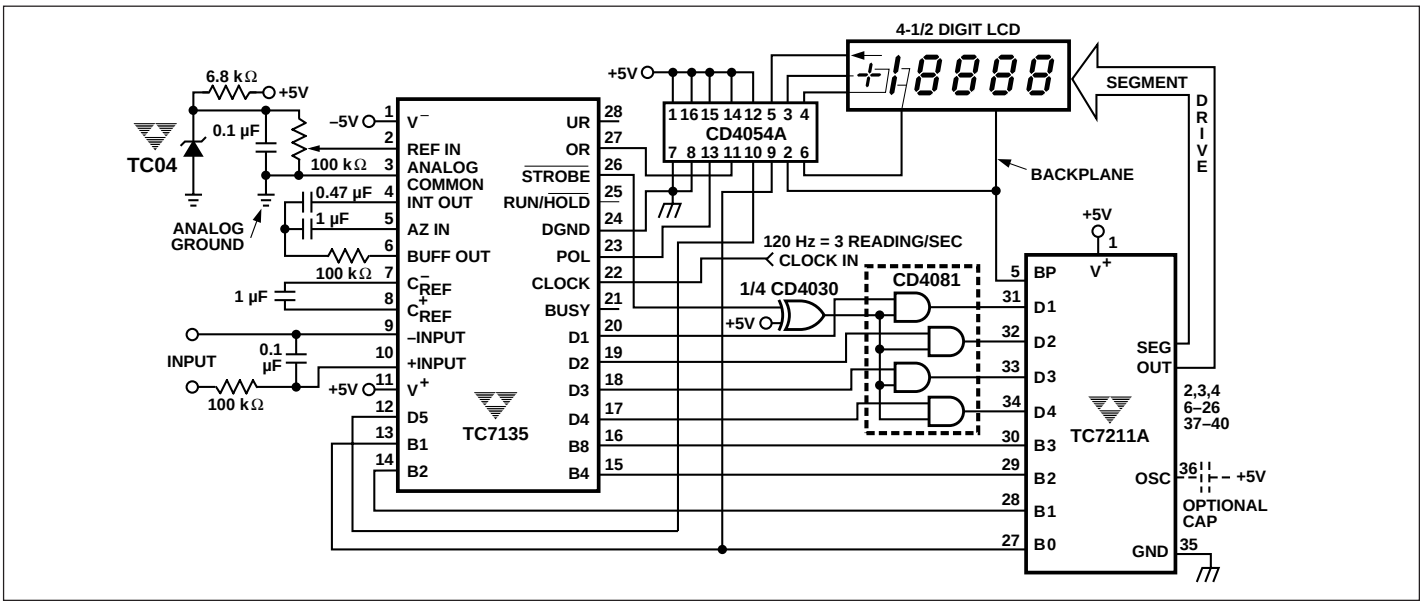
Microprocessor-based measurement systems are supported by BUSY, $\overline{\text{STROBE}}$, and RUN/$\overline{\text{HOLD}}$ control signals. Remote data acquisition systems with data transfer via UARTs are also possible. The additional control pins and multiplexed BCD outputs make the TC7135 the ideal converter for display or microprocessor-based measurement systems.

3

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC7135CBU	64-Pin Plastic Flat Package	0°C to +70°C
TC7135CLI	28-Pin PLCC	0°C to +70°C
TC7135CPI	28-Pin Plastic DIP	0°C to +70°C

TYPICAL 4-1/2 DIGIT DVM WITH LCD



TC7135

ABSOLUTE MAXIMUM RATINGS* (Note 1)

Positive Supply Voltage ..... +6V
Negative Supply Voltage ..... –9V
Analog Input Voltage (Pin 9 or 10) ..... V^+ to V^- (Note 2)
Reference Input Voltage (Pin 2) ..... V^+ to V^-
Clock Input Voltage ..... 0V to V^+
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... –65°C to +160°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Power Dissipation ($T_A \leq 70°C$)
Plastic DIP 1.14W
PLCC 1.00W
Plastic Flat Package 1.14W

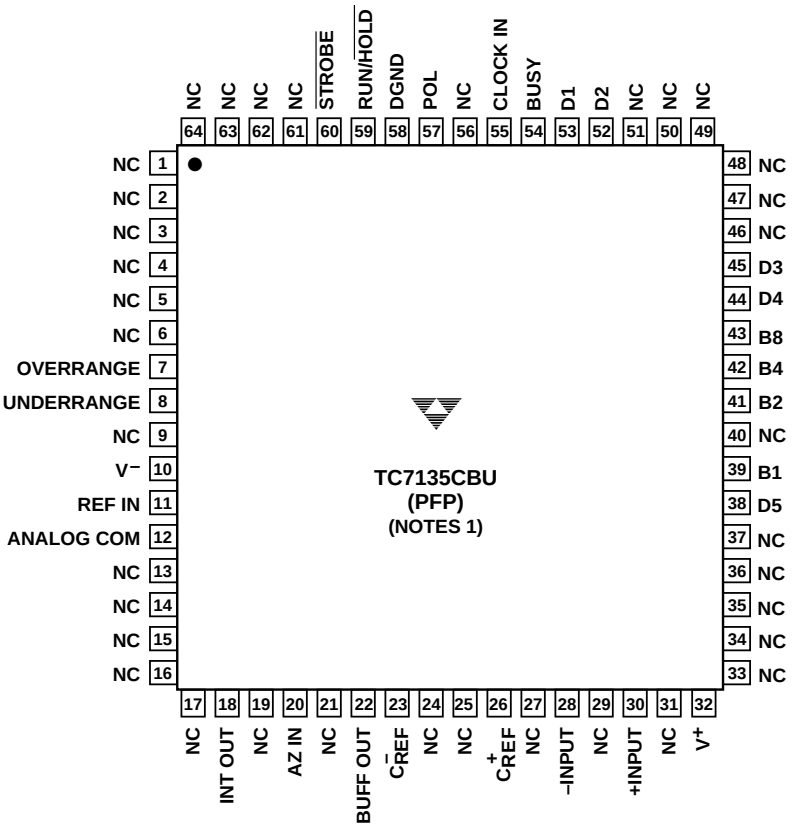
*Static-sensitive device. Unused devices must be stored in conductive material to protect them from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied.

ELECTRICAL CHARACTERISTICS: T_A = +25°C, f_{CLOCK} = 120 kHz, V^+ = +5V, V^- = –5V (Figure 1)

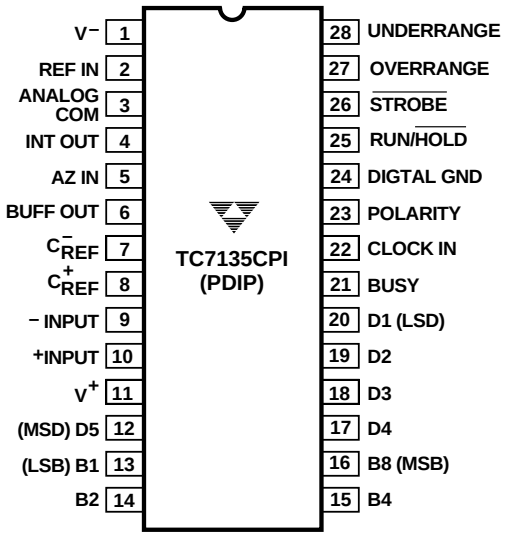
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Analog						
	Display Reading With Zero Volt Input	Notes 2 and 3	–0.0000	±0.0000	+0.0000	Display Reading
TC_Z	Zero Reading Temperature Coefficient	V_{IN} = 0V Note 4	—	0.5	2	µV/°C
TC_{FS}	Full-Scale Temperature Coefficient	V_{IN} = 2V Notes 4 and 5	—	—	5	ppm/°C
NL	Nonlinearity Error	Note 6	—	0.5	1	Count
DNL	Differential Linearity Error	Note 6	—	0.01	—	LSB
	Display Reading in Ratiometric Operation	$V_{IN} = V_{REF}$ Note 2	+0.9996	+0.9999	+1.0000	Display Reading
±FSE	± Full-Scale Symmetry Error (Roll-Over Error)	$–V_{IN} = +V_{IN}$ Note 7	—	0.5	1	Count
I_{IN}	Input Leakage Current	Note 3	—	1	10	pA
V_N	Noise	Peak-to-Peak Value Not Exceeded 95% of Time	—	15	—	μV_{P-P}
Digital						
I_{IL}	Input Low Current	V_{IN} = 0V	—	10	100	µA
I_{IH}	Input High Current	V_{IN} = +5V	—	0.08	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA	—	0.2	0.4	V
V_{OH}	Output High Voltage B_1, B_2, B_4, B_8, D_1–D_5 Busy, Polarity, Overrange, Underrange, Strobe	 I_{OH} = 1 mA I_{OH} = 10 µA	 2.4 4.9	 4.4 4.99	 5 5	 V V
f_{CLK}	Clock Frequency	Note 8	0	120	1200	kHz
Power Supply						
V^+	Positive Supply Voltage		4	5	6	V
V^-	Negative Supply Voltage		–3	–5	–8	V
I^+	Positive Supply Current	f_{CLK} = 0 Hz	—	1	3	mA
I^-	Negative Supply Current	f_{CLK} = 0 Hz	—	0.7	3	mA
PD	Power Dissipation	f_{CLK} = 0 Hz	—	8.5	30	mW

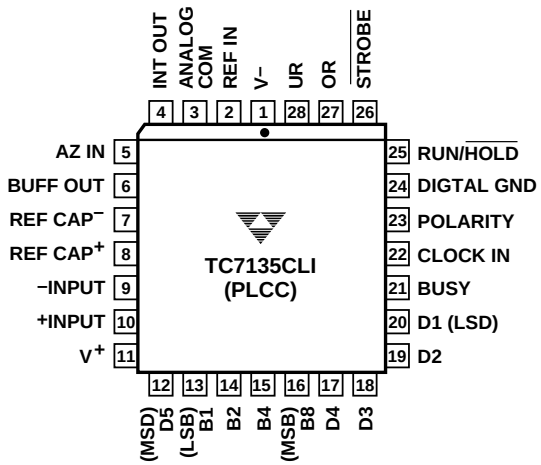
NOTES:
1. Limit input current to under 100µA if input voltages exceed supply voltage.
2. Full-scale voltage = 2V.
3. V_{IN} = 0V.
4. $0°C \leq T_A \leq +70°C$.
5. External reference temperature coefficient less than 0.01 ppm/°C.
6. $–2V \leq V_{IN} \leq +2V$. Error of reading from best fit straight line.
7. $|V_{IN}| = 1.9959$.
8. Specification related to clock frequency range over which the TC7135 correctly performs its various functions. Increased errors result at higher operating frequencies.

PIN CONFIGURATIONS



NOTES: 1. NC = No internal connection.





TC7135

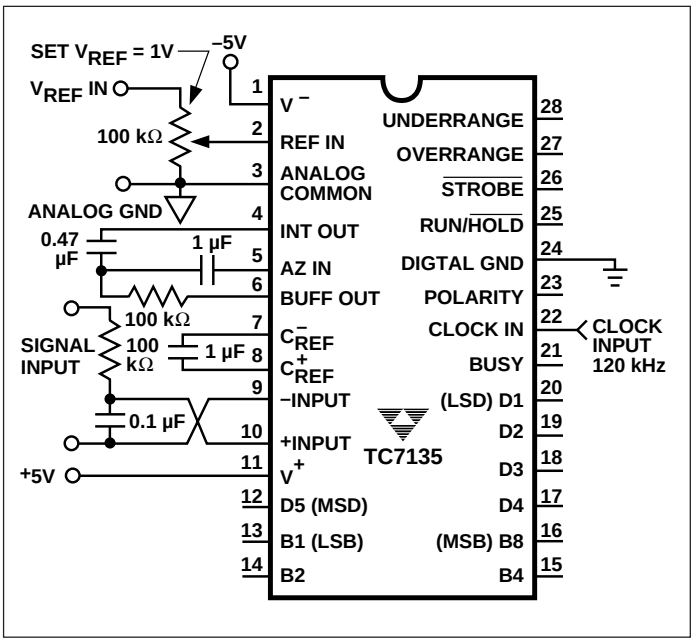


Figure 1. Test Circuit

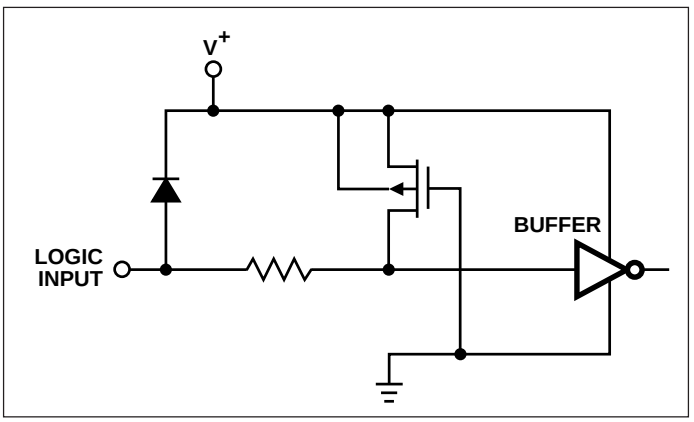


Figure 2. Digital Logic Input

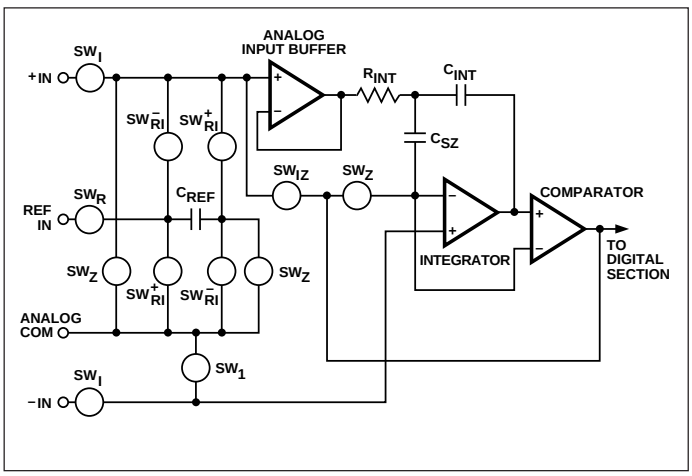


Figure 3A. Internal Analog Switches

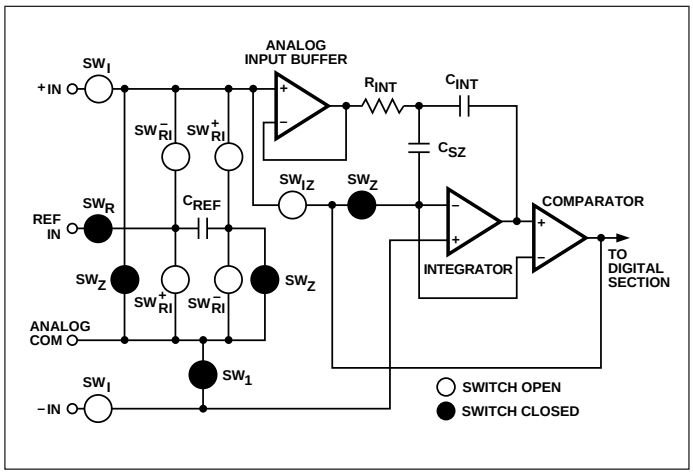


Figure 3B. System Zero Phase

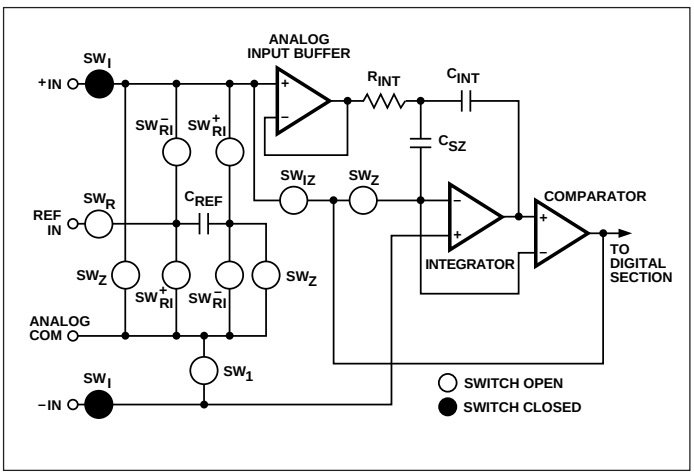


Figure 3C. Input Signal Integration Phase

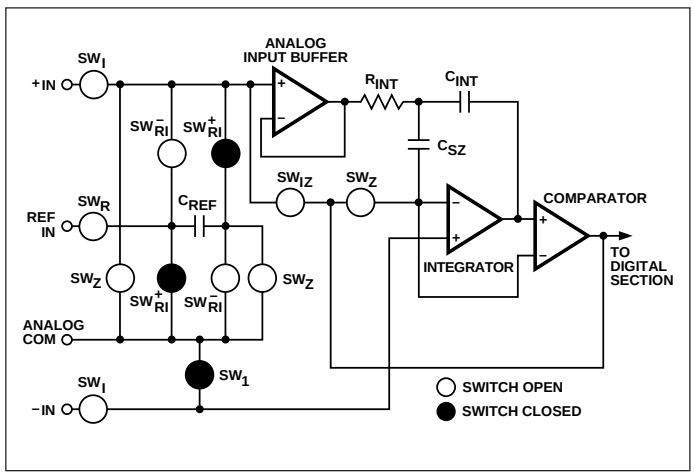


Figure 3D. Reference Voltage Integration Phase

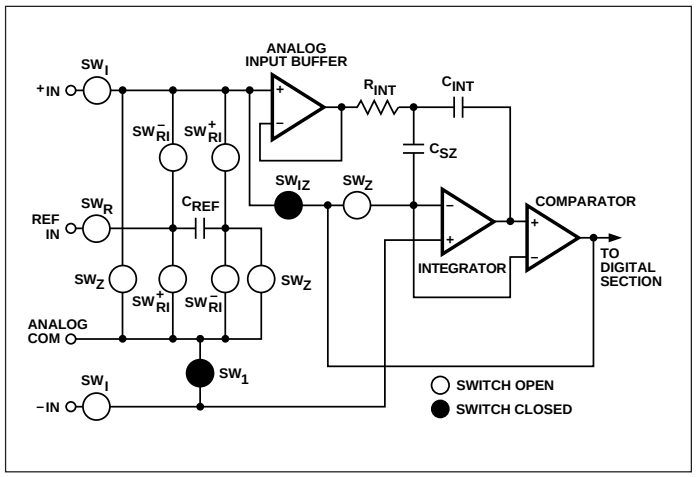


Figure 3E. Integrator Output Zero Phase

GENERAL THEORY OF OPERATION

(All Pin Designations Refer to 28-Pin DIP)

Dual-Slope Conversion Principles

The TC7135 is a dual-slope, integrating analog-to-digital converter. An understanding of the dual-slope conversion technique will aid in following detailed TC7135 operational theory.

The conventional dual-slope converter measurement cycle has two distinct phases:

(1) Input signal integration

(2) Reference voltage integration (deintegration)

The input signal being converted is integrated for a fixed time period, measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal.

In a simple dual-slope converter, a complete conversion requires the integrator output to "ramp-up" and "ramp-down."

A simple mathematical equation relates the input signal, reference voltage, and integration time:

$$\frac{1}{RC}\int_0^{t_{SI}} V_{IN}(t)\,dt = \frac{V_R\,t_{RI}}{RC},$$

where:

V_R = Reference voltage

t_{SI} = Signal integration time (fixed)

t_{RI} = Reference voltage integration time (variable).

For a constant V_{IN}:

$$V_{IN} = V_R\left[\frac{t_{RI}}{t_{SI}}\right]$$

The dual-slope converter accuracy is unrelated to the integrating resistor and capacitor values, as long as they are stable during a measurement cycle. Noise immunity is an inherent benefit. Noise spikes are integrated, or averaged, to zero during integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high-noise environments. (See Figure 4.)

TC7135 Operational Theory

The TC7135 incorporates a system zero phase and integrator output voltage zero phase to the normal two-phase dual-slope measurement cycle. Reduced system errors, fewer calibration steps, and a shorter overrange recovery time result.

The TC7135 measurement cycle contains four phases:

(1) System zero

(2) Analog input signal integration

(3) Reference voltage integration

(4) Integrator output zero

Internal analog gate status for each phase is shown in Table 1.

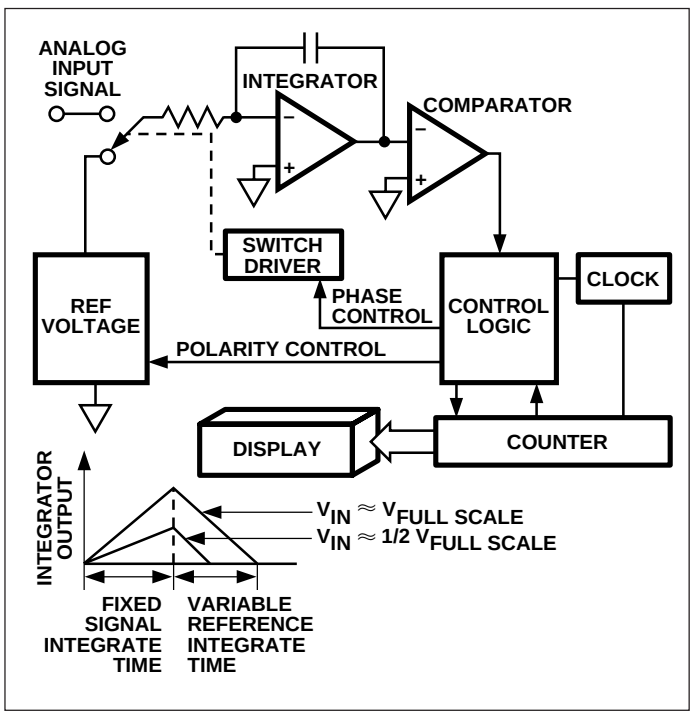


Figure 4. Basic Dual-Slope Converter

Table 1. Internal Analog Gate Status

Conversion Cycle Phase	Internal Analog Gate Status							Reference Schematic
	SW_I	SW_R^+	SW_R^-	SW_Z	SW_R	SW_1	SW_{IZ}	
System Zero				Closed	Closed	Closed		3B
Input Signal Integration	Closed							3C
Reference Voltage Integration		Closed*				Closed		3D
Integrator Output Zero						Closed	Closed	3E

***NOTE:** Assumes a positive polarity input signal. SW_R^- would be closed for a negative input signal.

System Zero Phase

During this phase, errors due to buffer, integrator, and comparator offset voltages are compensated for by charging C_{AZ} (auto-zero capacitor) with a compensating error voltage. With zero input voltage, the integrator output remains at zero.

The external input signal is disconnected from the internal circuitry by opening the two SW_I switches. The internal input points connect to analog common. The reference capacitor charges to the reference voltage potential through SW_R. A feedback loop, closed around the integrator and comparator, charges the C_{AZ} with a voltage to compensate for buffer amplifier, integrator, and comparator offset voltages. (See Figure 3B.)

Analog Input Signal Integration Phase

The TC7135 integrates the differential voltage between the +INPUT and –INPUT. The differential voltage must be within the device's common-mode range; –1V from either supply rail, typically.

The input signal polarity is determined at the end of this phase. (See Figure 3C.)

Reference Voltage Integration Phase

The previously-charged reference capacitor is connected with the proper polarity to ramp the integrator output back to zero. (See Figure 3D.) The digital reading displayed is:

$$\text{Reading} = 10{,}000 \left[\frac{\text{Differential Input}}{V_{REF}}\right].$$

Integrator Output Zero Phase

This phase guarantees the integrator output is at 0V when the system zero phase is entered and that the true system offset voltages are compensated for. This phase normally lasts 100 to 200 clock cycles. If an overrange condition exists, the phase is extended to 6200 clock cycles. (See Figure 3E.)

Analog Section Functional Description

Differential Inputs

The TC7135 operates with differential voltages (+INPUT, pin 10 and –INPUT, pin 9) within the input amplifier common-mode range which extends from 1V below the positive supply to 1V above the negative supply. Within this common-mode voltage range, an 86 dB common-mode rejection ratio is typical.

The integrator output also follows the common-mode voltage and must not be allowed to saturate. A worst-case condition exists, for example, when a large positive common-mode voltage with a near full-scale negative differential input voltage is applied. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. For these critical applications, the integrator swing can be reduced to less than the recommended 4V full-scale swing, with some loss of accuracy. The integrator output can swing within 0.3V of either supply without loss of linearity.

Analog Common

ANALOG COMMON (pin 3) is used as the –INPUT return during the auto-zero and deintegrate phases. If – INPUT is different from analog common, a common-mode voltage exists in the system. This signal is rejected by the excellent CMRR of the converter. In most applications, – INPUT will be set at a fixed known voltage (power supply common, for instance). In this application, analog common should be tied to the same point, thus removing the common-mode voltage from the converter. The reference voltage is referenced to analog common.

Reference Voltage

The reference voltage input (REF IN, pin 2) must be a positive voltage with respect to analog common. Two reference voltage circuits are shown in Figure 5.

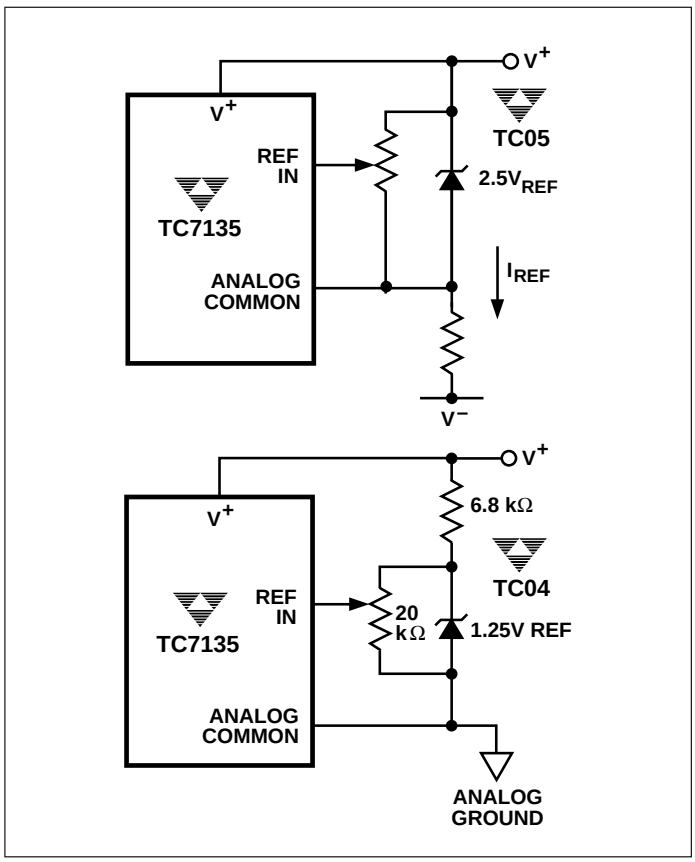


Figure 5. Using an External Reference Voltage

Digital Section Functional Description

The major digital subsystems within the TC7135 are illustrated in Figure 6, with timing relationships shown in Figure 7. The multiplexed BCD output data can be displayed on an LCD with the TC7211A.

The digital section is best described through a discussion of the control signals and data outputs.

RUN/$\overline{\text{HOLD}}$ Input

When left open, the RUN/$\overline{\text{HOLD}}$ (R/$\overline{\text{H}}$) input (pin 25) assumes a logic "1" level. With $\overline{\text{R}}$/H = 1, the TC7135 performs conversions continuously, with a new measurement cycle beginning every 40,002 clock pulses.

When $\overline{\text{R}}$/H changes to logic "0," the measurement cycle in progress will be completed, and data held and displayed, as long as the logic "0" condition exists.

A positive pulse (>300nsec) at $\overline{\text{R}}$/H initiates a new measurement cycle. The measurement cycle in progress when $\overline{\text{R}}$/H initially assumed logic "0" must be completed before the positive pulse can be recognized as a single conversion run command.

The new measurement cycle begins with a 10,001-count auto-zero phase. At the end of this phase, the busy signal goes high.

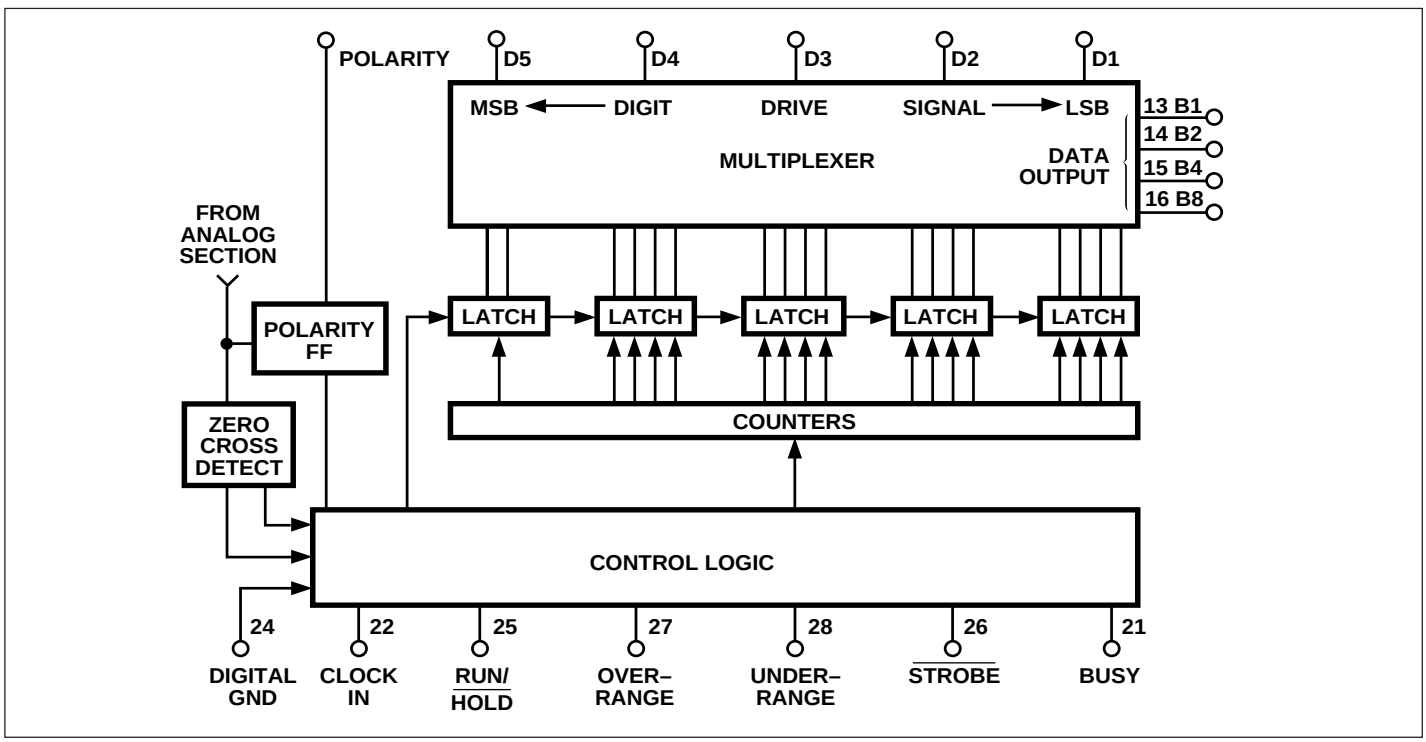


Figure 6. Digital Section Functional Diagram

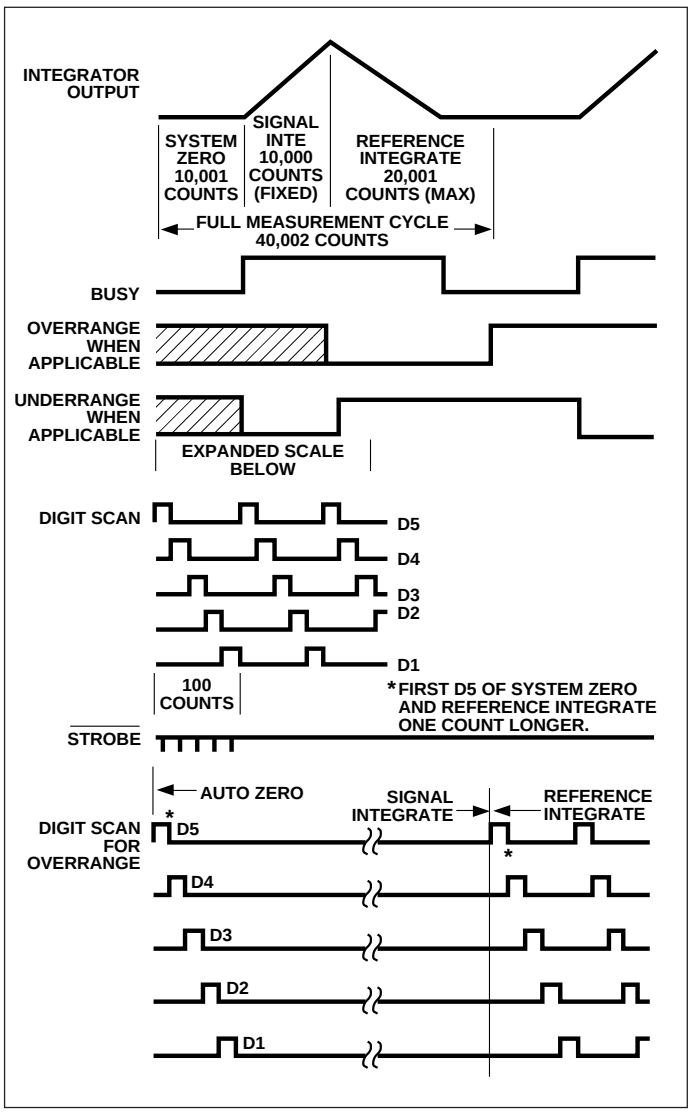


Figure 7. Timing Diagrams for Outputs

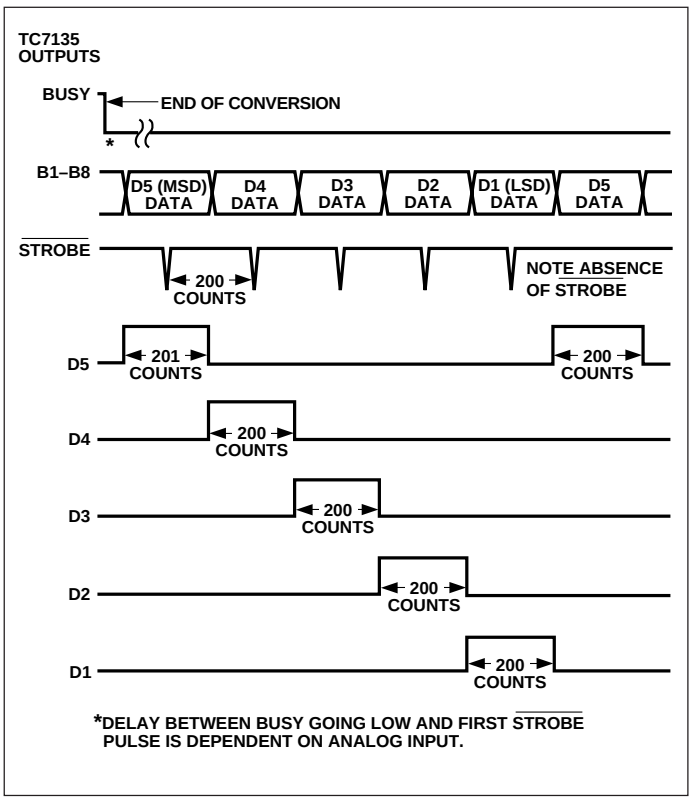


Figure 8. Strobe Signal Pulses Low Five Times per Conversion

STROBE Output

During the measurement cycle, the $\overline{\text{STROBE}}$ output (pin 26) control line is pulsed low five times. The five low pulses occur in the center of the digit drive signals (D_1, D_2, D_3, D_4 and D_5; see Figure 8).

D_5 goes high for 201 counts when the measurement cycles end. In the center of D_5 pulse, 101 clock pulses after the end of the measurement cycle, the first $\overline{\text{STROBE}}$ occurs for one-half clock pulse. After D_5 strobe, D_4 goes high for 200 clock pulses. $\overline{\text{STROBE}}$ goes low 100 clock pulses after D_4 goes high. This continues through the D_1 drive pulse.

The digit drive signals will continue to permit display scanning. $\overline{\text{STROBE}}$ pulses are not repeated until a new measurement is completed. The digit drive signals will not continue if the previous signal resulted in an overrange condition.

The active-low $\overline{\text{STROBE}}$ pulses aid BCD data transfer to UARTs, microprocessors, and external latches. (See Application Note AN-16.)

BUSY Output

At the beginning of the signal-integration phase, BUSY (pin 21) goes high and remains high until the first clock pulse after the integrator zero crossing. BUSY returns to logic "0" after the measurement cycle ends in an overrange condition. The internal display latches are loaded during the first clock pulse after BUSY and are latched at the clock pulse end. The BUSY signal does not go high at the beginning of the measurement cycle, which starts with the auto-zero phase.

OVERRANGE Output

If the input signal causes the reference voltage integration time to exceed 20,000 clock pulses, the OVERRANGE output (pin 27) is set to logic "1." The OVERRANGE output register is set when BUSY goes low and reset at the beginning of the next reference-integration phase.

UNDERRANGE Output

If the output count is 9% of full scale or less (≤1800 counts), the UNDERRANGE output (pin 28) register bit is set at the end of BUSY. The bit is set low at the next signal-integration phase.

POLARITY Output

A positive input is registered by a logic "1" polarity signal. The POLARITY output (pin 23) is valid at the beginning of reference integrate and remains valid until determined during the next conversion.

The POLARITY bit is valid even for a zero reading. Signals less than the converter's LSB will have the signal polarity determined correctly. This is useful in null applications.

Digit Drive Outputs

Digit drive outputs are positive-going signals. Their scan sequence is D_5, D_4, D_3, D_2 and D_1 (pins 12, 17, 18, 19 and 20, respectively). All positive signals are 200 clock pulses wide, except D_5, which is 201 clock pulses.

All five digits are continuously scanned, unless an overrange condition occurs. In an overrange condition, all digit drives are held low from the final $\overline{\text{STROBE}}$ pulse until the beginning of the next reference-integrate phase. The scanning sequence is then repeated, providing a blinking visual display.

BCD Data Outputs

The binary coded decimal (BCD) outputs, B_8, B_4, B_2 and B_1 (pins 16, 15, 14 and 13, respectively) are positive true-logic signals. They become active simultaneously with digit drive signals. In an overrange condition, all data bits are logic "0".

APPLICATIONS INFORMATION

Component Value Selection

Integrating Resistor

The integrating resistor (R_{INT}) is determined by the full-scale input voltage and output current of the buffer used to charge the integrator capacitor (C_{INT}). Both the buffer amplifier and the integrator have a Class A output stage, with 100 µA of quiescent current. A 20 µA drive current gives negligible linearity errors. Values of 5 µA to 40 µA give good results. The exact value of R_{INT} for a 20 µA current is easily calculated:

$$R_{INT} = \frac{\text{Full-scale voltage}}{20\ \mu A}.$$

Integrating Capacitor

The product of R_{INT} and C_{INT} should be selected to give the maximum voltage swing to ensure tolerance build-up will not saturate integrator swing (approximately 0.3V from either supply). For ±5V supplies, and analog common tied to supply ground, a ±3.5V to ±4V full-scale integrator swing is adequate. A 0.10 µF to 0.47 µF is recommended. In general, the value of C_{INT} is given by:

$$C_{INT} = \frac{[10{,}000 \times \text{clock period}] \times I_{INT}}{\text{Integrator output voltage swing}}$$

$$= \frac{(10{,}000)\ (\text{clock period})\ (20\ \mu A)}{\text{Integrator output voltage swing}}.$$

A very important characteristic of the C_{INT} is that it has low dielectric absorption to prevent roll-over or ratiometric errors. A good test for dielectric absorption is to use the capacitor with the input tied to the reference. This ratiometric condition should read half-scale 0.9999. Any deviation is probably due to dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polystyrene and polycarbonate capacitors may also be used in less critical applications.

Auto-Zero and Reference Capacitors

The size of the auto-zero capacitor (C_{AZ}) has some influence on system noise. A large capacitor reduces noise. The reference capacitor (C_{REF}) should be large enough such that stray capacitance from its nodes to ground is negligible.

The dielectric absorption of C_{REF} and C_{AZ} is only important at power-on, or when the circuit is recovering from an overload. Smaller or cheaper capacitors can be used if accurate readings are not required during the first few seconds of recovery.

Reference Voltage

The analog input required to generate a full-scale output is $V_{IN} = 2\ V_{REF}$.

The stability of the reference voltage is a major factor in overall absolute accuracy of the converter. Therefore, it is recommended that high-quality references be used where high-accuracy, absolute measurements are being made. Suitable references are:

Part Type	Manufacturer
TC04	TelCom Semiconductor
TC05	TelCom Semiconductor

Conversion Timing

Line Frequency Rejection

A signal-integration period at a multiple of the 60 Hz line frequency will maximize 60 Hz "line noise" rejection.

A 100 kHz clock frequency will reject 50 Hz, 60 Hz and 400 Hz noise, corresponding to 2.5 readings per second.

Table 2. Line Frequency Rejection

Oscillator Frequency (kHz)	Frequency Rejected (Hz)
300, 200, 150, 120, 100, 40, 33-1/3	60
250, 166-2/3, 125, 100	50
100	50, 60, 400

Table 3. Conversion Rate vs Clock Frequency

Conversion Rate (Conv/Sec)	Clock Frequency (kHz)
2.5	100
3.0	120
5.0	200
7.5	300
10.0	400
20.0	800
30.0	1200

Displays and Driver Circuits

TelCom Semiconductor manufactures three display decoder/driver circuits to interface the TC7135 to LCDs or LED displays. Each driver has 28 outputs for driving four 7-segment digit displays.

Device	Package	Description
TC7211AIPL	40-Pin Epoxy	4-Digit LCD Driver/Encoder

Several sources exist for LCDs and LED displays.

Manufacturer	Address	Display Type
Hewlett Packard Components	640 Page Mill Road Palo Alto, CA 94304	LED
AND	720 Palomar Ave. Sunnyvale, CA 94086	LCD and LED
Epson America, Inc.	3415 Kanhi Kawa St. Torrance, CA 90505	LCD

High-Speed Operation

The maximum conversion rate of most dual-slope ADCs is limited by frequency response of the comparator. The comparator in this circuit follows the integrator ramp with a 3 μs delay, and at a clock frequency of 160 kHz (6 μs period), half of the first reference integrate clock period is lost in delay. This means the meter reading will change from 0 to 1 with a 50 μV input, 1 to 2 with 150 μV, 2 to 3 with 250 μV, etc. This transition at midpoint is considered desirable by most users; however, if clock frequency is increased appreciably above 160 kHz, the instrument will flash "1" on noise peaks even when the input is shorted.

For many dedicated applications, where the input signal is always of one polarity, comparator delay need not be a limitation. Since nonlinearity and noise do not increase substantially with frequency, clock rates up to ~1 MHz may be used. For a fixed clock frequency, the extra count (or counts) caused by comparator delay will be constant and can be digitally subtracted.

The clock frequency may be extended above 160 kHz without this error, however, by using a low value resistor in series with the integrating capacitor. The effect of the resistor is to introduce a small pedestal voltage onto the integrator output at the beginning of reference-integrate phase. By careful selection of the ratio between this resistor and the integrating resistor (a few tens of ohms in the recommended circuit), the comparator delay can be compensated for and maximum clock frequency extended by approximately a factor of 3. At higher frequencies, ringing and second-order breaks will cause significant nonlinearities during the first few counts of the instrument.

The minimum clock frequency is established by leakage on the auto-zero and reference capacitors. With most devices, measurement cycles as long as 10 seconds give no measurable leakage error.

The clock used should be free from significant phase or frequency jitter. Several suitable low-cost oscillators are shown in the applications section. The multiplexed output means if the display takes significant current from the logic supply, the clock should have good PSRR.

Zero-Crossing Flip-Flop

The flip-flop interrogates data once every clock pulse after transients of the previous clock pulse and half-clock pulse have died down. False zero-crossings caused by clock pulses are not recognized. Of course, the flip-flop delays the true zero-crossing by up to one count in every instance, and if a correction were not made, the display would always be one count too high. Therefore, the counter

is disabled for one clock pulse at the beginning of the reference integrate (deintegrate) phase. This one-count delay compensates for the delay of the zero-crossing flip-flop, and allows the correct number to be latched into the display. Similarly, a one-count delay at the beginning of auto-zero gives an overload display of 0000 instead of 0001. No delay occurs during signal integrate, so true ratiometric readings result.

Generating a Negative Supply

A negative voltage can be generated from the positive supply by using a TC7660. (See Figure 9.)

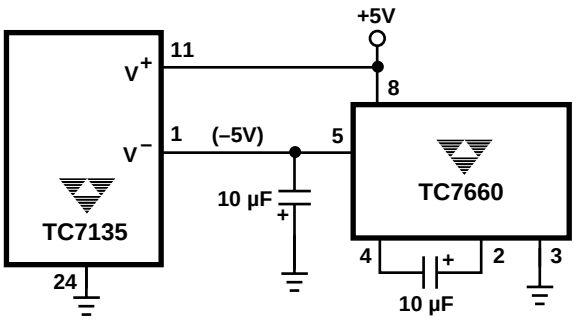
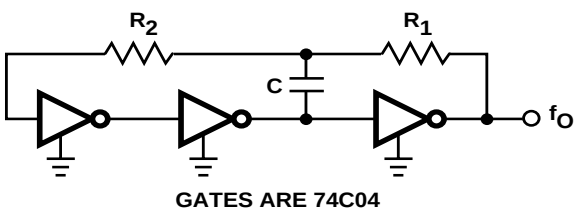


Figure 9. Negative Supply Voltage Generator

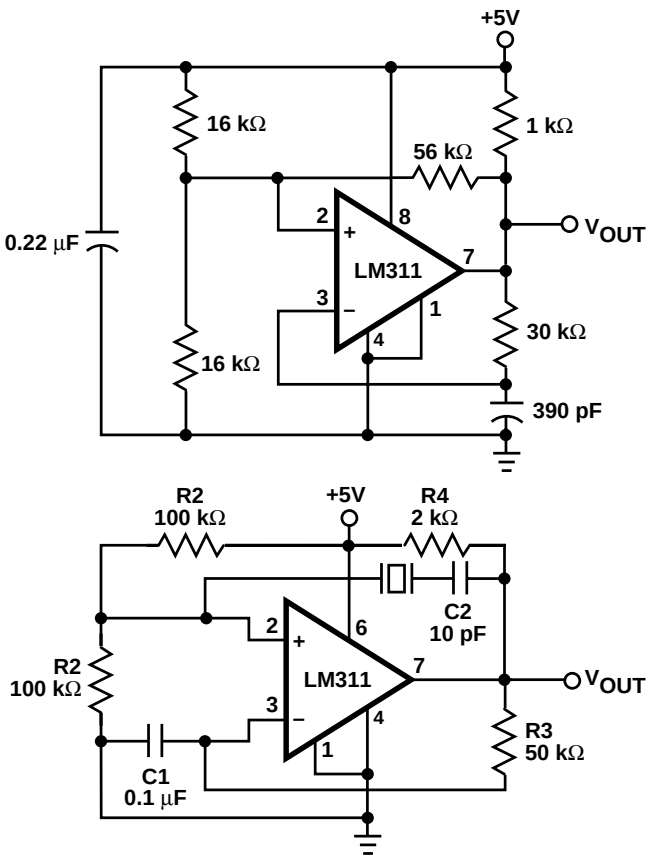
TYPICAL APPLICATIONS

RC Oscillator Circuit



1. $f_O \approx \frac{1}{2\,C[0.41\,R_P + 0.70\,R_1]}$, $R_P = \frac{R_1\,R_2}{R_1 + R_2}$
   a. If $R = R_1 = R_2$, $f \cong 0.55/RC$
   b. If $R_2 >> R_1$, $f \cong 0.45/R_1C$
   c. If $R_2 << R_1$, $f \cong 0.72/R_1C$
2. Examples:
   a. f = 120 kHz, C = 420 pF
      $R_1 = R_2 \approx 10.9\ k\Omega$
   b. f = 120 kHz, C = 420 pF, $R_2 = 50\ k\Omega$
      $R_1 = 8.93\ k\Omega$
   c. f = 120 kHz, C = 220 pF, $R_2 = 5\ k\Omega$
      $R_1 = 27.3\ k\Omega$

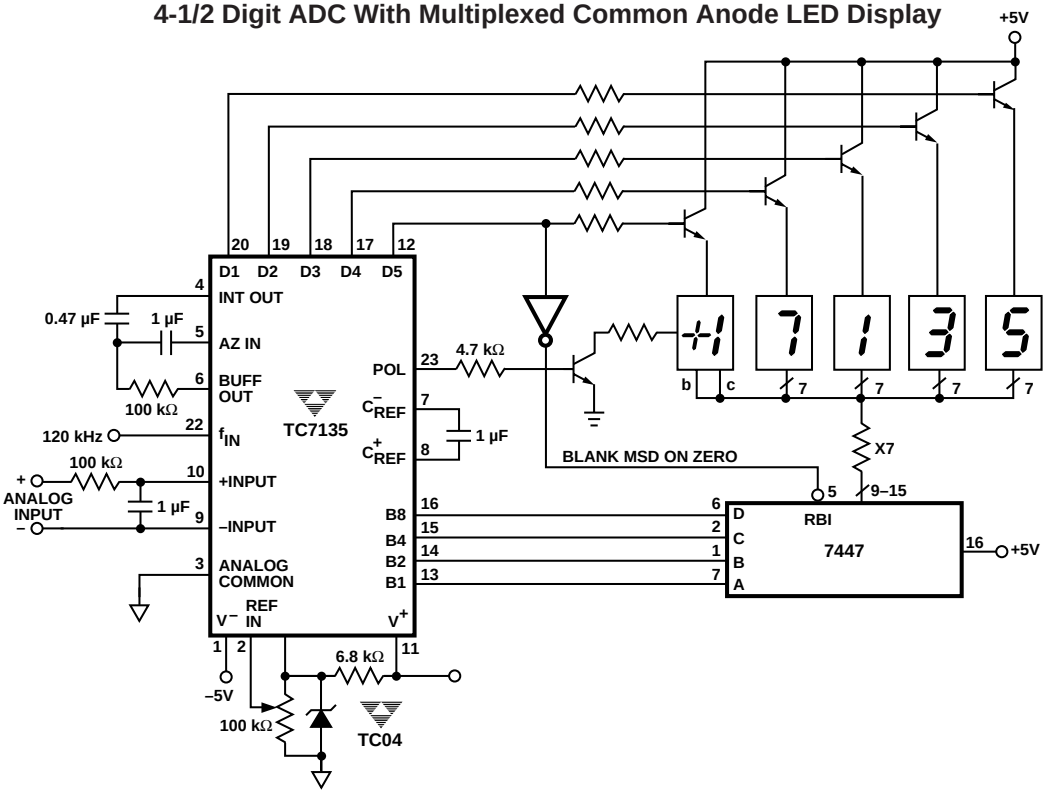
Comparator Clock Circuit



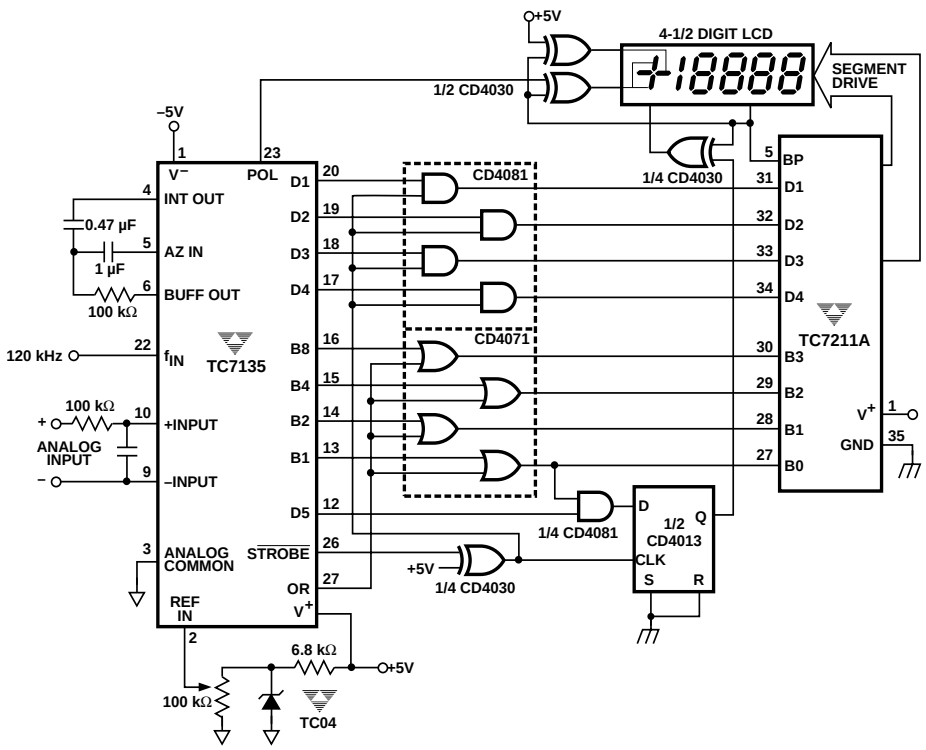
TC7135

TYPICAL APPLICATIONS (Cont.)

4-1/2 Digit ADC With Multiplexed Common Anode LED Display

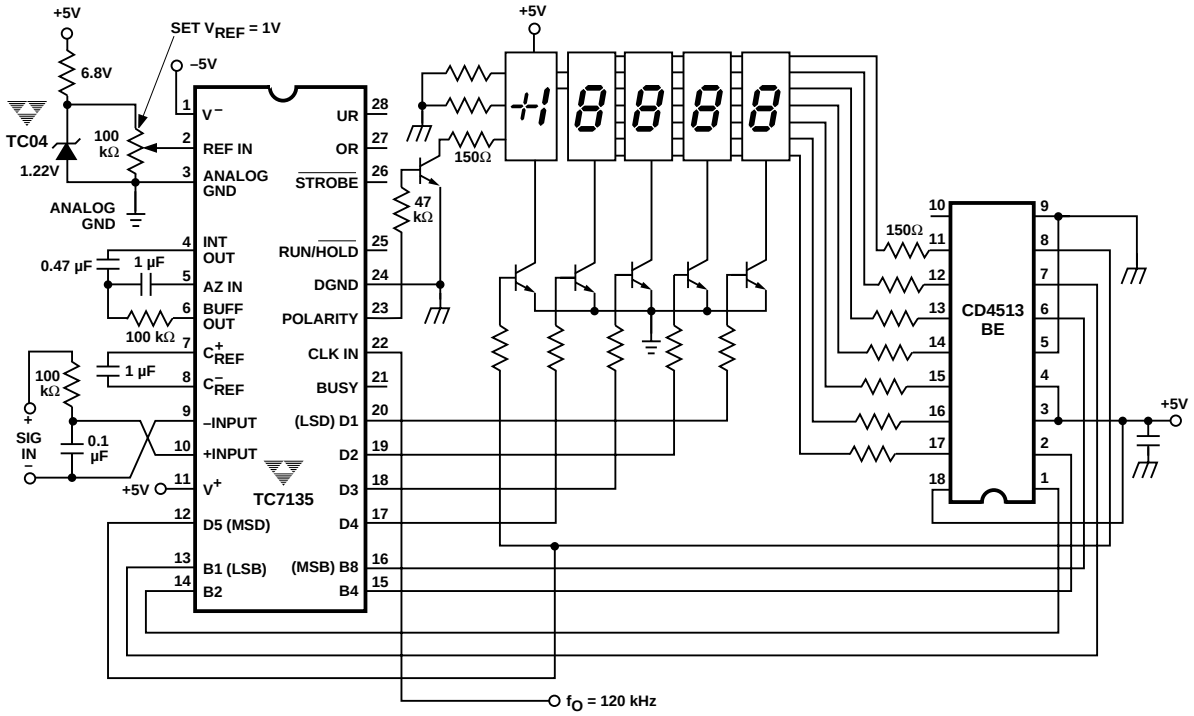
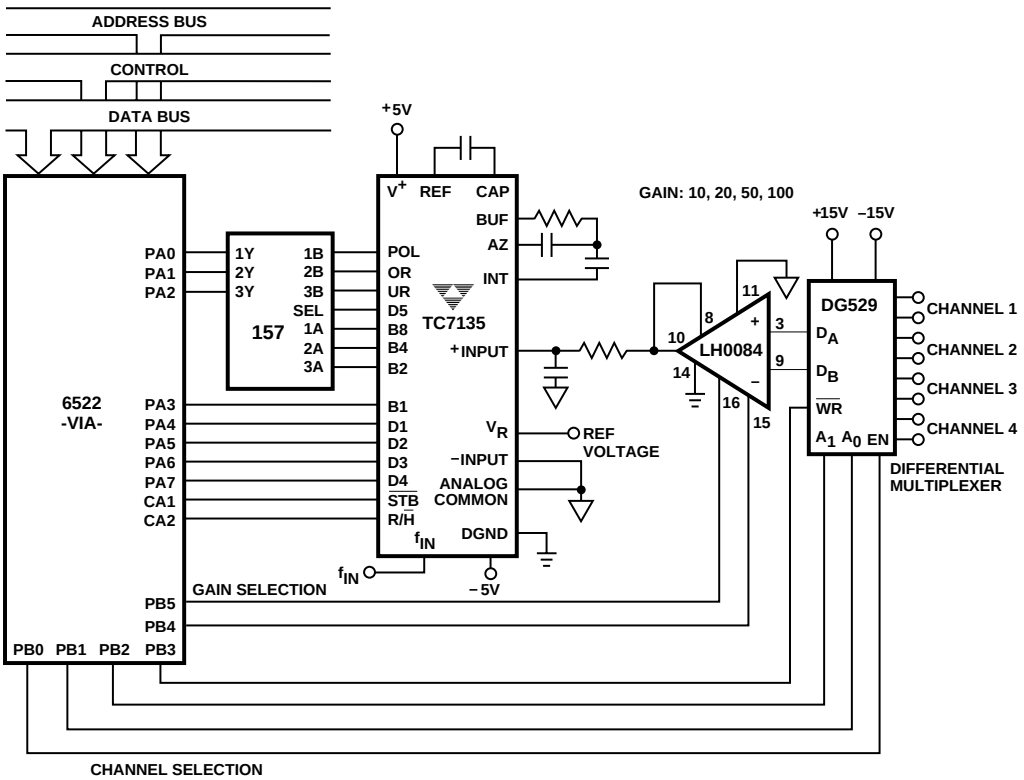


4-1/2 Digit ADC Interfaced to LCD With Digit Blanking on Overrange



TYPICAL APPLICATIONS (Cont.)

4-1/2 Digit ADC With Multiplexed Common Cathode LED Display



4-Channel Data Acquisition System