DSLAM

DSLAM APPS NOTE:

SIGNAL INTEGRITY AND TIMING SIMULATION FOR THE VORTEX CHIPSET

(S/UNI-DUPLEX, S/UNI-VORTEX, S/UNI-APEX AND S/UNI-ATLAS)

Released Issue 1

November 2000

REVISION HISTORY

Issue No.	Issue Date	Details of Change
1	November 2000	Document Creation

CONTENTS

LIST OF FIGURES

REFERENCES

1. Lee W. Ritchey, "High Speed PCB Design and System Design", Speeding Edge, July 1998
2. Montrose, Mark I., "Printed Circuit Board Design Techniques for EMC Compliance", IEEE Press, 1996.
3. PCI Industrial Computers manufacturers Group (PICMG) "CompactPCI Specification", PICMG 2.0 R2.1, September 2, 1997.
4. PMC-Sierra Inc., PMC-1990815, "DSLAM Reference Design: Core Card", Issue 3, September 2000

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1 INTRODUCTION

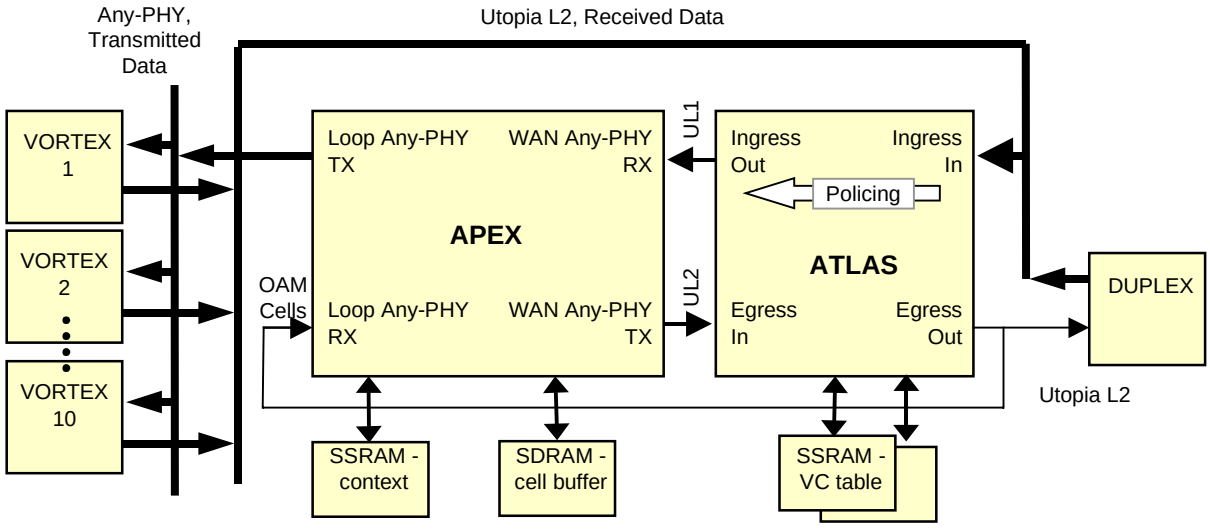
This simulation document for the Vortex Chipset describes:

- signal integrity and timing simulation for the PMC-Sierra VORTEX chipset. The VORTEX chipset consists of the S/UNI-APEX, S/UNI-VORTEX, S/UNI-DUPLEX, and S/UNI-ATLAS.
- the proposed bus configurations and simulation results that apply to the Utopia Level-2 and Any-PHY buses with clock at a 52 MHz and the S/UNI-APEX bus to the SSRAM and SDRAM with clock at 80 MHz.

The simulations are, in general, a paper-design only, without verification on the existing board.

FIGURE 1 shows the DSLAM Reference Design architecture block diagram (specific to this simulation document), which includes ten S/UNI-VORTEX devices, one S/UNI-DUPLEX device, one S/UNI-APEX device, and one S/UNI-ATLAS device.

FIGURE 1. DSLAM Core Card Architecture



1.1 Simulation Goals

This simulation project was instigated for these purposes:

- to address PMC-Sierra's customer needs for a pre-layout bus simulation
- to simulate multiple S/UNI-VORTEX/S/UNI-APEX/S/UNI-ATLAS bus
- to simulate 80 MHz RAM interface at S/UNI-APEX.

The following signal integrity and timing were simulated:

- bus signal integrity in the Received Data Utopia L2 direction
- bus signal integrity in the Transmit Data Any-PHY direction
- bus signal integrity on S/UNI-APEX-RAM interfaces
- clock signal integrity
- clock/data/address timing.

The following items were excluded from simulation: bus lines crosstalk, clock line crosstalk, electromagnetic interference (EMI), simultaneous switching noise, and power and ground noise. Time constraints, lack of simulation tools, and lack of noise models prevented the inclusion of those disturbances in this simulation project. Any source of interference may have significant magnitude. To help build a board with better signal integrity, we recommend:

- using a proper layout (with ground and power planes at minimum proximity working as low inductance capacitors)
- decoupling/coupling on power rails, integral copper planes without cutouts
- minimizing ground and power loops, avoiding long parallel runs of digital traces
- reducing back-reflections.

The signal integrity simulations and timing diagrams are presented later in this document.

1.2 Simulation Tools

For signal integrity simulation, two types of CAD tools were evaluated for this project:

- UNIX-based SpecctraQuest by Cadence
- PC-based (Win95/98/NT) LineSim by HyperLynx.

For bus timing, *TimingDesigner – Professional 32* by the Chronology Corporation was used.

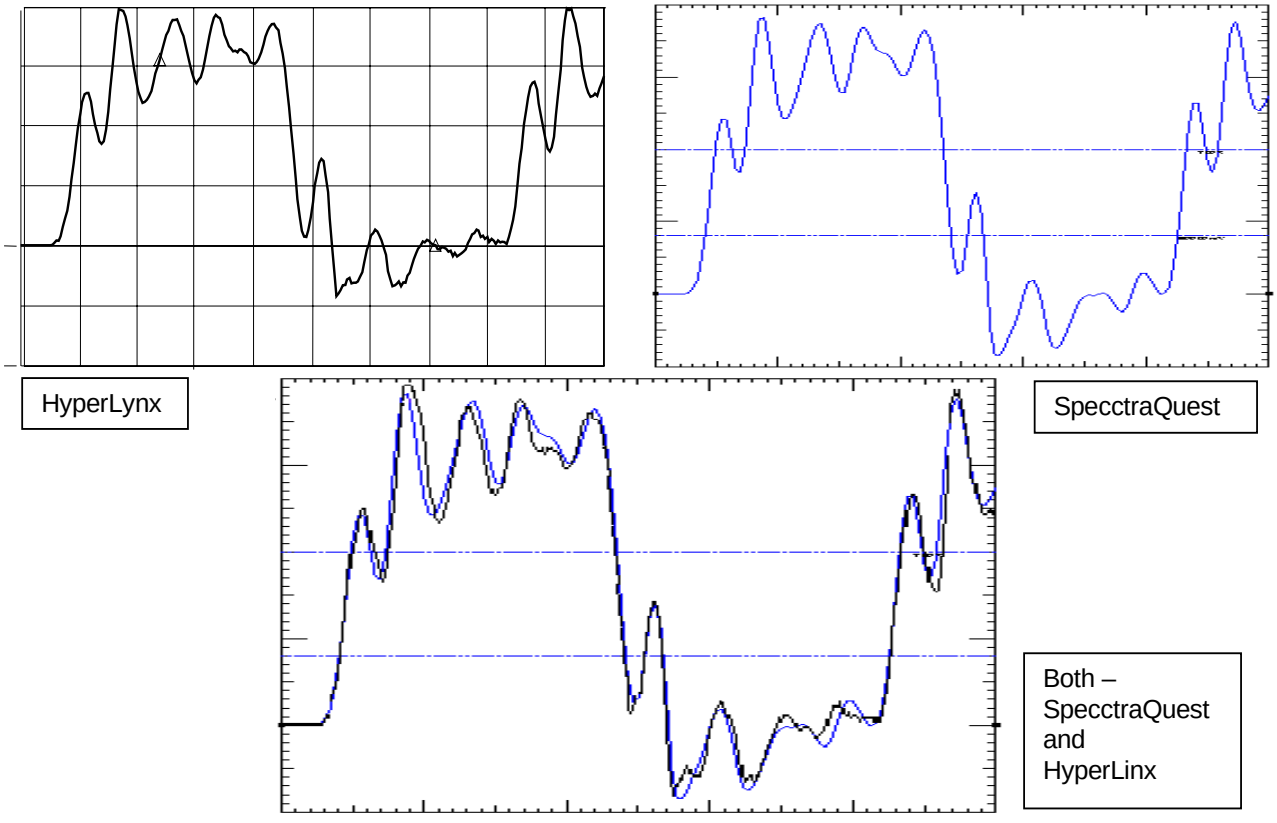
The first CAD simulation tool evaluated was the UNIX-based SpecctraQuest. The SpecctraQuest simulation began with a simplified board layout. That sets automatically trace impedance, calculated from board stack and additional parameter set manually. A limited number of components from the library was later imported. When the saved program was opened, the previous session components were moved and the connections (wiring) were overlapped, causing some confusion. The on-screen, displayed simulation results (graphs) can be

saved only as a PostScript file and could not be inserted directly into this document. The GSview (Ghostview) application software was used to convert PostScript into a bitmap file.

The second CAD simulation tool evaluated was the PC-based HyperLynx LineSim. The installation was typical for Windows-based applications. A server-based license allowed for key-less work. The learning curve was shorter than for SpecctraQuest. The pre-layout LineSim simulation tool opened with a fixed matrix of non-active connections and input/output devices. Clicking the element activated it. Typing in data set the parameters, and later copying-and-pasting sped up the procedure. The fixed matrix of components limited the flexibility of the simulation tool. When exiting, this version of the HyperLynx tool did not save the setup properly. Each time the tool is opened, some adjustments are required. There are other minor deficiencies in this simulation tool that are not detailed in this document.

The same circuit was entered in both CAD tools and was simulated. FIGURE 2 shows the signal simulation result curves, which are superimposed using the bitmap editor.

FIGURE 2. Superimposed Curves from HyperLynx and SpecctraQuest Simulations.



In general, both curves have a very similar shape. The most visible discrepancies show up on the highest overshoot peak, where falling slopes are offset. The differences are also visible in the below-zero voltage area (logic “0”), where HyperLynx has an output of sharp-shaped curves. Technical literature reports that CAD tools may simulate the same circuit with slightly different results. A reason may be a difference in the impedance calculation and the clamping diodes action, which is addressed later in this document.

CONCLUSION:
The simulation done with relatively advanced tools presents similar results, then it may be trustful to use those tools to predict real circuit behavior. In other words, pre-layout simulation may lead to better designs, may be cost-efficient, and may provide a faster time-to-market cycle. However, it is a must to verify simulation results by taking an oscilloscope measurement on the real board, and if needed, to adjust the termination resistors and layout. Proper oscilloscope measurement techniques are critical in gathering data.

NOTE 1. This simulation document contains mostly graphical results of the try-and-error simulations that have been executed while working on the project. All signal integrity simulations, shown later in this document, refer to the HyperLynx LineSim tool only. Timing simulations are done with Timing Designer.

NOTE 2: Technical documents stipulate that signal edge distortion cause data corruption in digital circuits, therefore, we put effort to investigate techniques controlling signal integrity. This document, in a large portion, shows hands-on exercises with simulation tools attempting signal edge control.

1.3 Any-PHY and UL2 Component Placement Configuration

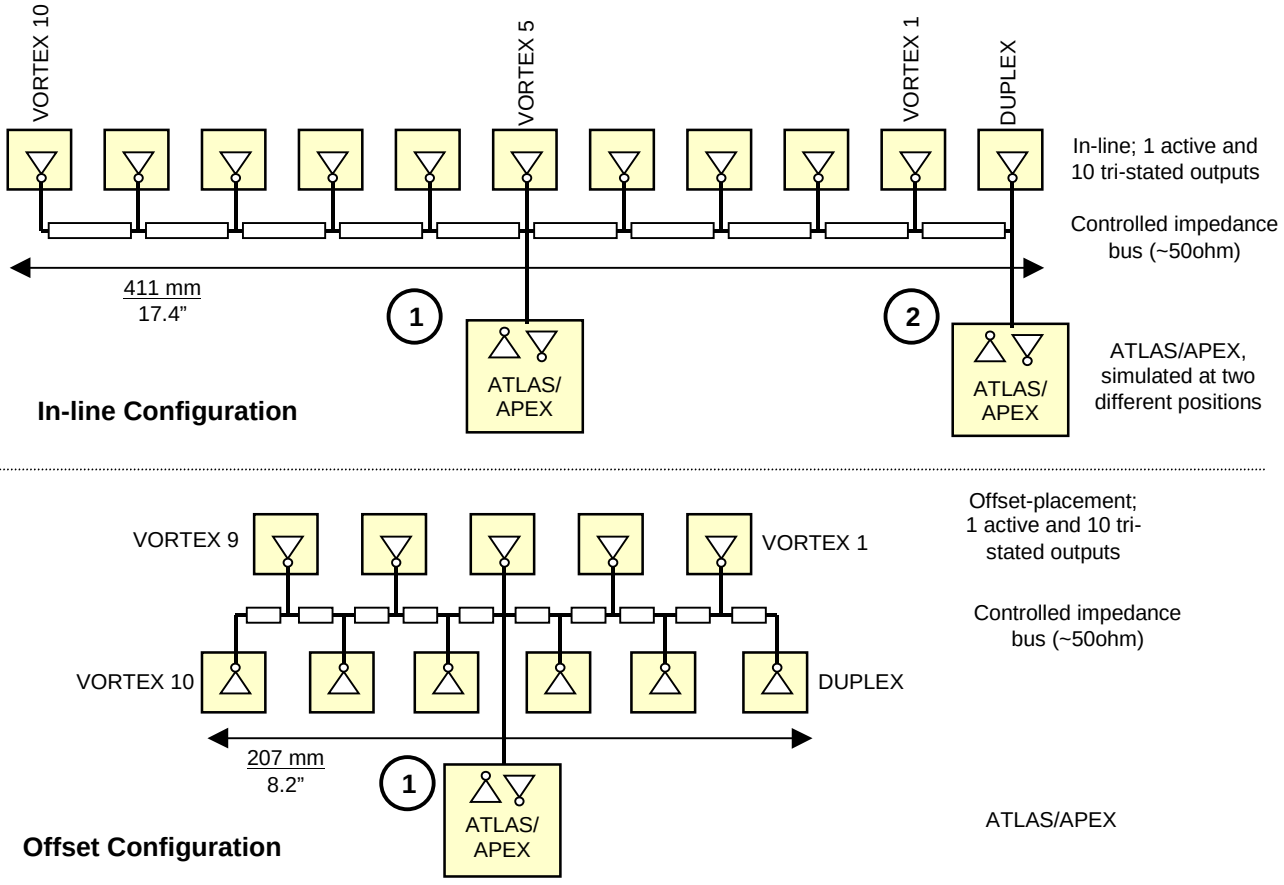
Two different S/UNI-VORTEX/S/UNI-DUPLEX layout configurations were evaluated:

- the in-line bus placement
- the offset bus placement.

The in-line configuration with ten S/UNI-VORTEX devices and one S/UNI-DUPLEX device extends to about 411mm (17.4 inches), which does not fit onto a 6U high board (standard height of the cPCI shelf card). Therefore, a narrower configuration was used as well.

FIGURE 3 shows the block diagram with the in-line and offset configurations. This in-line configuration has two subsets of the S/UNI-ATLAS/S/UNI-APEX connections, marked 1 and 2.

FIGURE 3. Component Placements



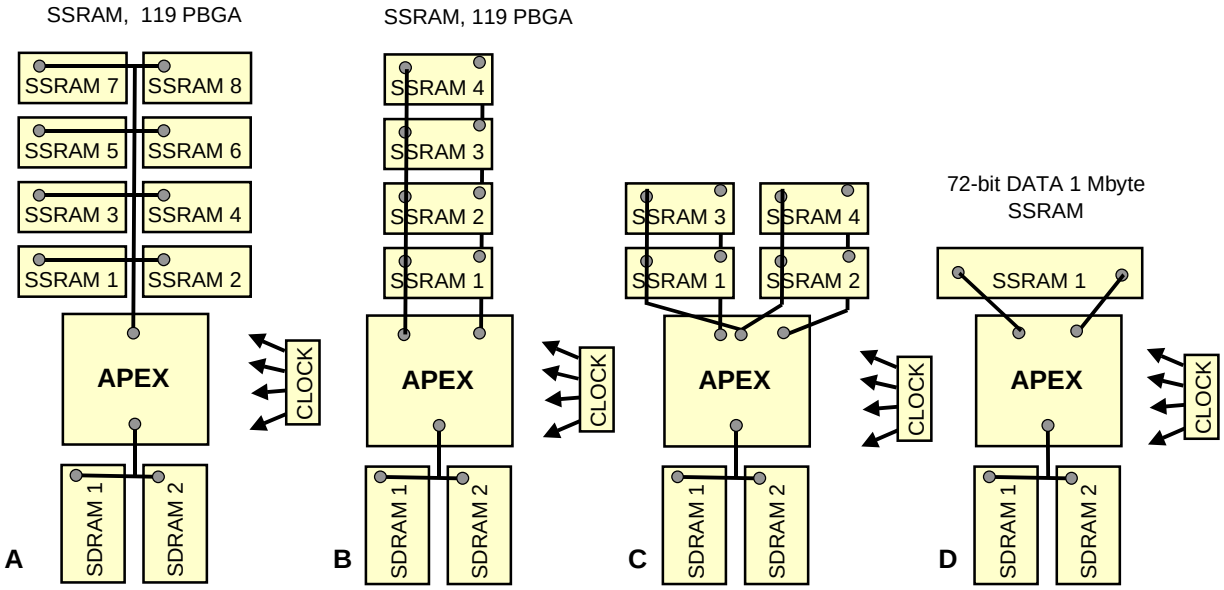
The figure shows the Receive Data bus (Utopia L2) direction (with S/UNI-DUPLEX included). Similar configurations are simulated in the Transmit Data (Any-PHY) bus direction (with the S/UNI-DUPLEX disconnected).

The offset placement configuration may allow fitting components onto a 6U high board. The total length of the S/UNI-VORTEX/S/UNI-DUPLEX assembly is estimated at about 8.2 inch (207mm). More about spacing and dimensions for each component placement is shown later in this document.

1.3.1 S/UNI-APEX - RAM Interface

FIGURE 4 shows the S/UNI-APEX – NBT SSRAM and S/UNI-APEX – SDRAM configuration.

FIGURE 4. S/UNI-APEX-RAM Configuration



The progress in RAM size has made the first two configurations obsolete. Some RAM manufacturers announced the 72-bit wide DATA interface in a single chip with 1 Mbyte size. The Core Card Reference Design uses two SSRAM chips similar to configuration C above, with SSRAM1 and SSRAM2 only.

1.3.2 S/UNI-ATLAS - RAM Interface

The S/UNI-ATLAS – SSRAM interface is not evaluated in this document, as it is relatively slower (50 MHz) and works without problems on other reference design boards.

2 MODELS

2.1 IBIS and SBGA Models

The semiconductor industry provides Input/Output Buffer Information Specification (IBIS) models for I/O pads with IBIS versions 1.1 to 2.1 (2.1 is ANSI/EIA-656 Approved, Dec. 1995). The version 3.2 is currently available on the Internet (3Q 2000). To obtain more information on the version 3.2, go to: http://www.vhdl.org/pub/ibis/ver3.2/ver3_2.txt

This simulation document is based on the IBIS 2.1 standard.

As of publication of this document, the I/O pads used for the simulation are limited to the following types (based on the PMC-Sierra PM-3350_ED2 and S/UNI-APEX-testchip):

- input	pic	S/UNI-VORTEX, S/UNI-DUPLEX and S/UNI-ATLAS
- output	pob12	S/UNI-VORTEX, S/UNI-DUPLEX and S/UNI-ATLAS
- i/o	pc3t02	S/UNI-APEX
- i/o	pc3b04	S/UNI-APEX

The pads have the corresponding IBIS models available in the PMC-Sierra IBIS library. However, this simulation project requires some component values to be modified for the 304-SBGA and 156-PBGA packages, adding or increasing parasitic components (package inductance, capacitance and resistance).

The PMC-Sierra IBIS model is created with elements obtained using the following techniques:

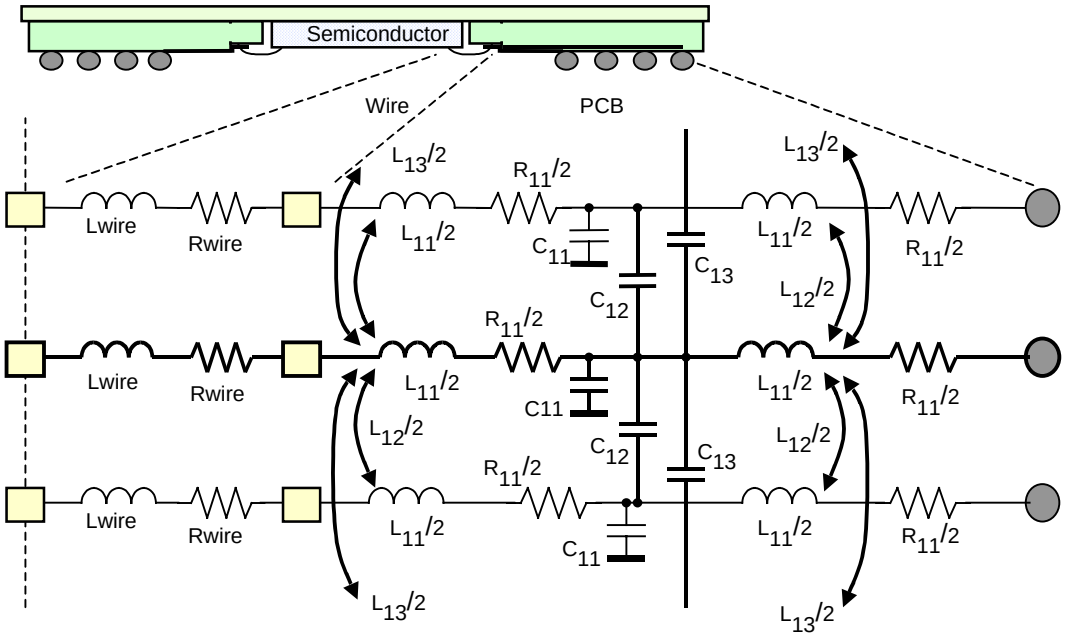
- SPICE model for the silicon I/O pad to derive parallel capacitance C_comp, and data transition speed on positive and negative edges into a 50 ohm load expressed as dV/dt.
- DC current measurement to determine internal DC resistance and characterize clamping diodes. The current flowing through the clamping diodes is limited to 200 mA, and linearly extrapolated above.
- parasitic resistance, inductance, and capacitance (RLC), derived from the SBGA package manufacturer’s electrical model (AMKOR Technology), which includes wire-bonding wire and copper traces on the BGA printed circuit board;

The IBIS standard describes the basics of the recommended measurement techniques and the format of the text file required for creating the IBIS models.

The complete BGA package model includes the first, second, and third order components. The first order elements for the wire and trace are: inductance, capacitance, and resistance. The second and third order components are: mutual inductance and mutual capacitance to the neighboring pads.

FIGURE 5 shows the BGA package cross-section and electrical model.

FIGURE 5. SBGA Package Electrical Model



The electrical model can be as complex as presented in the figure above. The model includes a T-configured third order filter with mutual inductance and capacitance to the first adjacent and second adjacent traces. The mutual components introduce cross-talk from the adjacent data/clock BGA connections.

The complexity of the complete BGA model cannot be reflected in the IBIS 2.1 model. A simplified electrical circuit was created and is shown in FIGURE 6 below. The mutual L12/13 and C12/13 components are included into L_pin and C_pin. The R_pin represents total DC resistance of the wire and trace. The inductance of the Vcc and GND planes is omitted for this model. The value, shown in the SBGA package data sheets, is approximately L_gnd/L_vcc = 0.1nH. The value is at least one order smaller than the L_pin. The significance of the L_gnd/L_vcc may be observed, when crosstalk from multiple switching I/O pads into a quiet I/O pad is simulated, but this topic goes beyond the scope of this document.
FIGURE 6 shows a simplified electrical circuit for the SBGA package and IBIS model.

FIGURE 6. Simplified Electrical Circuit for SBGA Package and IBIS Model

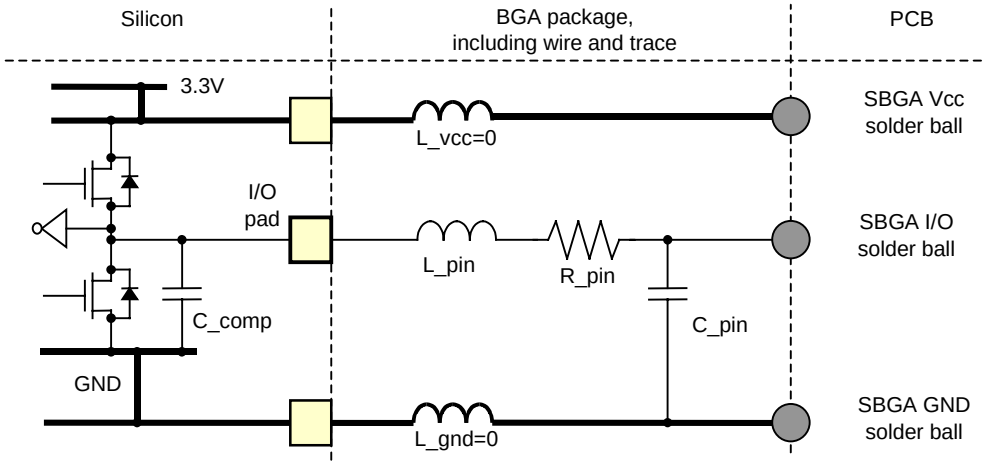


TABLE 1 shows the component values for the BGA and IBIS models.

TABLE 1. SBGA-304 Electrical and IBIS Models Data

			SBGA Electrical Model					
			Inductance [nH]		Capacitance [pF]		Resistance [mΩ]	
			L11		C11		R11	
Pkg	Size [mm]	Trace	trace	t+w	trace	t+w	trace	t+w
304 SBGA	Body: 31 x 31. Die size: 12.5 x 12.5.	Long		7.2		1.19		300
		Short		2.4		0.45		160
			L12		C12			
		Long		1.9		0.23		
		Short		1.0		0.16		
			L13		C13			
		Long		0.8		0.03		
		Short		0.6		0.02		

			IBIS Model			
			L_pin	**C_pin**	**R_pin**	**C_comp**
Pkg		Trace				Typ/min/max
304 SBGA		Long	**8.38**	**1.62**	**300**	**5.0/4.0/7.0**
		Short	**3.53**	**0.72**	**160**	**5.0/4.0/7.0**

The “short” stands for the center I/O pad with the shortest wire and trace length. The “long” stands for the corner I/O pad with the longest connections. The IBIS model requires entering the appropriate data for each pin length. However, some model creators shortcut that process, and all pads have the same parasitic values. Designers are encouraged to exercise effects of different wire bonding and trace length.

TABLE 2 shows the component values for the 304-SBGA and 156-PBGA models.

TABLE 2. PBGA-156 Electrical and IBIS Models Data

			PBGA Electrical Model					
			Inductance [nH]		Capacitance [pF]		Resistance [mΩ]	
			L11		C11		R11	
Pkg	Body [mm]	Trace	trace	t+w	trace	t+w	trace	t+w
156 PBGA	Body 15x15	Long		5.86		0.9		180
		Short		4.65		0.45		140
			L12		C12			
	Die size 5.6x 5.6	Long		1.1		0.14		
		Short		1.0		0.10		
			L13		C13			
		Long		1.0		0.13		
		Short		0.9		0.08		

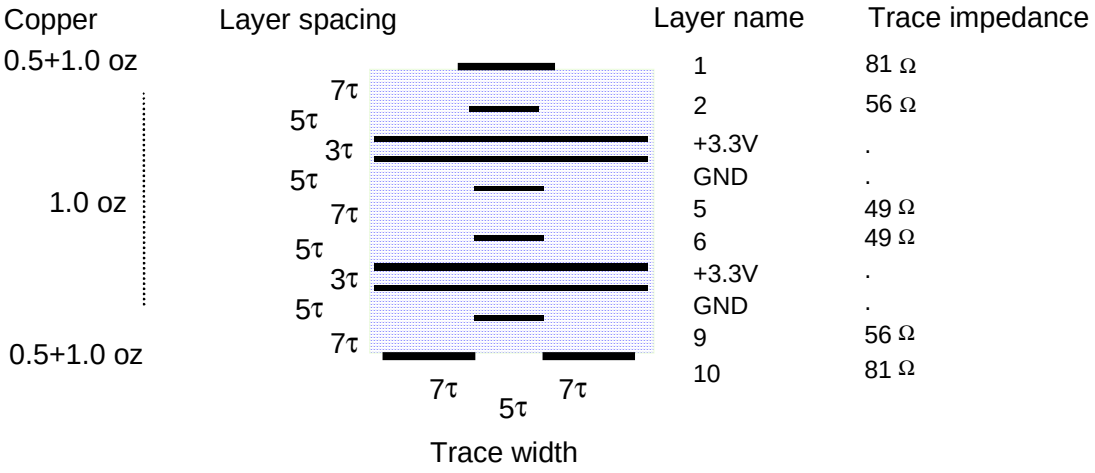
			IBIS Model			
			L_pin	**C_pin**	**R_pin**	**C_comp**
Pkg	Body	Trace				Typ/min/max
156 PBGA	-	Long	**6.61**	**1.37**	**180**	**5.0/4.0/7.0**
		Short	**5.43**	**0.74**	**140**	**5.0/4.0/7.0**

The length of wire and trace has a significant effect on the electrical and IBIS model parameters, which may vary from 10% to 100%. For example, Table 2 shows the C_pin on the short pin is about 40% lower than on the long one.

2.2 Printed Circuit Board (PCB) Cross-section

The simulation was done for the 10-layer PCB. FIGURE 7 shows layers of copper and dielectric. Copper thickness is expressed as 1 oz for the internal traces, and 1.5 oz for the top and bottom layers (shown as 1 and 10).

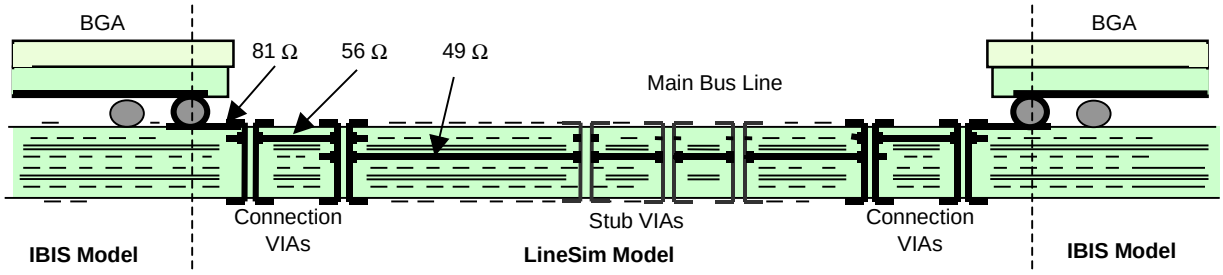
FIGURE 7. PCB Cross-section



The trace impedance is calculated by the HyperLynx program, and shown in the right-most column in the figure above.

FIGURE 8 shows a cross-section of the printed circuit board connections, between devices attached to the bus. The copper connections simulated with the LineSim are highlighted.

FIGURE 8. PCB Bus Connections



The BGA-to-BGA connection consists of three types of copper traces: 81 ohm, 56 ohm, and 49 ohm. The signal path includes four VIAs that connect the shorter traces to the main 49 ohm bus. The central VIA connect stubs to other S/UNI-VORTEX/S/UNI-DUPLEX devices on the bus.

It is believed that VIAs have a negligible effect on signal integrity for edges slower than 0.5 ns and are, therefore, omitted in the simulations.

2.3 FR-4 Material

A variation was found in the literature on the dielectric constant ε_r of the FR-4 glass-resin material. The ε_r value was quoted to be as low as 4.1 and as high as 5. The ε_r value depends on the ratio of the glass-to-resin content, and it may depend on the measuring techniques and other factors. The effect of that variation is suppressed as the ε_r is used in equations as a square root and also as one of the many factors in the sum. A value of ε_r =4.5 was chosen for the HyperLynx simulation and for the equation below. The equation calculates impedance of a buried microstrip line, shown as layers 2 and 9 in FIGURE 7:

$$Zo = 43.037 * \frac{Heigth}{Width} + 5.048 * \frac{Thicknes}{Width} + \frac{1.0676}{1.09\sqrt{\varepsilon_r}} = 49.8ohm.$$

The calculated value differs from the Zo = 56 ohm derived from the HyperLynx tool. (We have not investigated the discrepancy yet.) In general, digital lines are loaded with impedance significantly higher than Zo. Therefore, some impedance discrepancy may not be a significant factor in signal integrity simulations.

In general, the ε_r should be decreased for simulations with higher clock speed.

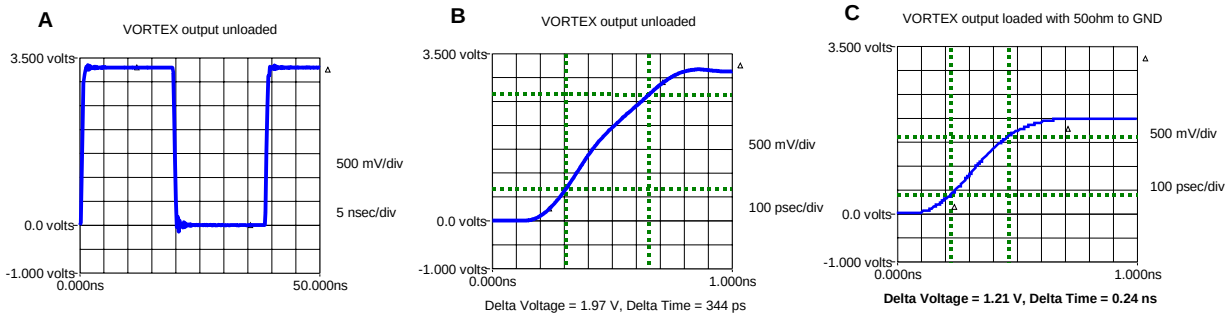
3 UNIFORM TRANSMISSION LINE EXERCISES

The following three sections briefly introduce the simulated behavior of a transmission line passing signal with edge rise time, which is shorter than the transition electrical length (TEL) for that line. TEL is the length of trace that the electromagnetic wave travels during the edge transition time.

3.1 Data Line Simulation

FIGURE 9 shows the LineSim that presents simulation results from two exercises conducted in an oscilloscope-like view.

FIGURE 9. I/O Pad Output Signal Transition



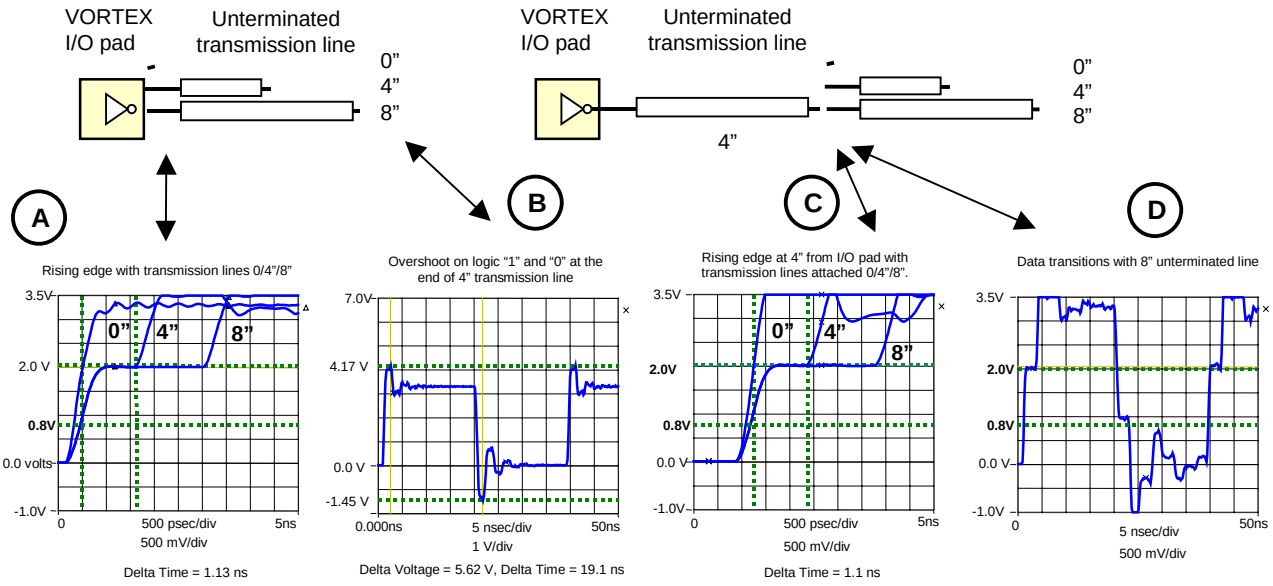
The first exercise was simulation with the I/O pad driving two options: no load and a 50-ohm load. Graphs A and B show an unterminated output with the time base at 5 ns/div and 100 ps/div. Graph C shows a rising edge at 50 ohm resistor to ground. The IBIS text file includes rise and fall time for the pbct12 silicone pad, which is calculated with the SPICE model. Text file shows edge speed at $1.23\ V/1.60 \times 10^{-10}$ sec, which can be converted to a slew rate of 7.5 V/ns. The slew rate derived from graph C in FIGURE 9 was calculated at 5.04 V/ns. The lower slew rate was most likely due to the LRC elements in the IBIS model, which are not included in the SPICE model.

The “monotonic edge” expression throughout this document means monotonic increasing or monotonic decreasing edge, excluding dv/dt = 0. The “non-monotonic” includes flat shelf and “bumps” dv/dt = 0 or dv/dt > 0 on the same edge in 0.8 V to 2 V region.

The next exercise was simulation with the I/O pad driving the long transmission line. The signal was probed at two different configurations. The first configuration probed the rising edge at a BGA pin with an unterminated transmission line at 0, 4 and 8 inches long. The second configuration probed the signal at the end of the four-inch long transmission line section with an additional

line attached at zero, four, and eight inch of length (shown as 0”, 4” and 8”). FIGURE 10 shows the simulation results.

FIGURE 10. Unterminated Transmission Line Simulation



Graphs A and C show the rising edges that have a similar character. The rising edges marked 0” are very monotonic because no transmission line is attached after the probe point. With attached transmission line length of 4” and 8” a flat ”shelf” is visible. The phenomenon occurs when a fast edge enters the transmission line, and there is no information yet on what is at the end of the line. Some hundreds of picoseconds later, the wave returns from the unterminated line end and adds up to the voltage level. A voltage divider consisting of internal I/O pad impedance and Zo determines the “shelf” level. Termination at the end of the line has no effect on the shelf voltage level. It is important to notice that the preceding transmission line has little effect on the signal edge. Graphs A and C look similar from 0 V to 3.0 V. The top of the square wave may have more ripples with a longer line overall.

The flat region of the edge is about 0.76ns long for the 4” line and about 2.1ns long for the 8” line. Graph D shows the 8” wave with a different time-base of 5ns/div. The flat section is visible on the rising and falling edges of the waveform. Technical literature reports that the ”shelf” on data signals may produce soft errors in digital circuits, which may happen a few times a minute or a few times a day, and are difficult to trace. To limit the flat region to about 150 ps, the unterminated transmission line should not exceed 2.5 inches with the transition speed of the pbct12 I/O pad. In general, the flat region on the signal edge(s) functions based on these two factors:

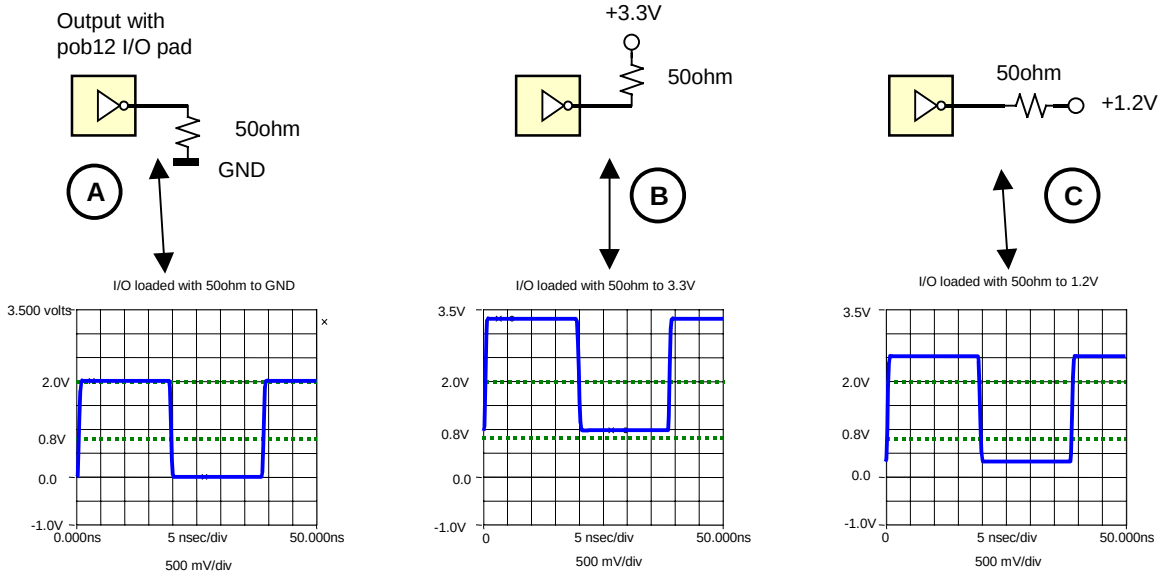
- speed of the edge itself
- length of the transmission line.

The faster the edge, the shorter the transmission line can be attached without signal deterioration. This implies ”shrinking” the package size of the integrated circuit and minimizing the bus length. A micro BGA package allows placing components with shorter bus lines maintaining better signal integrity.

Graphs B and D in FIGURE 10 show a significant voltage overshoot. The negative peak goes to about -1.45 V (and can go much lower as shown in the following sections). This voltage level drives the current through the clamping diodes at the I/O pad. A report indicated that the overshoot waveform that terminated at a pad was causing data corruption into the adjacent pads, which were connected to ”clean” waveforms. This type of interference may not be detectable with an oscilloscope, as this phenomenon is internal to the silicon and may not show up on the external pin. In this case, troubleshooting is difficult, and requires an experienced and knowledgeable engineering staff chasing rare occurrences, when unrelated data/clock I/O pads are interfered with overshot signal connected to another pin.

The question arises – why not to terminate transmission line with 50 ohm resistor and prevent back reflections? The following FIGURE 11 shows the answer. The output with pob12 I/O pad was loaded with a 50 ohm resistor and simulated with the LineSim.

FIGURE 11. Output loaded with 50 ohm.



Graph A shows a signal with a 50 ohm load terminated to ground. Graph B shows a wave with a 50 ohm resistor terminated to +3.3 V. Graph C shows a signal with a 50 ohm load terminated to 1.2 V.

The logic transition voltage for the 3.3 V devices (S/UNI-VORTEX, S/UNI-DUPLEX, S/UNI-ATLAS, and S/UNI-APEX) is specified at 0.8 V to 2.0 V. The logic *high* and *low* should have the appropriate voltage margin above and below those threshold levels respectively. The voltage margin is needed to prevent data corruption from ground bounces, power noise, cross-talk, EMI, timing inaccuracy and other signal deficiencies.

Graph A shows logic *high* at 2.0 V, providing no voltage margin for the input pad. Graph B shows logic *low* at 1.0 V, which is above the 0.8 V threshold. Graph C shows margins on logic *low* and *high* at about 500 mV. The margin is not enough to prevent data corruption in real circuits. The signal compression with the 50 ohm load is due to internal resistance of the MOSFET transistors at the I/O pad. This resistance is different for P and N transistors, creating an asymmetry with termination to ground and 3.3 V. The driver needs to source 60 mA to maintain the logic *high* at 3.0 V with a 50 ohm resistor connected to ground. The pob12 I/O pad cannot deliver this current.

The “C” circuit requires additional 1.2 V power rail on the printed circuit board. The noise on this power rail will be coupled into data lines through the 50 ohm resistors. A ”quiet” rail is required, which may not be feasible in a noisy digital environment. Regulated power supply and filtering capacitors are needed to maintain this power rail.

Also, 50 ohm terminations, to ground or power rail, require a high current at the driver, increasing the total power dissipation in a silicon device.

To conclude, the line impedance that matches the parallel termination (about 50 ohm) is not possible with the pob12 I/O pad under investigation.

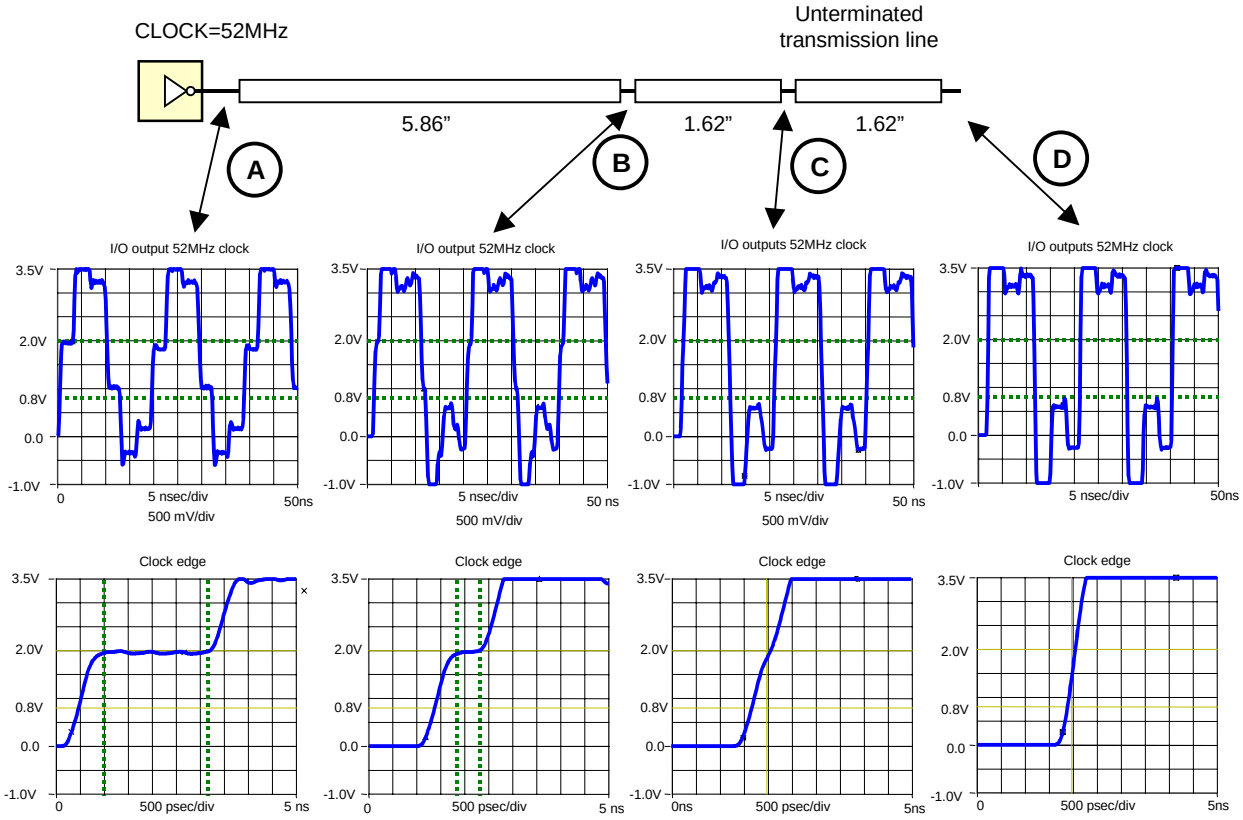
A theoretical solution may be to create transmission lines with a high Zo, for example, 150 ohm. This allows a termination resistor at 150 ohm, and in turn, the I/O pad may provide an adequate driving current to deliver logic *high* with the appropriate margin. However, such a high-Zo trace will be difficult to design with the 10-layer board. A stripline (layer 5 and 6 in FIGURE 7) at 1 mill (0.001 inch) wide is calculated to have Zo = 74 ohm. The layer 1 line at 1 mill has impedance at Zo = 129 ohm. The 1 mill wide trace is impossible to manufacture for commercial applications. The high-Zo transmission lines require very narrow copper traces manifesting residual inductive impedance due to the skin effect. This may limit the frequency bandwidth, and the edge and clock speed on the transmission line. Also, the 150 ohm line requires higher distance to a ground

plane, thus increasing crosstalk and EMI. If bus lines are split, the high impedance transmission line would show back-reflections the same way as the low-Zo transmission line. A typical bus layout comprises split bus lines.

3.2 Clock Line Signal

The clock signal integrity requires clock edges to be monotonic in the logic signal transition region of 0.8 V to 2.0 V. LineSim was used to simulate the clock signal at 52 MHz with an unterminated transmission line. FIGURE 12 shows the results of this exercise.

FIGURE 12. Clock Simulation with Unterminated Line



The clock signal is captured using two different time-bases. The upper row shows a multiple clock transition at 5 nsec/div, and the lower row shows a rising edge at 500 psec/div. Points A and B show rising edges that are not suitable for the most bus applications. Note that the ”shelf” is not clearly visible on the upper Graph B, which raises the issues of a proper setup of the simulation tools and measurement techniques on real boards.

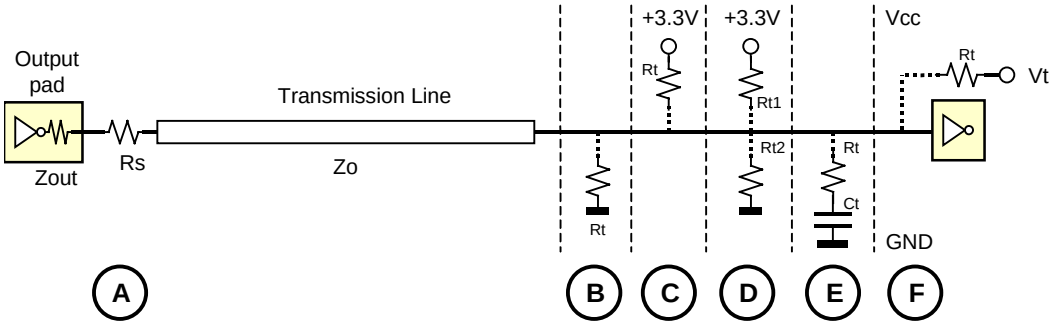
Graph C shows a monotonic edge at the probe point located 1.62 inch before the line end. As shown, the clock signal closer to the source has the edges more distorted than the same clock signal at the end of the transmission line. The overshoot and undershoot is significantly higher at the line end.

Graph D shows the clock edge is fastest at the line end. If two devices are at some distance from each other and are driven with the same clock line connected in series, some edge skew may be introduced not only by the trace length but also by the edge slope.

3.3 Serial and Parallel Termination

This section briefly analyzes signal integrity versus the serial and parallel termination resistors that are attached to the bus. The bus termination mythology implies inserting the serial termination resistors at the beginning of the line, and placing parallel terminations at the signal destination close to the line end. FIGURE 13 shows the termination models.

FIGURE 13. Line Termination Model



The line terminations shown above can be described briefly as follows:

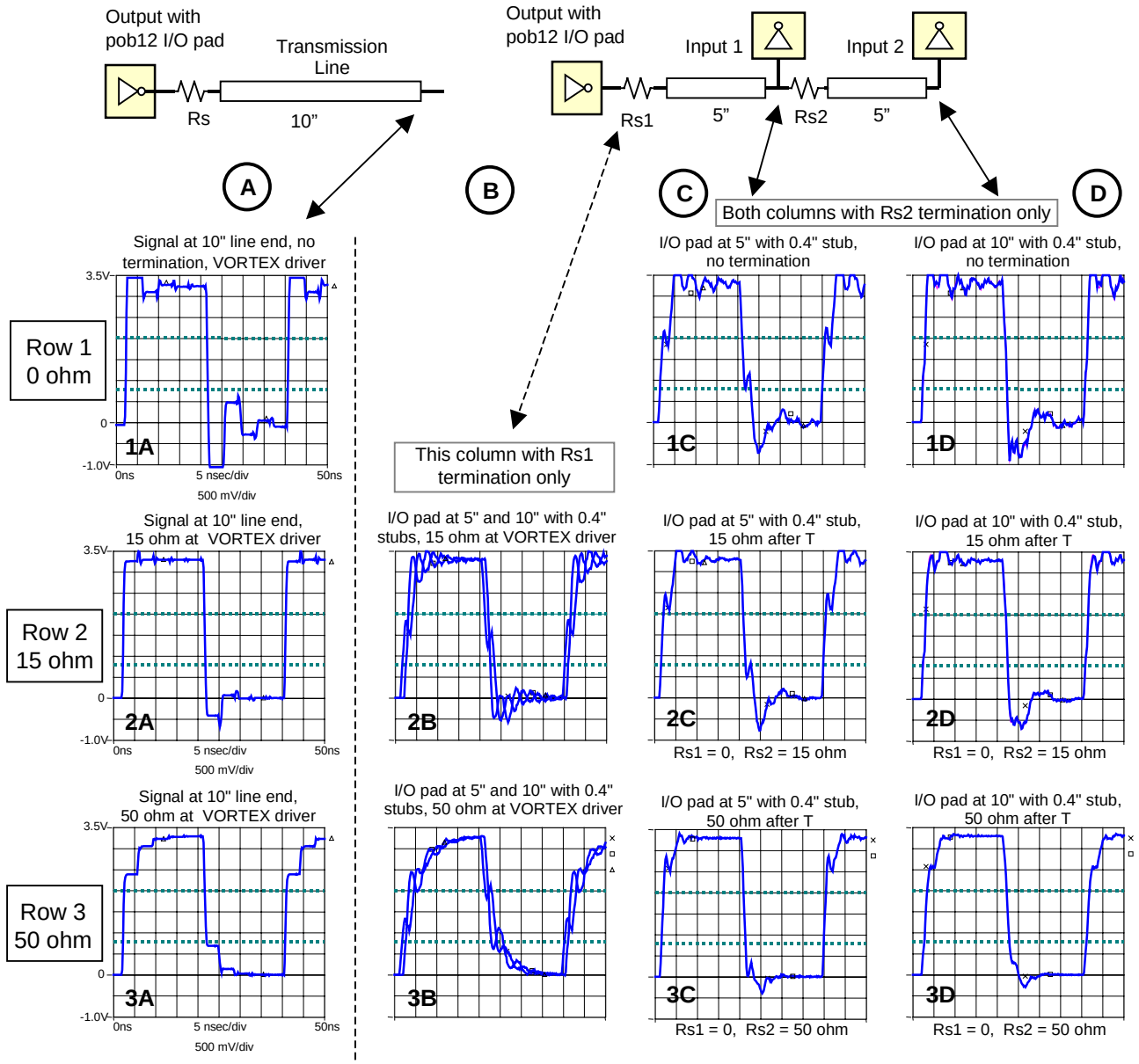
- A – a serial resistor, usually Rs ≤ |Zo – Zout|
- B – a parallel resistor to ground, Rt is usually matching or exceeding Zo.
- C – a parallel resistor to power (noise from power coupled into data line)
- D – the Thevenin termination consisting of Rt1 and Rt2 connected to Vcc and GND respectively. Impedance of the parallel resistors matches or exceeds Zo.
- E – a termination know as the “AC-termination”, where high frequency components of the signal edge are terminated with the Rt, and a DC content is blocked by the Ct capacitor.
- F – a parallel resistor to the power rail at about 1.2 V to 1.5V. The resistor value matches or exceeds Zo.

A recommended line-end termination is the Thevenin circuit, which provides good impedance matching and is not as demanding for the high current drive as the B and C terminations. The F termination requires an additional low noise power rail. All DC coupled parallel terminations decrease the logic voltage swing. The AC-termination targets the near-edge portion of the signal. However, in high-speed designs, the whole signal usually degrades with AC termination, and this type is rarely seen.

FIGURE 13, above, presents the termination circuits that apply to the point-to-point transmission line. In a bus environment, stubs and capacitive loads are distributed across lengthy transmission lines, and the classic terminations may not work. It is shown later in this document and measured on a real board, that serial termination at the beginning and parallel termination at the end are not the best solutions in split buses.

FIGURE 14 (below) shows a simulation which tries to explore a different placement of a serial termination and signal degradation effects.

FIGURE 14. Simulated Signal vs. Serial Termination



Column A in FIGURE 14 shows the signal at the end of the 10-inch long unloaded line. Graph 1A shows strong back-reflections with an unterminated line. Graph 2A shows a ’perfect’ logic *high*, and some overshoot on *low* with Rs = 15 ohm inserted immediately to the I/O driver. The 3A graph shows an over-terminated signal with the serial resistor Rs at 50 ohm.

Columns B, C, and D show simulated signals with two devices connected:

- Input 1 at 5 inch from the driver
- Input 2 at the end of the 10 inch line.

Column B shows two curves on each graph due to space limitations. The row 2 graph shows a signal at both Inputs 1 and 2, with serial resistor Rs1 = 15 ohm placed immediately to the driver. The signal at Input 1 has a non-monotonic edge in logic transition region 0.8 V to 2.0 V. Graph 3B shows multiple –back-reflections on both curves due to over-termination.

Columns C and D show simulated signals with serial resistor Rs2 placed at the beginning of the second 5 inch section of the transmission line, and Rs1 = 0 ohm. All four graphs in the lower right corner of FIGURE 14 (2C, 2D, 3C, and 3D) show monotonic edges in the 0.8 V to 2.0 V transition region with low overshoots. The over-terminated line with Rs2 = 50 ohm shown on graph 3C (only Rs2) has relatively the best performance for Input 1 (surprisingly).

The double edges in 2B and 3B show propagation delay at both inputs.

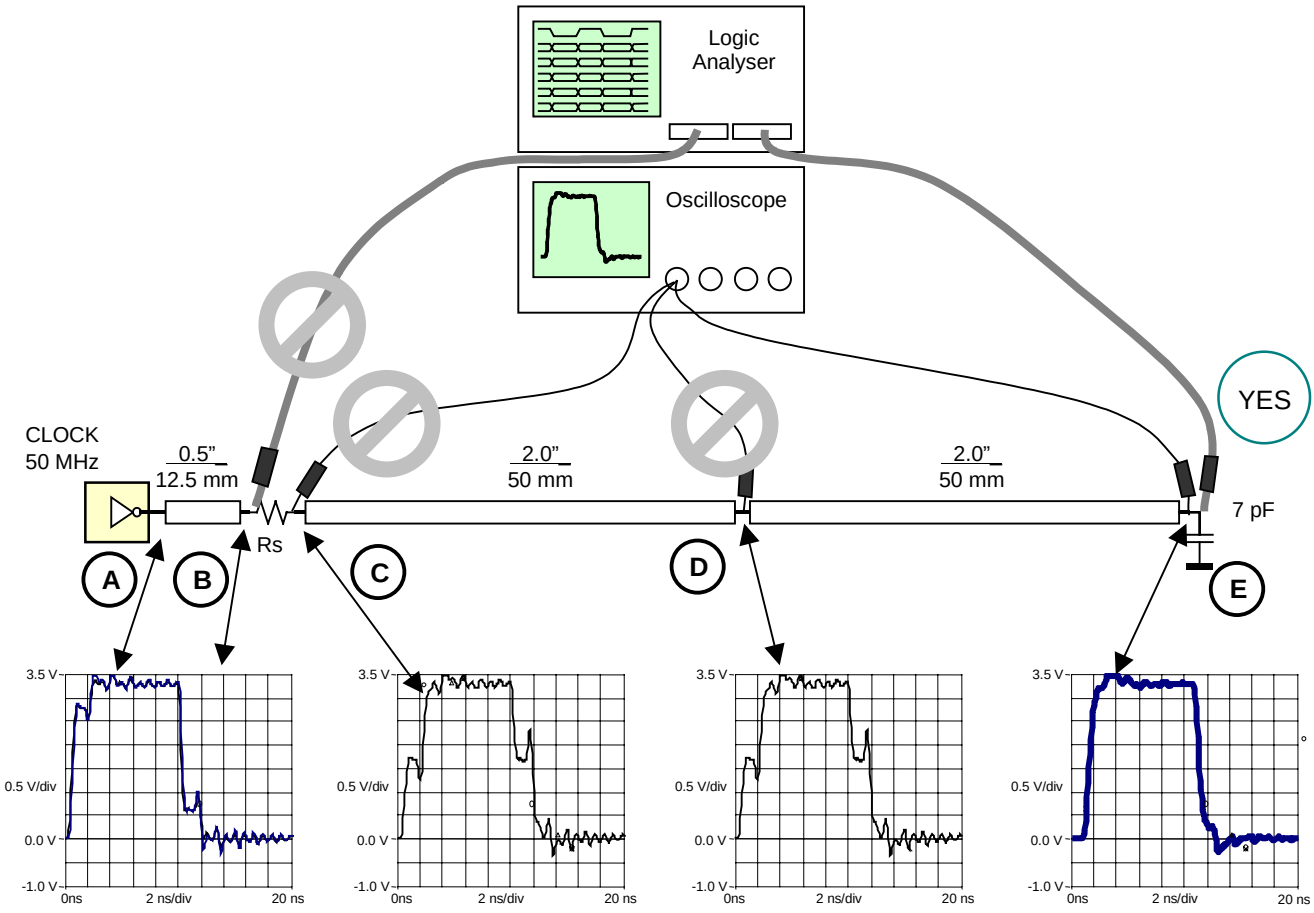
The above explanation and time consuming data gathering to show that the rule-of-a-thumb placement of the serial resistor, at the beginning of the transmission line, may not be the best solution in a bus configuration.

To conclude, the serial termination resistor may improve signal shape if the resistor is placed further in the middle or towards the end of the transmission line. Also, relatively high resistor values (50 ohm +) provide a better termination.

3.4 Test Points vs. Edge Distortion

The edge distortion, on a transmission line, may lead to a false conclusion regarding signal integrity and timing when tested at wrong spots. Examples of waveform distortion at different test point locations are shown in FIGURE 15 below.

FIGURE 15. Simulated Signal at Different Test Points



The signal integrity and timing should not be obtained at the beginning or in the middle of a transmission line. Testing waveforms at points A, B, C and D may lead to false conclusions due to significant backreflections. The proper test point is at the transmission line end - E, where the signal shows up without any edge distortion.

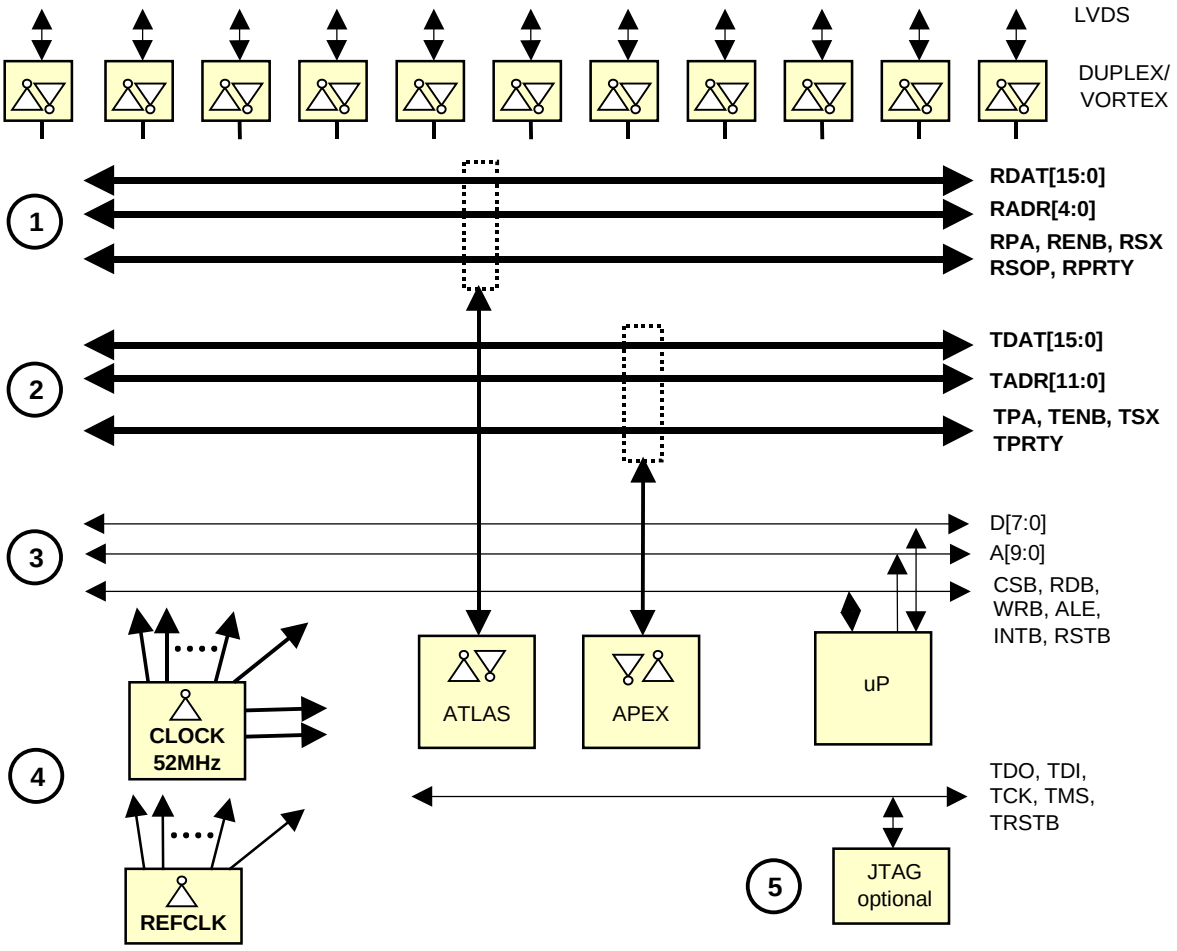
4 BUS SIMULATION

This section presents LineSim at work for the pre-layout circuit consisting of 10xS/UNI-VORTEX, 1xS/UNI-DUPLEX, 1xS/UNI-ATLAS, and 1xS/UNI-APEX devices.

4.1 Bus Complexity

FIGURE 16 shows the data and clock lines related to the S/UNI-VORTEX/S/UNI-DUPLEX interface. Digital lines are grouped into sections with different speed requirements. The bus list includes the Utopia L2 bus (1), the Any-PHY bus (2), the microprocessor interface bus (3), and the optional JTAG bus (5). Clock distribution (4) is also a vital part of the layout, and it is laid out in a point-to-point configuration. The total number of lines in all buses is over 88.

FIGURE 16. Example of VORTEX Chipset Bus Lines



Each S/UNI-VORTEX/S/UNI-DUPLEX needs three clocks: RCLK, TCLK and REFCLK. RCLK and TCLK can share the same clock signal, and in turn, the total of the two clock traces can be run to each device. The clock lines have to be designed and verified, with the simulation tools and real board oscilloscope measurement to avoid the non-monotonic edges. In some designs clock skew to RCLK and TCLK is necessary – timing simulation is required to optimize circuit. Also, timing skew may be required between different entities connected to the same bus – as shown further in this document. The signal simulation described in this document applies to some of the high-speed bus lines highlighted in FIGURE 16 above.

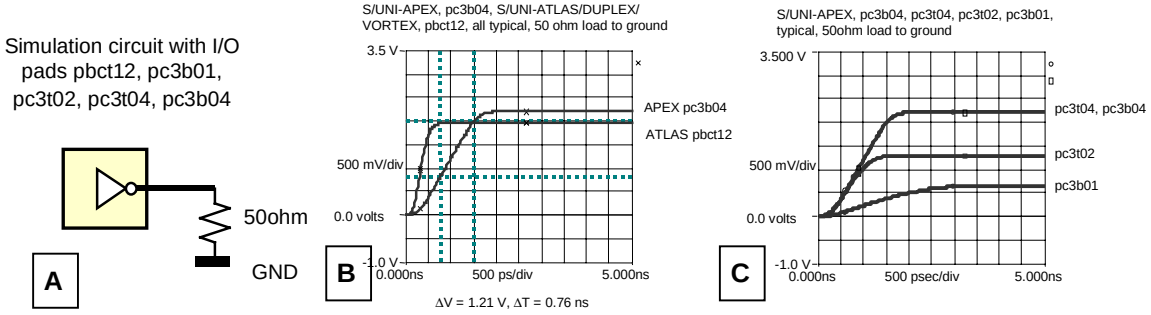
RCLK and TCLK can be up to 52 MHz. The REFCLK is at 1/8 of the LVDS link clock, for example, if the LVDS interface is at 200 Mbs, then the REFCLK is 25 MHz. The fastest clocks are usually running Utopia and Any-PHY buses up to 52 MHz. The interfaces between the S/UNI-APEX and RAMs can be at 80 MHz. The RAM interfaces are not shown in FIGURE 16 and are addressed later in this document.

The appropriate layout techniques must be implemented to place all 88 high-speed data bus lines, 22 point-to-point clock lines and termination resistors. At the same time signal integrity with low crosstalk and controlled back-reflections must be maintained.

4.2 S/UNI-ATLAS and S/UNI-APEX I/O Pads Driving Capability

The IBIS model for the S/UNI-APEX and S/UNI-ATLAS I/O pads is used in simulation to determine the driving capability. FIGURE 17 shows the simulation plots that are shown together for comparison purposes.

FIGURE 17.)S/UNI-APEX S/UNI-ATLAS I/O Pads



The highest current is delivered by the S/UNI-APEX pc3b04 and pc3t04 I/O pads (0.25u process). The fastest edge is delivered by the S/UNI-ATLAS/S/UNI-VORTEX/S/UNI-DUPLEX pbct12 I/O pad (0.35u process). The pc3b04/pc3t04 pads drive the SSRAM Address/Data, Utopia L2 or Any-PHY buses, with ten devices attached to the bus (in this simulation document). The pbct12 pad drives the Utopia L2 bus with eleven devices at the bus.

The pc3t02 has an edge speed similar to the pc3b04 with a lower current drive. The pc3t02 pad is used for SSRAM control lines.

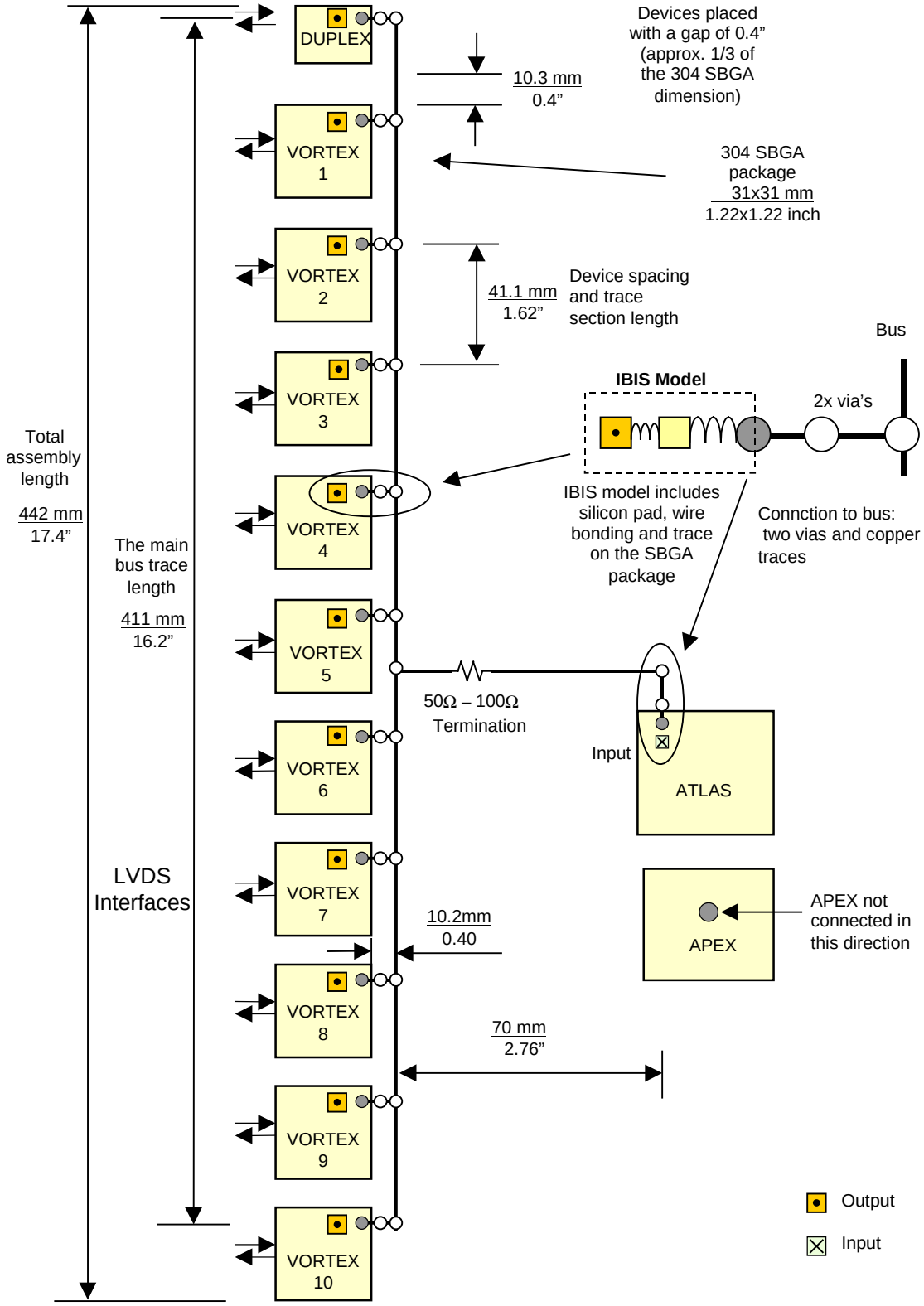
The S/UNI-APEX pc3b01 pad delivers a significantly lower current and lower speed. This pad drives the WAN site bus between the S/UNI-APEX and the S/UNI-ATLAS. The bus has only two devices connected as a point-to-point configuration.

NOTE**:** All Utopia interfaces are done with the IBIS model set at “typical”. The strong/fast and weak/slow IBIS models are used for the SSRAM – S/UNI-APEX interface only. Designers can choose whether to repeat simulations with different IBIS model settings.

4.3 S/UNI-DUPLEX/S/UNI-VORTEX/S/UNI-ATLAS In-line Bus Configuration

The DSLAM devices are placed in an in-line configuration, and signal integrity is simulated. FIGURE 18 shows the in-line configuration.

FIGURE 18. In-line Bus Configuration

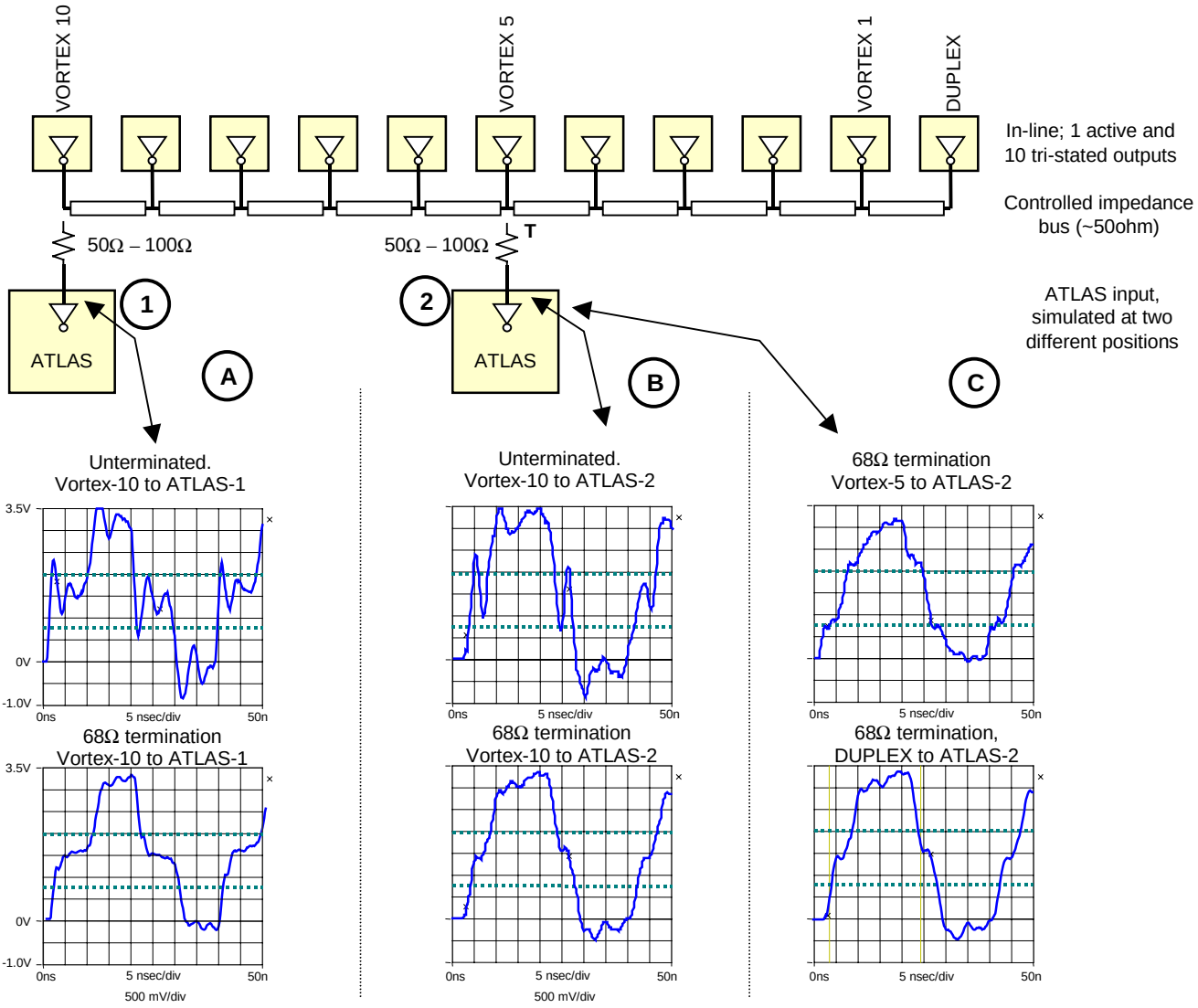


The in-line configuration provides a natural data flow with the LVDS interfaces on one side and bus connections on the opposite side of the S/UNI-VORTEX devices. Bus lines are connected for the simulation purposes with 0.4-inch stubs. The total height of the S/UNI-VORTEX/S/UNI-DUPLEX assembly is about 442 mm (17.4 inches), and the main bus line is about 16.2-inch long (with 0.4-inch spacing between ICs).

4.3.1 Many-to-Single In-line Bus Configuration

FIGURE 19 shows the simulation results for the in-line placement in the Receive Data direction.

FIGURE 19. In-line Component Placement Simulation



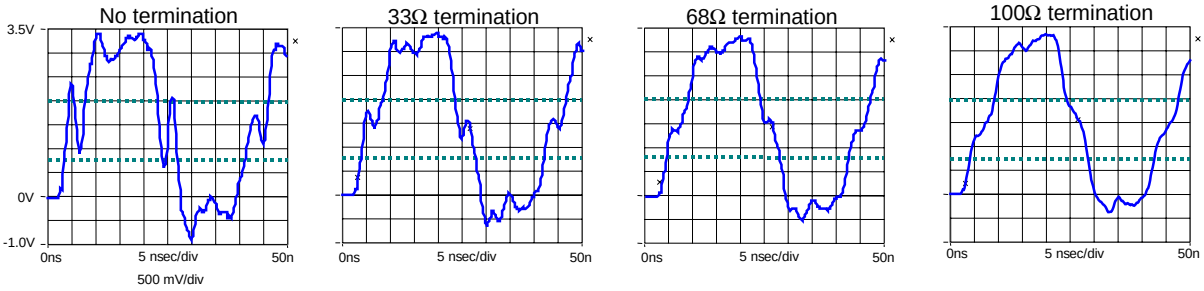
The S/UNI-ATLAS is connected in two configurations marked as 1 at the bus end, and 2 at the center of the bus. A serial resistor is placed at the beginning of the trace connecting to the S/UNI-ATLAS. The LineSim enables one device at a time to transmit towards the S/UNI-ATLAS.

The graphs in column A show simulation with the S/UNI-ATLAS connected at the bus end. The higher row shows a signal at the S/UNI-ATLAS without any resistive termination. The lower graphs show the same simulation with a 68 ohm resistor placed at the junction towards the S/UNI-ATLAS. It is clearly visible that the serial termination provides a significant improvement in the signal quality. However, the bus-end configuration (1) creates a very long flat shelf at the rising and falling edges of the signal. The edge distortion on the transmission line, shown in FIGURE 10 (flat shelf), manifests itself here as well. This distortion is inherent to the end-of-bus placement due to the very long-time needed to bounce the signal from the opposite bus end (bounce at the S/UNI-DUPLEX).

The graphs in columns B and C show signals with the S/UNI-ATLAS placed at the bus center. The top graph in column B shows the signal without termination, and the lower graph shows the same signal with a 68 ohm serial resistor termination. The graphs in column C show simulation with a 68 ohm serial resistor termination and the S/UNI-VORTEX #5 or the S/UNI-DUPLEX as a driver.

FIGURE 20 shows the simulated signal at the S/UNI-ATLAS that is connected at the center as a function of the serial termination resistor.

FIGURE 20. S/UNI-VORTEX-10 to S/UNI-ATLAS-2 vs. Serial Resistor

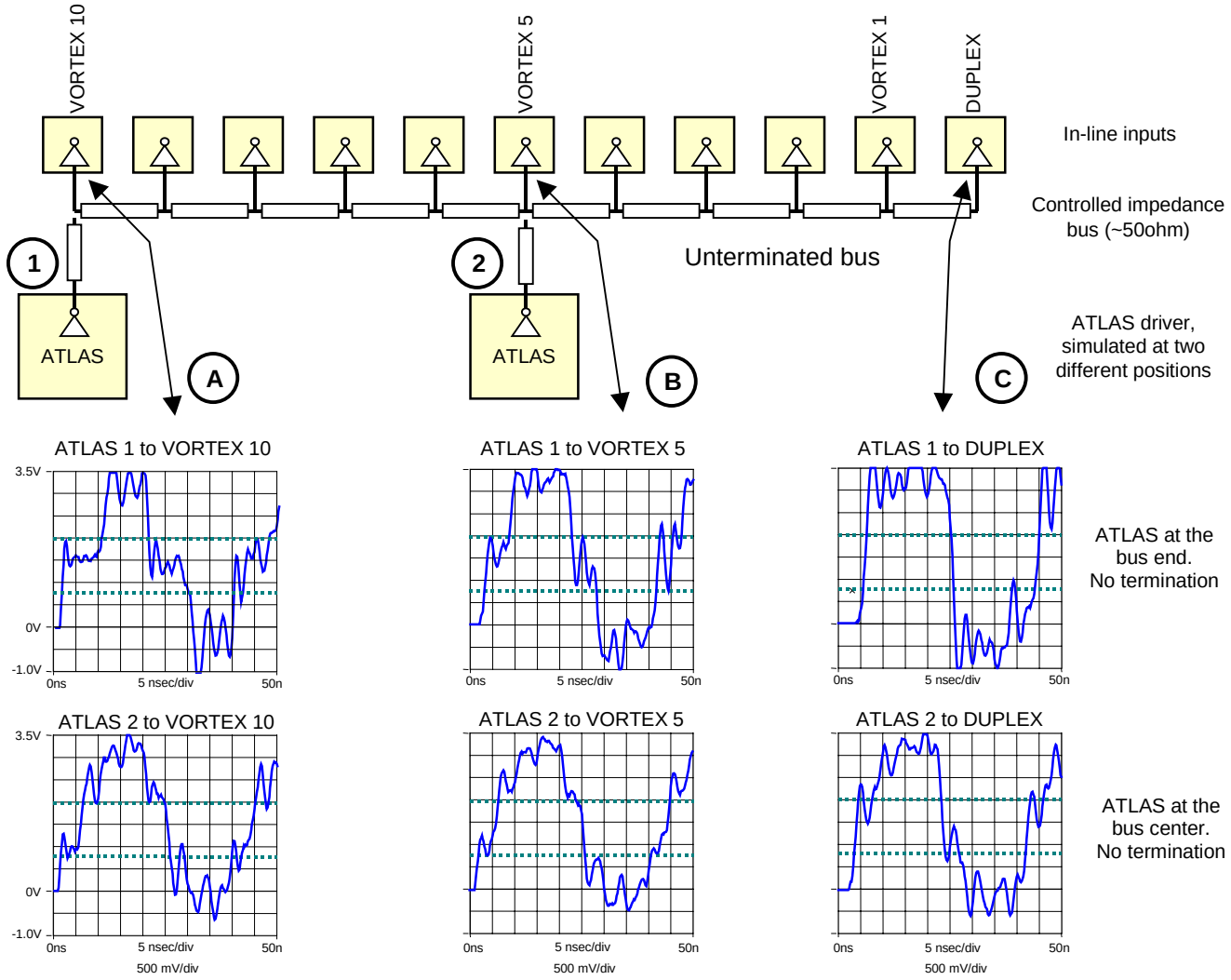


The serial resistor eliminates non-monotonic shape of the simulated signals. At the same time, the average slope of the rising and falling edges is decreased. To conclude, the resistor value between 68 and 100 ohms is optimal for the in-line Utopia bus configuration.

4.3.2 Single-to-many In-line Bus Configuration

This simulation was conducted with the S/UNI-ATLAS / S/UNI-APEX connected at the bus end and at the bus center. FIGURE 21 shows the simulation results for the unterminated bus.

FIGURE 21. Simulation with S/UNI-ATLAS Driving In-line Bus

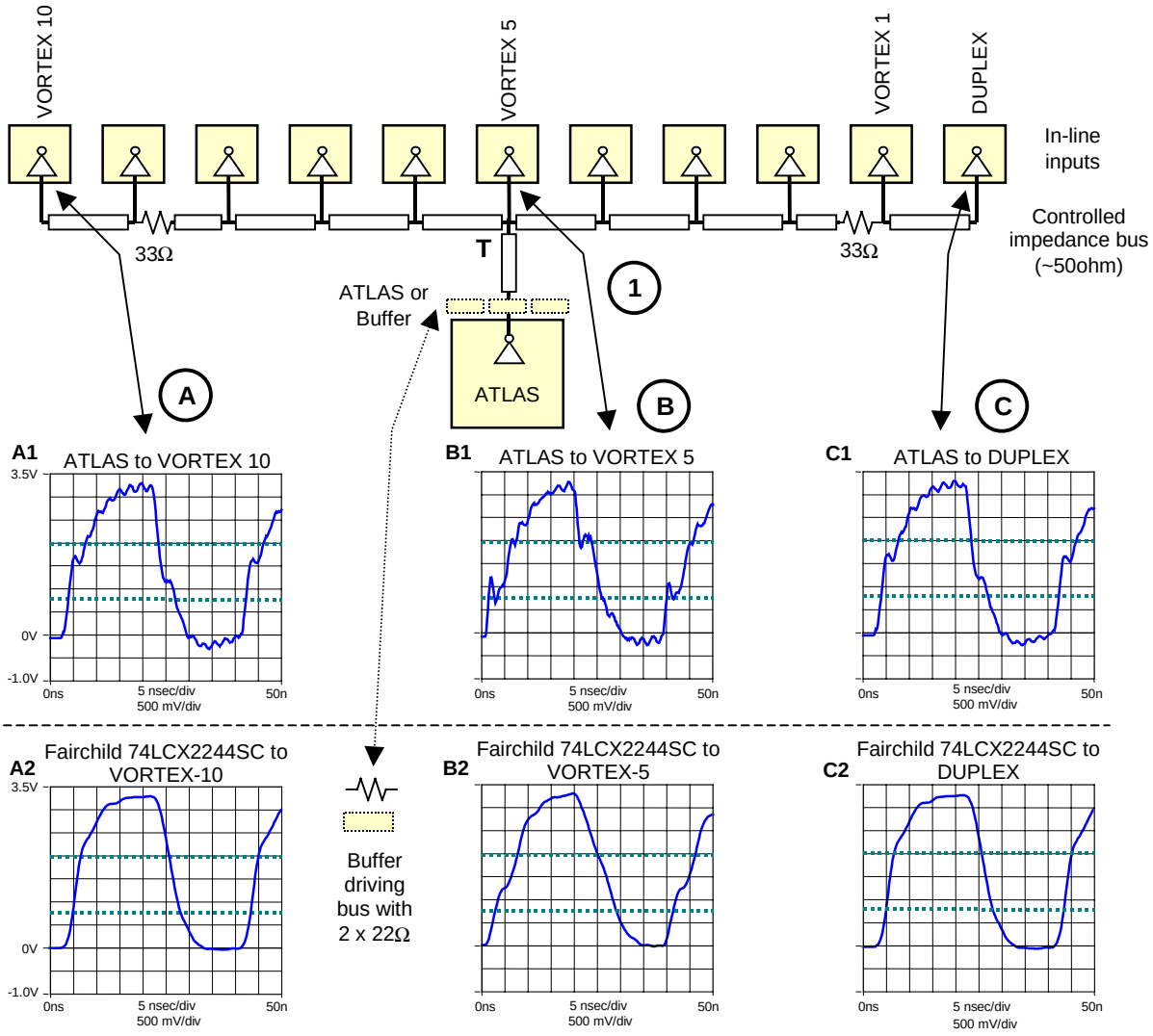


The signal transmitted from the S/UNI-ATLAS 1 at the bus end has a flat shelf at the S/UNI-VORTEX 10 input and multiple back-reflections on all destinations.

The simulated signal transmitted from the S/UNI-ATLAS 2 connected at the bus center shows multiple bumps on all inputs. To clean back-reflections, signal conditioning attempts were made. The signal was simulated with serial

termination resistors placed near the bus ends. A configuration with a buffer driven bus was also tested. FIGURE 22 shows the simulation results.

FIGURE 22. S/UNI-ATLAS to Bus In-line with Termination Resistors



The upper row, with graphs A1, B1, and C1, shows a signal on the bus driven with the S/UNI-ATLAS. The lower row, with graphs A2, B2, and C2, shows a signal on the bus driven with the Fairchild 74LCX2244SC.

The S/UNI-ATLAS driven bus simulates a saw-tooth type of signal due to an energy split at the T joint and an energy loss in serial resistors. In FIGURE 21, it is easily visible, with the upper right graph showing very sharp edges, as the bus energy flows in one direction and reaches its destination point (no splits).

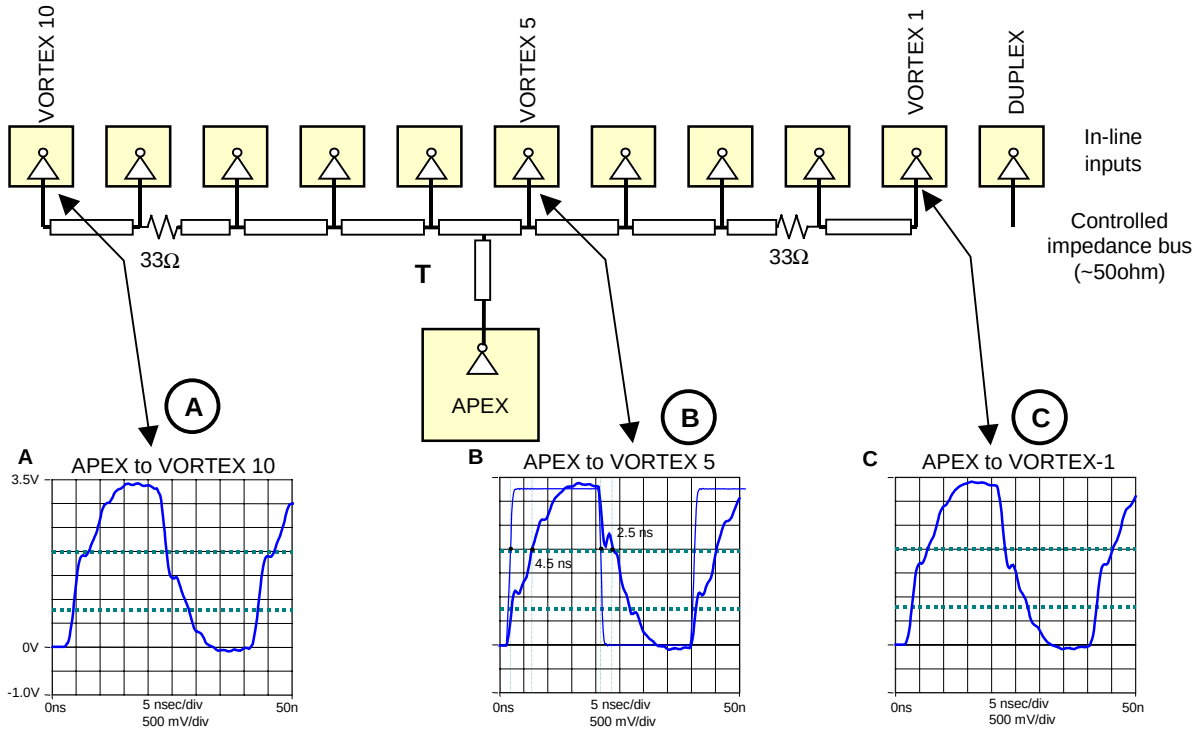
In FIGURE 22, the 33 ohm termination resistors give an improved signal quality, suppressing most of the non-monotonic ripples at the bus ends. However, the center of the bus still simulates a signal with non-monotonic edges. A workaround is to insert 68 ohm serial resistors at the stubs towards the S/UNI-VORTEX #4/5/6. This workaround eliminates non-monotonic edges, though complicating the layout in which a large number of resistors (five for each bus line) must be used. A serial resistor also decreases edge speed.

In search of monotonic edges, a relatively slow 74LCX2244SC 3.3 V line driver (with 5 V compatible inputs) was used as a bus driver. The signal edges, shown on graphs A2, B2, and C2 in FIGURE 22, are monotonic without any overshoots or undershoots. The signal at the S/UNI-VORTEX-5 (bus center) shown in graph B2 simulates slow and monotonic transition across 0.8 V and 2.0 V. In addition, a major timing trap awaits a designer. Slow buffers inherent long propagation delay time, specified in the Fairchild data sheet at tmin = 1.5 ns and tmax=7.5 ns. A higher clock skew is also guaranteed. The propagation delay variation of that magnitude may ”kill” bus timing.

The faster drivers, such as LPT, LVC, ALVC, or ALVCH, show simulation with very non-monotonic edges. We were unable to simulate the monotonic signal with less than three serial termination resistors for each bus line. The energy split effect at the T-joint and back-reflections cannot be overcome (with S/UNI-ATLAS I/O pad).

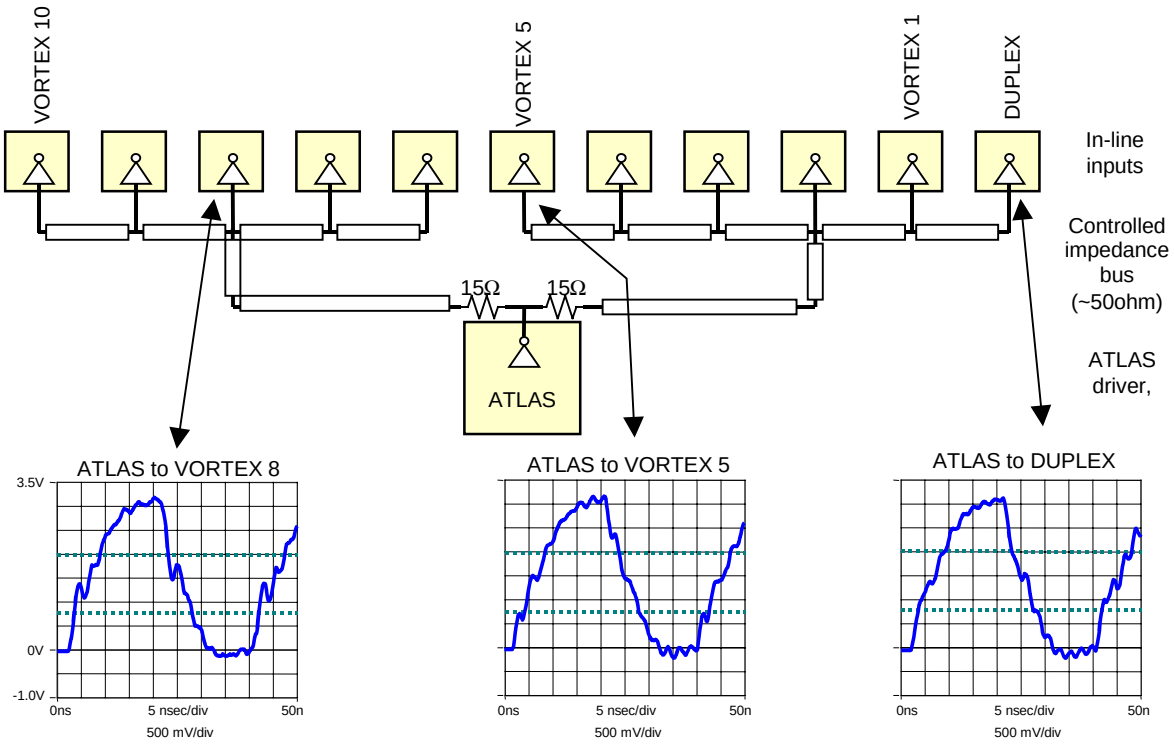
FIGURE 23 shows the S/UNI-APEX to the Any-PHY in-line bus simulation.

FIGURE 23. S/UNI-APEX to Bus In-line with Termination Resistors



A split configuration was simulated in an attempt to find the solution to get monotonic signals. FIGURE 24 shows the bus divided into two branches.

FIGURE 24. S/UNI-ATLAS Driving Dual-branch Bus



The signal is similar to the one shown in the previous 33 ohm in-line simulation in FIGURE 22. Non monotonic edges are simulated on some inputs. The signal is more saw-tooth like with the lower amplitude. In turn, the timing of logic *high* (above 2.0 V) is adversely affected. The multiple energy split on the T-joints (and energy loss in serial resistors) distorts the square wave into a triangle wave. In technical literature, this bus connection is called a “crow-feet” configuration.

The conclusion for the one-to-many and many-to-one in-line configurations are:

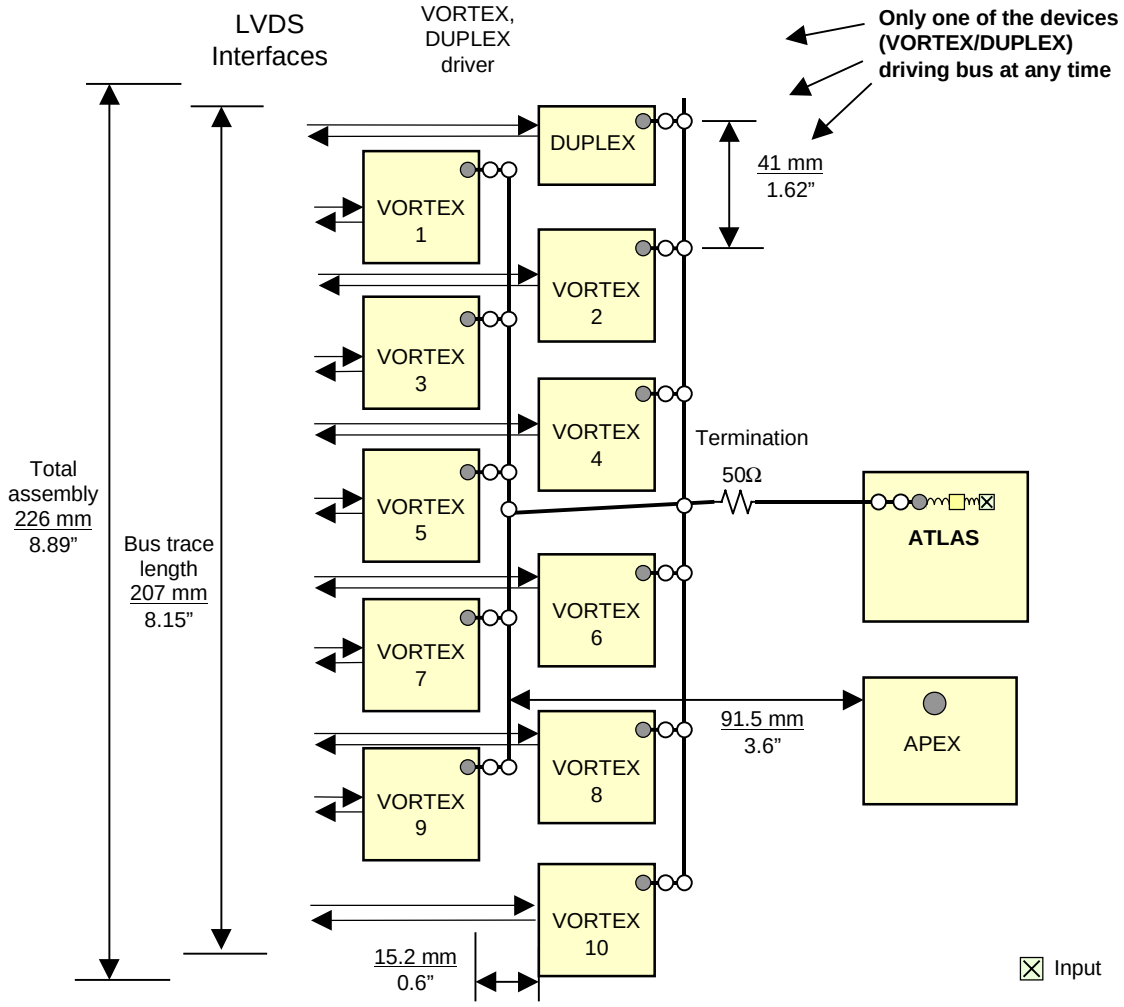
- The best placement of the S/UNI-ATLAS / S/UNI-APEX driving directly the bus is at the center of the bus, with some non-monotonic signal near the bus center

- An additional high-speed bus driver with dedicated lines at the central position provides a “good” signal, however, resulting in a more complex circuit and the penalty of a significant propagation delay and skew.

4.4 Utopia and Any-PHY Dual Bus Offset Configuration

FIGURE 25 shows the Utopia/SCI-PHY Receive Direction dual bus with an offset component placement that fits onto the 6U double eurocard, compatible with a standard cPCI shelf.

FIGURE 25. Offset Bus Configuration

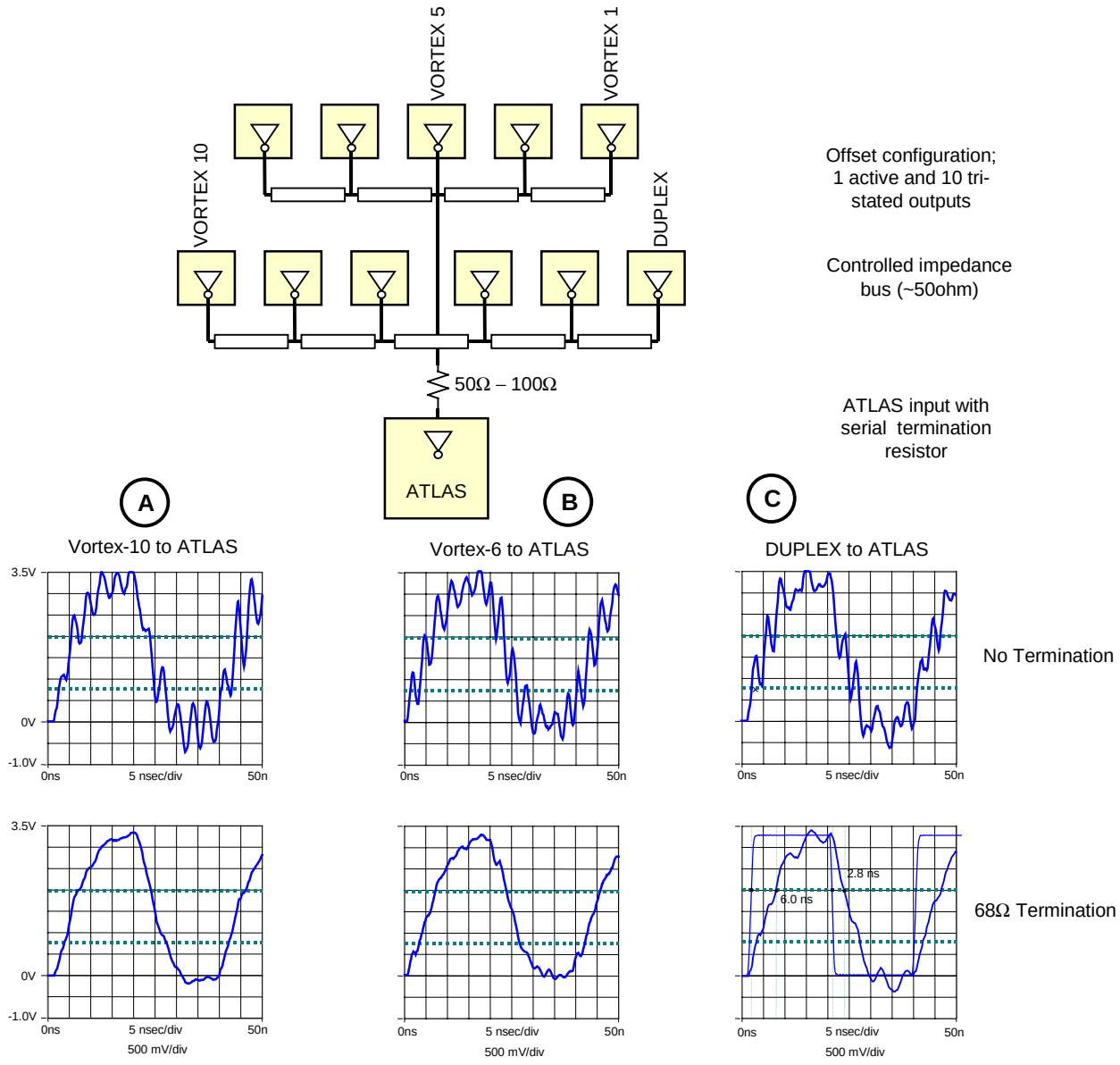


The bus is split into two uni-line sections. The first section connects to five devices and the second one connects to six devices. A short trace with a terminating resistor connects to the S/UNI-ATLAS. The S/UNI-VORTEX/S/UNI-DUPLEX BGA package has the Receive Direction Utopia bus interface placed in the upper right corner of the SBGA package (as shown above). It is natural to have the bus running on that side of the device.

4.4.1 Many-to-single Dual Offset Bus Simulation

FIGURE 26 shows the S/UNI-DUPLEX / S/UNI-VORTEX to S/UNI-ATLAS signals simulated with the dual bus offset configuration.

FIGURE 26. Receive Data Offset Bus Signal Simulation

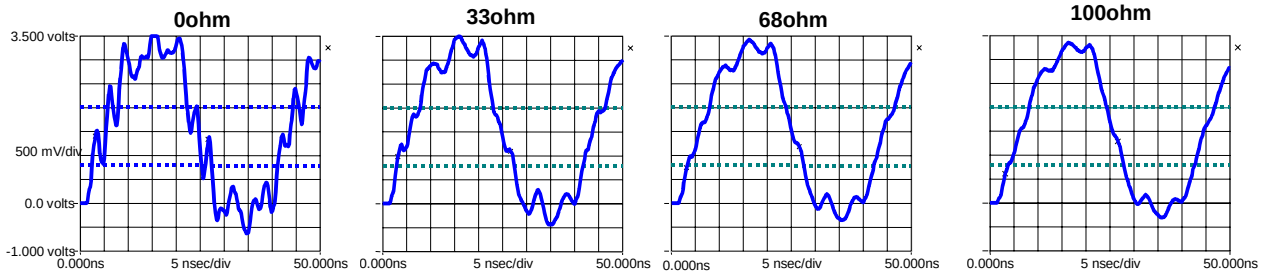


The upper row of graphs presents a signal at the S/UNI-ATLAS without any termination resistors. Each curve has a different driver placement on the bus. Multiple back-reflections are clearly visible. The lower row of graphs is for the 68

ohm serial termination. The simulation shows a monotonic signal and low overshoots/undershoots for all output points. However, all curves are “rounded” with an adverse effect on timing. The most lower-right graph shows hypothetical square wave in comparison to a distorted saw-tooth one. It is clearly visible that timing is shifted by 2.8 to 6.0 ns.

FIGURE 27 shows the simulated signal at the S/UNI-ATLAS versus the termination resistor. The driver for the simulation is the S/UNI-DUPLEX.

FIGURE 27. S/UNI-DUPLEX to S/UNI-ATLAS vs. Termination Resistor

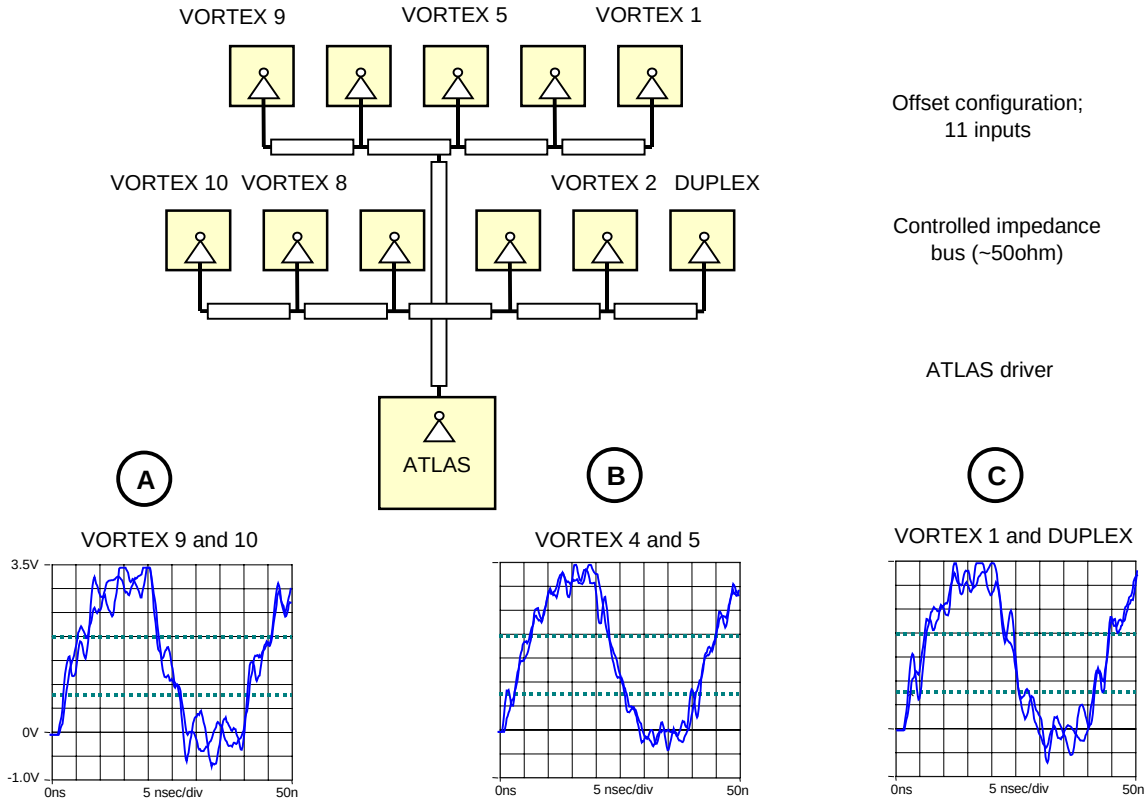


The resistor value between 68 and 100 ohm provides an adequate termination for the monotonic edges and low overshoots/undershoots. The higher the resistor value, the slower the rising and falling edges are, due to the low-pass filter effect. Also, branches split the signal edge energy amplifying the saw-tooth (triangle) effect, as seen in the simulation.

4.4.2 Single-to-many Dual Offset Bus Simulation

The S/UNI-ATLAS to the S/UNI-DUPLEX / S/UNI-VORTEX with a dual bus offset configuration places the S/UNI-ATLAS at the center of the bus. The first simulation is done with the bus placed in a double uni-line configuration. The interface on the S/UNI-VORTEX SBGA is at the center of the right side of the package, and the bus flows naturally along that side. FIGURE 28 shows the offset configuration and simulated bus signals.

FIGURE 28. One-to-many in Dual Bus Offset Configuration



The S/UNI-ATLAS to the S/UNI-DUPLEX / S/UNI-VORTEX simulated signals show multiple back-reflections and non-monotonic edges on all destination points. Each graph shows two waveforms.

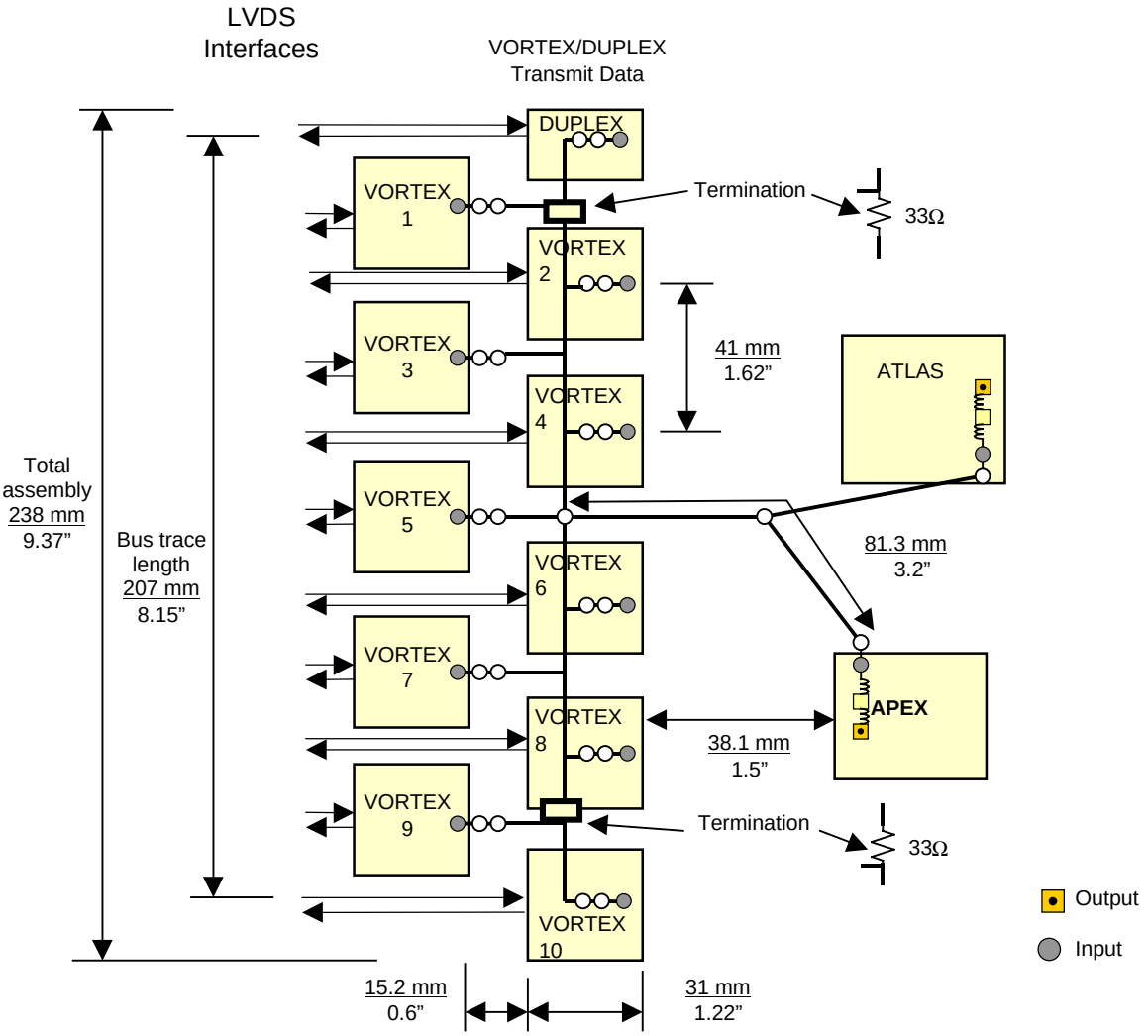
We were unable to find an easy way to implement a termination solution. A configuration with multiple serial termination resistors, distributed along the bus, simulates saw-tooth (triangle) signals with a variable level of non-monotonic edges.

The next exercise is with a redesigned offset bus.

4.5 Utopia and Any-PHY Single Bus Offset Configuration

The bus was changed to minimize the total length of copper traces. FIGURE 29 shows the layout and bus dimensions.

FIGURE 29. Single Bus Offset Component Placement

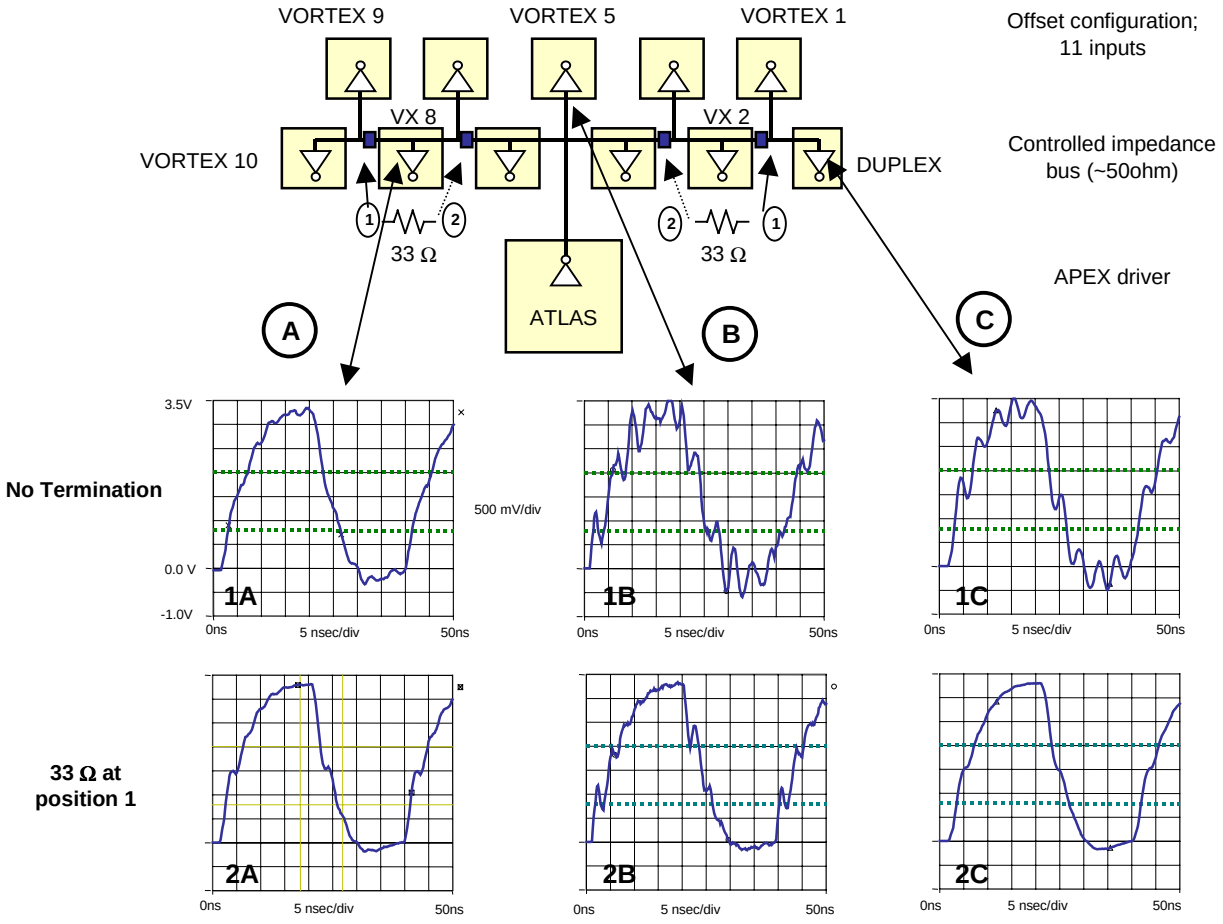


The serial termination resistors were placed symmetrically in both branches of the bus line. The signal was simulated with and without termination resistors. FIGURE 30 shows the simulation results.

The simulation shows an improvement at most destinations with symmetrically placed termination resistors. The middle of the bus S/UNI-VORTEX 5 input has the least significant improvement and shows the non-monotonic edges. The only solution is to insert a serial termination resistor (33 ohm) next to the input. However, the area around the S/UNI-VORTEX 5 is congested with bus lines, and it may be challenging to place multiple termination resistors at that place.

An unexpected minor signal degradation appears at the S/UNI-VORTEX 2 and 8 with the termination resistor, a small bump on the edges at about 1.5 V is visible in the lower row (2A and 2C). The middle of the bus (2B) shows a decrease in ripples.

FIGURE 30. S/UNI-ATLAS in a Single Bus Offset Configuration

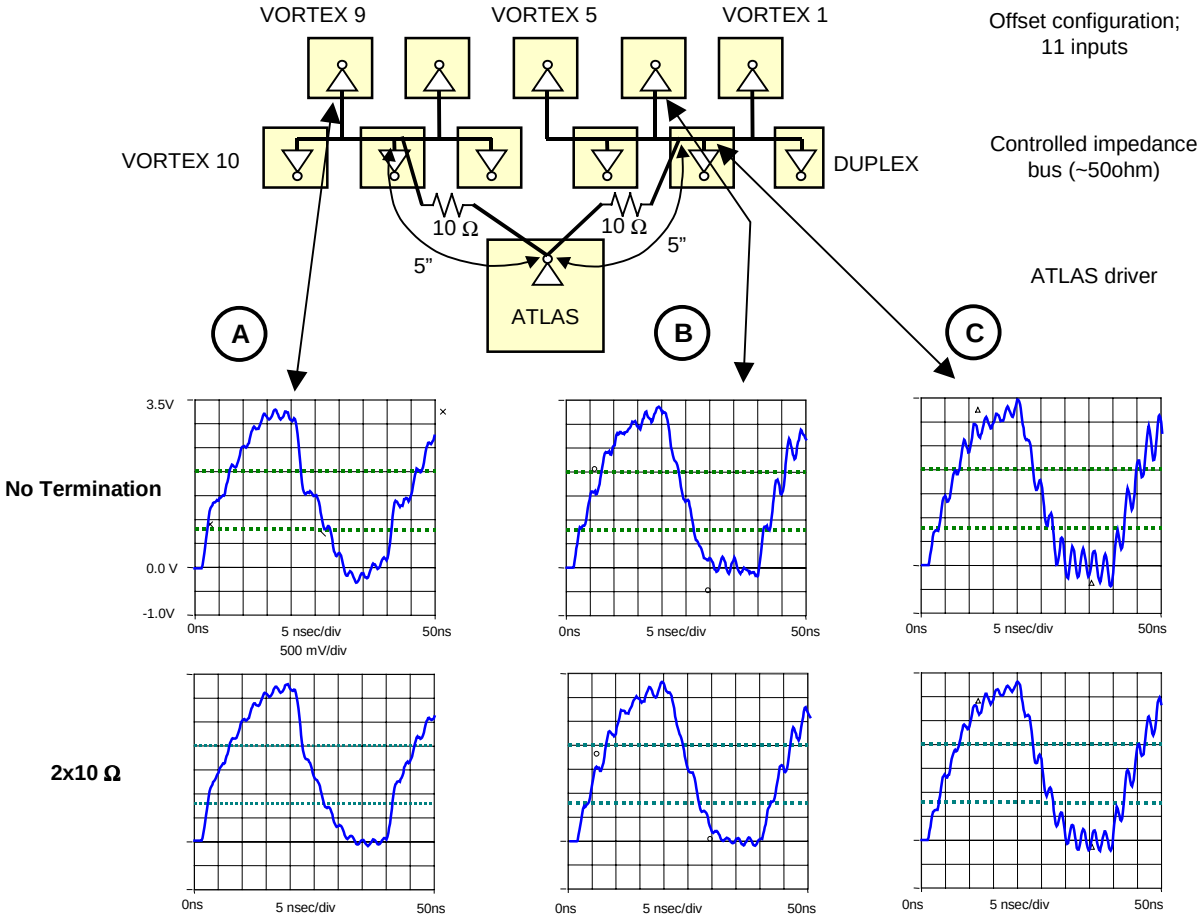


The serial termination resistors in both branches can be placed at position 1 or 2, as shown in FIGURE 30 above. Position 1 is preferable, and position 2 may deliver the signal with slightly higher non-monotonic edges. The symmetry in each bus line has to be maintained. The S/UNI-VORTEX-5 still has the non-monotonic edge.

4.6 Multi-Branch Offset Configuration

The industry nickname for layout with a longer trace branching at a single point is “crow-feet”. This exercise is completed with connections similar to crow-feet, though not exactly the same. The bus is split into two chunks with five and six devices attached. Each set is fed with a five-inch long line and a 10 ohm serial resistor. FIGURE 31 shows the simulation results.

FIGURE 31. S/UNI-ATLAS in Crow-feet Configuration

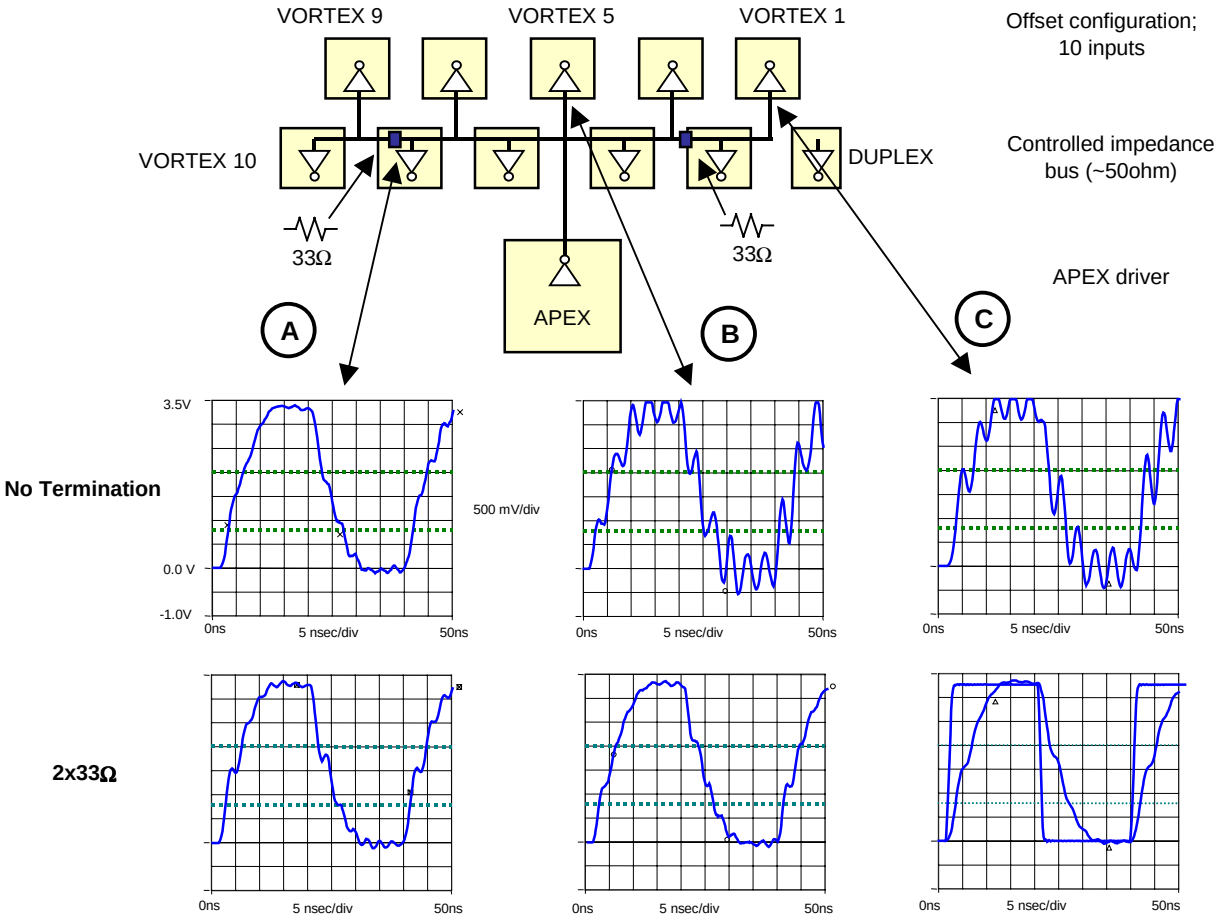


Simulated signals without terminations have less significant bumps than the configuration shown in FIGURE 30. Termination resistors can be increased up to 33 ohm, decreasing the back-reflections and applying a penalty of more saw-tooth like curves. The energy split at the S/UNI-ATLAS output and the dumping effect introduced by inserted resistors decrease the edge speed. Also, inputs near the trunk connection still exhibit significant ringing.

4.7 S/UNI-APEX to Any-PHY Bus

FIGURE 32 shows the S/UNI-APEX driving offset configuration bus.

FIGURE 32. S/UNI-APEX to Bus Simulation



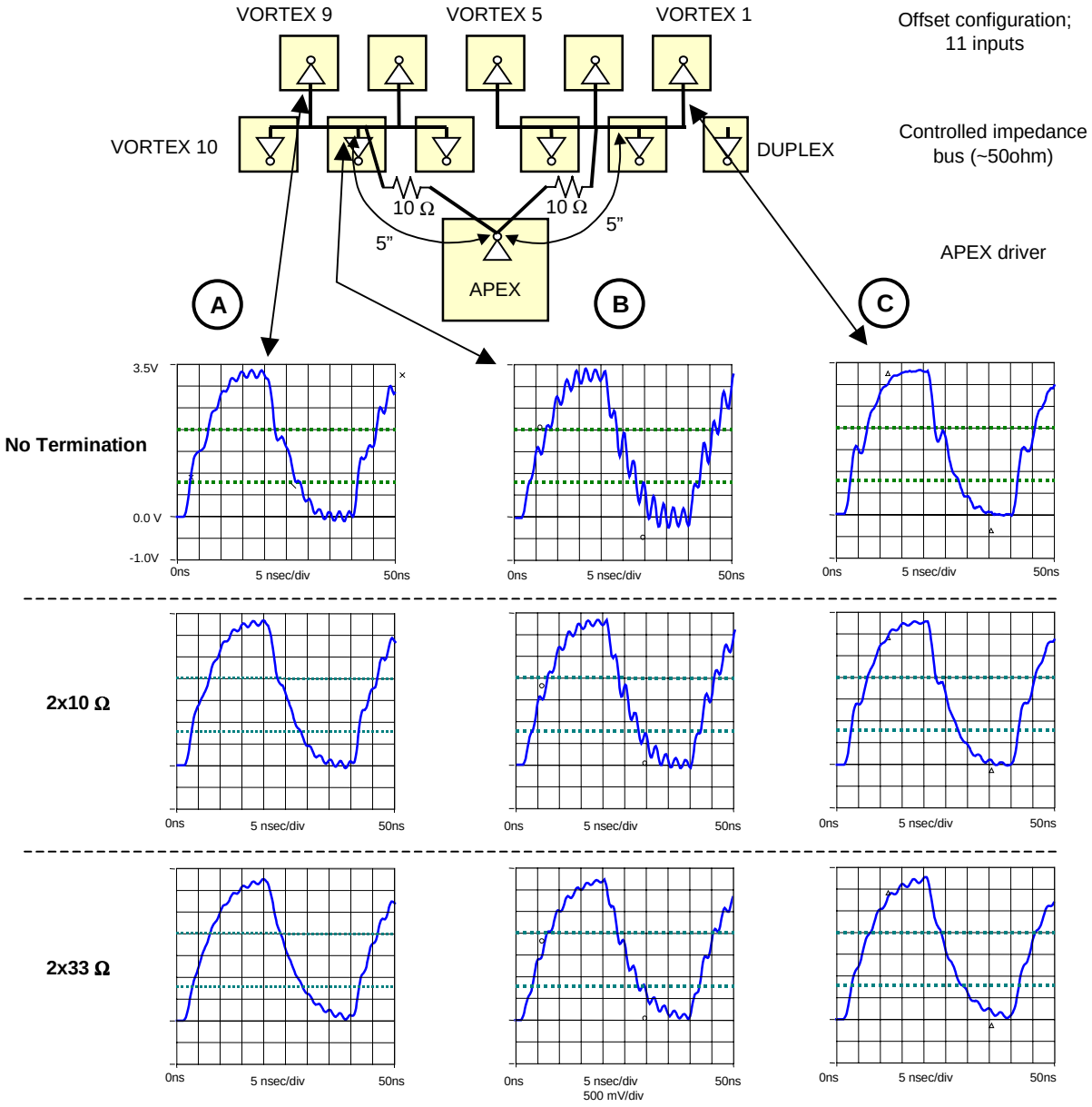
The unterminated simulated waveforms (upper row of graphs) show significant back-reflections and rounded edges. The signal has a visibly better logic high/low plateau than the one shown in FIGURE 30 that has the same configuration with the S/UNI-ATLAS driver. This can be attributed mainly to the higher driving current on the pc3b04 I/O pad. The minor improvement is a smaller number of inputs attached to the Any-PHY bus (the S/UNI-DUPLEX is not connected). Back-reflections are also smaller due to a lower edge speed (see edges and driving current in FIGURE 17).

One of the graphs above shows two curves to visualize signal distortion when an idealized square wave is compared to the simulated wave at the destination point.

A comparison of FIGURE 30 and FIGURE 32 shows that current drive capability is critical to deliver a better signal. Edge speed may have an adverse effect, with faster edges creating higher back-reflections and needing better termination.

FIGURE 33 shows the S/UNI-APEX driving bus in a near-crow-feet configuration.

FIGURE 33. S/UNI-APEX to Any-PHY bus in Crow-feet Configuration



Two five-inch long lines connect to a set of five devices each. Serial resistors dump back-reflections and, at the same time, increase the saw-tooth effect.

A comparison of the graphs from FIGURE 31 and FIGURE 33 shows that the higher current driver (S/UNI-APEX) with a lower edge speed simulates the signal with less bumps in a similar configuration (the more driving capability, the better the wave shape).

The penalty for a high speed and high current I/O pads is increased parallel switching ground cross talk, which may add up to a significant voltage and corrupt data, and can be a serious problem in the high-speed silicon. To maintain signal integrity with lower current I/Os, the solution is to reduce the number of integrated circuits on the bus, or reduce the physical dimensions of the bus (maybe double-sided component placement). Decreasing bus clock speed may ease timing problem, however, backreflections on fast edges will still exist.

Possible solutions: Monotonic edges may be achieved with multiple serial termination resistors distributed across the bus line. That requires a large number of resistors across multiple buses adding easily to hundreds of additional resistors assembled on a board. Buried resistors may help elevate real estate and assembly issues. Buried resistors may increase substantially board price. If progress in PCB technology allows for cost effective solutions, then designer should investigate that technology. However, a decision to implement new technology should be carefully simulated and evaluated before board is laid out and manufactured.

4.8 Clock Distribution Simulation

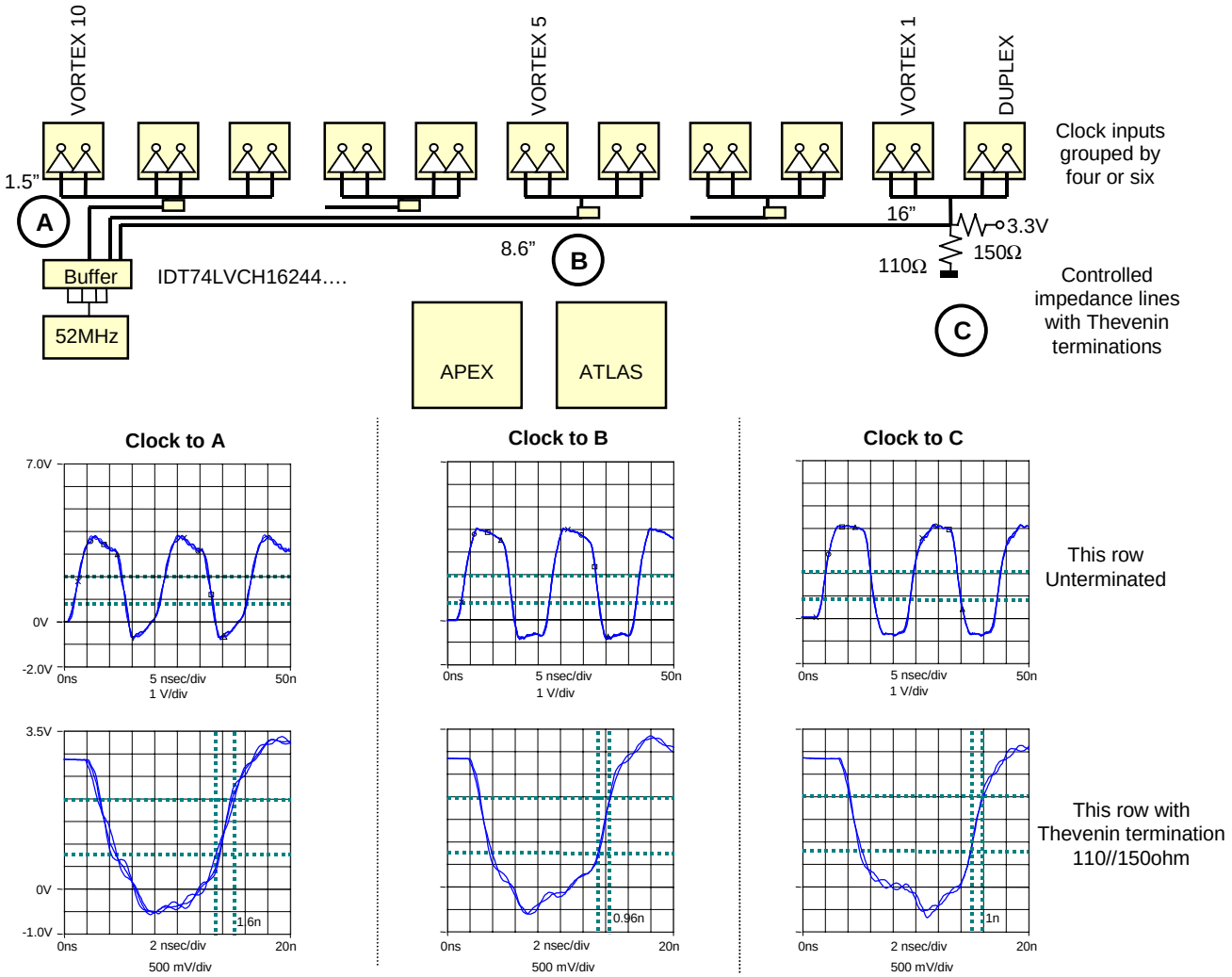
4.8.1 Clock Transmission Line

The clock lines need special attention to provide absolutely monotonic transition between 0.8 V to 2.0 V, and a reasonable margin below and above the logic thresholds without major overshoots/undershoots. To prevent forcing current into the silicon, the overshoot has to be kept within clamping voltage levels.

The clock signal transmission analysis, presented in one of the previous sections, shows that bus-type clock distribution creates an unacceptable shelf on the clock edge. Therefore, we evaluated semi-dedicated clock lines to eliminate shelf distortion. Devices are grouped two or three each, with four or six inputs connected together. The symmetry at the line end is maintained. A single transmission line drives each group. The total number of five clock lines (and five buffers) is required in this configuration.

FIGURE 34 shows the simulated clock distribution circuit for the in-line configuration. The S/UNI-VORTEX / S/UNI-DUPLEX requires two 52 MHz RCLK and TCLK clock signals. Multiple inputs can share the same clock line.

FIGURE 34. Clock Distribution Simulation



The clock is placed arbitrarily on one side of the bus. The clock is buffered with an IDT74LVCH16244 line driver. This placement may require a clock skew adjustment for each line. Each line is terminated next to the T-joint with the Thevenin termination. The simulation shows a clock signal at three different destinations (see FIGURE 34). The upper row shows an unterminated signal with the LineSim ”oscilloscope” set at 1 V/div and 5 ns/div. The lower row shows terminated clocks with the zoom at 0.5 V/div and 2 ns/div for a better view on the clock edges. The simulated clock on all destinations is monotonic with a moderate overshoot/undershoot, with some margin on logic *high* or *low*. Visible waves on the clock edges in column A are most likely from the highest number of

capacitive loads driven (six inputs). The solution is to decrease the number of inputs driven by the specific buffer.

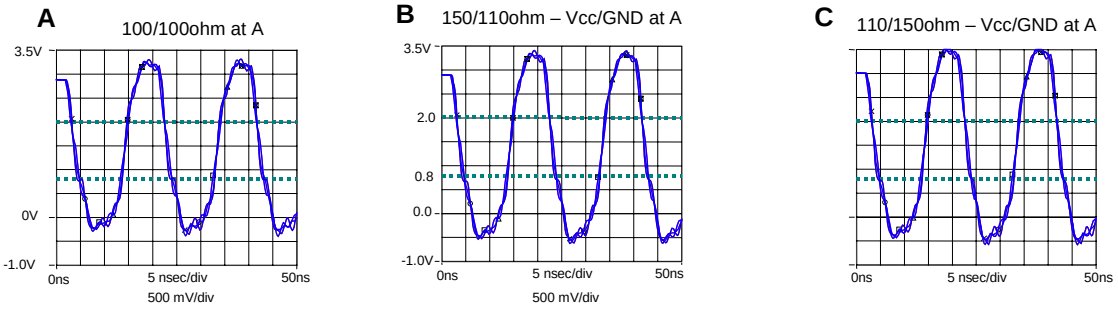
The logic *high* overshoots to about 3.4 V, and logic, and the logic *low* extends to about –0.7 V. The *low* overshoot may generate some current through clamping diodes.

The positive edge transition across 0.8 V to 2.0 V is in a range 0.96 ns to 1.6 ns at different destination points. Clock inputs can be split further into smaller sections to improve edge speed and decrease skew.

FIGURE 34 shows 150 ohm to Vcc and 110 ohm to ground. The equivalent impedance is about 63 ohm. Signals with other combinations of resistor values are shown in FIGURE 35.

CLOCK1 was simulated at the “A” destination as a function of a resistor value in the Thevenin termination. FIGURE 35 shows the simulated curves.

FIGURE 35. Clock signal at A vs. Thevenin Termination



The duty cycle of the clock is set to 55%. Graphs show little change in the signal shape with a different termination. The most visible is the amplitude variation. Graph B shows a logic “low” level that extends to -0.7 V, and this level may force the current through the clamping diodes. Resistor values in Graphs A and C provide better termination.

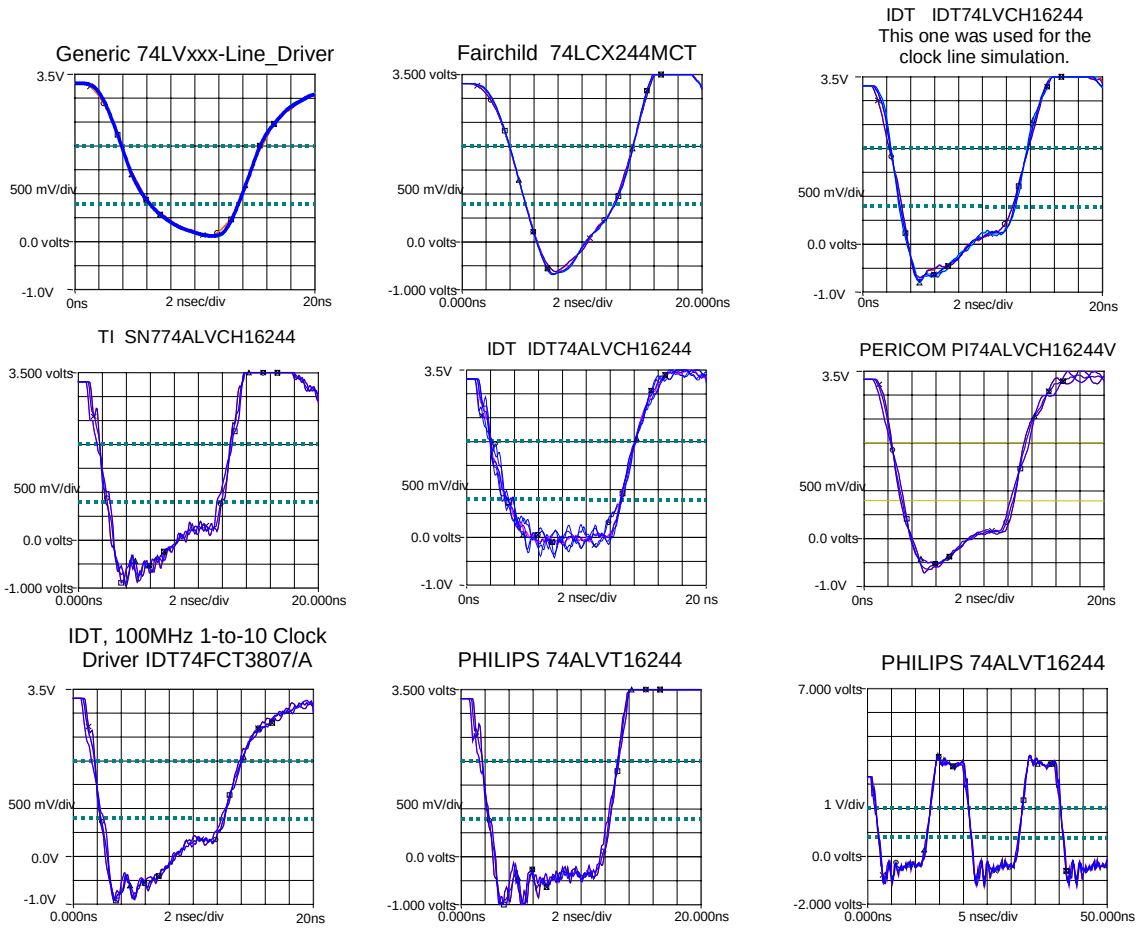
A buffer inserted in the clock/data path introduces propagation delay and edge skew. Slower buffers and ”general purpose” data buffers may not be suitable if bus timing becomes critical.

4.8.2 Buffer Evaluation

While working on the clock line simulation, a number of buffers was tested. A significant difference in signal performance was observed. FIGURE 36 shows the

clock signal versus different line drivers at the “A” destination with an *unterminated* transmission line (shown in FIGURE 34).

FIGURE 36. Clock vs. Line Driver Type on Unterminated Line



The same type of the ALVCH16244 driver, from three major manufacturers, is shown in the second row. The simulation shows a difference in waveforms, which may question the reliability of the IBIS models or compliance with industry standards for the same type of a silicon device. Discrepancies point to a need for performance verification in critical applications, where a new and unknown part is about to be implemented.

The fastest rising edge is simulated with the 74ALVT16244 made by Philips Semiconductor. The signal is shown with two time-bases and gains for better view. The driver is simulated for the clock signal distribution and performed with significantly higher overshoots than the IDT driver shown in FIGURE 35.

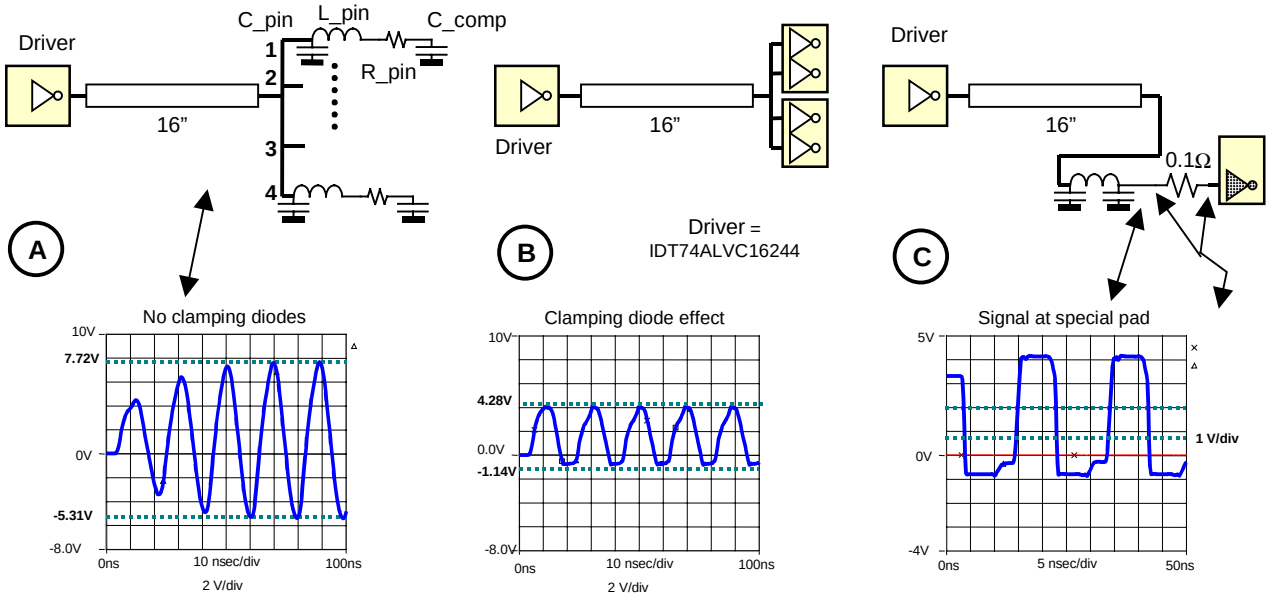
The unterminated signals show monotonic clock edges for most buffers. Signal peaks extend beyond clamping diode ranges on Vcc and ground rails, and a proper termination is needed for most drivers.

NOTE: Both clock edges - rising and falling - must be monotonic without any flat shelves and bumps in the transition region of 0.8 V to 2.0 V.

4.8.3 Clamping Diodes Current

It was mentioned previously, that an overshoot on digital inputs may cause an interference to adjacent I/O pads. This section tries to address the problem by the current simulation at clock input. FIGURE 37 shows the simulation setup and simulation results.

FIGURE 37. Clock Line Current

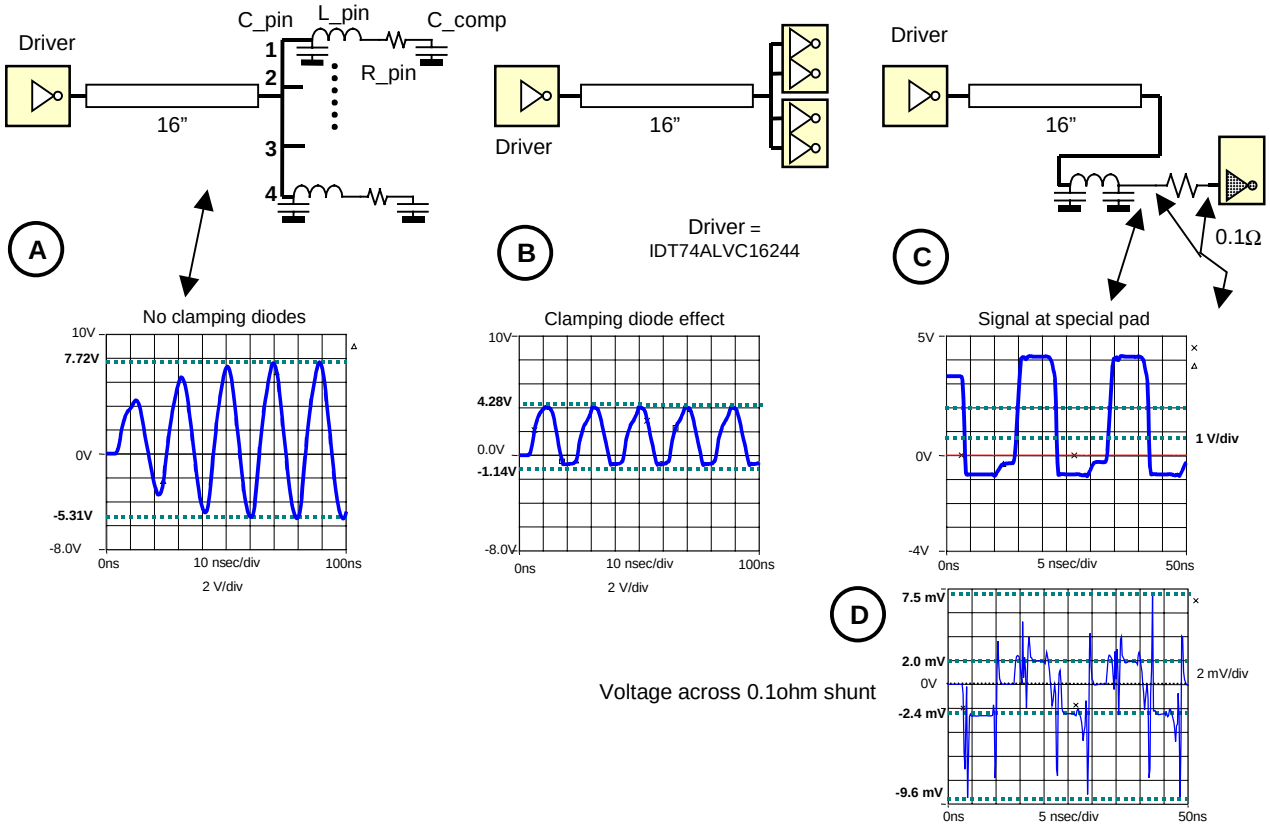


The setup and procedure to visualize and determine the clamping diode current is as follows:

The first setup (A). Four I/O pads, at the end of a 16-inch long transmission line, are substituted with RLC elements equivalent to the IBIS model C_comp, C_pin, L_pin, and R_pin. Clamping diodes are eliminated. The IDT74ALVC16244 buffer drives the transmission line. Graph A shows the simulated circuit behaving as a resonance circuit with signal peaks at –5.31 V and +7.72 V, resulting in a 13.03 Vp-p.

The second setup (B). The S/UNI-VORTEX/S/UNI-DUPLEX devices are placed at the line end. Graph B shows the clock signal suppressed by the clamping diodes. The voltage peaks are at –1.14 V and 4.28 V. The both clamping diodes to Vcc and to ground conduct current.

FIGURE 38. Clock Line Current



The third setup (C). A special I/O pad in the IBIS model was created with minimum values of the parasitic RLC element. The pad is placed as shown at position C in the above figure. A 0.1 ohm current-sensing resistor is placed at the I/O input. The external RLC elements, matching the IBIS model, are inserted before the sensing resistor. As a result, the current flowing through the C_comp and C_pin is not included at the 0.1 ohm serial resistor. Only the clamping diode current creates a voltage drop across the current-sensing resistor.

The simulated current reaches a negative peak at about -96mA and a positive peak at about +75 mA. However, the peaks coincide with signal edges. It is not clear, at this time, if this is attributed to the clamping diode currents. The flat pedestals on graph D converts to about 20 mA and –24 mA. Those levels are

most likely due to clamping diode currents. The highest peaks of the simulated current should not trigger the latch-up condition. The clamping current may cause interference into another data/address lines. The PMC-Sierra 3.3 V 0.35 u devices are tested for I/O pad latch-up, up to 200 mA. Properly designed I/O pads help to minimize the digital crosstalk through the silicon.

The above exercise highlights a need for a proper termination, especially on clock lines with dedicated drivers on each line. The data/address lines, in a bus-type configuration may show significant overshoot peaks due to accumulated capacitive loads and long unterminated traces.

4.8.4 Crosstalk and EMI

The crosstalk and EMI (electromagnetic interference) for the data and clock transmission lines are not simulated in this document. Clock lines tend to create very strong harmonics in the electromagnetic field that may be subject to FCC regulations. The edges of the clock lines are faster than the data lines, which may cause interference to the data lines. Therefore, special care is needed for the clock transmission line layout and termination.

5 DATA SHEET DERIVED TIMING

The following sections present the results for signal integrity and timing simulation using the LineSim (HyperLynx) and Timer Designer (Chronology) software tools. The goal of these exercises is proper calculation of timing margins with unconventional use of IBIS models, simulation tools, and datasheet AC timing.

5.1 VORTEX Chipset Hold and Setup Time

The setup and hold time derived from corresponding datasheets for the VORTEX chipset is shown in FIGURE 39 and FIGURE 40 below. The smallest margin on hold time equal to 0 ns (zero nanosecond), as shown in section A of FIGURE 40, is at the interface with the S/UNI-ATLAS polling S/UNI-VORTEX and S/UNI-DUPLEX. If signal integrity is not included in the timing calculations, bus timing, derived directly from a data sheet, may lead to false conclusions. Timing margins, based on signal integrity, are described in the following sections.

FIGURE 39. VORTEX Chipset Data Sheet Timing

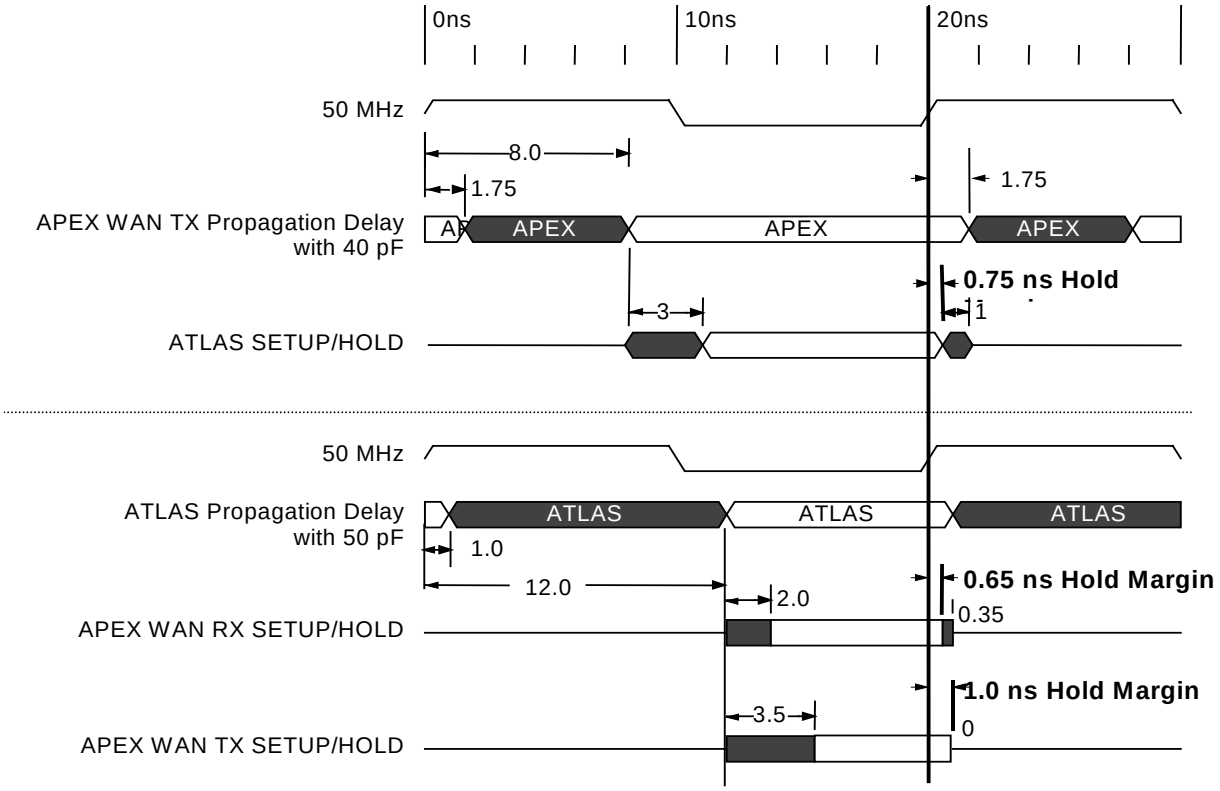
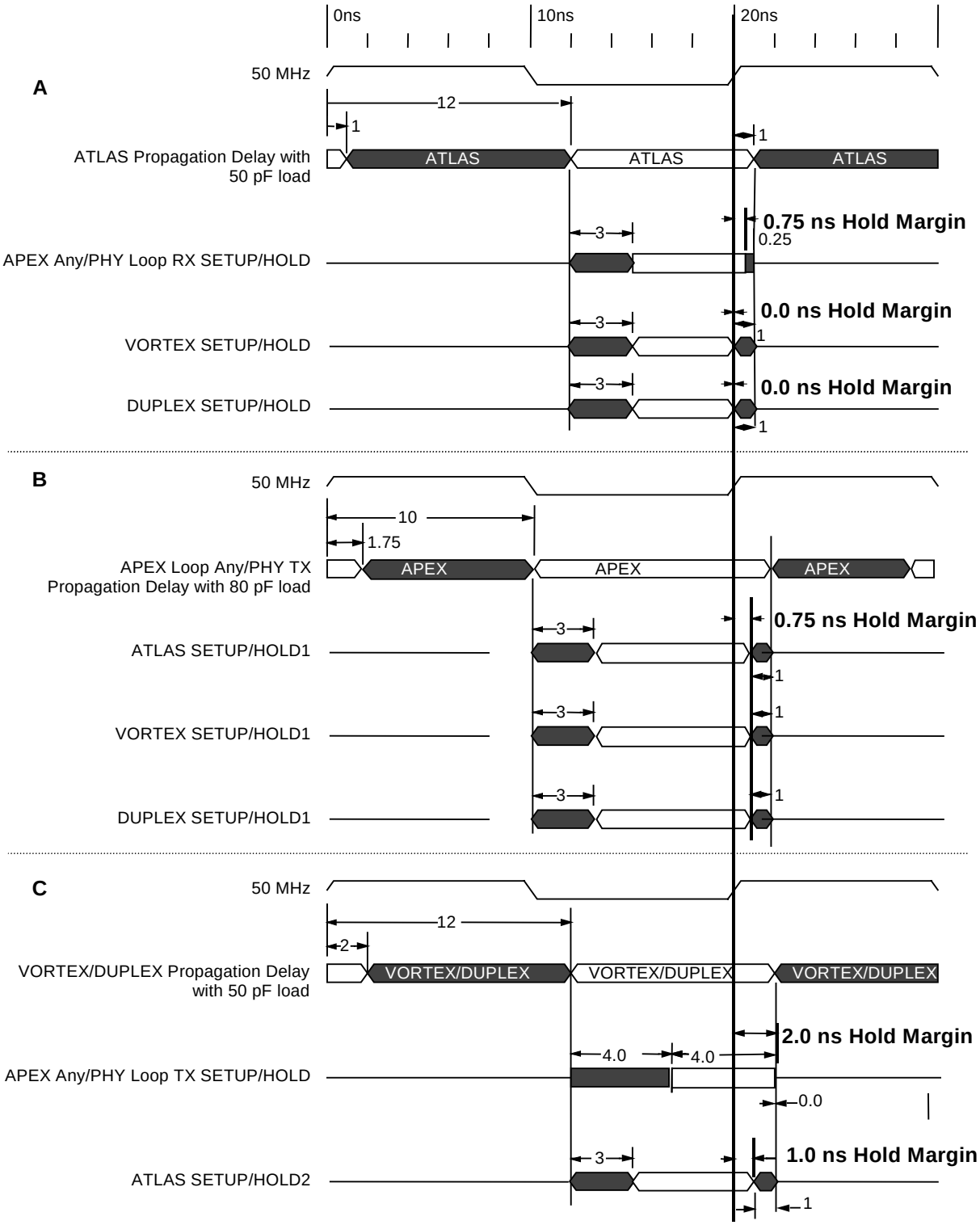


FIGURE 40. VORTEX Chipset Data Sheet Timing



5.2 S/UNI-APEX I/O Drivers

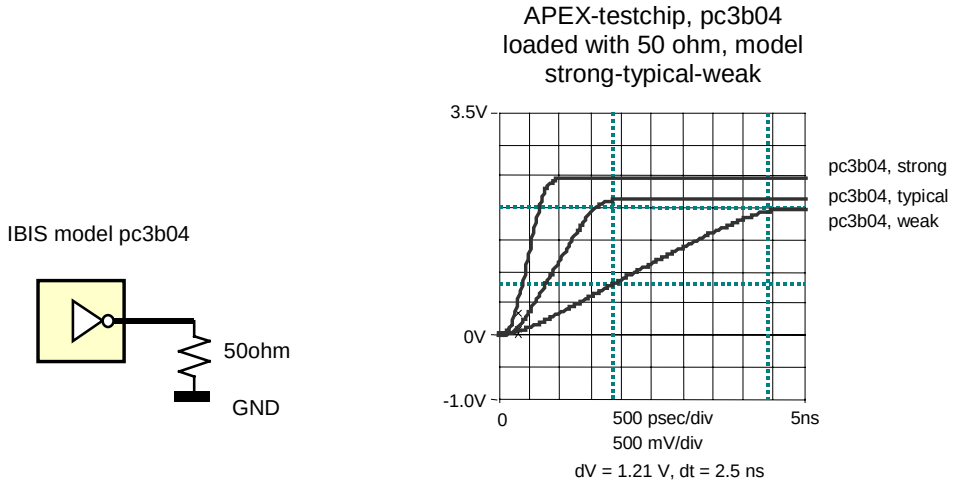
The S/UNI-APEX interfaces are specified in the data sheets as follows:

- Any-PHY TX Loop	80 pF load	52 MHz	pc3b04/pc3t04
- Any-PHY RX Loop	50 pF load	52 MHz	pc3b04/pc3t04
- UTOPIA WAN side	40 pF load	52 MHz	pc3b04/pc3t04
- UTOPIA WAN side	40 pF load	52 MHz	pc3b01
- SSRAM	40 pF load	80 MHz	pc3b04/pc3t04
- SDRAM	20 pF load	80 MHz	pc3t02

The in-line example placement with clock lines is shown in FIGURE 47. An increase in RAM size may deem this placement obsolete. The drawing is done in 1:1 scale and helps to visualize the size of the S/UNI-APEX assembly.

To clarify the simulation process flow, FIGURE 41 shows the S/UNI-APEX I/O pc3b04 pad driving capability (also shown in FIGURE 17).

FIGURE 41. S/UNI-APEX IBIS-typical with 50 ohm Load



This simulation was completed with the IBIS model set at “strong-fast”, “typical”, and “weak-slow”. This pad drives the SSRAM Address (also the Utopia L2 and Any-PHY buses).

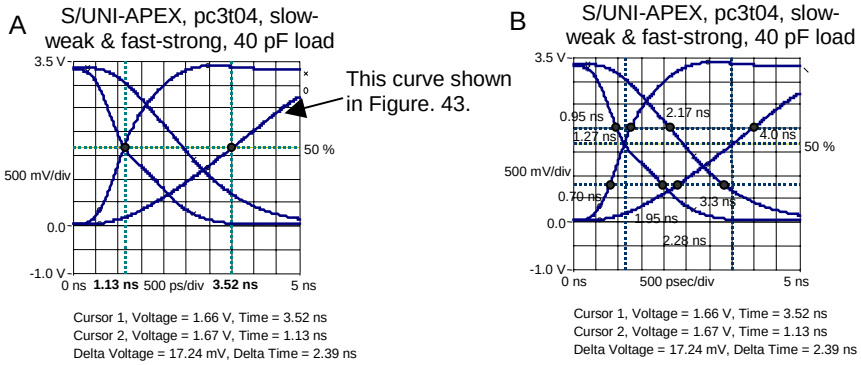
The “strong” IBIS model is created with an I/O performance at –40 C and 3.63 V. The “typical” model is at 25 C and 3.3 V. The “weak” model is at +80 C and 2.97 V.

As expected, the “strong” IBIS model delivers the highest current and the fastest edge. The “weak” model is significantly slower. Variation in edge speed may create timing problems within the operating temperature range.

The S/UNI-APEX data sheet specify timing at 50 % of output swing, what is equivalent to 50 % of the power rail (+3.3 V / 2 = 1.65 V).

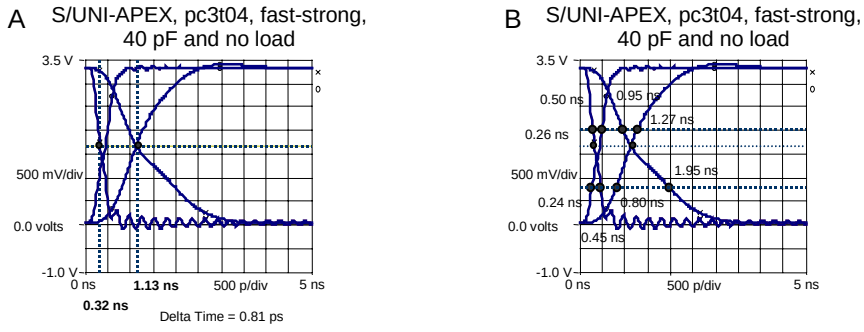
FIGURE 42 shows the IBIS model pc3b04 loaded with 40 pF.

FIGURE 42. S/UNI-APEX pc3b04 loaded with 40 pF



The graph shows the rising and falling edges of the IBIS model slow-weak and fast-strong loaded with 40 pF. Simulation was completed with the capacitor connected to the output without any transmission line and termination resistor. The rising slow-weak edge reaches 50 % at 3.52 ns. The strong-fast edge reaches 50 % at 1.13 ns. Graph B shows timing for TTL logic levels.

FIGURE 43. S/UNI-APEX I/O pc3b04, fast-strong with 40 pF and no load



The 50% crossing points for no load and 40 pF loads are at 0.32 ns and 1.13 ns respectively. The TTL levels timing is shown in graph B.

5.3 S/UNI-APEX- pc3b04/pc3t04 Valid Signal Correction

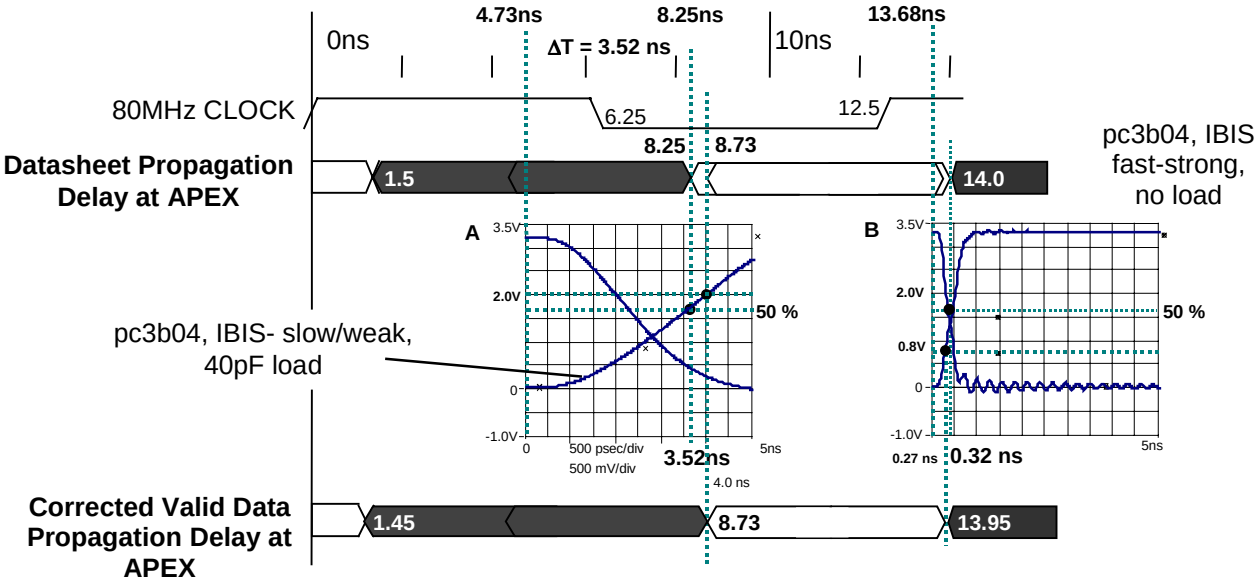
The data sheet derived “Propagation Delay” and “Setup/hold” time needs correction before it can be used for timing simulation based on the bus signal integrity simulation. The following sections try to interpret data sheet AC timing with signal integrity simulation, and to pass collected data to the timing analysis..

The goal of the following exercise is to separate digital circuit delay from I/O pad delay. This is the author’s way of interpreting the data sheet, and designers are encouraged to investigate other ways of interpreting data sheets

5.3.1 S/UNI-APEX with 40 pF Load

The S/UNI-APEX propagation delay TP_{SCLK} for SSRAM interface is specified in the data sheet at 1.5 ns to 8.25 ns, with 40 pF load at the I/O pad, and measured at 50% of the transition. The propagation delay consists of two factors: digital circuit delay and loaded I/O delay. FIGURE 44 shows a graphical representation of those factors at 80 MHz.

FIGURE 44. Propagation Delay for pc3b04 IBIS weak/slow with 40 pF



The LineSim graph A is positioned in such a way that the pc3b04 weak-slow IBIS model loaded with 40 pF (shown earlier in FIGURE 42) crosses the 50% level at the **8.25 ns** mark at the clock scale. The logic *high* valid signal is reached when the curve crosses 2.0 V at the **8.73 ns** mark. A similar procedure applies to the non-valid signal determined around 14 ns on graph B with a fast-strong model and no capacitive load. The 50% line is crossed at 0.32 ns from the IBIS model

start point. The 50% crossing is aligned with the 14 ns mark derived from the data sheet (12.5 ns + 1.5 ns = 14.0 ns). The signal is invalid after 0.27 ns, when the IBIS model slow-weak without load crosses the logic *low* at 0.8 V.

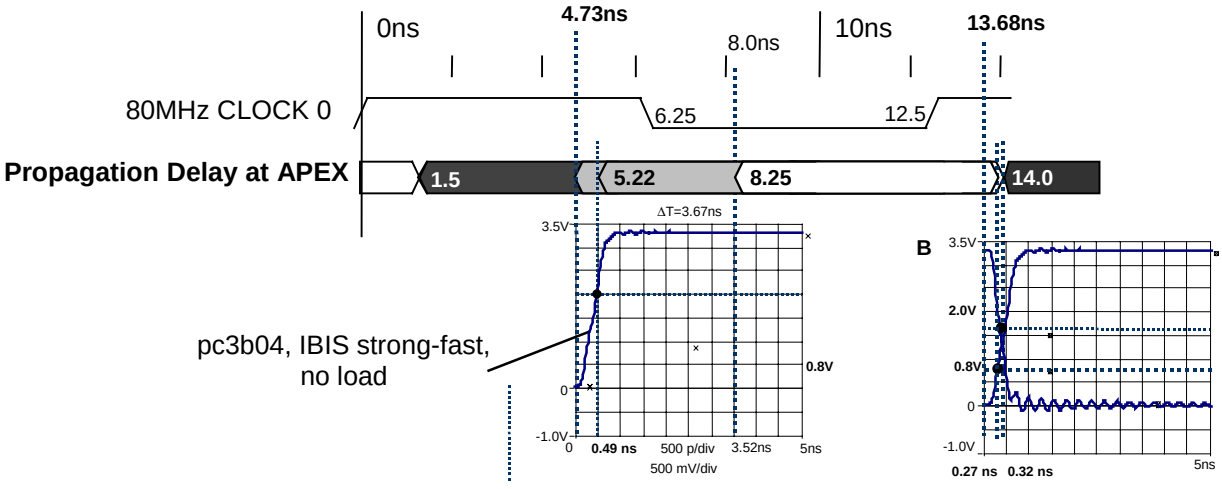
The lower timing bar shows a corrected TTL-level valid data propagation delay, set at **1.45 ns** and **8.73 ns**. The TTL-levels are 0.8 V and 2.0 V. The difference is about 14.0 - 13.95 = 0.05 ns for an invalid signal and 8.73 – 8.25 = 0.48 ns for a valid signal. Those few hundreds of picoseconds may not be critical in one design and may become a major issue in another circuit.

The **4.73 ns** and **13.95 ns** points are important for the timing simulation based on the LineSim simulation. The simulation program starts I/O simulation process at those marks (4.73 ns / 12.87 ns). This also means, that the digital delay must not exceed **4.73 ns**. The S/UNI-APEX meets the digital delay requirement to be less than 4.73 ns. The difference of **3.52 ns** is needed by the slow-weak I/O pad loaded with 40 pF to reach 50 % mark. The I/O also needs 4.0 ns to reach a valid logic level *high*. The 4.73 ns mark is “time-zero” when an idealized digital signal drives the I/O pad *high* (or *low*).

The **4.73 ns** and **13.68 ns** marks are artificially created start points for the LineSim edge that travels along the bus line. Those two points and time differences are entered into timing diagrams (shown later in this document).

FIGURE 45 shows the fast-strong IBIS model loaded with 40 pF that is simulated and aligned with the timing bar.

FIGURE 45. Propagation Delay for pc3b04 IBIS fast-strong with 40 pF



The timing point **4.73 ns**, determined with the previous diagram, is also the start point for the pc3b04 strong-fast IBIS model loaded with 40 pF, even if the strong-

fast charges 40 pF faster. Our understanding is that the 4.73 ns point is the absolutely worst case digital delay (the longest delay) on the S/UNI-APEX device, and no signal edge can start later than that point. The unloaded strong-fast simulation is positioned the same way as on the previous graph. The **13.68 ns** point is the start point for both fast-strong and slow-weak IBIS models.

The 5.22 ns point (shown above) is the valid ADDRESS with unloaded outputs for the IBIS fast-strong model. This point has no importance to timing simulation; however, it visualizes a relatively long valid signal (from 5.22 ns to 13.68 ns) with the fast-strong model.

The pc3b04 IBIS fast-strong and slow-weak models have the artificial start points at **4.73 ns** and **13.68 ns**, which will be used for the timing diagram.

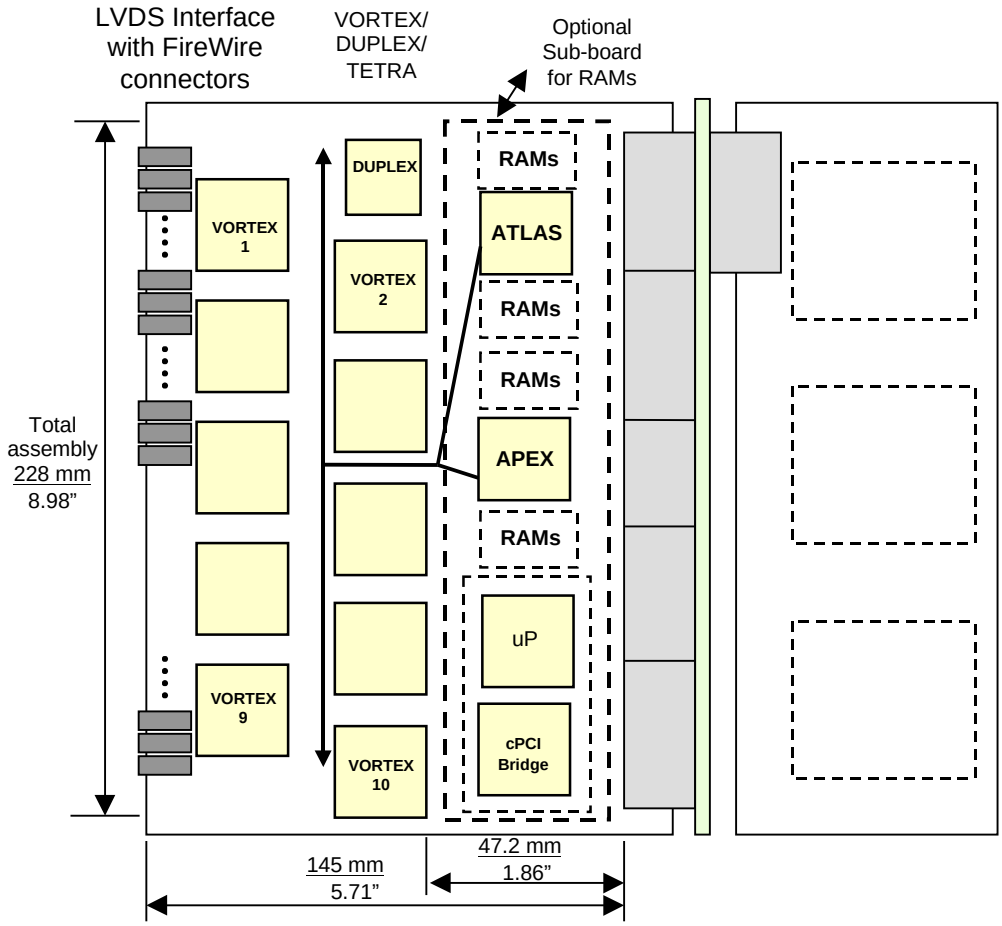
6 S/UNI-APEX RAM INTERFACE SIMULATION

The S/UNI-APEX interface to SSRAM and SDRAM are simulated and the results are described in the following sections.

6.1 Example of Component Placement

FIGURE 46 shows an example of component placement on a standard cPCI card.

FIGURE 46. DSLAM Chipset Placement



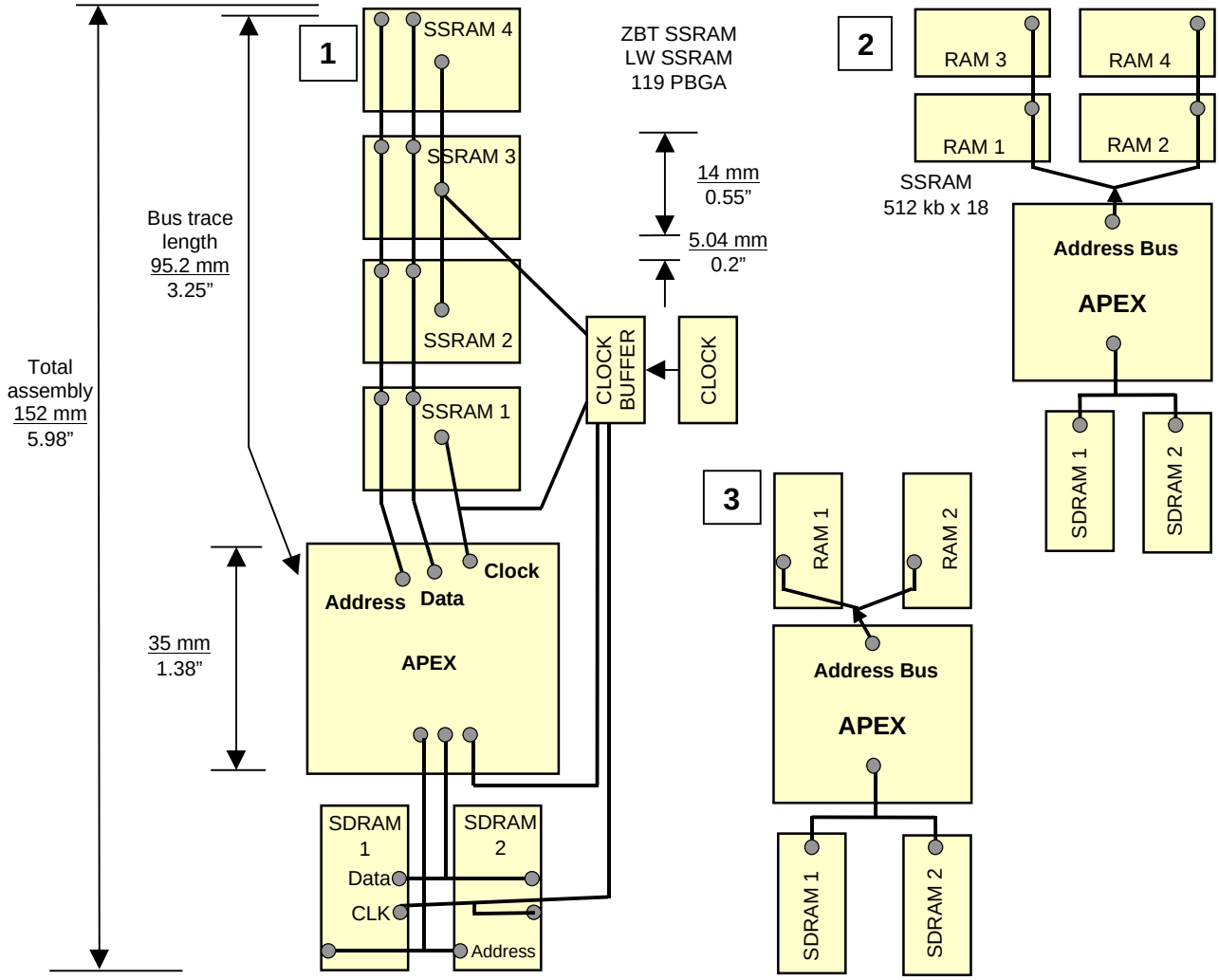
After all the S/UNI-VORTEX and S/UNI-DUPLEX devices are placed, a narrow strip of about 1.89" is left for the S/UNI-APEX, S/UNI-ATLAS and RAM. A high count of components on a board makes it difficult to place all the RAM required for the S/UNI-ATLAS and S/UNI-APEX. The LateWrite or ZBT SRAM and SDRAM associated with the S/UNI-APEX operate at 80 MHz and require special

attention. The 80 MHz RAM should be placed near the S/UNI-APEX. The 50 MHz S/UNI-ATLAS associated with the RAM may have longer traces or be placed on a daughter board with proper serial termination.

6.2 S/UNI-APEX RAM Bus Configuration Examples

FIGURE 47 shows three examples of RAM placement. The Reference Design Core Card has RAMs placed as shown on circuit "3".

FIGURE 47. Example of S/UNI-APEX Interface to SSRAM and SDRAM

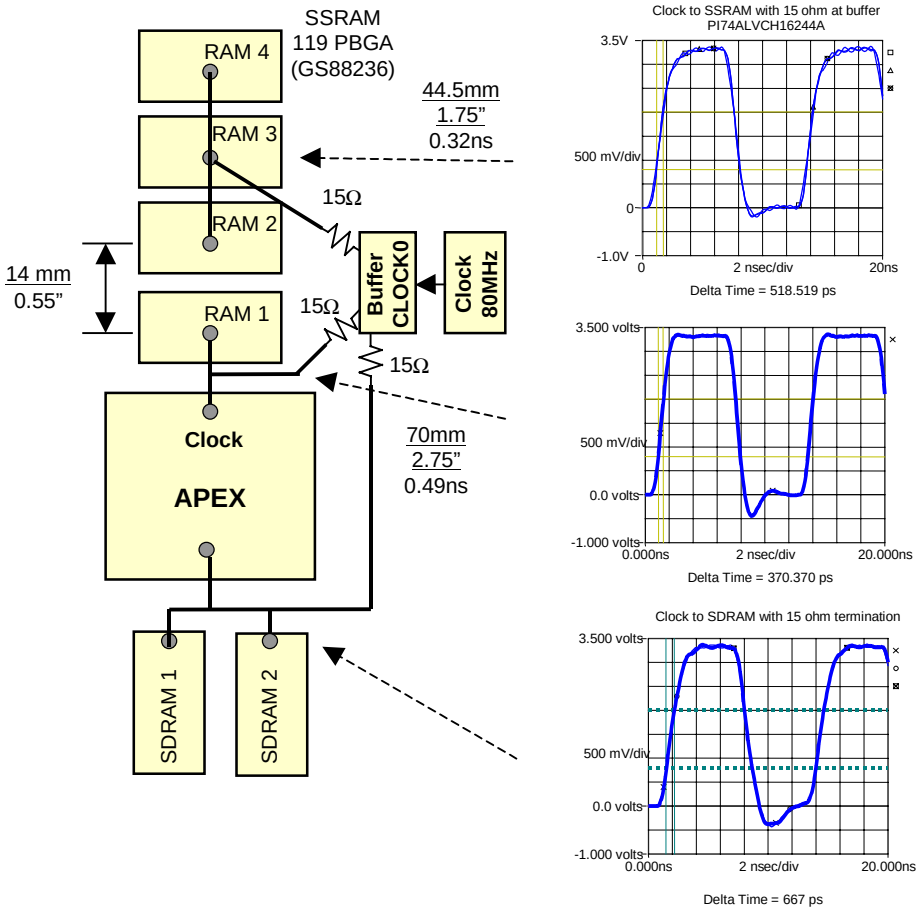


6.3 Clock Signal to S/UNI-APEX and RAMs Simulation

The target for the clock signal integrity simulation is to have monotonic edges and no overshoot exceeding clamping diode ranges, that means for +3.3 V supply rail
3.3 V + 0.6 V = 3.9 V and –0.6 V for logic *low*. The rising/falling edge slope, dV/dt, must be high, between 0.8 V and 2.0 V.

FIGURE 48 shows the results from the clock signal integrity that was simulated at 80 MHz.

FIGURE 48. Clock Simulation at 80 MHz



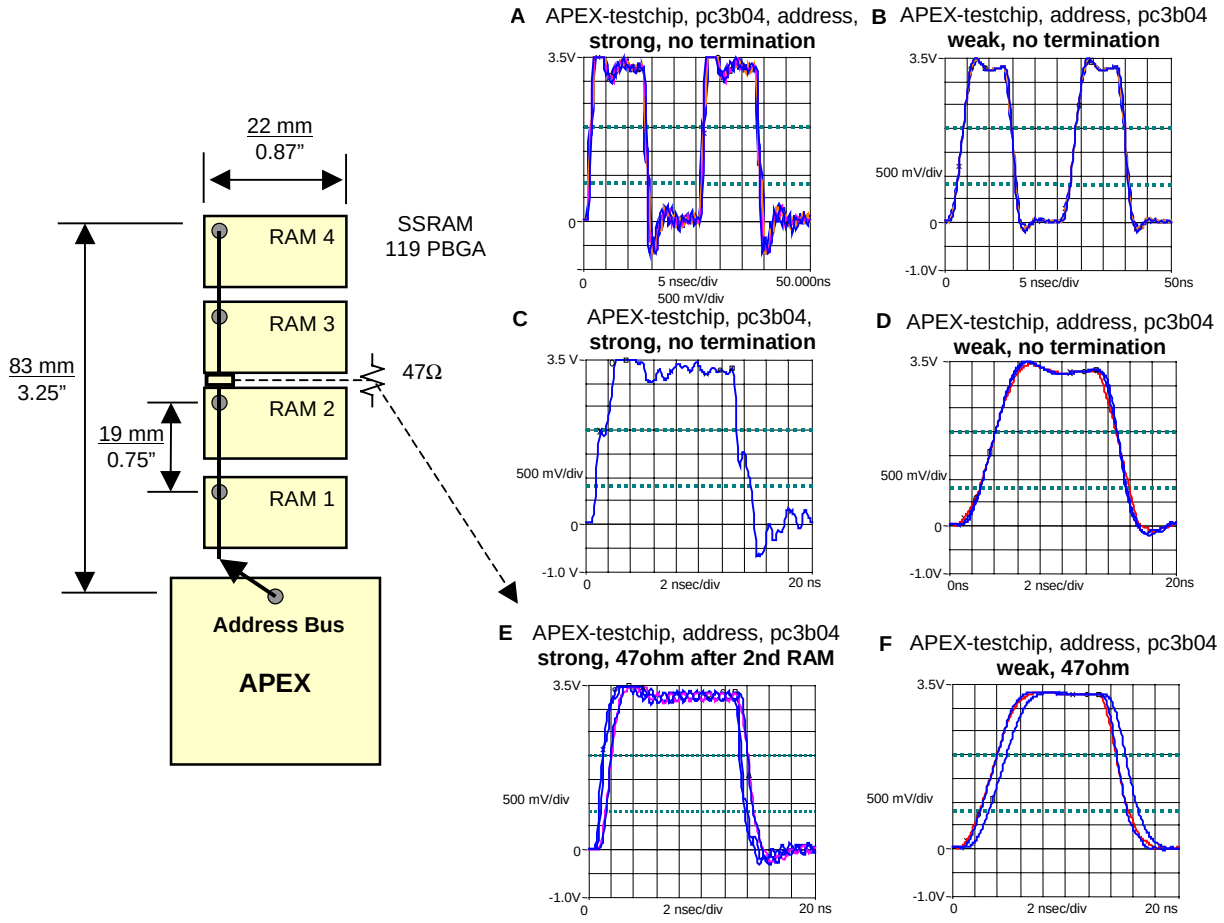
The clock distributed with the buffer shows monotonic edges with a low overshoot. Clock traces to SSRAM interface have a travel time of 0.32 ns. The buffer is PERICOM PI74ALVCH16244A.

6.4 S/UNI-APEX – SSRAM Interface

6.4.1 4x1MB SSRAM In-line Configuration at 80 MHz

The address bus was simulated with a preliminary IBIS model for ZBT SSRAM GS880Z36 from GSI Technology in pipeline mode. The RAM is 256kb x 36 SSRAM (119 PBGA) requiring 4 MB of RAM in four packages. Clock was set at 80 MHz. FIGURE 49 shows the simulation results.

FIGURE 49. Address Bus Simulation for 16MB SSRAM at 80 MHz



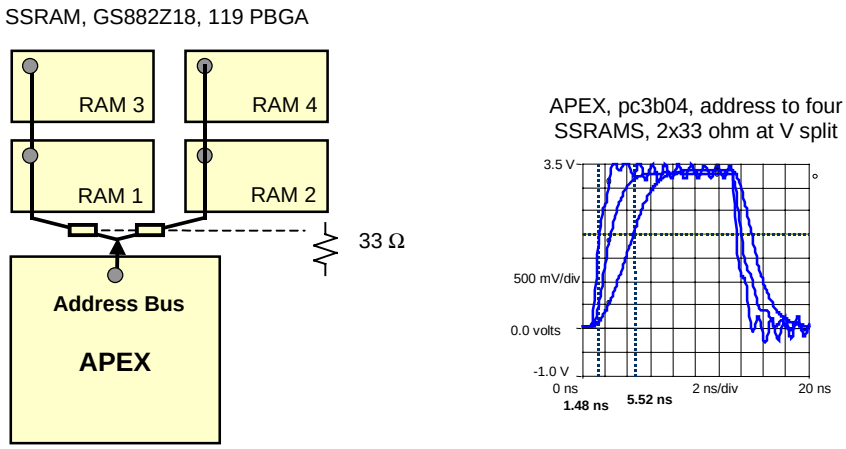
The unterminated strong/fast signals, shown on graphs A and C, have visible bumps on both edges and significant overshoot peaks. The unterminated slow/weak on graphs B and D has very monotonic edges with a minor overshoot. The in-line configuration simulates acceptable ADDRESS signal, as shown on graphs E and F, with the 47 ohm serial resistor after RAM-2.

The DATA from SSRAM to the S/UNI-APEX, in configuration exercised above, with the IBIS model set at strong/fast creates high back-reflections. We were unable to provide a single resistor termination to produce monotonic edges. The DATA bus is bi-directional, adding more difficulties to bus termination. This configuration failed the SSRAM DATA strong/fast simulation.

6.4.2 4x1MB SSRAM Parallel Configuration at 80 MHz

FIGURE 50 shows the placement of SSRAMs in 2 x 2 configuration. This component placement requires each RAM chip size at 512 kb x 18 (GS882Z18). The IBIS model available at the present time is for GS880Z18.

FIGURE 50. ADDRESS to SSRAM

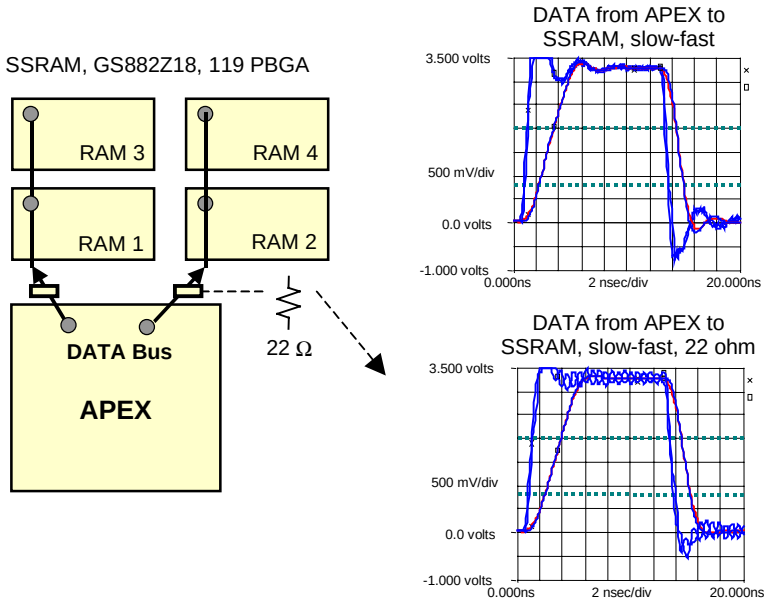


The ADDRESS to SSRAM is simulated with a moderate edge overshoot and almost monotonic edges even without any termination resistor. Graph shown above is for two 33 ohm serial termination resistors. Minor bumps are visible on falling edges near logic *low* – it should be acceptable for most applications.

The DSLAM Core Card Reference Design [4], built with RAM1 and RAM2 only, uses a single serial resistor to reduce back-reflections. Address trace is laid out with T junction.

FIGURE 51 shows the DATA bus from S/UNI-APEX to SSRAM.

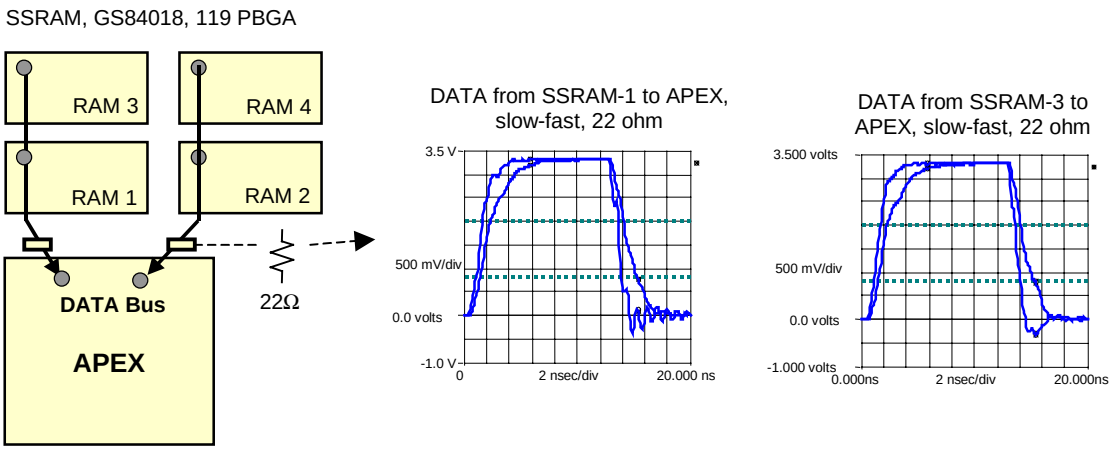
FIGURE 51. DATA from S/UNI-APEX to SSRAM



The DATA from the S/UNI-APEX to SSRAM needs a serial resistor to prevent signal overshooting with the IBIS fast-strong model. The serial resistor 22 ohm provides some termination. The higher value may be needed to eliminate waves at *high* and *low*.

The DATA from the SSRAM to the S/UNI-APEX must have a 22 ohm resistor inserted, as shown in the simulation in FIGURE 51. FIGURE 52 shows the simulated DATA signal on the bus from the SSRAM to the S/UNI-APEX.

FIGURE 52. DATA from SSRAM to S/UNI-APEX



DATA at the S/UNI-APEX simulates monotonic edges with 22 ohm serial resistor.

If the temperature and supply voltage range generates a fast-strong performance of the I/O pad, the simulations will need a serial termination resistor. The DSLAM Core Card Reference Design [4], with RAM1 and RAM2 only, has no serial termination resistor, as we do not expect a fast-strong I/O performance on our card (central office and lab environment/temperature range). Designers are encouraged to evaluate the signal integrity for the full range of IBIS models, from slow-weak to fast-strong.

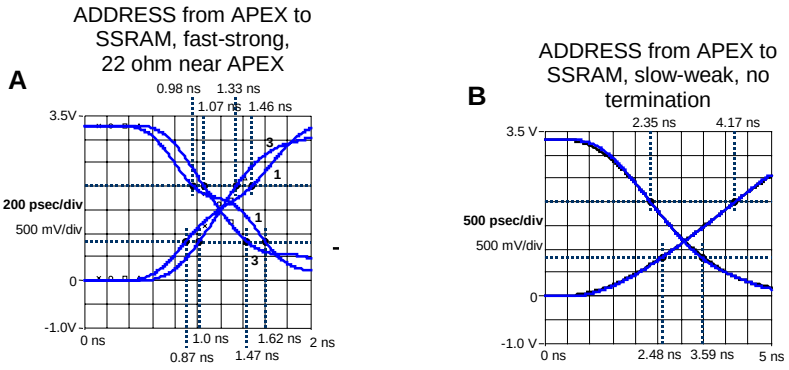
6.5 S/UNI-APEX – SSRAM Timing

The S/UNI-APEX – SSRAM bus timing requires proper edge timing and valid signal correction. That can be derived form a simulation. The components are configured as shown in FIGURE 50, FIGURE 51, and FIGURE 52 (2 x 2 SSRAM) and timing is described in following sections.

6.5.1 S/UNI-APEX – SSRAM Edge Timing

The timing simulation for ADDRESS / DATA needs edge delays derived from simulation. FIGURE 53 shows the zoomed edge delays.

FIGURE 53. ADDRESS to SSRAM, strong/fast, weak/slow



Graph A shows that the signal at SSRAM-1 (marked 1) is reaching logic *low* and *high* later than the SSRAM-3 (marked 3) placed further on the bus. This phenomenon is due to back-reflections and a wave on the rising/falling edges. The slow-weak signal is about the same for all SSRAMs.

FIGURE 54 and FIGURE 55 show edge timing for DATA from SSRAM at the S/UNI-APEX (with a 22 ohm serial termination).

FIGURE 54. DATA from SSRAM-3 at the S/UNI-APEX

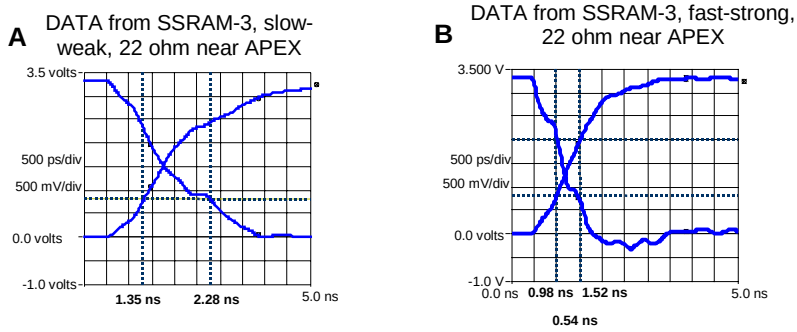


FIGURE 55. DATA from SSRAM-1 at the S/UNI-APEX

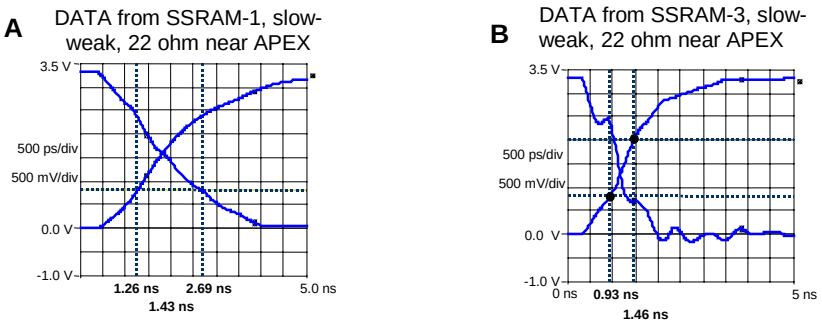
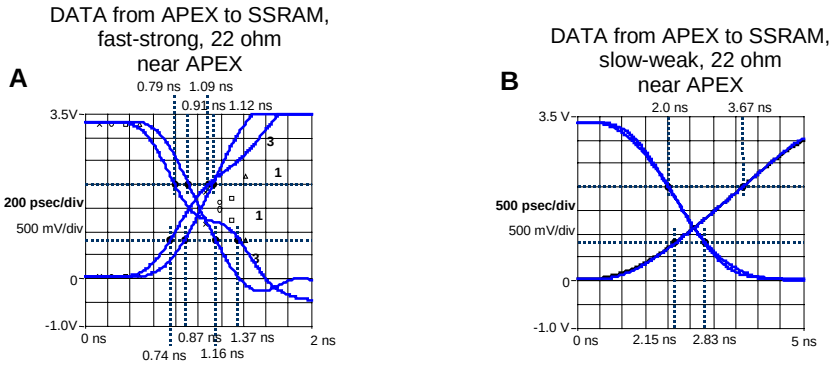


FIGURE 56 show edge timing for DATA from the S/UNI-APEX at SSRAM-3 with a 22 ohm serial termination.

FIGURE 56. DATA at SSRAM slow-weak and fast-strong with 22 ohm



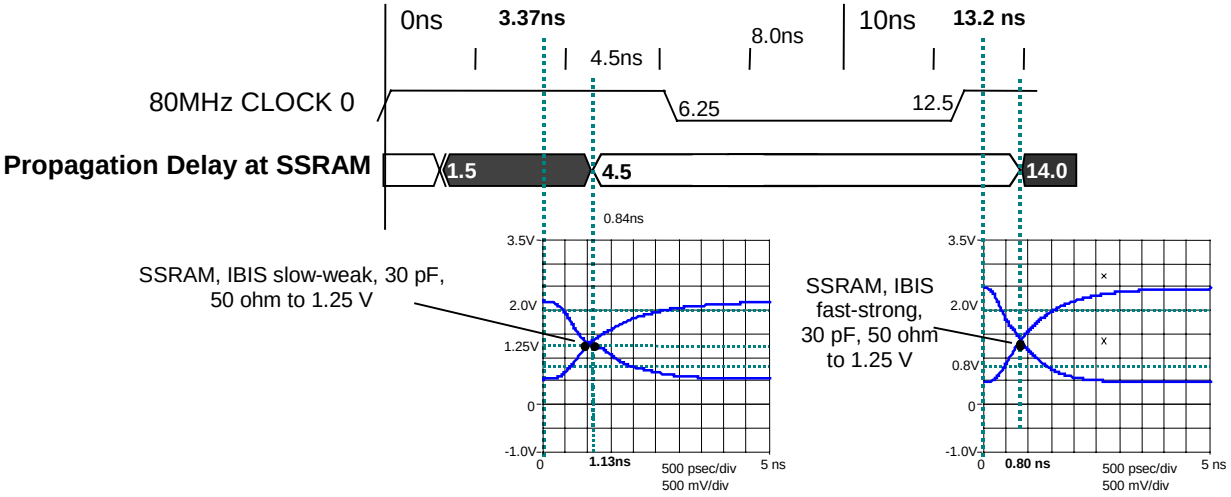
Edge delays are derived from the figures above. We are now ready to do timing on ADDRESS to SSRAM and DATA to S/UNI-APEX.

6.5.2 SSRAM Valid Signal Correction

The AC timing for the SSRAM devices is specified with 30 pF and 50 ohm to 1.25 V. The logic threshold is set at 1.25 V. This differs from the S/UNI-APEX load model that is of a pure capacitive type with a logic threshold at 50 % of Vdd. Also, the SSRAM data sheet does not specify a different load for maximum and minimum propagation delay - it is completed in the S/UNI-APEX, where the maximum propagation delay is with 40 pF and the minimum propagation delay is with 0 pF.

The minimum propagation delay is determined with SSRAM IBIS fast-strong loaded with 30 pF and 50 ohm to 1.25 V. This may be the worst case, however, unless timing is clearly stated in the data sheets with the minimum and maximum load, we decided to use that approach. FIGURE 57 shows the timing diagram and LineSim graphs for the SSRAM DATA output IBIS fast-strong.

FIGURE 57. SSRAM DATA output IBIS-weak/slow with 30 pF/50 ohm



The SSRAM IBIS models slow-weak and fast-strong have the artificial digital reference points at **3.37 ns** and **13.20 ns**. This means the adjusted (artificial) propagation delay for the SSRAM is from 0.7 ns to 3.37 ns. Bus timing is determined using that adjusted propagation delay, plus the delay from I/O, and signal propagation over a copper trace.

6.5.3 Timing Diagram for 2 x 2 SSRAM Configuration

FIGURE 58 shows the results of the timing correction values that are entered into the timing diagram. The timing is done with no termination on the ADDRESS line and with a 22 ohm serial termination on the DATA bus.

FIGURE 58. S/UNI-APEX to SSRAM-1 with IBIS slow-weak at 80 MHz

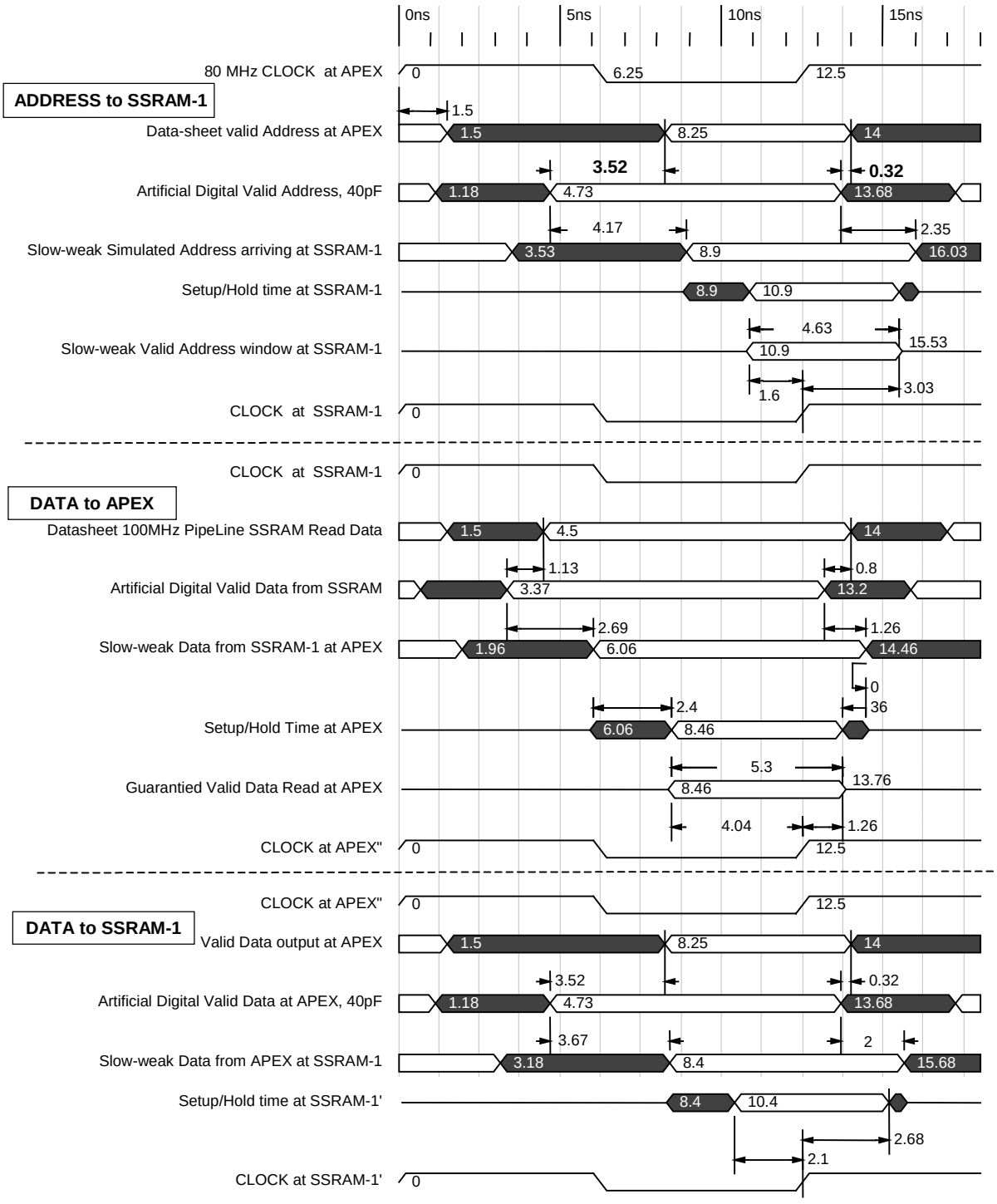
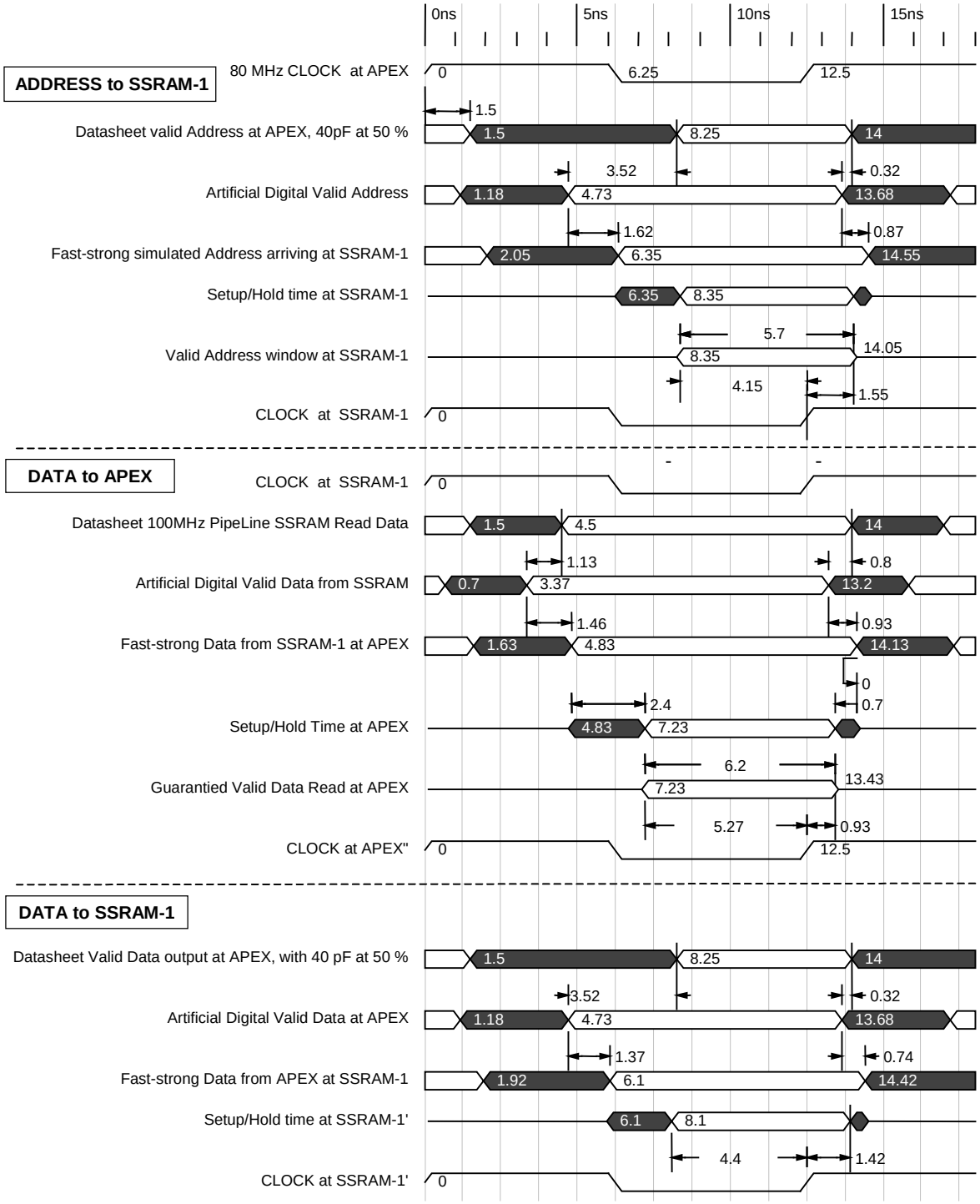


FIGURE 59 shows the S/UNI-APEX - SSRAM fast-strong timing.

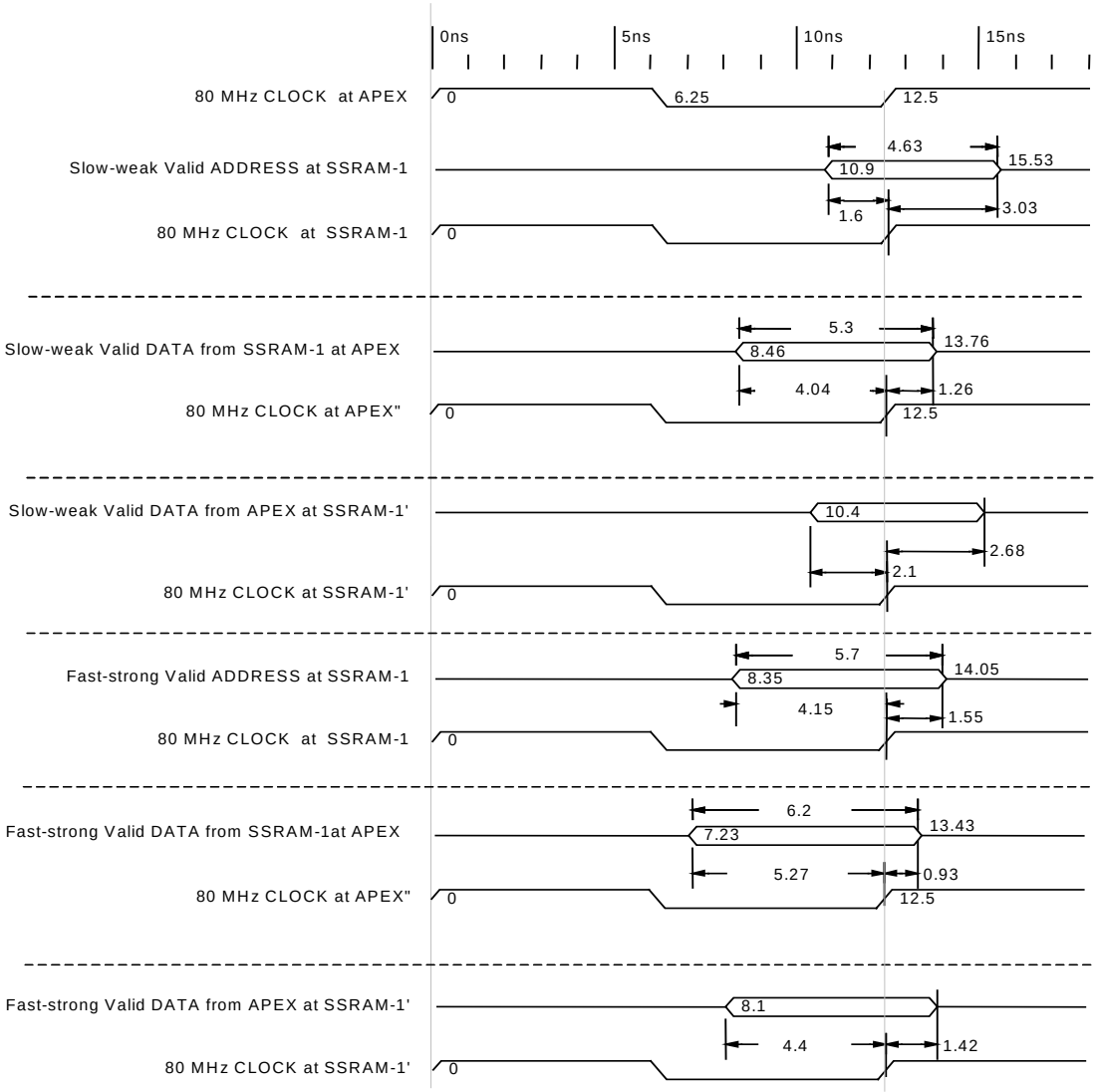
FIGURE 59. S/UNI-APEX to SSRAM-1 with IBIS Fast-strong at 80 MHz



6.5.4 Timing Summary for 2 x 2 SSRAM Configuration

FIGURE 60 shows the summary of the timing diagrams shown in 0 and in FIGURE 59. This applies to the 2 x 2 SSRAM offset configuration.

FIGURE 60. Timing Summary for SSRAM-1 with IBIS slow - fast



The timing above shows only the valid data or address sequence after subtracting the setup and hold time. The timing chart is based on signal simulation and corrected data sheet timing for the S/UNI-APEX. The SSRAM1 interface shows appropriate margins at weak/slow and strong/fast simulations. The smallest margin, **0.93 ns**, is at the bottom of the drawing with timing named

"Fast-strong Valid DATA from SSRAM-1 at APEX". Other timing diagrams show at least 1.26 ns margins.

It is important to observe that the above timing calculations do not include any clock edge degradation, such as: clock skew, jitter, and power/ground noise. Also, the clock is timed as a perfect transition. In a real circuit, the TTL level transition from 0.8 V to 2.0 V on a clock edge can be as long as 2 ns, which significantly decreases timing margins.

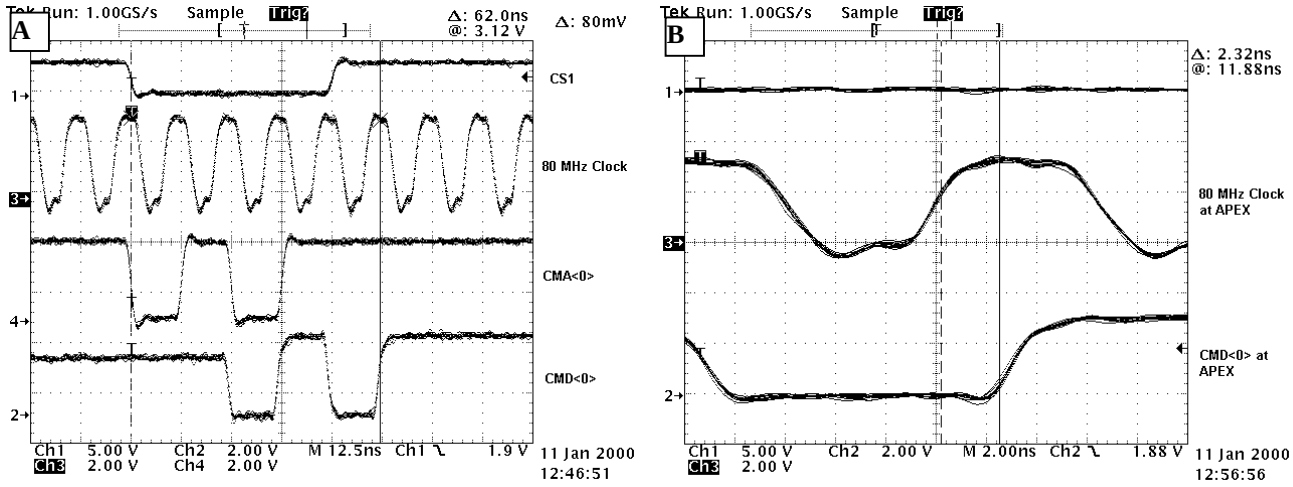
Power noise and crosstalk is not included in timing simulation.

FIGURE 61 and FIGURE 62 show examples of measured waveforms.

IMPORTANT NOTE: The waveforms are obtained with a circuit limited to two ZBT SSRAM chips. This circuit is shown in the DSLAM Core Card Reference Design document [4].

FIGURE 61 shows a read from the SSRAM to the S/UNI-APEX.

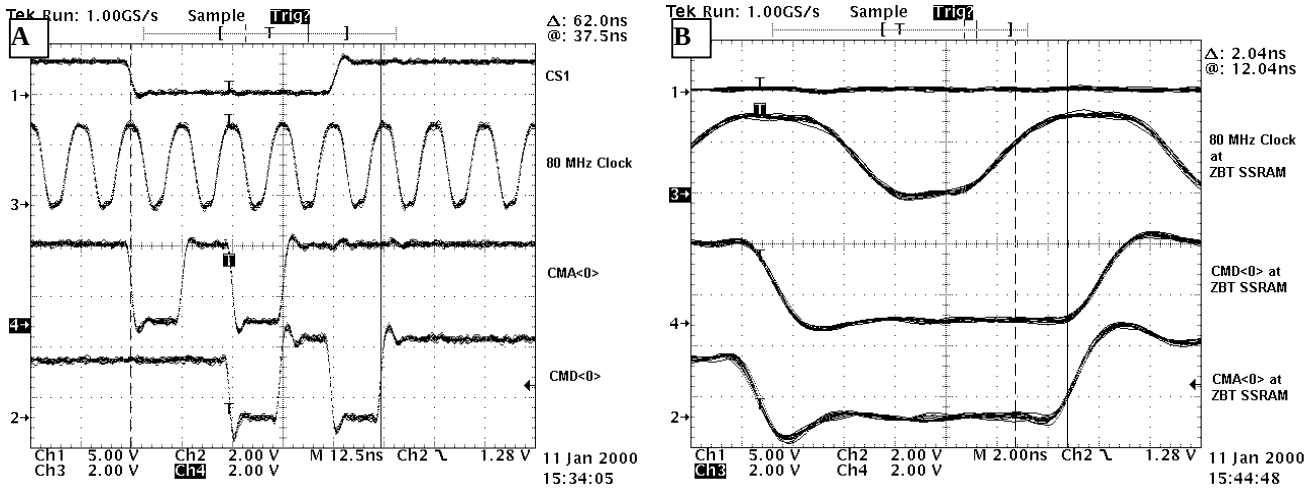
FIGURE 61. Waveforms at S/UNI-APEX at 80 MHz



Graphs A and B show curves that are derived through the accumulation of ten consecutive reads from the ZBT SSRAM. The signal integrity is appropriate for this interface. The timing margin, shown in graph B, at 2.32 ns, leaves plenty of room for a 0.7 ns hold time that is specified in the S/UNI-APEX data sheets.

FIGURE 62 shows a write from the S/UNI-APEX to SSRAM.

FIGURE 62. Waveforms at ZBT SSRAM at 80 MHz



Graphs A and B show curves that are derived through the accumulation of ten consecutive writes to the ZBT SSRAM. The signal integrity, compared with the previous graphs, shows higher overshoots on the data lines CMD<0>. This is due to a lower current and higher speed delivered by the S/UNI-APEX I/O drivers. The signal integrity can be tested by using different serial termination resistors. The current design uses 22 ohm resistors. The timing margin, which is at about 2 ns and shown on graph B, leaves plenty of room for a 0.5 ns hold time that is specified in the GSI ZBT SSRAM data sheets.

The clock in FIGURE 62 graph B is more “rounded” then in FIGURE 61 graph B, as it drives two RAM clock pins. The faster edges can be generated using separate drivers connected to each clock input. Separate drivers may introduce an edge skew.

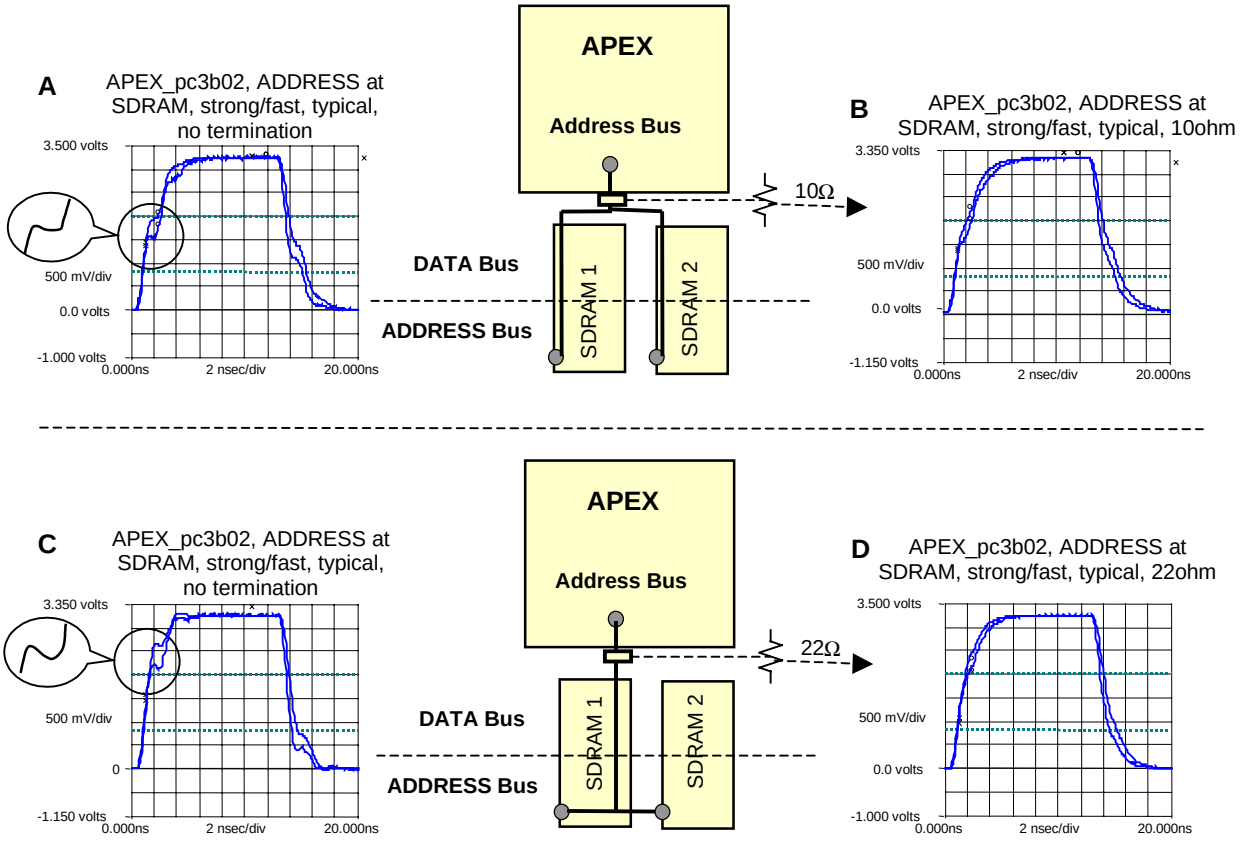
6.6 S/UNI-APEX - SDRAM Interface

The S/UNI-APEX to SDRAM signal integrity and timing margin calculation is not shown in this document. It can be completed in the same way as it is completed for the ZBT SSRAM interface.

Preliminary simulation shows some signal degradation and a need for serial termination resistors as shown in the figures below.

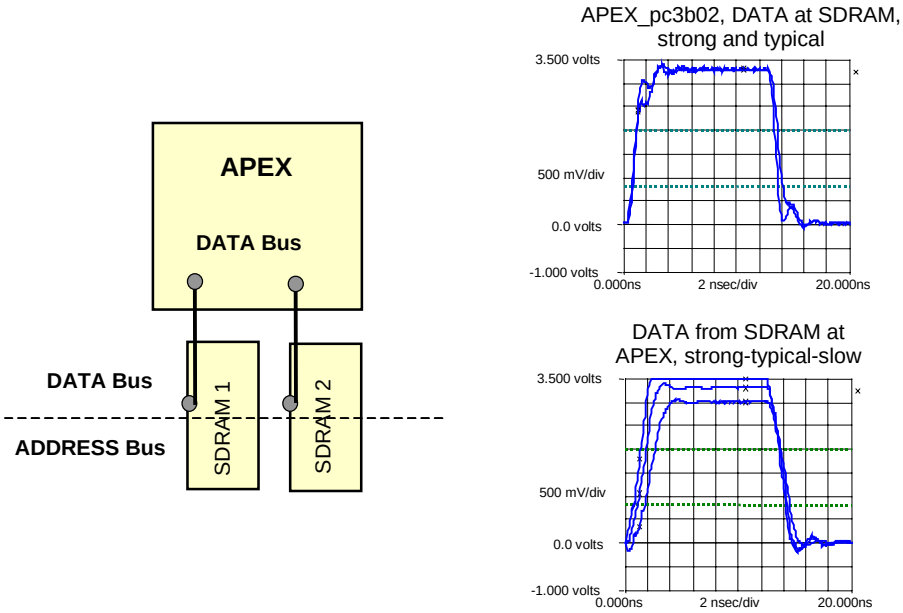
FIGURE 63 shows the signal integrity simulation for the S/UNI-APEX ADDRESS to the SDRAM.

FIGURE 63. ADDRESS to SDRAM



The difference between the upper and lower drawings is in the copper trace shape that connects the ADDRESS to the SDRAMs, and resistor values. Reference Design Core Card Issue 3 has address lines CBA[11:0] connected as shown in lower drawing.

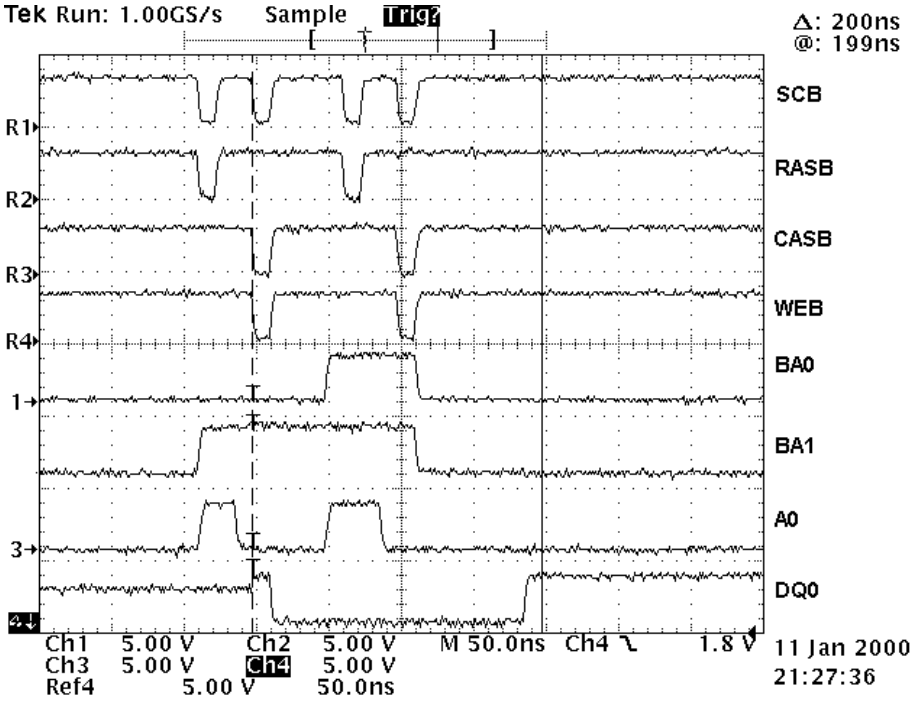
FIGURE 64. DATA to/from SDRAM



The DATA bus in both directions simulates monotonic edges across the transition region, 0.8 V to 2.0 V, with some margins above and below those logic levels. The MOSEL SDRAM IBIS model outputs a different peak voltage depending on the "weak-typical-strong" option. The S/UNI-APEX model it is always at 3.3 V. This is due to the IBIS model differences, where the MOSEL SDRAM uses a more accurate parameter called `[Rising Waveform]`, which cannot be simulated at the present time with the S/UNI-APEX model. The expected difference is estimated at about two hundred ps, and it should not cause major upsets in real bus timing.

The figures below show examples of measured waveforms. FIGURE 66 shows a write to SDRAM from the S/UNI-APEX.

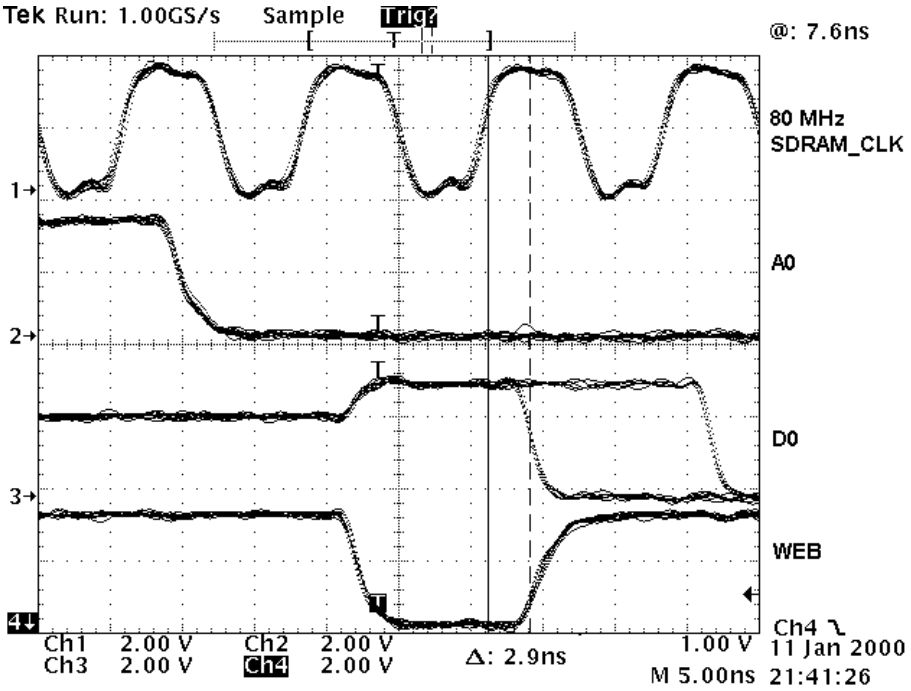
FIGURE 65. Waveforms at SDRAM at 80 MHz



The trace descriptions (next to the right edge of the above graph) apply to the SDRAM pinout shown on the Core Card SDRAM schematics (document [4]). The clock signal is not shown in the figure above. The oscilloscope captures digital signals that show sixteen consecutive write cycles to the SDRAM executed by the S/UNI-APEX. The DQ0 trace between 200 ns cursors shows the binary data pattern 1000000000000001 written to the SDRAM.

FIGURE 66 shows the zoomed pattern with clock and timing margins.

FIGURE 66. Waveforms at SDRAM at 80 MHz



The digital lines shown above are:

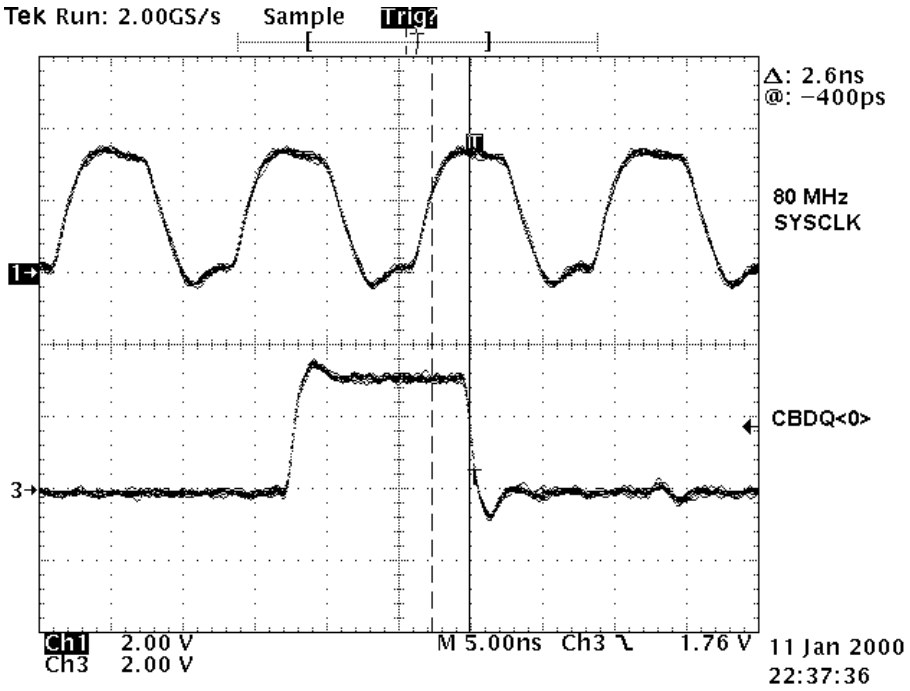
- A0 – address to SDRAM
- D0 – data to SDRAM
- WEB – write enable to SDRAM.

The oscilloscope is triggered with the WEB signal.

The timing shows about a 2.9 ns margin that is enough for a 1.0 ns hold time for the 100 MHz SDRAM (as specified in the Micron™ data sheets).

FIGURE 67 shows the data flowing from the SDRAM to the S/UNI-APEX.

FIGURE 67. Waveforms at the S/UNI-APEX at 80 MHz



The digital line CBDQ<0> is the data at the S/UNI-APEX coming from the SDRAM. The clock at the S/UNI-APEX pin SYSCLK is abut 2.6 ns ahead of the data, leaving enough of a margin with a 0.7 ns hold time as specified in the S/UNI-APEX data sheets.

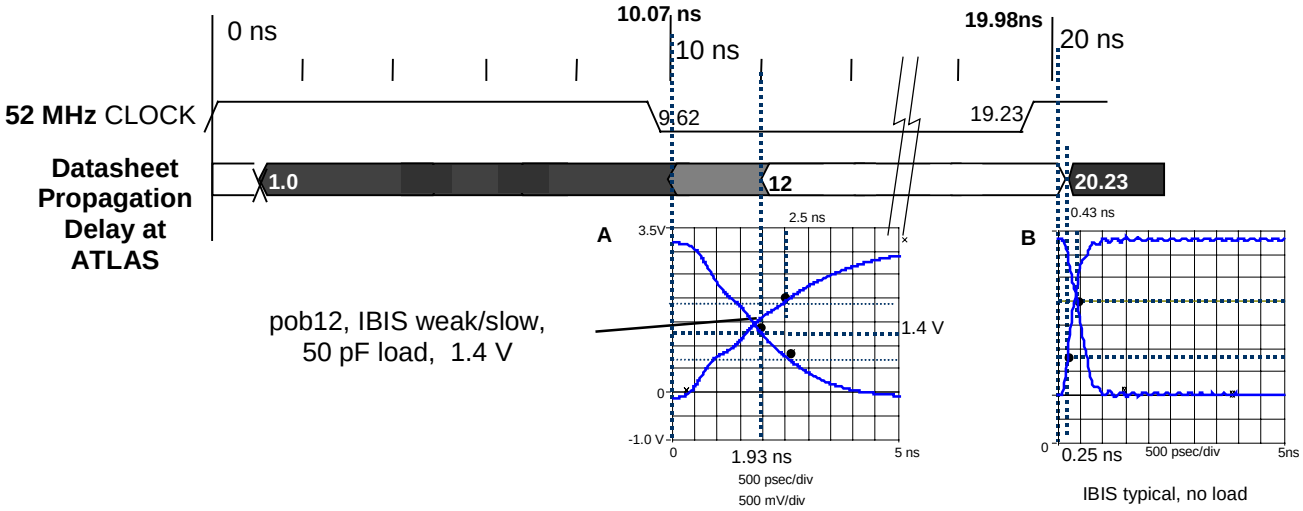
7 S/UNI-ATLAS/ and S/UNI-APEX UTOPIA L2 AND ANY-PHY BUS TIMING

The S/UNI-ATLAS and the S/UNI-APEX timing on Utopia L2 and Any-PHY buses is presented in this section. The signal integrity simulation for the S/UNI-ATLAS, S/UNI-VORTEX, and S/UNI-DUPLEX are based on a preliminary IBIS typical model only.

7.1 S/UNI-ATLAS Timing Correction

The S/UNI-ATLAS data sheet specified a propagation delay of 50 pF and 20 pF. This simulation is based on a 50 pF delay time. The RADDR[4..0] propagation delay is specified at 1 to 12 ns with 50 pF at 1.4 V. FIGURE 68 shows the pbct12 IBIS typical model plots. The clock frequency is 52 MHz, which is the maximum clock speed for the Utopia L2 bus.

FIGURE 68. Adjusted Propagation Delay for pbct12 IBIS Typical



Graph A shows the IBIS pob12 pad loaded with 50 pF. The graph is aligned with a falling edge crossing point at 1.4 V with 12 ns mark on the time scale. The correction point is calculated at 10.07 ns. Graph B shows the IBIS typical unloaded pad aligned with 20.32 ns. This point is derived by adding one nanosecond to the clock period (20.23 ns = 1000/ (52 [MHz]) +1 = 19.23 + 1).

The correction points for the S/UNI-ATLAS pob12 I/O pad are determined at **10.07 ns** and **19.98 ns** for the IBIS typical model. The very same performance is simulated for the S/UNI-VORTEX and the S/UNI-DUPLEX Utopia I/O pads (pbcst12).

7.2 UTOPIA L2 Timing with Offset Configuration

After reviewing different configurations, it was decided to work on bus timing which simulates the most monotonic edges. Ttechnical literature points to data corruption with non-monotonic signals. The offset configuration, shown earlier in FIGURE 29 and FIGURE 30, was slightly modified by adding a serial resistor at the S/UNI-VORTEX-5. The simulation shows monotonic edges with very small bumps that should be acceptable in most applications. FIGURE 69 shows the bus configuration and signal edges for RADDR[4..0] and RRDENB.

FIGURE 69. Modified In-line Configuration and Edge Timing

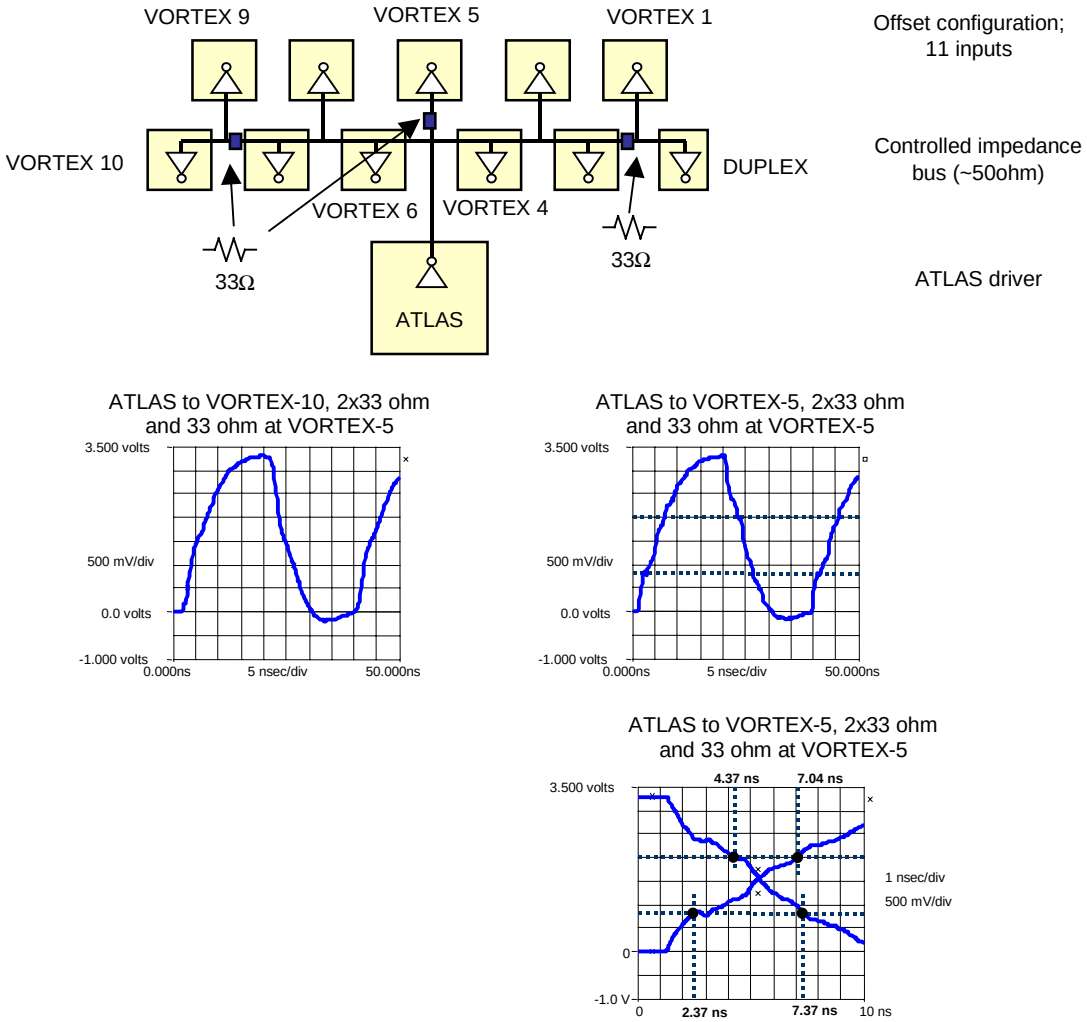
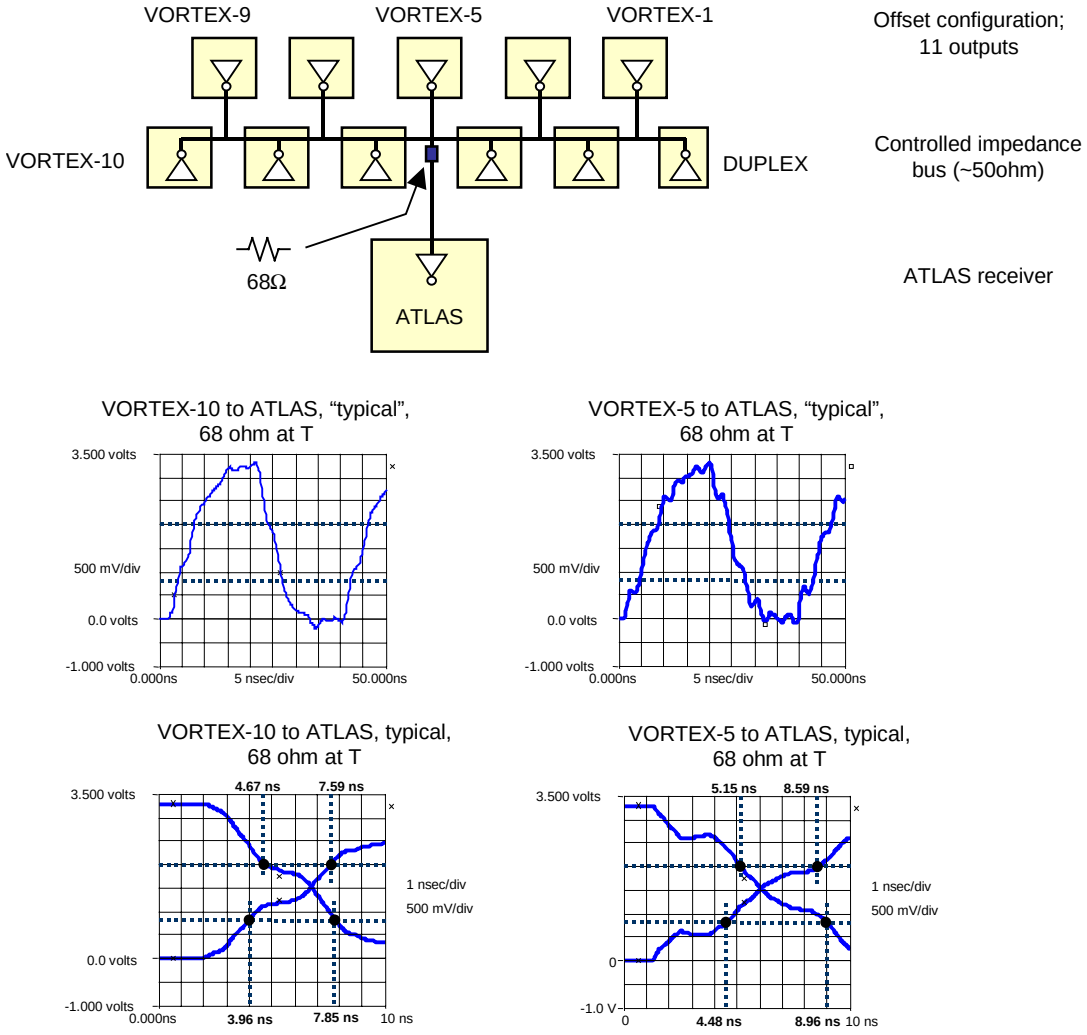


FIGURE 70 shows the simulation that applies to the RDAT[15..0], RCA, RPRTY and RSOC bus signals.

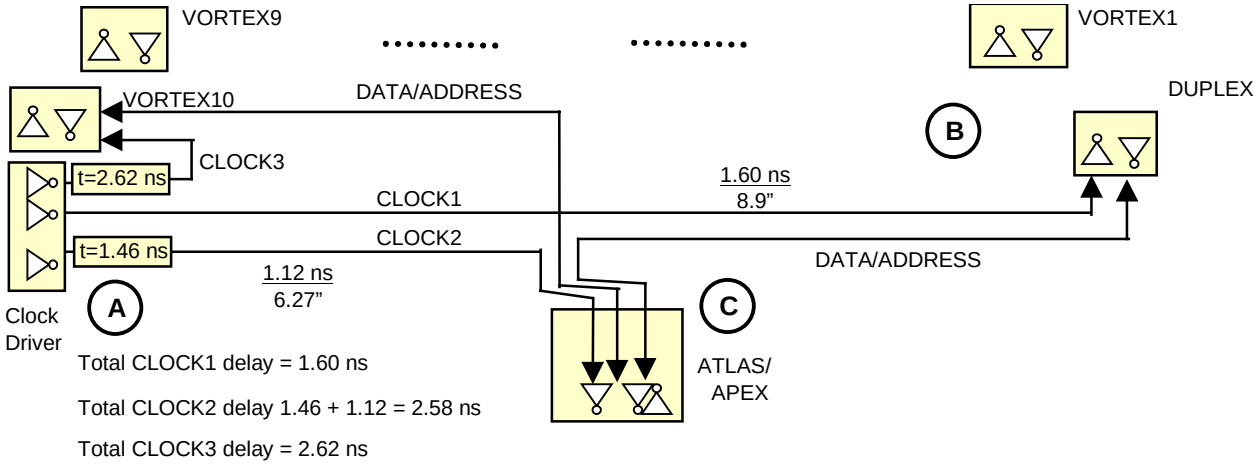
FIGURE 70. In-line Configuration and Edge Timing



7.3 Clock Propagation Timing in Offset Configuration

The clock propagation delay along copper traces is determined in the offset configuration (as shown in FIGURE 69). FIGURE 71 show the delays.

FIGURE 71. CLOCK Propagation Delays with Offset Configuration

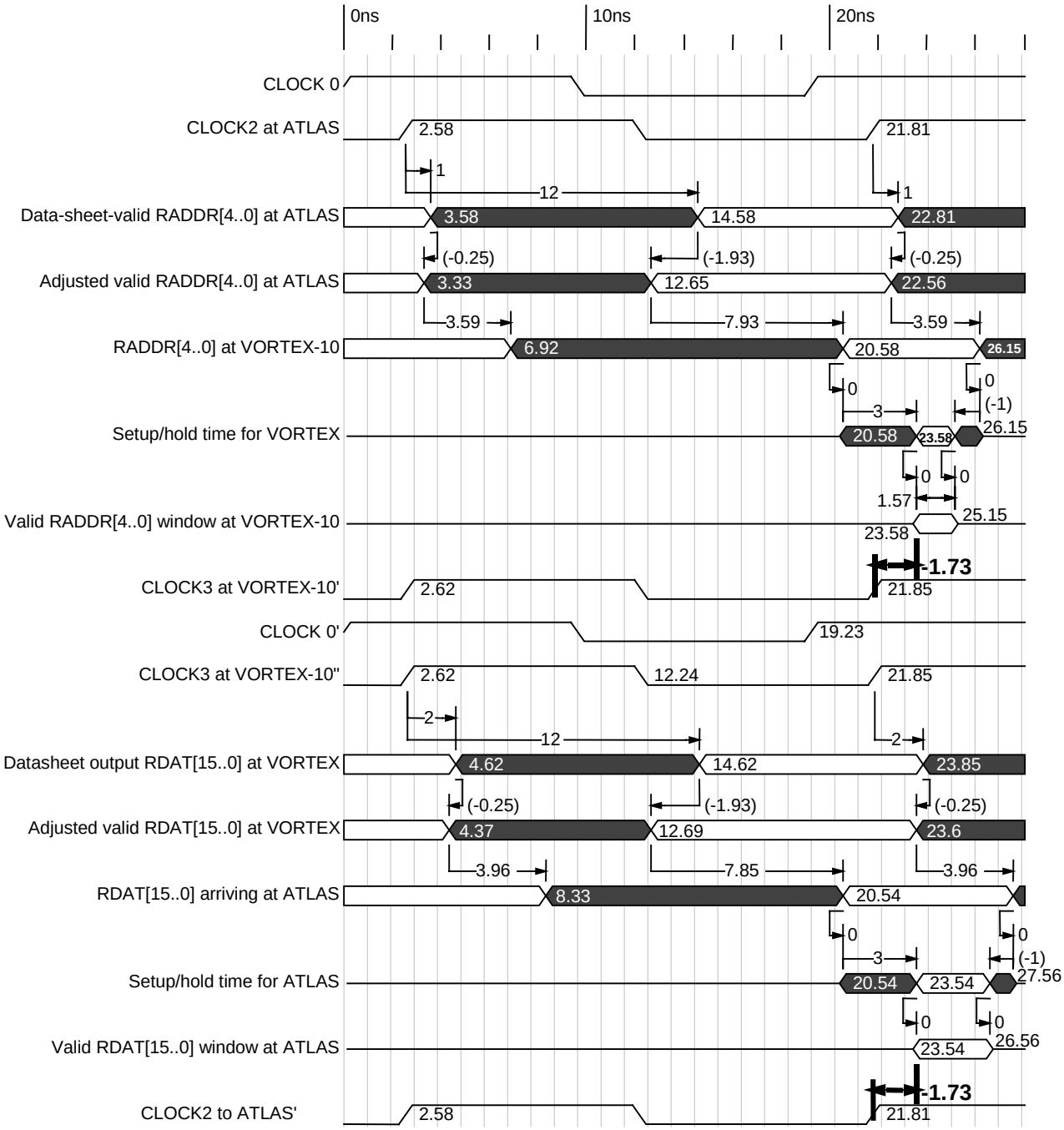


The clocking is referred to an idealized CLOCK0. CLOCK1 from A to the S/UNI-VORTEX-1 at B travels in 1.60 ns. CLOCK2 from A to C is set to have the delay at 2.58 ns, which consists of line A to C with a delay of 1.12 ns (6.44 inches long) and an additional skew of 1.46 ns. CLOCK3 from A to S/UNI-VORTEX-10 is the shortest distance, and it has inserted a delay at 2.62 ns. Those values are entered later in the timing diagram in FIGURE 72. The delays through buffers and on copper traces are critical for clocking the ADDRESS and DATA on the Utopia bus. As it is shown above and in the timing diagram, the clock edge skew at the destination does not need to be 0.0 ns (zero ns) for the best timing performance. The optimal clock skew depends on the signal integrity.

To simplify, the clock is timed as it would be an ideal square wave. An edge distortion may affect the physical board timing. The signal integrity simulation is not used for clock propagation and timing.

All ingredients needed for the bus timing are now derived through the signal integrity simulation (done earlier in this document) and through the copper trace propagation timing (above). FIGURE 72 shows the bus timing simulation that can be done now.

FIGURE 72. UTOPIA L2 Bus “typical” ADDRESS and DATA at 52MHz

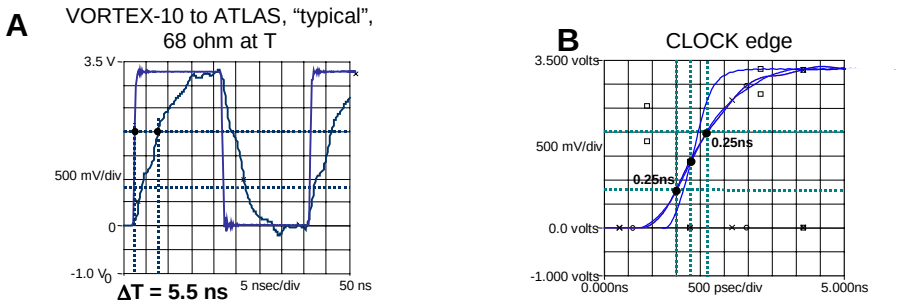


The S/UNI-ATLAS to/from S/UNI-VORTEX-10 valid ADDRESS and DATA misses clock with **1.73 ns** on setup time. The equal delay on both timings is achieved

through adjusting the clock delay at the S/UNI-APEX and at the S/UNI-VORTEX-10. The clock skew is 2.62 – 2.58 = 0.08 ns.

The saw-tooth distortion of the signal is the main reason why the timing margin failed on setup time. Graph A in FIGURE 73 shows the square wave on an unloaded output with the saw-tooth signal.

FIGURE 73. DATA and Clock Edge Distortion



The edge-distorted signal loses about 5.5 ns, if it is compared to an idealized square wave. The Utopia bus with ten S/UNI-VORTEX devices, one S/UNI-DUPLEX device, and one S/UNI-ATLAS device cannot simulate a square wave. and therefore, the bus cannot run at 52 MHz.

The clock edge transition time is not included in the timing above. The clock edge, shown in FIGURE 73 graph B, has a transition time of about ±0.25 ns. This may further decrease the margins in the analyzed timings.

The obvious solutions it to slow down the clock. (or violate rules and pray it works ☺). The clock frequency is recalculated as follows:

$$Fnew = 52 * \frac{19.23}{19.23+1.73} = 46.59 \text{ MHz},$$

19.23 ns is the clock period at 52 MHz.
1.73 ns is the timing violation from FIGURE 72.

At the frequency of 46.59 MHz the clock edge will be exactly at the beginning of the valid data window, as shown in FIGURE 72.

If the hold time would be violated, then slowing down the clock *may not help*. The hold time violation can be improved by increasing the device minimum propagation time (for example, from 2 ns to 3 ns) and decreasing the hold time at

receiving device (for example, from 1 ns to 0.5 ns), which is impossible as those parameters are embedded into the silicone.

The timing simulation process shown above has to be repeated for all combinations of the S/UNI-ATLAS, S/UNI-VORTEX, S/UNI-DUPLEX, ADDRESS, and DATA. We recommend that you check the performance with the IBIS model set at “weak/slow” and “strong/fast”. There are numerous permutations and simulations.

The data sheet timing, as shown in FIGURE 39 and FIGURE 40, shows zero or very little margin on the **hold time**, and our exercise shows a violation on the **setup time** - what can be summarized as … surprise, surprise!!!. We had received numerous questions about hold time near-violation (0.0 ns margin) as shown in FIGURE 39 and FIGURE 40. The above exercise highlights need for signal integrity simulation, and timing simulation based on signal integrity. If that is not done, unexpected timing violations may show up on a board, which might be prevented if signal simulations are done to pre-layout (and post-layout circuit, but before making PCB).

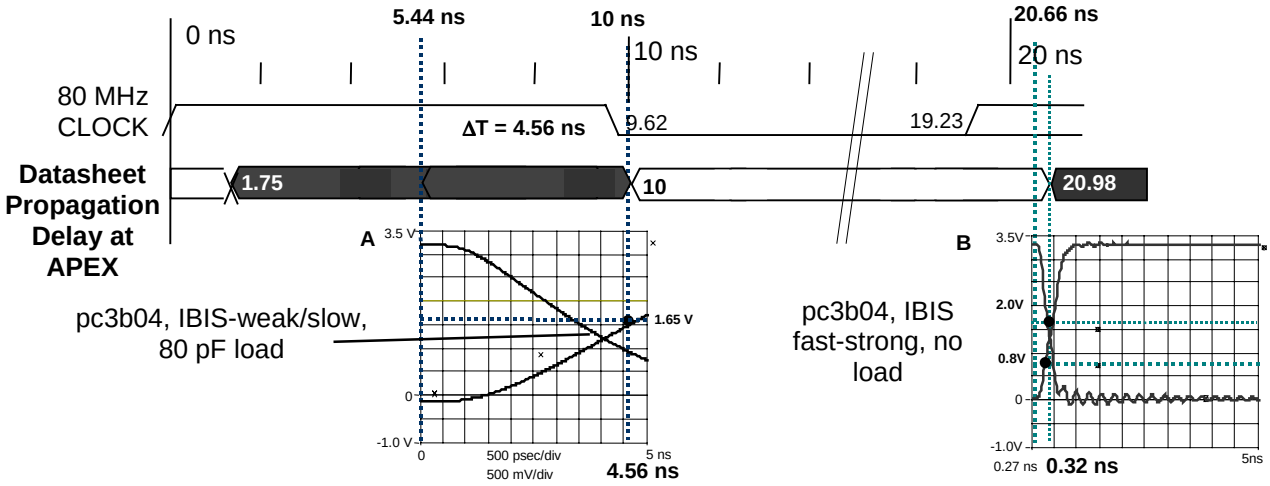
7.4 S/UNI-APEX Timing

7.4.1 S/UNI-APEX Timing Correction

The S/UNI-APEX timing on the Any-PHY bus is derived in the same way as the S/UNI-APEX – RAM timing described in the previous sections. The data sheet specifies the propagation delay TP_{LCLK} at 1.75 ns to 10 ns with 80 pF load at 50 %. The Any-PHY I/O timing is different from the RAM interface timing, and therefore correction parameters have to be recalculated.

FIGURE 74 shows the digital and I/O delays at 52 MHz.

FIGURE 74. Propagation Delay for pc3b04 IBIS slow-weak with 80 pF



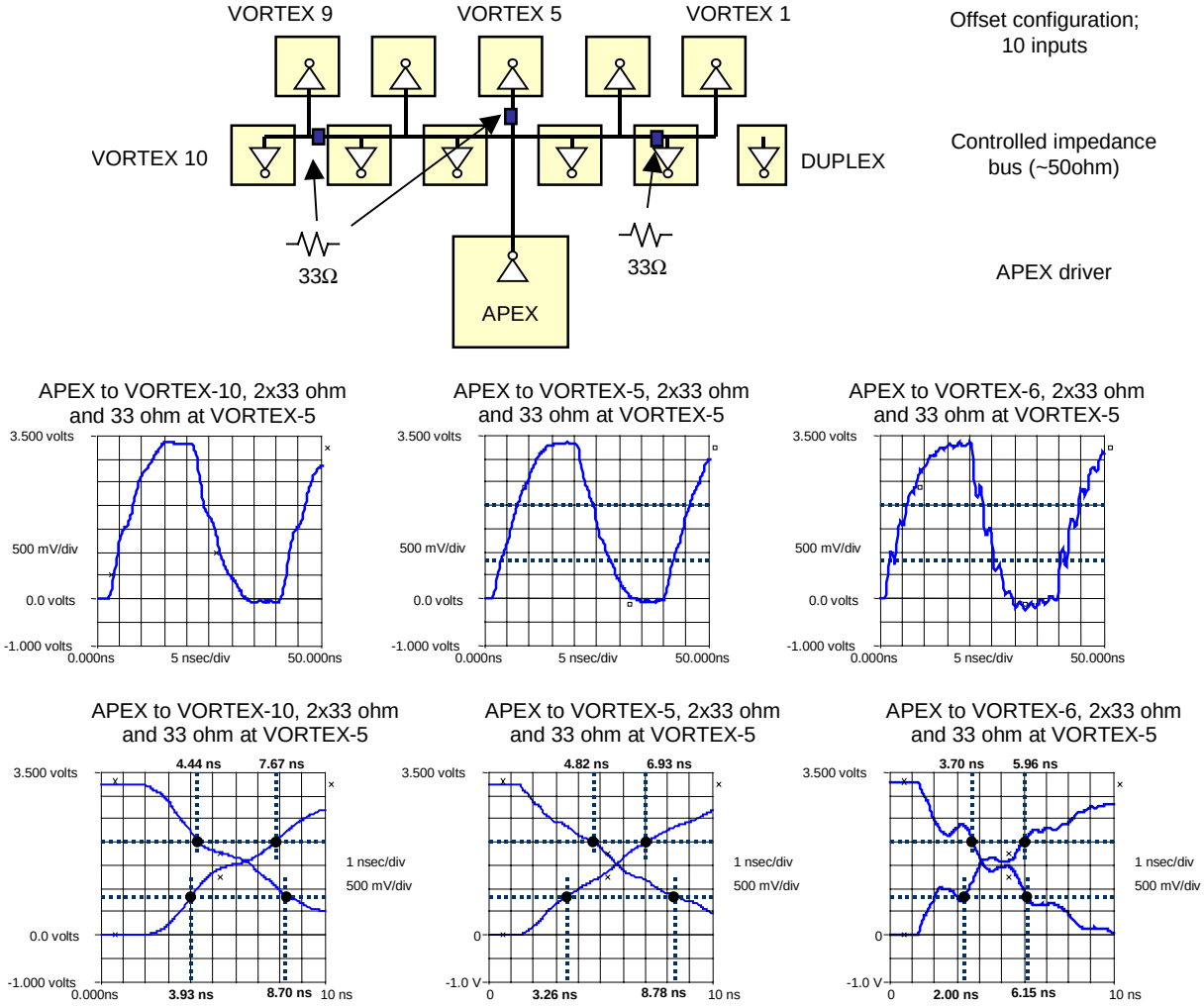
The LineSim graph A is positioned in such a way that the pc3b04 slow-weak IBIS model loaded with 80 pF crosses 1.65 V (50 %) at the 10.0 ns mark at the timing bar. The LineSim tool starts the simulation process at about the **5.44 ns** mark. This means the digital delay must not exceed 5.44 ns. Graph B shows the unloaded falling and rising edges at fast-strong. This graph is positioned in such a way that the edge at 1.65 V is aligned with the 20.98 ns mark on the timing diagram, setting the **20.66 ns** point.

The **5.44 ns** and **20.66 ns** marks are artificially created start points for LineSim edge that travels along bus line. Those points and time differences (0.32 ns and 4.56 ns) are also entered into timing diagrams (shown later in this document).

7.4.2 S/UNI-APEX Driving Offset Bus with Multiple Termination

The S/UNI-APEX I/O pad pc3b04 differs from the S/UNI-ATLAS I/O in speed and current, and therefore creates different back-reflection patterns. FIGURE 75 shows edge distortions.

FIGURE 75. Edge Distortion Delay



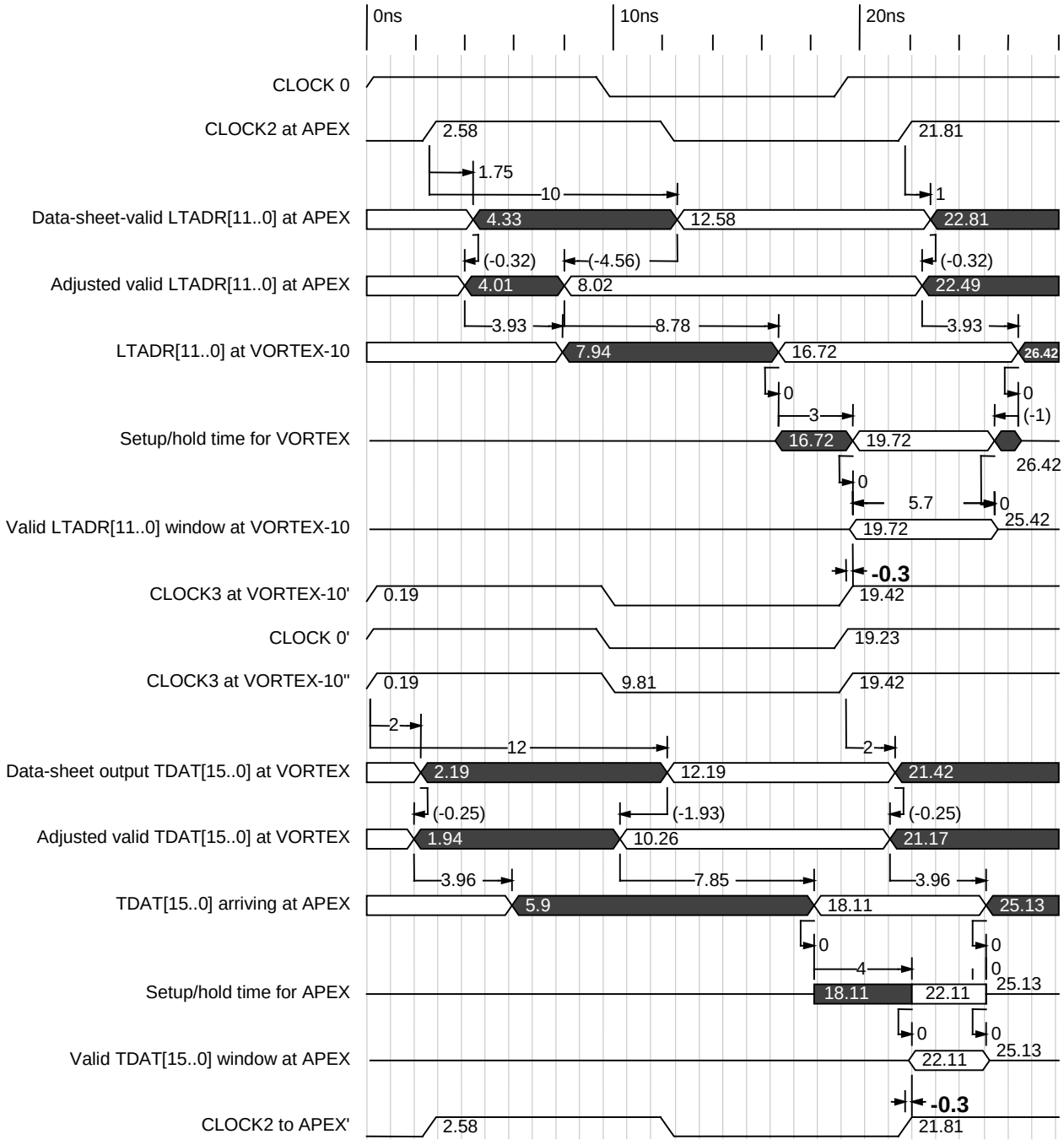
The signal edges at S/UNI-VORTEX-6 show multiple back-reflections. The only solution is to add a serial resistor at the S/UNI-VORTEX-6 (and maybe the S/UNI-VORTEX-7), and that will simulate similar to the signal at the S/UNI-VORTEX-5. The total number of resistors for each bus will increase to four, and that may not be a realistic solution. There is no guarantee that, even with four resistors, the bus can run at 52 MHz.

The edge-distorted signal, from the S/UNI-APEX to the Any-PHY bus, may prevent the building of the Any-PHY bus size. The pc3b04 I/O pad cannot deliver the required signal to simulate the low distorted monotonic edges with the given bus size. Clock edge transition, jitter, and skew further deteriorate timing

margins. However, to close this exercise, bus timing is simulated and shown below.

FIGURE 76 shows how the Any-PHY bus timing.

FIGURE 76. Any-PHY Bus Timing Simulation at 52 MHz



The S/UNI-APEX – S/UNI-VORTEX-10 valid ADDRESS and DATA misses the clock with **0.3 ns** on setup time. The equal delays on both timing charts are achieved through adjusting the clock delay at the S/UNI-APEX and at the S/UNI-VORTEX-10. The clock skew is 2.58 – 0.19 = 2.39 ns.

Similar to the previous Utopia L2 bus simulation, the saw-tooth distortion of the signal is the main reason for setup time failure.

The clock frequency, allowing setup at 0.0 ns margin, can be calculated at:

$$Fnew = 52 * \frac{19.23}{19.23+0.3} = 51.20 \text{ MHz},$$

19.23 ns is the clock period at 52 MHz.
0.3 ns is the timing violation from FIGURE 76.

At 51.20 MHz frequency, the clock edge will be exactly at the beginning of the valid data window, as shown in FIGURE 76.

8 VORTEX CHIPSET SIMULATION SUMMARY

8.1 Simulation Tools

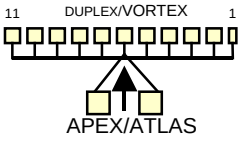
Three CAD tools have been evaluated for the bus simulation project: *SpecctraQuest* and *LineSim* for the pre-layout signal integrity simulation, and *TimingDesigner – Professional 32* for bus timing simulation.

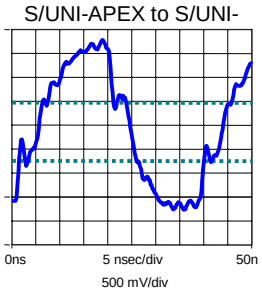
LineSim is a relatively low cost CAD tool, suitable for pre-layout simulation in an applications environment. Its advantage over the UNIX-based SpecctraQuest is its easy installation in a Win95/98/2000 environment, its click-and-build simulation circuit, and its easy transfer of the simulation results (graphs) into MSWord documents. Minor deficiencies do exist and may frustrate its user.

TimingDesigner – Professional 32 was only evaluated for graphical representation of timing derived from signal integrity. The tool provided adequate functionality for this exercise.

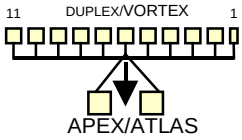
8.2 In-line Configuration

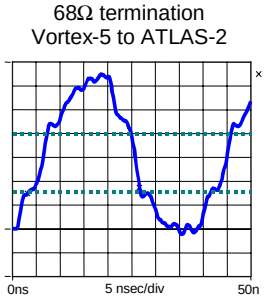
The in-line configuration with the central connection to the S/UNI-ATLAS and the S/UNI-APEX is more preferable over the bus-end connection. The address and data from the S/UNI-ATLAS/S/UNI-APEX shows a strong saw-tooth shape, non-monotonic edges near the bus center, and rounded edges near the bus-end.



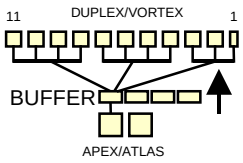


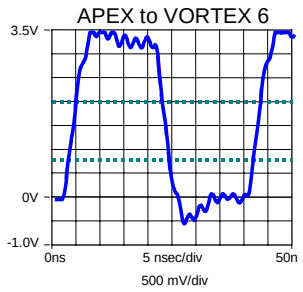
The S/UNI-VORTEX/S/UNI-DUPLEX to S/UNI-ATLAS/S/UNI-APEX in the bus-center connection shows a saw-tooth distortion. The serial termination resistor is required at the T joint to the S/UNI-ATLAS/S/UNI-APEX.



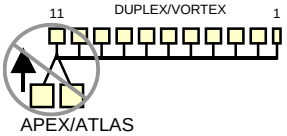


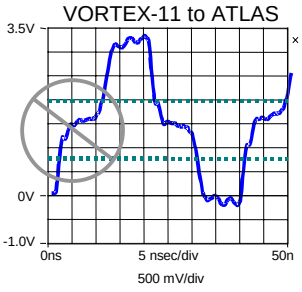
The bus-center configuration, going from the S/UNI-APEX/S/UNI-ATLAS towards the bus, is significantly improved if an additional high-speed buffer is inserted. The bus is split into three sub-sections. However, you need six 16-bit drivers, and the bus line count goes from 31 to 93. Buffer propagation delay and skew may "kill" bus timing.



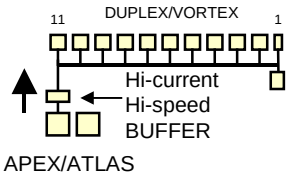


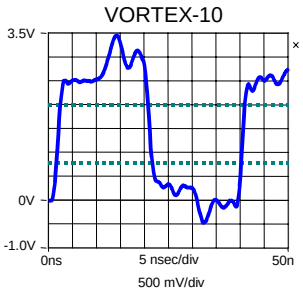
The S/UNI-ATLAS/S/UNI-APEX at the bus-end is not suitable as the simulated signal shows a very long edge-shelf.



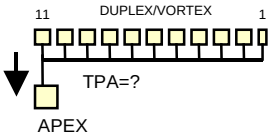


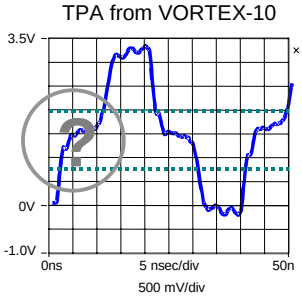
The S/UNI-APEX at the bus-end may work with a high-current high-speed buffer. Also, high impedance traces, at least Zo=100 ohm, with termination resistors at the bus ends are required. High Zo traces are difficult for PCB layout and manufacture.





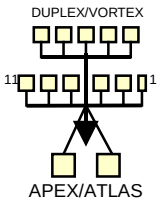
The TPA line goes towards the S/UNI-APEX on the bus, and simulation shows a long shelf from the S/UNI-VORTEX devices, near the beginning of the bus, making it impossible to clock the data.

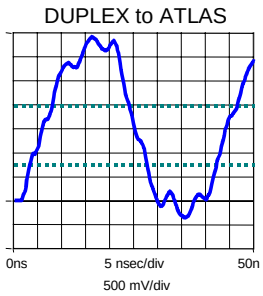




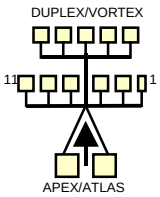
8.3 Offset Configuration

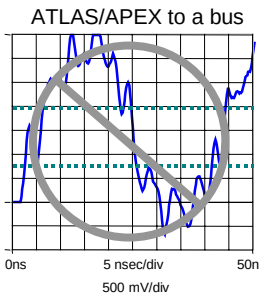
The offset configuration naturally supports central connection of the S/UNI-ATLAS and the S/UNI-APEX. The bus is split into two subsections to ease the Receive/Transmit ports connection. The simulated signal in the Receive Data direction shows slow rising/falling edges that add delays to the timing simulation.





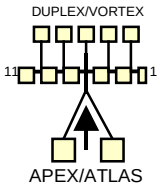
The Transmit Data direction shows relatively high distortions and difficulties to terminate transmission lines.

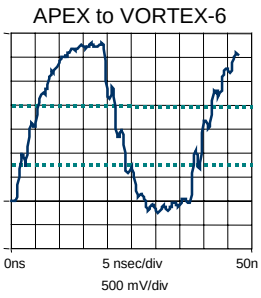




The offset configuration with a single bus simulates a slightly better signal on the far ends of the bus. However, the center of the bus shows the non-monotonic edges. Multiple termination resistors are needed across the bus.

The Receive Data direction simulates a signal similar to the double offset bus shown on the previous page.

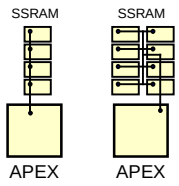


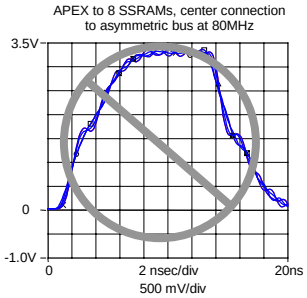


8.4 S/UNI-APEX-RAM Interface

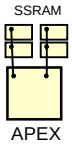
The S/UNI-APEX RAM interface was simulated with the IBIS model options set to weak/slow and strong/fast.

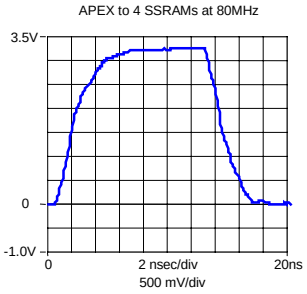
The S/UNI-APEX cannot provide an interface with four/eight SSRAM devices connected at 80 MHz, as shown here →.





The S/UNI-APEX can provide an interface with two/four SSRAM devices connected at 80 MHz, as shown here.

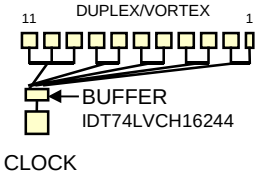


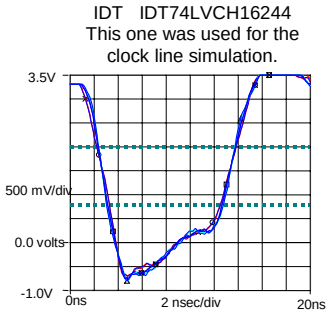


8.5 Clock Signal Integrity

To avoid non-monotonic edges in the logic transition window 0.8 to 2.0 V, the clock must be distributed with multiple lines.

The buffer has to be chosen to provide adequate speed and driving capacity. The clock lines need serial termination and/or Thevenin terminations to suppress overshoots and the high current through the clamping diodes, and in turn a “silicon” noise to adjacent “quiet” I/O pads or electron injection dipper into silicon. Silicone crosstalk applies to any bus lines with a high overshoot as well.





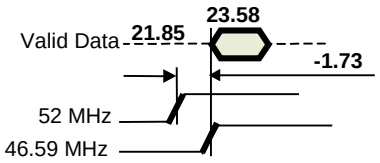
The fast and high current drivers may create EMI problems– that are not addressed in this document. A driver that is too fast (such as Philips 74ALVT16244) may cause problems with overshoots.

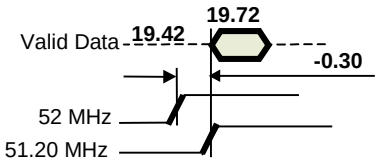
8.6 Bus Timing

The S/UNI-APEX and S/UNI-ATLAS interface to Utopia L2 and Any-PHY bus is simulated in this document using the IBIS “slow-weak” model.

Single Bus Offset Placement Configuration

The timing simulation, shown in FIGURE 72, with the S/UNI-ATLAS, ten S/UNI-VORTEX devices, and the S/UNI-DUPLEX on a Utopia L2 bus calculates a 1.73 ns setup violation with the clock at 52 MHz. Clock at about 46 MHz works.





The timing simulation shown in FIGURE 72 with the S/UNI-APEX and ten S/UNI-VORTEX devices on an Any-PHY bus calculates a 0.30 ns setup violation with the clock at 52 MHz.

Slowing down the clock helps to eliminate setup time violations.

Possible timing improvements can be done by:

- improving signal integrity on the bus, which is the most important (one suggestion may be to add multiple serial terminating resistors);
- decreasing physical size and trace length on the bus;
- decreasing the number of devices connected to the bus;
- slowing down the clock (helps with setup time violations)

8.7 Future Simulations

We need to investigate simulations based on signal integrity with a data sheet correction approach to bus timing. We must question:

- Is timing simulation based on signal integrity and adjusted data sheet timing correct?
- What can be done to bring simulation closer to the measured signal integrity on tested boards?

A need for additional simulations was pointed throughout this document. We need to investigate the following possible directions:

- Improve signal integrity and eliminate the saw-tooth delay, which kills timing at 52 MHz.
- Place components in closer proximity to decrease the overall bus dimension.
- Place components double sided (some RAM manufacturers are introducing double sided footprints).
- Place less devices on the bus simulation;
- Compare signal integrity simulation done with HyperLynx against other simulation tools.
- Verify simulations presented throughout this document on a built and tested boards.

9 DISCLAIMER

This document is based on hands-on experience with simulation tools and is an unconventional interpretation of the data sheet AC timing. In the author's opinion, the data sheet AC timing (for any silicone device throughout the silicone industry) cannot be directly used for signal integrity and timing simulation.

The proposed method of timing calculation, based on signal integrity and an artificially created starting point for the IBIS model, needs further investigation and comparison with built and tested large Utopia and Any-Phy buses.

Simulation results are general direction pointers, which may not prove or disprove bus timing and signal integrity. It is always required to verify simulated results. However, simulation tools utilized for pre-layout simulations can capture timing violations and signal integrity problems preventing a major disappointment when assembled board, with a large bus, experience soft errors due to bus signal irregularities.

PMC-Sierra does not approve, disapprove, or recommend any CAD or simulation tools.

10 GLOSSARY

Any-PHY	PMC-Sierra proprietary ATM cell size with a 2-byte prepend
IBIS	Input/Output Buffer Information Specification
I/O	Input/Output
S/UNI	Saturn User Network Interface Development Group
BGA	Ball Grid Array
DSLAM	Digital Subscriber Line Access Multiplexer
PCB	Printed Circuit Board

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