12-Bit, Multichannel, DAC/ADC Temperature Sensor and Current Sense for Monitor and Control Applications

Preliminary Technical Data

AD7294

FEATURES

4-channel 12-bit DAC
- **Guaranteed monotonic**
- **10 µs settling time**
- **10 mA sink and source capability**
- **Offset in for range adjustment**
- **Output span: 5 V in 0 to 15 V range**

9-channel, 12-bit ADC
- **200 kSPS throughput**
- **Input range: 0 to V_{REF}, 0 to 2 V_{REF}**
- **Differential/single-ended**
- **Limit registers per channel**

2 high-side current sense
- **48 V max operation**
- **±1% FS accuracy**
- **±200 mV input range**

3-channel temperature sensor
- **Diode temperature measurement**
- **±2°C accuracy**
- **Measurement range: −10°C to +90°C**

Internal 2.5 V reference
I²C®-compatible serial interface
Temperature range: −40°C to +105°C
Alert function
Package type: LFCSP-56, TQFP-64

APPLICATIONS

Cellular base station (GSM, EDGE, UMTS, CDMA)
Point-to-multipoint and other RF transmission systems
12 V, 24 V, 48 V automotive applications
Industrial control

GENERAL DESCRIPTION

The AD7294 contains all the functions required for general-purpose monitoring and control of current, voltage, and temperature integrated into a single-chip solution. The part includes low voltage (±200 mV) analog-input sense amplifiers for current monitoring across shunt resistors, temperature-sense inputs, and four uncommitted analog input channels multiplexed into a 200 kSPS SAR ADC. An internal low ppm reference is provided to drive both the DAC and ADC. Four 12-bit DACs provide the outputs for voltage control. The AD7294 also includes limit registers for alarm functions. The part is designed on a high voltage DMOS process for a high voltage compliance, 48 V on the current-sense inputs, and up to 15 V DAC output voltage.

The part is ideal for bias current control of the power transistors used in power amplifiers employed in CDMA, GSM, EDGE, and UMTS cellular base stations.

The DACs provide digital control with 1.2 mV resolution to control the bias currents of the power transistors. They can also be used to provide control voltages for variable gain amplifiers or impedance match networks in the main signal chain. Thermal diode based temperature sensors are incorporated to compensate for temperature effects. The ADC monitors the high-side current and temperature. All this functionality is provided in an LFCSP package operating over a temperature range of −40°C to +105°C.

FUNCTIONAL BLOCK DIAGRAM

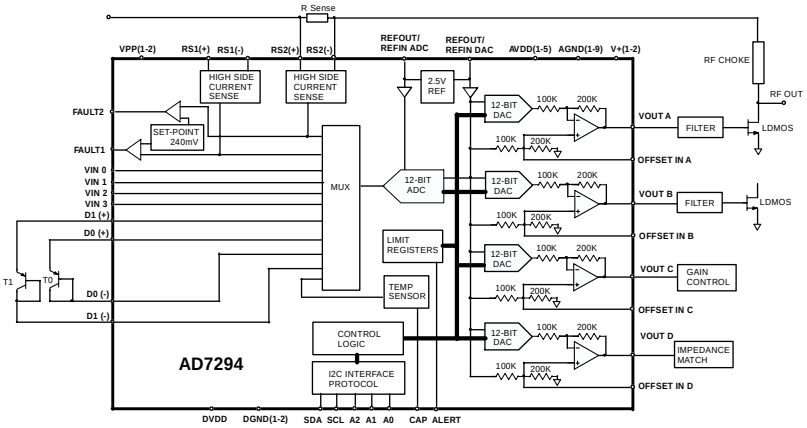

Figure 1. Typical Configuration for AD7294 in Cellular Base Station RF LDMOS Power Amplifier Control

Rev. PrB

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REVISION HISTORY

10/05—Revision PrA: Preliminary Version

SPECIFICATIONS

DAC SPECIFICATIONS[1]

AV_{DD} = DV_{DD} 4.5 V to 5.5 V, AGND = DGND= 0 V, external 2.5 V reference. Temperature range for B version: −40°C to +105°C. All specifications T_{MIN} to T_{MAX}, unless otherwise noted. Offset pin is open, so range is from 0 to 5V.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions / Comments
ACCURACY					
Resolution	12			Bits	
Relative Accuracy (INL)			±4	LSB	
Differential Nonlinearity (DNL)			±1	LSB	Guaranteed monotonic
Zero-Scale Error			4	mV	
Full-Scale Error			TBD		
Offset Error			±4	mV	Measured in the linear region
Offset Error TC		±5		µV/°C	
Gain Error			±0.024	% FSR	
Gain Temperature Coefficient		2		ppm FSR/°C	
DC Crosstalk			0.5	LSB	
DAC OUTPUT CHARACTERISTICS					
Output Voltage Range	0		5	V	With a 2.5 V internal reference
Output Voltage Span	0		15	V	The 5 V o/p voltage range can be positioned on the span by the offset
Output Voltage Settling Time		TBD			
Slew Rate		TBD			
Output Noise Spectral Density		TBD			
Short-Circuit Current			40	mA	FS current shorted to ground
Load Current			±10	mA	Source/Sink within 200 mV of supply
Capacitive Load Stability					
$R_L = \infty$			1000	pF	
DC Output Impedance			0.5	Ω	
Power Supply Sensitivity					
$\Delta Vout/\Delta AV_{DD}$		–85		dB	
OFFSET INPUT					
Input Range	0			V	$V_{OUT} = 3\ V_{OFFSET} - 2V_{REF} + V_{DAC}$
			5	V	
DC Input Impedance		75		kΩ	
REFERENCE					
Reference Output Voltage	2.49		2.51	V	
Reference Input Voltage Range	0.1		2.5	V	
DC Leakage Current			±30	µA	
Input Capacitance		20		pF	
V_{REF} Output Impedance		25		Ω	
Reference Temperature Coefficient			25	ppm/°C	10 ppm/°C typ

[1] Guaranteed by design and characterization; not subject to production testing.

ADC SPECIFICATIONS[1]

AV_{DD} = DV_{DD} 4.5 V to 5.5 V, AGND = DGND= 0 V, external 2.5 V reference. Temperature range for B version: −40°C to +105°C. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Parameter	Min	Typ	Max	Unit	Test Conditions / Comments
ACCURACY					
Resolution		12		Bits	
Integral Nonlinearity (INL)		±0.5	±1	LSB	Differential Mode
					Single Ended or Pseudo-Differential Mode
Differential Nonlinearity (DNL)			±1	LSB	Differential Mode
					Single Ended or Pseudo-Differential Mode
Offset Error			±3	LSB	
Gain Error			±2	LSB	
Total Unadjusted Error (TUE)			TBD	LSB	
Conversion Rate			3	µS	
Analog Input Range	0		V_{REF} or 2 V_{REF}	V	
Input Capacitance		30		pF	
DC Input Leakage Current			±1	µA	
TEMPERATURE SENSOR					
Accuracy			±2	°C	External temperature sensors × 2 T_A = −10°C to +90°C
Accuracy			±2	°C	Internal temperature sensor T_A = −10°C to +90°C
Resolution		11		Bits	0.25 °C LSB size
Low Level Output Current Source		8		µA	
Medium Level Output Current Source		32		µA	
High Level Output Current Source		128		µA	
CURRENT SENSE					
Common-Mode Input Range	AV_{DD}		48	V	±200 mV Full Scale Voltage
Full-Scale Sense Voltage		200		mV	
RS(+) and RS(–) Input Bias Current		25		µA	
CMRR / PSRR		80		dB	Pin connected to power supply
Maximum Series Resistance for external diode			10	k Ω	
Gain			±1	% FS	$T_A = T_{MIN}$ to T_{MAX}
Accuracy					
Offset					
Bandwidth		300		kHz	
Amplifier Equivalent RMS Noise			0.8	LSB	60 µV RMS referred to input
REFERENCE					
Reference Output Voltage	2.49		2.51	V	
Reference Input Voltage Range	0.1		2.5	V	
DC Leakage Current			±30	µA	
Input Capacitance		20		pF	
V_{REF} Output Impedance		25		Ω	
Reference Temperature Coefficient			25	ppm/°C	10 ppm/°C typ

GENERAL SPECIFICATIONS[1]

AV_{DD} = DV_{DD} 4.5 V to 5.5 V, AGND = DGND= 0 V, external 2.5 V reference. Temperature range for B version: −40°C to +105°C. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Parameter	Min	Typ	Max	Unit	Test Conditions / Comments
LOGIC INPUTS (SDA, SCL ONLY)					
V_{IH}, Input High Voltage	0.7 V_{DRIVE}			V	
V_{IL}, Input Low Voltage			0.3 V_{DRIVE}	V	
I_{IN}, Input Leakage Current			±1	µA	
V_{HYST}, Input Hysteresis	0.05 DV_{DD}			V	
C_{IN}, Input Capacitance		8		pF	
Glitch Rejection			50	ns	Input filtering suppresses noise spikes of less than 50 ns
LOGIC OUTPUTS (SDA, ALERT, FAULT)					
V_{OL}, Output Low Voltage			0.4	V	I_{SINK} = 3 mA
			0.6	V	I_{SINK} = 6 mA
Three-State Leakage Current			±1	µA	
Three-State Output Capacitance		8		pF	
POWER REQUIREMENTS					
V_{PP}	AV_{DD}		48	V	
AV_{DD}	4.5		5.5	V	
V(+)	4.5		16.5	V	
DV_{DD}	4.5		5.5	V	
V_{DRIVE}	3		5.5	V	
I_{PP}	TBD				
AI_{DD}	TBD			mA	Outputs unloaded
DI_{DD}			1	mA	V_{IH} = DV_{DD}, V_{IL} = DGND
AI_{DD} (Power-Down)			5	µA	
DI_{DD} (Power-Down)			5	µA	
Power Dissipation			TBD	mW	

[1] Guaranteed by design and characterization; not subject to production testing.

TIMING CHARACTERISTICS[1,2]

I²C Serial Interface

DV_{DD} = 4.5 V to 5.5 V, AGND = DGND = 0 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Description
F_{SCL}	400	kHz max	SCL clock frequency
t_1	2.5	µs min	SCL cycle time
t_2	0.6	µs min	t_{HIGH}, SCL high time
t_3	1.3	µs min	t_{LOW}, SCL low time
t_4	0.6	µs min	$t_{HD,STA}$, start/repeated start condition hold time
t_5	100	ns min	$t_{SU,DAT}$, data set-up time
t_6[3]	0.9	µs max	$t_{HD,DAT}$, data hold time
	0	µs min	$t_{HD,DAT}$, data hold time
t_7	0.6	µs min	$t_{SU,STA}$, set-up time for repeated start
t_8	0.6	µs min	$t_{SU,STO}$, stop condition set-up time
t_9	1.3	µs min	t_{BUF}, bus free time between a stop and a start condition
t_{10}	300	ns max	t_R, rise time of SCL and SDA when receiving
	0	ns min	t_R, rise time of SCL and SDA when receiving (CMOS compatible)
t_{11}	300	ns max	t_F, fall time of SDA when transmitting
	0	ns min	t_F, fall time of SDA when receiving (CMOS compatible)
	300	ns max	t_F, fall time of SCL and SDA when receiving
	$20 + 0.1C_b$[4]	ns min	t_F, fall time of SCL and SDA when transmitting
C_b	400	pF max	Capacitive load for each bus line

[1] Guaranteed by design and characterization; not subject to production test.
[2] See Figure 2.
[3] A master device must provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH} min of the SCL signal) to bridge the undefined region of SCL's falling edge.
[4] C_b is the total capacitance in pF of one bus line. t_R and t_F are measured between 0.3 DV_{DD} and 0.7 DV_{DD}.

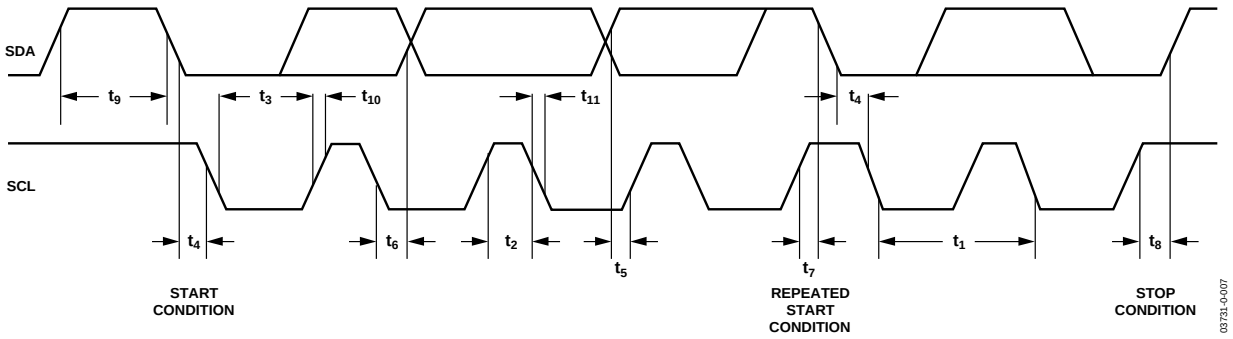


Figure 2. I²C-Compatible Serial Interface Timing Diagram

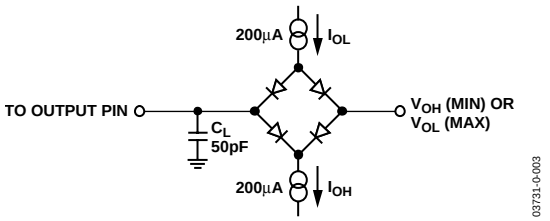


Figure 3. Load Circuit for Digital Output

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.[1]

Table 3.

Parameter	Rating
V_{PP} to AGND	−0.3 V to +70 V
AV_{DD} to AGND	−0.3 V to +7 V
V(+) to AGND	−0.3 V to +17 V
DV_{DD} to DGND	−0.3 V to +7 V
Digital Inputs to DGND	−0.3 V to DV_{DD} + 0.3 V
SDA/SCL to DGND	−0.3 V to + 7 V
Digital Outputs to DGND	−0.3 V to DV_{DD} + 0.3 V
RS(+)/RS(−) to AGND	−0.3 V to V_{PP} + 0.3 V
REFIN to AGND	−0.3 V to AV_{DD} + 0.3 V
AGND to DGND	−0.3 V to +0.3 V
VOUTx to AGND	−0.3 V to AV_{DD} + 0.3 V
Analog Inputs to AGND	−0.3 V to AV_{DD} + 0.3 V
Operating Temperature Range	
Commercial (B Version)	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J Max)	150°C
LFCSP-56 Package	
θ_{JA} Thermal Impedance	30°C/W
θ_{JC} Thermal Impedance	2.9°C/W
Reflow Soldering Peak Temperature	230°C

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

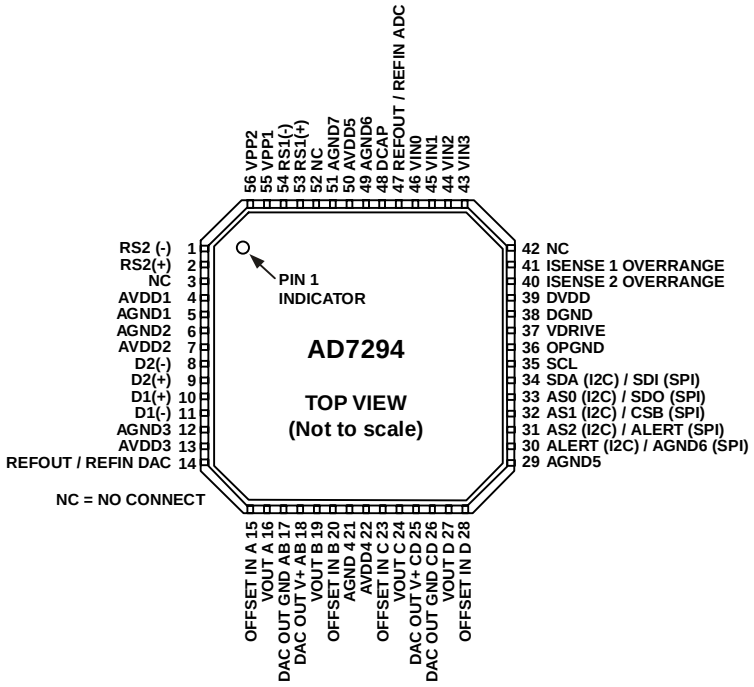


Figure 4.

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 54	RS2(–), RS1(–)	Low-Side Connection for External Sense Resistor.
2, 53	RS2(+), RS1(+)	High-Side Connection for External Sense Resistor.
3, 42, 52	NC	No Connection
4, 7, 13, 22, 50	AVDD1 to AVDD5	Analog Supply Pins. These pins should be decoupled with a 0.1 µF ceramic capacitor and a 10 µF tantalum capacitor. Operating range is 4.5 V to 5.5 V.
5, 6, 12, 21, 29, 49, 51	AGND 1 to AGND7	Analog Ground Reference Point. All AGND pins should be connected externally to the AGND plane.
8, 11	D2(–), D1(–)	Analog Input. Connected to cathodes of the external temperature-sensing diodes.
9, 10	D2(+), D1(+)	Analog Input. Connected to anodes of the external temperature-sensing diodes.
14	REFOUT/REFIN DAC	The AD7294 contains a REFOUT/REFIN DAC pin common to all four DAC channels. When the internal reference is selected, this pin is the reference output. If the application requires an external reference, it can be applied to this pin, and the internal reference can be disabled via the control register. The default for this pin is a reference input.
15, 20, 23, 28	OFFSET IN A to OFFSET IN D	Used to set the desired output range for each DAC channel. Input range is 0 V to 5 V.
16, 19, 24, 27	VOUT A to VOUT D	Buffered Analog Outputs for DAC Channels A to D. Each analog output is driven by an output amplifier that can be offset using the offset in pin. DACs provide 12-bit resolution in a 5 V range, providing an output voltage from 0 V to 15 V. Each output is capable of sourcing and sinking 10 mA and driving a 1,000 pF load.
17, 18	DAC OUT GND AB, DAC OUT V+ AB	Analog Supply Pins for Output Amplifiers on VOUTA and VOUTB.
25, 26	DAC OUT V+ CD, DAC OUT GND CD	Analog Supply Pins for Output Amplifiers on VOUTC and VOUTD.
30	ALERT	Digital Output. This pin acts as an out-of-range indicator and becomes active when a conversion result violates the $DATA_{HIGH}$ or $DATA_{LOW}$ register values associated with each channel input.
31 to 33	AS2, AS1, AS0	Logic Inputs. These inputs are used to select unique addresses for the AD7294. Device address depends on the voltage applied to these pins.
34	SDA	Digital I/O. Serial bus bidirectional data. Open-drain output.
35	SCL	Digital Input. Serial bus clock. The data transfer rate in I^2C mode is compatible with both 100 kHz

Pin No.	Mnemonic	Description
		and 400 kHz operating modes.
36	OPGND	Dedicated Ground Pin for I^2C Interface.
37	VDRIVE	This pin should be connected to the supply that the I^2C bus is pulled up to. This is not a supply pin in I^2C mode—it just sets up the input threshold levels.
38	DGND	Ground for All Digital Circuitry.
39	DVDD	Logic Power Supply. Guaranteed operating range is 2.7 V to 5.5 V. It is recommended that these pins be decoupled with 0.1 µF ceramic and 10 µF tantalum capacitors to DGND.
40, 41	$I_{SENSE}1$ Overrange, $I_{SENSE}2$ Overrange	Outputs from Fault Comparators Connected to High-Side Current Sense Amplifiers.
43 to 46	VIN3 to VIN0	Single-Ended Analog Inputs with Input Range from 0 V to REFIN/REFOUT ADC.
47	REFOUT/REFIN ADC	The AD7294 contains REFOUT/REFIN ADC pin for the ADC. When the internal reference is selected, this pin is the reference output. If the application requires an external reference, it can be applied to this pin, and the internal reference can be disabled via the control register. The default for this pin is a reference input.
48	DCAP	External Decoupling Capacitor Input for Internal Temperature Sensor. A 0.1 µF capacitor to AGND should be connected to this pin.
55, 56	VPP1, VPP2	Analog Supply Pins. Power supply pins for the high-side current sense amplifiers. Operating range is from AVDD to +60 V.

TYPICAL PERFORMANCE CHARACTERISTICS

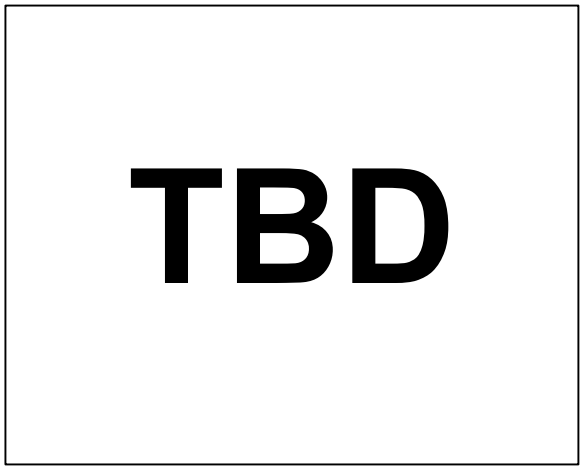


Figure 5.

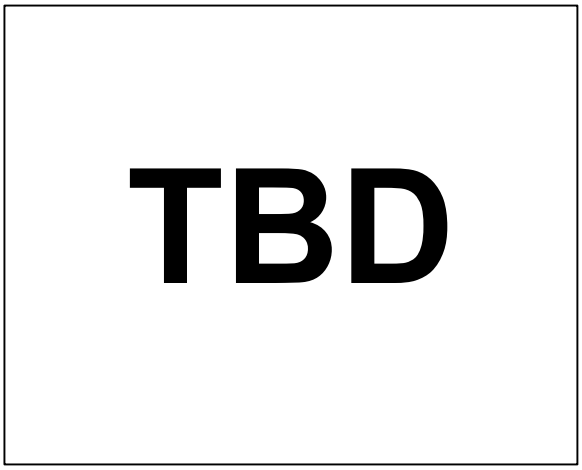


Figure 8.

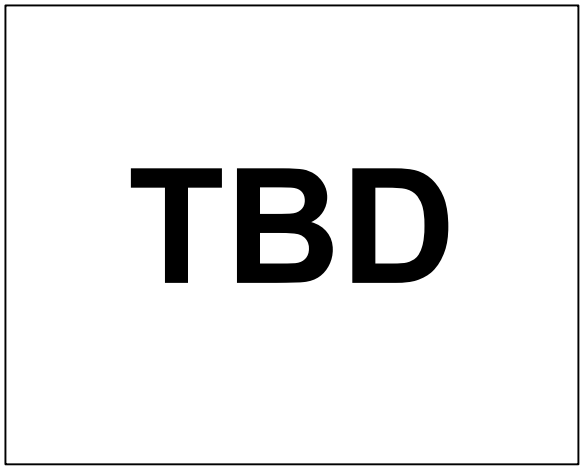


Figure 6.

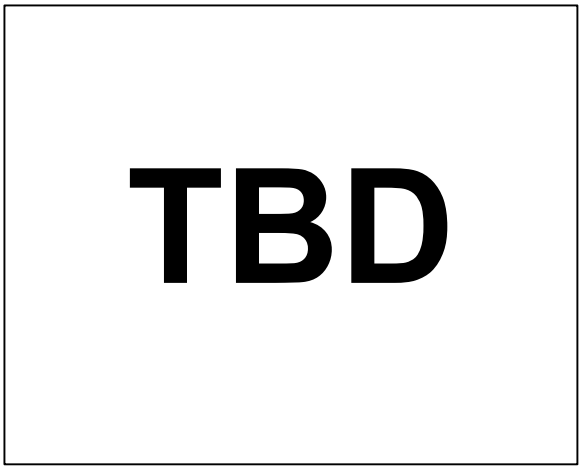


Figure 9.

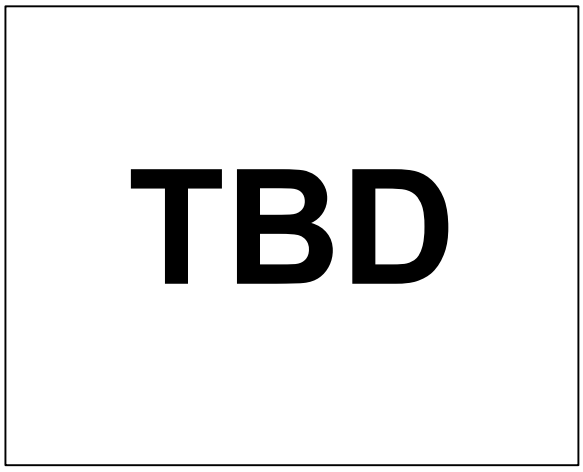


Figure 7.

TERMINOLOGY

Integral Nonlinearity
The maximum deviation from a straight line passing through the endpoints of the ADC/DAC transfer function. The endpoints are zero scale, a point 1 LSB. below the first code transition, and full scale, a point 1 LSB above the last code transition.

Differential Nonlinearity
Differential nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity.

Gain Error
Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from ideal, expressed as a percentage of the full-scale range.

Gain Error Match
The difference in gain error between any two channels.

Zero-Code Error
Zero-code error is a measure of the output error when zero code (0x000) is loaded into the DAC register. Ideally, the output should be 0 V. Zero-code error is due to a combination of the offset errors in the DAC and output amplifier. Zero-code error is expressed in mV.

Full-Scale Error
Full-scale error is a measure of the output error when full-scale code (0xFFFF) is loaded into the DAC register. Ideally, the output should be V_{DD} − 1 LSB. Full-scale error is expressed in mV.

Zero-Code Error Drift
Zero-code error drift is a measure of the change in zero-code error with a change in temperature. It is expressed in µV/°C.

Gain Error Drift
Gain error drift is a measure of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-s and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x2000 to 0x1FFF).

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nV-s and is measured with a full-scale code change on the data bus—from all 0s to all 1s or vice versa.

Channel-to-Channel Isolation
A measure of the level of crosstalk between channels, taken by applying a full-scale sine wave signal to the unselected input channels and determining how much of the 108 Hz signal is attenuated in the selected channel. The sine wave signal applied to the unselected channels is then varied from 1 kHz up to 2 MHz, and each time it is determined how much of the 108 Hz signal in the selected channel is attenuated. This figure represents the worst-case level across all channels.

Aperture Delay
The measured interval between the sampling clock's leading edge and the point at which the ADC takes the sample.

Aperture Jitter
The sample-to-sample variation in the effective point in time at which the sample is taken.

Offset Error
The deviation of the first code transition (00 … 000) to (00 … 001) from the ideal—that is, AGND + 1 LSB.

Offset Error Match
The difference in offset error between any two channels.

SYSTEM DESCRIPTION

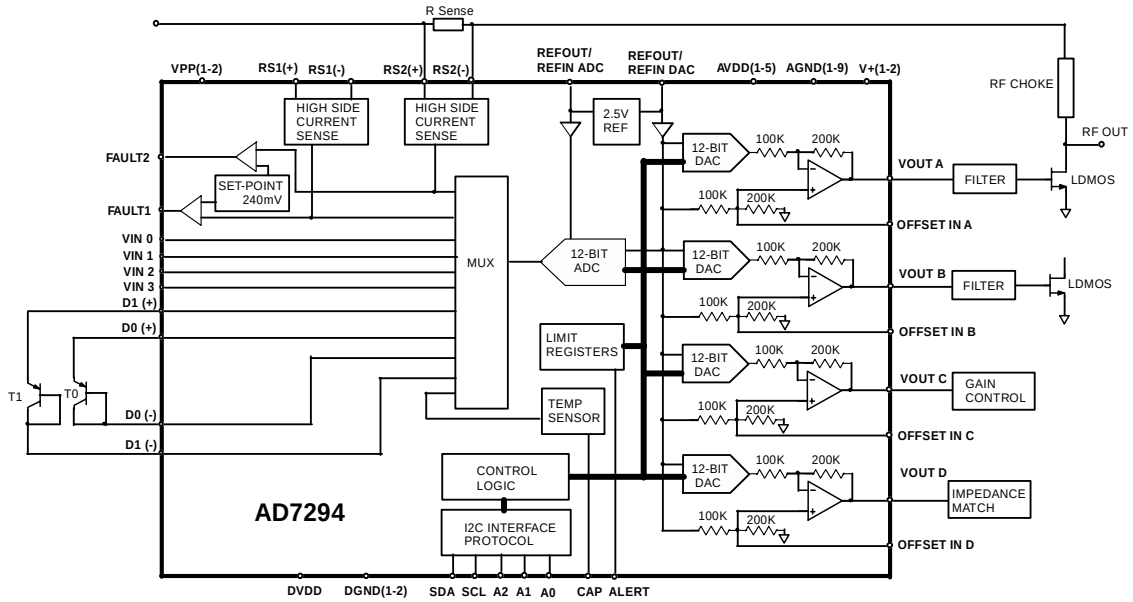


Figure 10. System Diagram

The AD7294 contains all the functions required for general-purpose monitoring and control of current, voltage, and temperature integrated into a single-chip solution. The part includes low voltage (±200 mV) analog-input sense amplifiers for current monitoring across shunt resistors, temperature-sense inputs, and four uncommitted analog input channels multiplexed into a 200 kSPS SAR ADC.

An internal low ppm reference is provided to drive both the DAC and ADC. Four 12-bit DACs provide the outputs for voltage control. The AD7294 also includes limit registers for alarm functions. The limit registers can alert the user to when the ADC outputs go above or below certain predefined values. The part is designed on a high voltage DMOS process for high voltage compliance, 60 V on the current-sense inputs, and up to 15 V DAC output voltage.

The DACs provide digital control with 1.2 mV resolution to control the bias currents of the power transistors; they can also be used to provide control voltages for variable gain amplifiers or impedance-match networks in the main signal chain. Thermal diode based temperature sensors are incorporated to compensate for temperature effects. The high side current sense is specified to manage LDMOS FETs up to 48 V with bias currents ranging from 300 mA to 800 mA and gate voltages of 4 V to 9 V.

The ADC monitors the high-side current and temperature sensors as shown in Figure 11. If the temperature of the LDMOS transistor rises above predetermined limits, out of limit comparisons generate flags. The on-chip DAC will use the digital correction loop to decrease the V_{GS} of the device to maintain the desired output voltage. An external resistor is used to sense the transistors drain current and so automatically control the gate bias voltage of the device.

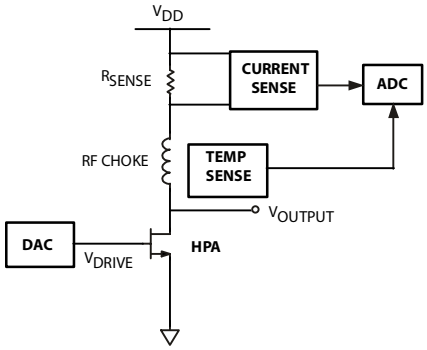


Figure 11. Simplified Diagram of System

The part is ideal for bias current control of the power transistors in power amplifiers employed in CDMA, GSM, EDGE, and UMTS cellular base stations. The I^2C digital interface allows the flexibility of programming the bias points using an external controller. The I^2C bus also allows a number of devices to be connected in parallel to control multiple FETS, the standard in single-carrier and multi-carrier base station systems.

RFPA provide from 2 W to over 200 W of output power per channel and require extremely good linearity to maximize the data throughput in a given channel. The overall performance of an RFPA, for base station transceivers, is dictated by tradeoffs between linearity, efficiency and gain. These tradeoffs lead to an optimum bias condition for the LDMOS PA transistors. Dynamically controlling the drain bias current, in order to maintain a constant value over temperature and time, can

significantly improve the overall performance of the power amplifier.

ADC INFORMATION

The AD7294 consists of a successive 200 kSPS approximation analog-to-digital converter based around a capacitive DAC. The analog input range for the part can be selected to be a 0 V to V_{REF} input or a 2 × V_{REF} input, configured with either single-ended or differential analog inputs. The AD7294 has an on-chip 2.5 V reference that can be overdriven when an external reference is preferred. If the internal reference is to be used elsewhere in a system, the output must be buffered first.

The various monitored and uncommitted input signals are multiplexed into the ADC. The nine channel-allocation address bits select which analog input channel to convert using the multiplexer. Four uncommitted analog input channels are multiplexed to the ADC, VIN (0 to 3). These four channels allow differential and pseudodifferential mode measurements of various system signals.

ADC OPERATION

Figure 12 shows a very simplified schematic of the ADC. The control logic, SAR and capacitive DACs are used to add and subtract fixed amounts of charge from the sampling capacitor arrays to bring the comparator back to a balanced condition.

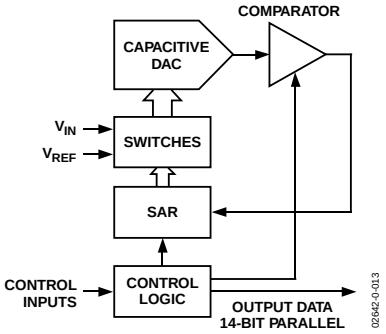


Figure 12. Simplified ADC Block Diagram

Figure 13 and Figure 14 show simplified schematics of the ADC during its acquisition and conversion phases in differential mode, respectively. Figure 13 shows the ADC during its acquisition phase. SW3 is closed, SW1 and SW2 are in Position A, the comparator is held in a balanced condition, and the sampling capacitor arrays acquire the differential signal on the input.

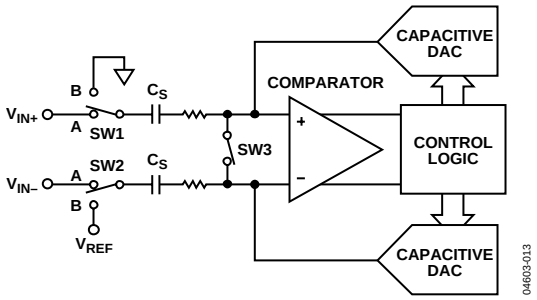


Figure 13. ADC Acquisition Phase

When the ADC starts a conversion, as shown in Figure 14, SW3 opens, and SW1 and SW2 move to Position B, causing the comparator to become unbalanced. Both inputs are disconnected once the conversion begins. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. The output impedances of the sources driving the V_{IN+} and V_{IN-} pins must be matched; otherwise, the two inputs will have different settling times, resulting in errors.

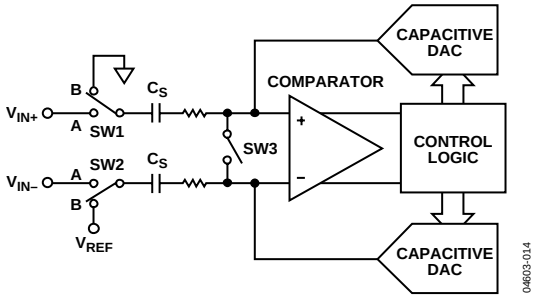


Figure 14. ADC Conversion Phase

ADC TRANSFER FUNCTIONS

The designed code transitions occur at successive integer LSB values (1 LSB, 2 LSB, and so on). In single-ended mode, the LSB size is V_{REF}/4,096 when the 0 V to V_{REF} range is used and 2 × V_{REF}/4,096 when the 0 V to 2 × V_{REF} range is used.

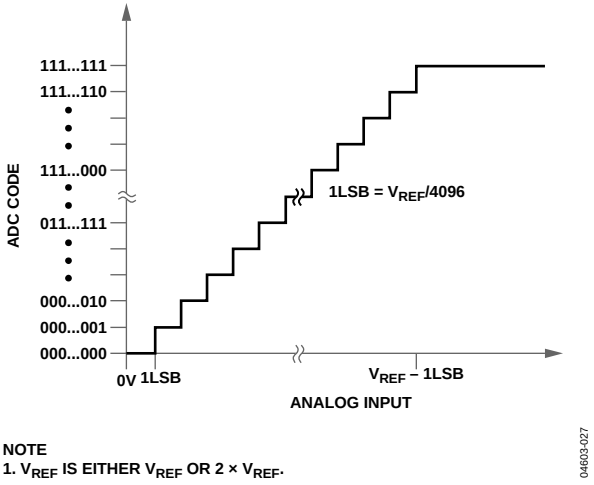


Figure 15. Straight Binary Transfer Characteristic

In differential mode, the LSB size is $2 \times V_{REF}/4{,}096$ when the 0 V to V_{REF} range is used and $4 \times V_{REF}/4{,}096$ when the 0 V to $2 \times V_{REF}$ range is used. The ideal transfer characteristic for the ADC when outputting straight binary coding is shown in Figure 15, and the ideal transfer characteristic for the ADC when outputting twos complement coding is shown in Figure 16 (this is shown with the $2 \times V_{REF}$ range).

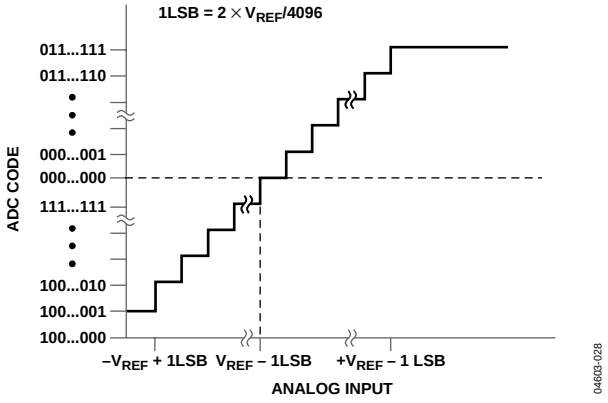


Figure 16. Twos Complement Transfer Characteristic with $V_{REF} \pm V_{REF}$ Input Range

For Channels 1 to 4 in single-ended mode, the output code is straight binary, where 000 = 0 V, FFF = V_{REF}.

In differential mode, the code is twos complement, where 000 =0 V, 7FF = $+V_{REF}$, 800 = $-V_{REF}$, and FFF = 0 V − 1 LSB.

Channels 5 and 6 are twos complement, where 000 = 0 mV, 7FF = +200 mV, 800 = −200 mV, and FFF = 0 V − 1 LSB.

Channels 7 to 9 are twos complement with LSB = 0.25°C, where 000 = 0°C, 7FF = +255.75°C, 800 = −256°C, and FFF = −0.25°C.

ANALOG INPUTS

The AD7294 has a total of four analog inputs. Depending on the configuration register setup, they can be configured as two single-ended inputs, two pseudodifferential channels or two fully differential channels. See the Register Setting section for further details.

Single-Ended Mode

The AD7294 can have four single-ended analog input channels. In applications where the signal source has high impedance, it is recommended to buffer the analog input before applying it to the ADC. The analog input range can be programmed to be either 0 to V_{REF} or 0 to $2 \times V_{REF}$.In 2 × Vref mode, the input is effectively divided by 2 before the conversion takes place, so the input range becomes 0 to $2 \times V_{REF}$. Note that the voltage on the input channel pins with respect to GND cannot exceed VDD.

If the analog input signal to be sampled is bipolar, the internal reference of the ADC can be used to externally bias up this signal so that it is correctly formatted for the ADC. Figure 17 shows a typical connection diagram when operating the ADC in single-ended mode.

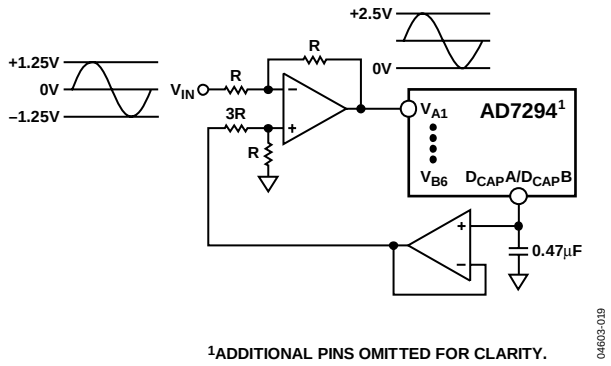


Figure 17. Single-Ended Mode Connection Diagram

Differential Mode

The AD7294 can have two differential analog input pairs. Differential signals have some benefits over single-ended signals, including noise immunity based on the device's common-mode rejection and improvements in distortion performance. Figure 18 defines the fully differential analog input of the AD7294.

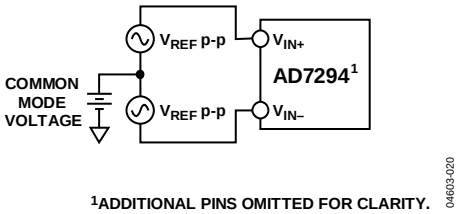


Figure 18. Differential Input Definition

The amplitude of the differential signal is the difference between the signals applied to the V_{IN+} and V_{IN-} pins in each differential pair ($V_{IN+} - V_{IN-}$). For the various differential modes, refer to the ADC Channel Allocation section. The resulting converted data is stored in 2s complement format in the Result Register. V_{IN+} and V_{IN-} should be driven simultaneously by two signals each of amplitude V_{REF} (or $2 \times V_{REF}$, depending on the range chosen) that are 180° out of phase. Assuming the 0 to V_{REF} range is selected, the amplitude of the differential signal is therefore $-V_{REF}$ to $+V_{REF}$ peak-to-peak ($2 \times V_{REF}$), regardless of the common mode (CM).

The common mode is the average of the two signals

$$(V_{IN+} + V_{IN-})/2$$

And is therefore the voltage on which the two inputs are centered.

This results in the span of each input being CM ± $V_{REF}/2$. This voltage has to be set up externally, and its range varies with the reference value, V_{REF}. As the value of V_{REF} increases, the common-mode range decreases. When driving the inputs with an amplifier,

the actual common-mode range is determined by the amplifier's output voltage swing.

Figure 19 and Figure 20 show how the common-mode range typically varies with V_{REF} for a 5 V power supply using the 0 to V_{REF} range or 2 × V_{REF} range, respectively. The common mode must be in this range to guarantee the functionality of the AD7294.

When a conversion takes place, the common mode is rejected, resulting in a virtually noise-free signal of amplitude −V_{REF} to +V_{REF}, corresponding to the digital codes of 0 to 4,096. If the 2 × V_{REF} range is used, the input signal amplitude extends from −2 V_{REF} ($V_{IN}0$ = 0 V , $V_{IN}1$ = V_{REF}) to +2 V_{REF} ($V_{IN}1$ = 0 V , $V_{IN}0$= V_{REF}).

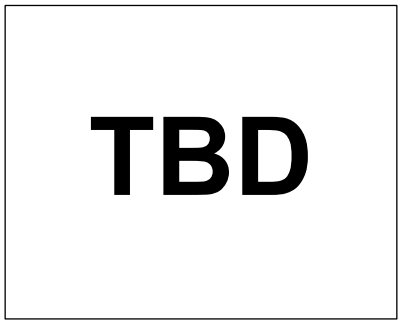


Figure 19. Input Common-Mode Range vs. V_{REF} (0 to V_{REF} Range, V_{DD} = 5 V)

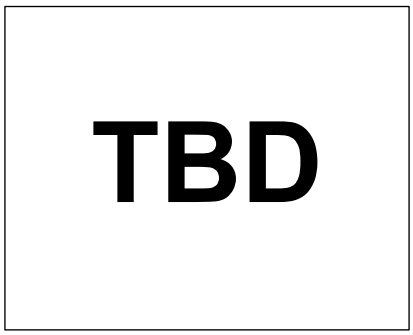


Figure 20. Input Common-Mode Range vs. V_{REF} (2 × V_{REF} Range, V_{DD} = 5 V)

Driving Differential Inputs

The differential modes available on Channels 1 to 4 in Table 7 requires that V_{IN+} and V_{IN-} be driven simultaneously with two equal signals that are 180° out of phase. The common mode must be set up externally. The common-mode range is determined by V_{REF}, the power supply, and the particular amplifier used to drive the analog inputs. Differential modes of operation with either an ac or dc input provide the best THD performance over a wide frequency range. Since not all applications have a signal preconditioned for differential operation, there is often a need to perform single-ended-to-differential conversion.

Using an Op Amp Pair

An op amp pair can be used to directly couple a differential signal to one of the analog input pairs of the AD7294. The circuit configurations illustrated in Figure 21 and Figure 22 show how a dual op amp can be used to convert a single-ended signal into a differential signal for both a bipolar and unipolar input signal, respectively.

The voltage applied to Point A sets up the common-mode voltage. In both diagrams, Point A is connected to the reference, but any value in the common-mode range can be input here to set up the common mode. The AD8022 is a suitable dual op amp that can be used in this configuration to provide differential drive to the AD7294.

Take care when choosing the op amp; the selection depends on the required power supply and system performance objectives. The driver circuits in Figure 21 and Figure 22 are optimized for dc coupling applications requiring best distortion performance. The circuit configuration shown in Figure 21 converts a unipolar, single-ended signal into a differential signal. The differential op amp driver circuit shown in Figure 22 is configured to convert and level shift a single-ended, ground-referenced (bipolar) signal to a differential signal centered at the V_{REF} level of the ADC.

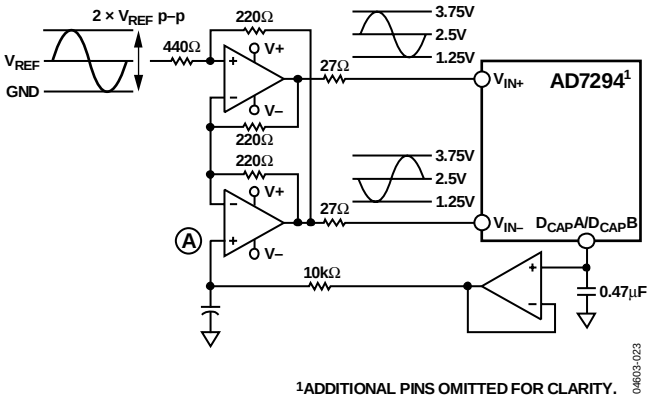


Figure 21. Dual Op Amp Circuit to Convert a Single-Ended Unipolar Signal into a Differential Signal

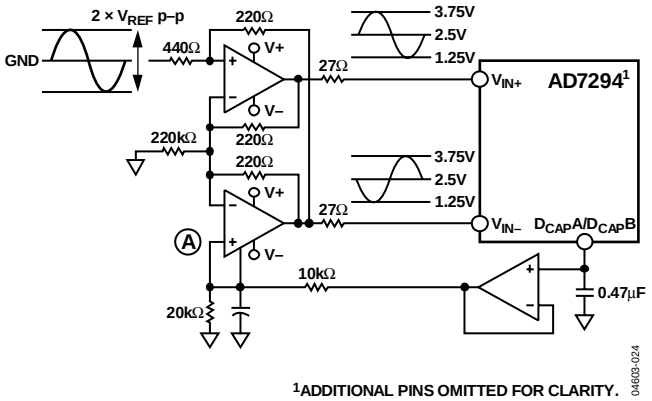


Figure 22. Dual Op Amp Circuit to Convert a Single-Ended Bipolar Signal into a Differential Unipolar Signal

Pseudodifferential Mode

The AD7294 can have two pseudodifferential pairs, see the Configuration Register section for register details. Uncommitted input channels 1 and 2 are a pseudodifferential pair, as are channels 3 and channel 4 . In this mode, V_{IN+} is connected to the signal source, which must have amplitude of V_{REF} (or $2 \times V_{REF}$, depending on the range chosen) to make use of the full dynamic range of the part. A dc input is applied to the V_{IN-} pin. The voltage applied to this input provides an offset from ground or a pseudoground for the V_{IN+} input. Which channel is VIN+ is determined by the ADC channel allocation. The differential mode must be selected in order to operate in the pseudodifferential mode. The resulting converted pseudodifferential data is stored in 2s complement format in the result register.

The governing equation for the pseudodifferential mode, for channel 1 is:

$$V_{OUT} = 2(V_{IN}0 - V_{IN}1) - V_{REF\_ADC}$$

Where $V_{IN}0$ is the single-ended signal on channel 1 and VIN1 is the single-ended signal on channel 2.

The benefit of pseudodifferential inputs is that they separate the analog input signal ground from the ADC's ground, allowing dc common-mode voltages to be cancelled. The typical voltage range for the V_{IN-} pin while in pseudodifferential mode is shown in Figure 23 and Figure 24. Figure 25 shows a connection diagram for pseudodifferential mode.

TBD

Figure 23. V_{IN-} Input Voltage Range vs. V_{REF} in Pseudodifferential Mode with V_{DD} = 3 V

TBD

Figure 24. V_{IN-} Input Voltage Range vs. V_{REF} in Pseudodifferential Mode with V_{DD} = 5 V

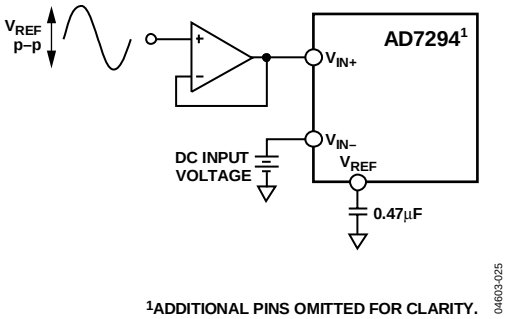


Figure 25. Pseudodifferential Mode Connection Diagram

DIGITAL INPUTS

The digital inputs applied to the AD7294 are not limited by the maximum ratings that limit the analog inputs. Instead, the digital inputs can be applied at up to 7 V and are not restricted by the V_{DD} + 0.3 V limit as are the analog inputs, see the Absolute Maximum Ratings section for more information. Another advantage of the SDA, SCL, and A0 to A2 not being restricted by the V_{DD} + 0.3 V limit is that power supply sequencing issues are avoided. If one of these digital inputs is applied before V_{DD}, there is no risk of latch-up, as there would be on the analog inputs if a signal greater than 0.3 V were applied prior to V_{DD}.

V_{DRIVE}

The AD7294 also has a V_{DRIVE} feature to control the voltage at which the I^2C interface operates. Because the I^2C pins are open-drain, there is not a corresponding V_{DD} pin. The V_{DRIVE} pin should be connected to the supply that the I^2C bus is pulled up to. This is not a supply pin in I^2C mode—it merely sets up the input threshold levels. V_{DRIVE} allows the ADC to easily interface to both 3 V and 5 V processors. For example, if the AD7294 is operated with a V_{DD} of 5 V, the V_{DRIVE} pin can be powered from a 3 V supply, allowing a large dynamic range with low voltage digital processors. Thus, the AD7294 can be used with the $2 \times V_{REF}$ input range with a V_{DD} of 5 V while still being able to interface to 3 V digital parts.

DAC OPERATION

The AD7294 DAC core is a thin film 12-bit string DAC with a 5 V internal buffer to drive the high voltage output stage. The DAC has a range of 0 to 5 V with a 2.5 V reference input. The output span of the DAC, which is controlled by the offset input, can be positioned anywhere between 0 to 15 V. Figure 26 is a block diagram of the DAC architecture. The DAC can maintain 12-bit accuracy for up to a 500 Ω load.

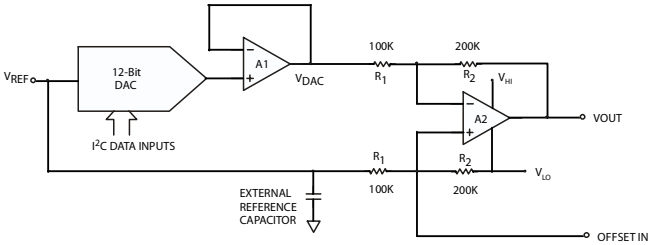


Figure 26. DAC Architecture

To improve functionality of the device, the DAC output is digitally inverted. Therefore, although the input coding to the DAC is straight binary, the ideal output voltage is given by

$$V_{DAC} = V_{REF} - V_{DAC}^*$$

$$\text{Where } V_{DAC}^* = \left[V_{REF} \times \left(\frac{D}{2^n} \right) \right]$$

where *D* is the decimal equivalent of the binary code that is loaded to the DAC register, and *n* is the bit resolution of the DAC.

Table 5. DAC Output Code Table

Digital Input	Analog Output (V)
0000 0000 0000	$V_{REF} - V_{REF}$ (0/4,096)=V_{REF}
0000 0000 0001	$V_{REF} - V_{REF}$ (1/4,096)
1000 0000 0000	$V_{REF} - V_{REF}$ (2048/4,096) = $V_{REF}/2$
1111 1111 1111	$V_{REF} - V_{REF}$ (4095/4,096)

Resistor String

The resistor string structure is shown in Figure 27. It is simply a string of 2^n resistors, each of value R. The code loaded to the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. This architecture is inherently monotonic, voltage out, and low glitch. It is also linear due to the fact that all of the resistors are of equal value.

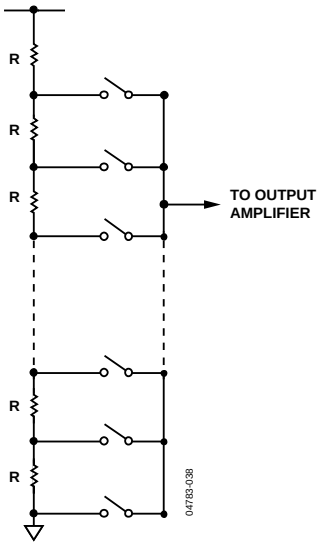


Figure 27. Resistor String Structure

Output Amplifier

Referring to Figure 26, the purpose of A1 is to buffer the DAC output range from 0 V to V_{REF}. The second amplifier, A2, is configured such that when an offset is applied to OFFSET IN, its output voltage is three times the offset voltage minus twice the DAC voltage.

$$V_{OUT} = 3V_{OFFSET} - 2V_{DAC}$$

The DAC word is digitally inverted on-chip such that

$$V_{OUT} = 3V_{OFFSET} + 2(V_{DAC}^* - V_{REF})$$

The user has the option of leaving the offset pin open, in which case the voltage on the noninverting input of op amp, A2, is set by the resistor divider, giving

$$V_{OUT} = 2V_{DAC}$$

This generates the 5 V output span from a 2.5 V reference. Digitally inverting the DAC allows the circuit to operate as a generic DAC when no offset is applied.

The DACs provide digital control with 1.2 mV resolution to control the bias currents of the power transistors. The DAC output buffer, A2, is capable of driving a 1 nF capacitor with current source and sink capabilities of 10 mA to within 200 mV off the supply. The output buffer has a supply range of 20 V with a slew rate of 1 V/μs. Current limiting should take effect at about 40 mA. Note that a significant amount of power could be dissipated in this situation; a thermal shutdown circuit will set the DAC outputs to high impedance if a die temperature of >150°C is measured by the internal temperature sensor.

CURRENT SENSOR

Two current-sense amplifiers are provided, which can accurately amplify small differential current shunt voltages in the presence of rapidly changing common mode voltages. Each accepts a (V_{PP}) ±200 mV full-scale input voltage and supplies a (VCC/2) ± 2.5 V signal to the ADC.

The current sense in the AD7294 is a high-side current sense amplifier, which allows for the monitoring of currents on the V_{DD} line ranging from AVDD up to 48 V, see Figure 28. The sense amplifier works correctly for common mode voltages on RS(−) and RS(+) of between 47 V (VPP − 1 V) and 48.2 V (VPP + 200 mV). It gives a full scale output to the ADC for a differential input of ± 200 mV, e.g. 48 V on RS+ and 47.8 on RS−. An input signal of greater than 240 mV magnitude should trigger an alert. An alert will also be triggered if the common mode voltages on RS+ and RS− go outside the specified limits, as the amplifier will no longer be in its linear region. The inputs can be sampled at approximately 6 µs intervals, giving a Nyquist frequency of approximately 160 KHz.

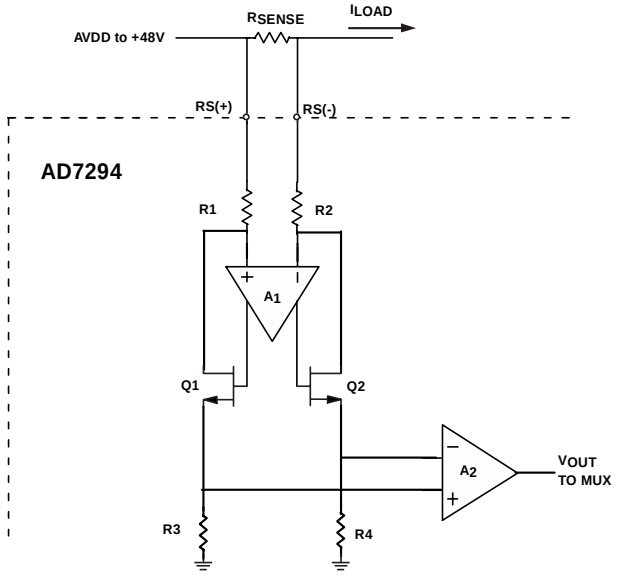


Figure 28. High-Side Current Sense

The AD7294 is comprised of two main blocks, a differential and an instrumentation amplifier. A load current flowing through the external shunt resistor produces a voltage at the input terminals of the AD7294. The input terminals are connected to the differential amplifier (A1) by Resistors R1 and R2. A1 nulls the voltage appearing across its own input terminals by adjusting the current through R1 and R2 with transistors Q1 and Q2. When the input signal to the AD7294 is 0, the currents in R1 and R2 are equal. When the differential signal is nonzero, the current increases through one of the resistors and decreases in the other. The current difference is proportional to the size and polarity of the input signal. Since the differential input voltage is converted into a current, common-mode rejection is no longer reliant on resistor matching, and high accuracy and performance is provided throughout the wide common-mode voltage range. The amplifier is chopper stabilized with a switching frequency of approximately 300kHz.

The differential currents through QI and Q2 are converted into a differential voltage due to R3 and R4. A2 is configured as an instrumentation amplifier, and this differential input signal is converted into a single-ended output voltage by A2. The gain is internally set with thin-film resistors to 12.5V/V. Hence for an input voltage of ± 200 mV an output span of ± 2.5 V will be generated.

Note that when using the external reference for the ADC, the maximum I_{SENSE} input span is 240 mV with a gain of 12.5 in the I_{SENSE} amplifier. Therefore, the maximum usable span on the ADC is 3 V. If an external reference of 5 V is required by the user, only 60% the ADC span will be used for the I_{SENSE} conversion.

Choosing R_{SENSE}

The AD7294 current sense has a specified full-scale sense range of 200 mV. In applications monitoring very high currents, R_{SENSE} must be able to dissipate the I^2R losses. If the resistor's rated power dissipation is exceeded, its value may drift or it may fail altogether, causing a differential voltage across the terminals in excess of the absolute maximum ratings. If I_{SENSE} has a large high frequency component, care should be taken to choose a resistor with low inductance. Wire-wound resistors have the highest inductance, metal-film resistors are somewhat better, and low inductance metal-film resistors are best suited for these applications.

Kelvin Sense Resistor Connection

When using a low value sense resistor for high current measurement, the problem of parasitic series resistance can arise. The lead resistance can be a substantial fraction of the rated resistance, making the total resistance a function of lead length. This problem can be avoided by using a Kelvin sense connection. This type of connection separates the current path through the resistor and the voltage drop across the resistor. Figure 29 shows the correct way to connect the sense resistor between the VCC and SENSE pins of the AD7294.

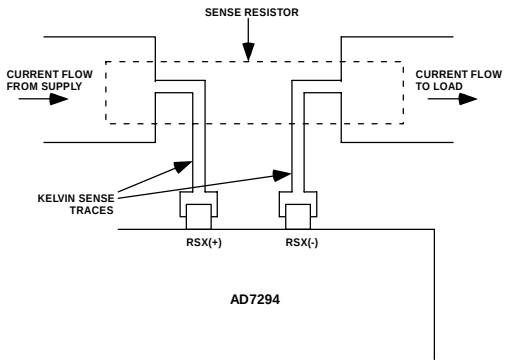


Figure 29. Kelvin Sense Connections

TEMPERATURE SENSOR

The AD7294 consists of one local and two remote temperature sensors. The analog input multiplexer can alternately select either the on-chip band gap temperature sensor, to measure the temperature of the system, or one of the two remote diode temperature sensors. The 12-bit ADC digitizes these signals, and the results are stored in the T_{SENSE}INT, T_{SENSE}1, and T_{SENSE}2 registers. These results are compared with their respective $DATA_{LOW}$, $DATA_{HIGH}$, and hysteresis registers. Out-of-limit comparisons generate flags, and further information on these are stored in the alert registers. A result that exceeds the high temperature limit, the low temperature limit, or an external diode fault causes the ALERT output to assert high.

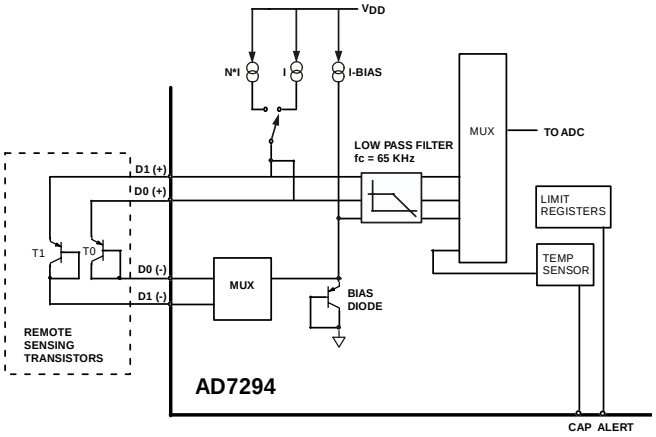


Figure 30. Internal and Remote Temperature Sensors

The temperature reading from the ADC is stored in a 10-bit twos complement format and in a sign bit format, D10 to D0, to accommodate both positive and negative temperature measurements. The temperature data format is shown in Table 6, which shows the achievable temperature measurement range. The ADC can theoretically measure a 512°C temperature span, ranging from −256°C to +255.75°C with an LSB of 0.25°C.

The temperature sensor module on the AD7294 is based on the 3-current principle, see Figure 30, where three currents are passed through a diode and the forward voltage drop is measured at each diode, allowing the temperature to be calculated free of errors caused by series resistance.

Each input is integrated in turn over a period of several hundred microseconds. This takes place continuously in the background, leaving the user free to perform conversions on the other channels. When integration is complete, a signal is passed to the control logic to automatically initiate a conversion. If the ADC is in command mode, the temperature conversion is performed as soon as the next conversion is completed. In autocycle mode, the conversion is inserted into an appropriate place in the current sequence; see the Register Setting section for further details. If the ADC is idle, the conversion takes place immediately.

Three registers store the result of the last conversion on each temperature channel; these can be read at any time. In addition, in command mode, one or both of the two external channel registers can be read out as part of the output sequence. The MSB of the registers is set if an open-circuit condition is detected on the input of the external sensors, indicating an invalid result.

Table 6. T_{SENSE} Data Format

Digital Input	Bit Weight (°C)
111 1111 1111	−0.25
100 0000 0000	−256
011 1111 1111	+255.75
000 0000 0000	+0.0

Remote Temperature Sensing

The AD7294 can measure the temperature of two remote diode sensors or diode-connected transistors connected from D0(+) to D0(−) and from D1(+) to D1(−).

The forward voltage of a diode or diode-connected transistor operated at constant current exhibits a negative temperature coefficient of about 2 mV/°C. Unfortunately, the absolute value of V_{BE} varies from device to device, and individual calibration is required to null this; therefore, the technique is unsuitable for mass production.

The technique used in the AD7294 is to measure the change in V_{BE} when the device is operated at three different currents, see Figure 30.

This is given by

$$\Delta V_{BE} = KT/q \times 1n(N)$$

where:
K is Boltzmann's constant.
q is the charge on the carrier.
T is the absolute temperature in Kelvin.
N is the ratio of the two currents.

If a discrete transistor is used for T1 and T0, such as a 2N3904/2N3906, the collector is not grounded and should be linked to the base. If a PNP transistor is used, the base is connected to the D− input and the emitter to the D+ input. If an NPN transistor is used, the emitter is connected to the D− input and the base to the D+ input. Figure 31 and Figure 32 show how to connect the AD7294 to an NPN or PNP transistor for temperature measurement. To prevent ground noise from interfering with the measurement, the more negative terminal of the sensor is not referenced to ground, but is biased above ground by an internal diode at the D− input.

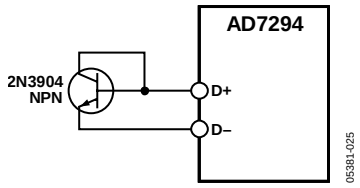


Figure 31. Measuring Temperature Using an NPN Transistor

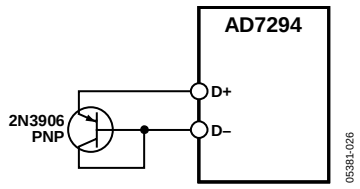


Figure 32. Measuring Temperature Using a PNP Transistor

To measure ΔV_{BE}, the sensor is switched between operating currents of I and N × I. The resulting waveform is passed through a 65 kHz low-pass filter to remove noise, and to a chopper-stabilized amplifier that performs the functions of amplification and rectification of the waveform to produce a dc voltage proportional to ΔV_{BE}. This voltage is measured by the ADC to give a temperature output in 10-bit, twos complement format.

Series Resistance Cancellation

Parasitic resistance to the D+ and D– inputs to the AD7294, seen in series with the remote diode, is caused by a variety of factors, including PCB track resistance and track length. This series resistance appears as a temperature offset in the remote sensor's temperature measurement. This error typically causes a 0.5°C offset per ohm of parasitic resistance in series with the remote diode.

The AD7294 automatically cancels out the effect of this series resistance on the temperature reading, giving a more accurate result, without the need for user characterization of this resistance. The AD7294 is designed to automatically cancel typically up to 3 kΩ of resistance. By using an advanced temperature measurement method, this is transparent to the user. This feature allows resistances to be added to the sensor path to produce a filter, allowing the part to be used in noisy environments.

Noise Filtering

For temperature sensors operating in noisy environments, previous practice was to place a capacitor across the D+ pin and D– pin to help combat the effects of noise. However, large capacitances affect the accuracy of the temperature measurement, leading to a recommended maximum capacitor value of 1000 pF.

This capacitor reduces the noise, but does not eliminate it. Sometimes, this sensor noise is a problem in a very noisy environment. In most cases, a capacitor is not required as differential inputs, by their very nature, have a high immunity to noise.

Remote Sensing Diode

The AD7294 is designed to work with either substrate transistors built into RF front end gain stages or with discrete transistors. Substrate transistors are generally PNP types with the collector connected to the substrate. Discrete types can be either PNP or NPN transistors connected as a diode (base-shorted to the collector). If an NPN transistor is used, the collector and base are connected to D+ and the emitter to D–. If a PNP transistor is used, the collector and base are connected to D– and the emitter is connected to D+.

To reduce the error due to variations in both substrate and discrete transistors, a number of factors should be taken into consideration:

- The ideality factor, n_f, of the transistor is a measure of the deviation of the thermal diode from ideal behavior. The AD7294 is trimmed for an n_f value of 1.008. Use the following equation to calculate the error introduced at a temperature T (°C), when using a transistor whose n_f does not equal 1.008. See the processor data sheet for the n_f values.

  $$\Delta T = (n_f - 1.008) \times (273.15\ \text{K} + T)$$

  To factor this in, the user can write the ΔT value to the offset register. The AD7294 then automatically adds it to or subtracts it from the temperature measurement.

- Some HPA manufacturers specify the high and low current levels of the substrate transistors. The high current level of the AD7294, I_{HIGH}, is 128 μA and the low level current, I_{LOW}, is 8 μA. If the AD7294 current levels do not match the current levels specified by the HPA manufacturer, it might be necessary to remove an offset. The HPA's data sheet advises whether this offset needs to be removed and how to calculate it. This offset can be programmed to the offset register. If more than one offset must be considered, the algebraic sum of these offsets must be programmed to the offset register.

If a discrete transistor is used with the AD7294, the best accuracy is obtained by choosing devices according to the following criteria:

- Base-emitter voltage greater than 0.25 V at 11 μA, at the highest operating temperature.
- Base-emitter voltage less than 0.95 V at 180 μA, at the lowest operating temperature.
- Base resistance less than 100 Ω.
- Small variation in h_{FE} (approximately 50 to 150) that indicates tight control of V_{BE} characteristics.

Transistors, such as 2N3904, 2N3906, or equivalents in SOT-23 packages, are suitable devices to use.

REFERENCE FOR ADC/DAC

The internal reference on the AD7294 is a well regulated, low ppm 2.5 V reference with low drift voltage and a stable output. The reference is common to all four DAC channels and the SAR ADC. If the application requires an external reference, it can be applied to the REFOUT/REFIN DAC pin or to the REFOUT/ REFIN ADC pin. If the reference is driving external nodes, a buffer is required to achieve a low impedance output. For stability, the reference buffers each require at least 470 nF on the output pin. Note that on power up, the ADC and DAC reference buffers are switched off by default ; note the power-down register in the Register Setting section.

When using an external reference to achieve the desired performance from the AD7294, thought should be given to the choice of a precision voltage reference. There are four possible sources of error that should be considered when choosing a voltage reference for high accuracy applications: initial accuracy, ppm drift, long-term drift, and output voltage noise. To minimize these errors, a reference with high initial accuracy is preferred. In addition, choosing a reference with an output trim adjustment, such as the on-chip internal reference or the AD431, allows a system designer to trim system errors by setting a reference voltage to a voltage other than the nominal.

Long-term drift is a measure of how much the reference drifts over time. A reference with a tight long-term drift specification ensures that the overall solution remains stable during its entire lifetime. If choosing an external reference, consider a tight temperature coefficient specification to reduce the temperature dependence of the system output voltage on ambient conditions.

ANALOG COMPARATOR LOOP

The AD7294 consists of two setpoint comparators that are used for independent analog control. The advantage of using analog control for current sensing is the dynamic speed of the analog loop vs. the speed of the digital loop, in that the analog control loop does not have the digital delays inherent in ADC-to-DAC signal processing. A 240 mV fixed setpoint is used in the comparator to sense high currents.

APPLICATIONS

The overall performance of a PA configuration is determined by the tradeoffs in efficiency, gain, and linearity. The AD7294 is used in a PA signal chain to achieve the optimal bias for the LDMOS bias transistor. The main factors influencing the bias conditions are temperature, supply voltage, gate voltage drift, and general processing parameters. The AD7294 contains all the functions required for general-purpose monitoring and control of current, voltage, and temperature.

Depending on the signal chain, a number of amplifiers can be used in predrive and drive modes prior to the PA final stage to increase the overall power gain of the signal, see Figure 33 .

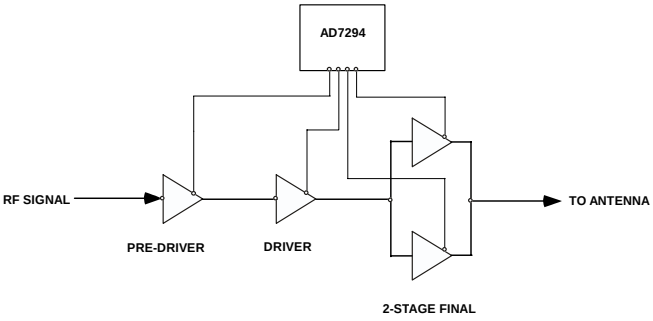


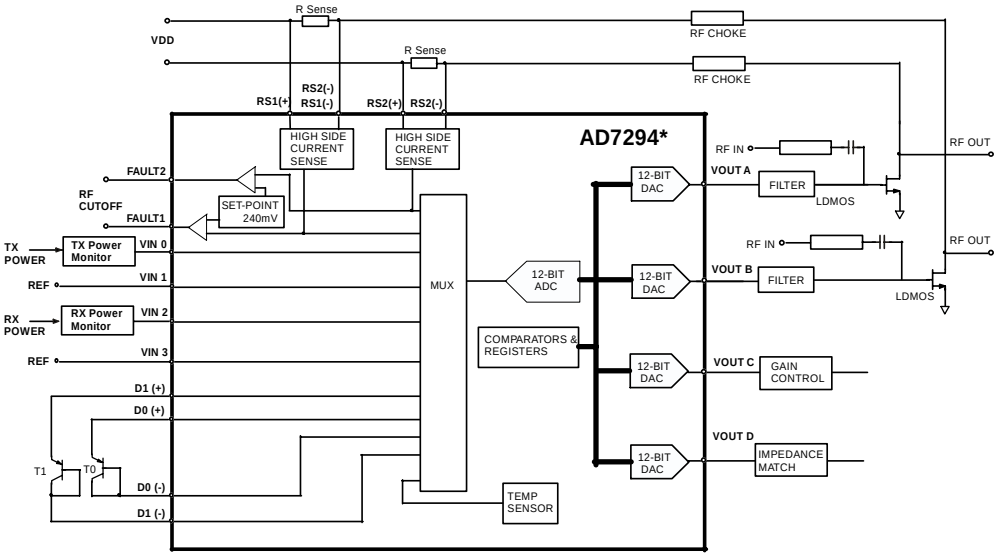
Figure 33. Typical HPA Signal Chain

This addition of power gain has an adverse effect on the overall efficiency of the PA. To minimize the degradation of the PA's efficiency, the drivers must be monitored and controlled to optimize performance.

TYPICAL RF FRONT-END APPLICATION

The circuit in Figure 34 is a typical application for the AD7294. The device is used to monitor and control the overall performance of a two final stage amplifiers. The gain control and phase adjustment of the driver stage are incorporated in the application and are carried out by the two available uncommitted outputs of the AD7294. Both high-side current senses measure the amount of current on the respective final stage amplifiers. The comparator output, RF cutoff, is the controlling signal for a switch on the RF input of the LDMOS power FET. If the high-side current sense reads a value above a specified limit compared with the setpoint, the RF IN signal is switched off by the comparator.

By measuring the transmitted power (Tx) and the received power (Rx), the device can dynamically change the drivers and PA signal to optimize performance. This application requires a logarithmic detector/controller, such as Analog Devices AD8317.

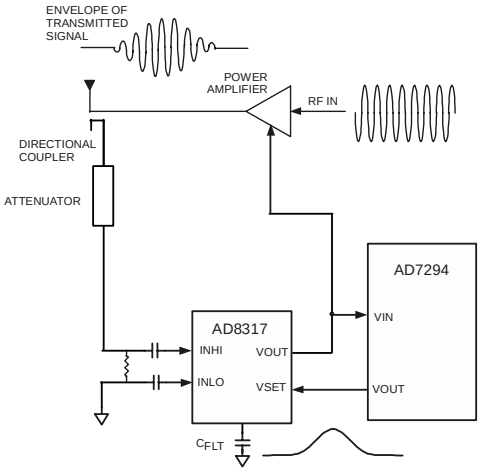


* ADDITIONAL PINS OMITTED FOR CLARITY

Figure 34. Typical HPA Monitor and Control Application

GAIN CONTROL OF PA

In this mode, a setpoint voltage, proportional in dB to the desired output power, is applied to a Logarithmic Amplifier such as the AD8317. A sample of the output power from the PA, via a directional coupler and attenuator (or by other means), is fed to the input of the AD8317. The V_{OUT} is connected to the gain control terminal of the PA. Based on the defined relationship between V_{OUT} and the RF input signal, the AD8317 will adjust the voltage on V_{OUT} (V_{OUT} is now an error amplifier output) until the level at the RF input corresponds to the applied V_{SET}. The AD7294 completes a feedback loop, which can track the output of the AD8317 and adjust the V_{SET} input of the AD8317 accordingly.



. Setpoint Controller Operation

V_{OUT} of the AD8317 is applied to the gain control terminal of the power amplifier. In order for this output power control loop to be stable, a ground-referenced capacitor must be connected to the C_{FLT} pin. This capacitor integrates the error signal (which is actually a current) that is present when the loop is not balanced. In a system where a Variable Gain Amplifier or Variable Voltage Attenuator feeds the power amp only one AD8317 is required. In such a case the gain on one of the parts (VVA, PA) is fixed and V_{OUT} feeds the control input of the other.

REGISTER SETTING

The AD7294 contains 43 internal registers (see Figure 35) that are used to store conversion results, high and low conversion limits, and information to configure and control the device. There are 42 data registers and one address pointer register.

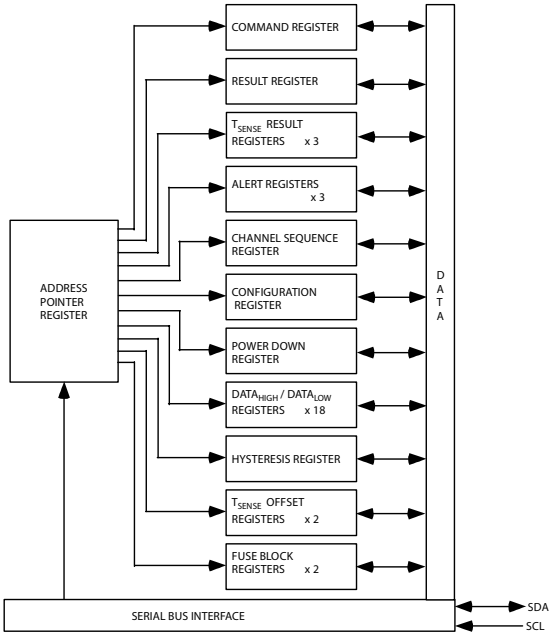


Figure 35. AD7294 Register Structure

Each data register has an address to which the address pointer register points when communicating with it. The command register and fuse block registers are the only registers that are write-only registers; the rest are read/write registers.

ADDRESS POINT REGISTER

The address pointer register does not have and does not require an address, because it is the register to which the first data byte of every write operation is written automatically. The address pointer register is an 8-bit register, in which the 6 LSBs are used as pointer bits to store an address that points to one of the AD7294's data registers. The first byte following each write address is the address of one of the data registers, which is stored in the address pointer register and selects the data register to which subsequent data bytes are written. On power-up, the address pointer register contains all 0s, pointing to the command register.

ADC CHANNEL ALLOCATION

These nine channel address bits select which analog input channel is to convert using the multiplexer, see Table 7. Choosing Channels 1 to 4 selects the standard analog voltage inputs. Channels 5 and 6 represent the analog-input sense amplifiers for current monitoring. Channel 7 and 8 designate the use of the external temperature-sensing diodes, whereas Channel 9 represents the internal temperature sensor.

Table 7. ADC Channel Allocation

Channel	Function	Channel ID
CH1	$V_{IN}0$ or ($V_{IN}0 - V_{IN}1$)	000
CH2	$V_{IN}1$ or ($V_{IN}1 - V_{IN}0$)	001
CH3	$V_{IN}2$ or ($V_{IN}2 - V_{IN}3$)	010
CH4	$V_{IN}3$ or ($V_{IN}3 - V_{IN}2$)	011
CH5	$I_{SENSE}1$	100
CH6	$I_{SENSE}2$	101
CH7	$T_{SENSE}1$	110
CH8	$T_{SENSE}2$	111
CH9	$T_{SENSE}INT$	–

There are two modes of operation with respect to the ADC. In command mode, a sequence is written to the ADC, and on subsequent reads, the next channel in the sequence is converted as the current sequence is read out. In autocycle mode, a sequence is programmed, and then the ADC automatically cycles through the selected channels, outputting an alert if one of the channels goes outside its preset range.

COMMAND REGISTER

Writing in this register puts the part into command mode. While in command mode, the part cycles through the selected channels on each subsequent read. If the external T_{SENSE} channels are selected in the command word, it is not actually requesting a conversion, but the result of the last automatic conversion will be output in sequence. See the Channel Sequence Register section for information on autocycle mode.

Table 8. Address Pointer Byte—Command Bits

Parameter	Function
C1	Convert on CH1
C2	Convert on CH2
C3	Convert on CH3
C4	Convert on CH4
C5	Convert on $I_{SENSE}1$
C6	Convert on $I_{SENSE}2$
C7	Read out last result from $T_{SENSE}1$
C8	Read out last result from $T_{SENSE}2$

RESULT REGISTER

The result register is a 16-bit read/write register. Writing to this register sets the DAC1 output code. The register consists of bits D14 to D12 to identify the ADC channel allocation. Bits D11 to D0, in the result register, are the data bits sent to DAC1. While the MSB, D15, is reserved as an Alert_Flag bit. The Alert_Flag bit indicates whether the conversion result being read or any other channel result has violated the limit registers associated with it. If an alert occurs, the master may wish to read the alert status register to obtain more information on where the alert occurred if the Alert_Flag bit is set.

Table 9 shows the contents of the first byte to read from the AD7294; Table 10 shows the contents of the second byte read.

Table 9. Result Register (First Read)

MSB							LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Alert_Flag	CH_{ID2}	CH_{ID1}	CH_{ID0}	M S B	B10	B9	B8

Table 10. Result Register (Second Read)

MSB							LSB
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
B7	B6	B5	B4	B3	B2	B1	B0

Table 11. AD7294 Register Addresses

P7	P6	P5	P4	P3	P2	P1	P0	Registers
0	0	0	0	0	0	0	0	Command register (W)
0	0	0	0	0	0	0	1	Result register (R)/DAC1 value (W)
0	0	0	0	0	0	1	0	$T_{SENSE}1$ result (R)/DAC2 value (W)
0	0	0	0	0	0	1	1	$T_{SENSE}2$ result (R)/DAC3 value (W)
0	0	0	0	0	1	0	0	T_{SENSE}INT result (R)/DAC4 value (W)
0	0	0	0	0	1	0	1	Alert Register A (R/W)
0	0	0	0	0	1	1	0	Alert Register B (R/W)
0	0	0	0	0	1	1	1	Alert Register C (R/W)
0	0	0	0	1	0	0	0	Channel sequence register (R/W)
0	0	0	0	1	0	0	1	Configuration register (R/W)
0	0	0	0	1	0	1	0	Power-down register (R/W)
0	0	0	0	1	0	1	1	$DATA_{LOW}$ register CH1 (R/W)
0	0	0	0	1	1	0	0	$DATA_{HIGH}$ register CH1 (R/W)
0	0	0	0	1	1	0	1	Hysteresis register CH1 (R/W)
0	0	0	0	1	1	1	0	$DATA_{LOW}$ register CH2 (R/W)
0	0	0	0	1	1	1	1	$DATA_{HIGH}$ register CH2 (R/W)
0	0	0	1	0	0	0	0	Hysteresis register CH2 (R/W)
0	0	0	1	0	0	0	1	$DATA_{LOW}$ register CH3 (R/W)
0	0	0	1	0	0	1	0	$DATA_{HIGH}$ register CH3 (R/W)
0	0	0	1	0	0	1	1	Hysteresis register CH3 (R/W)
0	0	0	1	0	1	0	0	$DATA_{LOW}$ register CH4 (R/W)
0	0	0	1	0	1	0	1	$DATA_{HIGH}$ register CH4 (R/W)
0	0	0	1	0	1	1	0	Hysteresis register CH4 (R/W)
0	0	0	1	0	1	1	1	$DATA_{LOW}$ register $I_{SENSE}1$ (R/W)
0	0	0	1	1	0	0	0	$DATA_{HIGH}$ register $I_{SENSE}1$ (R/W)
0	0	0	1	1	0	0	1	Hysteresis register $I_{SENSE}1$ (R/W)
0	0	0	1	1	0	1	0	$DATA_{LOW}$ register $I_{SENSE}2$ (R/W)
0	0	0	1	1	0	1	1	$DATA_{HIGH}$ register $I_{SENSE}2$ (R/W)
0	0	0	1	1	1	0	0	Hysteresis register $I_{SENSE}2$ (R/W)
0	0	0	1	1	1	0	1	$DATA_{LOW}$ register $T_{SENSE}1$ (R/W)
0	0	0	1	1	1	1	0	$DATA_{HIGH}$ register $T_{SENSE}1$ (R/W)
0	0	0	1	1	1	1	1	Hysteresis register $T_{SENSE}1$ (R/W)
0	0	1	0	0	0	0	0	$DATA_{LOW}$ register $T_{SENSE}2$ (R/W)
0	0	1	0	0	0	0	1	$DATA_{HIGH}$ register $T_{SENSE}2$ (R/W)
0	0	1	0	0	0	1	0	Hysteresis register $T_{SENSE}2$ (R/W)
0	0	1	0	0	0	1	1	$DATA_{LOW}$ register T_{SENSE}INT (R/W)
0	0	1	0	0	1	0	0	$DATA_{HIGH}$ register T_{SENSE}INT (R/W)
0	0	1	0	0	1	0	1	Hysteresis register T_{SENSE}INT (R/W)
0	0	1	0	0	1	1	0	$T_{SENSE}1$ offset register (R/W)
0	0	1	0	0	1	1	1	$T_{SENSE}2$ offset register (R/W)

$T_{SENSE}1$, $T_{SENSE}2$ RESULT REGISTERS

Registers $T_{SENSE}1$ and $T_{SENSE}2$ are 16-bit read/write registers. General alert is flagged by the MSB, D15. Bits D14 to D12 are reserved for the ADC channel allocation. D11 is reserved for flagging diode open-circuits. The temperature reading from the ADC is stored in a 10-bit twos complement format plus a sign bit, D10 to D0. Writing to the $T_{SENSE}1$ register sets the DAC2 output code while writing to the $T_{SENSE}2$ register sets the DAC3 output code.

T_{SENSE}INT RESULT REGISTER

The T_{SENSE}INT register is a 16-bit read/write register used to store the ADC data generated from the internal temperature sensor. Similar to the $T_{SENSE}1$ and $T_{SENSE}2$ result registers, this register stores the temperature readings from the ADC in a 10-bit twos complement format and in a sign bit format, D10 to D0, and uses the MSB as a general alert flag. However, Bits D14 to D11 are not used. In the case of the internal temperature, it is not possible to read it via the ADC result register; instead, the user should point to the T_{SENSE}INT register and read the result of the last conversion from there. Conversions take place approximately every 5 ms. Writing to this register sets the DAC4 output code. The temperature data format in Table 6 also applies to the internal temperature sensor data.

T_{SENSE} OFFSET REGISTERS

Due to the high frequency clock signals of the system, some temperature errors can be attributable to noise coupled onto the D+/D− lines of the remote temperature sensors even when the layout guidelines are followed. Constant high frequency noise usually attenuates/increases the temperature measurements by a linear constant value. The AD7294 has temperature offset 8-bit twos complement registers for both Remote Channels $T_{SENSE}1$ and $T_{SENSE}2$. By completing a one-time calibration of the system, the user can determine the offset caused by system board noise and null it using the offset registers. The offset registers for $T_{SENSE}1$ and $T_{SENSE}2$ are 8-bit read/write registers that store data in a twos complement format. This data is subtracted from the temperature readings taken by $T_{SENSE}1$ and $T_{SENSE}2$ temperature sensors. The offset is carried out before the values are stored in the result register.

Table 12. TSENSE Offset Data Format

Digital Input	Bit Weight (°C)
1111 1111	− 0.25
1000 0000	− 32
0111 1111	+ 31.75
0000 0000	+ 0.0

ALERT STATUS REGISTERS

The alert status registers are 8-bit read/write registers that provides information on an alert event. If a conversion results in activating the ALERT pin or Alert_Flag bit in the result register or T_{SENSE} registers, the alert status register can be read to gain further information.

Register A , see Table 13, consists of four channels with two status bits per channel, one corresponding to each of the $DATA_{HIGH}$ and $DATA_{LOW}$ limits. It stores the alert event data for Channels 1 to 4, which are the standard voltage inputs. The bit with a status of 1 shows where the violation occurred—that is, on which channel—and whether the violation occurred on the upper or lower limit. If a second alert event occurs on another channel between receiving the first alert and interrogating the alert status register, the corresponding bit for that alert event is also set.

Register B, see Table 14, reserves two bits for user input. It also consists of three channels with two status bits per channel, representing the specified $DATA_{HIGH}$ and $DATA_{LOW}$ limits. Bits B3 to B0 correspond to the high and low limit alerts for the current sense inputs. Bits B5 to B4 represent the I_{SENSE} over the full-scale range of 200 mV.

Register Cs most significant bit, see Table 15, is used to alert the user if an open diode flag occurs on the external temperature sensors. An over temperature alert for the external temperature sensor occupies C6. The remaining 6 bits in this register are used to store alert event data for channels 7 to 9 with two status bits per channel, one corresponding to each of the $DATA_{HIGH}$ and $DATA_{LOW}$ limits.

The entire contents of the alert status register can be cleared by writing 1 to bit D1 and 1 to bit D2 in the configuration register, as shown in Table 17. This can also be achieved by writing all 1s to the alert status register itself. Therefore, if the alert status register is addressed for a write operation, which is all 1s, the contents of the alert status register are cleared or reset to all 0s.

CHANNEL SEQUENCE REGISTER

The channel sequence register is an 8-bit read/write register that allows the user to sequence the ADC conversions in autocycle mode. This mode must first be selected in the configuration register, see. This is an extremely useful mode, for example, when checking for alerts on a channel. On power-up, the channel sequence register contains all 0s, thus disabling automatic cycle operation of the AD7294. To enable the automatic cycle mode, the user must write a 1 to the desired channel. Autocycle mode can be activated on the channels shown in Table 16.

The temperature sense channels, including T_{SENSE}INT, are a special case. The conversions on these channels take place automatically, unless the temperature sense circuit is powered down, either after certain other conversions or in other quiet times. This is transparent to the user.

CONFIGURATION REGISTER

The configuration register is a 16-bit read/write register that is used to set the operating modes of the AD7294. The bit functions of the configuration register are outlined in. Table 17

Table 13. Alert Status Register A

Alert Bit	A7	A6	A5	A4	A3	A2	A1	A0
Function	CH4 high alert	CH4 low alert	CH3 high alert	CH3 low alert	CH2 high alert	CH2 low alert	CH1 high alert	CH1 low alert

Table 14. Alert Status Register B

Alert Bit	B7	B6	B5	B4	B3	B2	B1	B0
Function	Reserved	Reserved	$I_{SENSE}2$ overrange	$I_{SENSE}1$ overrange	$I_{SENSE}2$ high alert	$I_{SENSE}2$ low alert	$I_{SENSE}1$ high alert	$I_{SENSE}1$ low alert

Table 15. Alert Status Register C

Alert Bit	C7	C6	C5	C4	C3	C2	C1	C0
Function	Open-diode flag	Over-temp alert	CH9 high alert	CH9 low alert	CH8 high alert	CH8 low alert	CH7 high alert	CH7 low alert

Table 16. Channel Sequence Register

Channel Bit	D7	D6	D5	D4	D3	D2	D1	D0
Function	Reserved	Reserved	$I_{SENSE}2$	$I_{SENSE}1$	CH4	CH3	CH2	CH1

Table 17. Configuration Register Bit Function Description

Config. Bit	Comment
D15	Reserved
D14	Enable noise-delayed sampling. Used to delay critical sample intervals from occurring when there is activity on the I^2C bus.
D13	Enable noise-delayed bit trials. Used to delay critical bit trials from occurring when there is activity on the I^2C bus.
D12	Enable autocycle mode.
D11	Enable pseudodifferential mode for CH3/CH4
D10	Enable pseudodifferential mode for CH1/CH2
D9	Enable differential mode for CH3/CH4
D8	Enable differential mode for CH1/CH2
D7	Enable 2 V_{REF} range on CH4
D6	Enable 2 V_{REF} range on CH3
D5	Enable 2 V_{REF} range on CH2
D4	Enable 2 V_{REF} range on CH1
D3	Enable I^2C filters
D2	Enable alert pin
D1	Enable busy pin (D2 = 0)/clear alerts (D2 = 1)
D0	Sets polarity of alert pin (active high/active low)

Table 18. ALERT/BUSY Function

D2	D1	ALERT/BUSY Pin Configuration
0	0	Pin does not provide any interrupt signal.
0	1	Pin configuration as a BUSY output
1	0	Pin configuration as an ALERT output.
1	1	Resets the ALERT output pin, the Alert_Flag bit in the conversion result register, and the entire alert status register (if any is active). If 1/1 is written to Bits D2/D1 in the configuration register to reset the ALERT pin, the Alert_Flag bit, and the alert status register, the contents of the configuration register read 1/0 for D2/D1, respectively, if read back.

SAMPLE DELAY AND BIT TRIAL DELAY

It is recommended that no I²C Bus activity occurs when a conversion is taking place; however, this may not be possible, for example when operating in automatic cycle mode. To maintain the performance of the ADC in such cases, Bits D14 and D13 in the configuration register are used to delay critical sample intervals and bit trials from occurring while there is activity on the I²C bus. This may increase the conversion time. When Bits D14 and D13 are both 1, the bit trial-and-sample interval delaying mechanism are implemented. The default setting of D14 and D13 is 0. If bit trial delays extend longer than 1 µs, the conversion terminates. When D14 is 1, the sampling instant delay is implemented. When D13 is 1, the bit trial delay is implemented. To turn off both the sample delay and bit trial delay, set D14 and D13 to 0.

POWER-DOWN REGISTER

The power-down register is an 8-bit read/write register that is used to power down various sections on the AD7294 device.

Table 19. Power-Down Register Description

Bit	Function
P7	Power down full chip (apart from DACs)
P6	Reserved
P5	Power down ADC reference buffer (to allow external reference, 1 at power-up)
P4	Power down DAC reference buffer (to allow external reference, 1 at power-up)
P3	Power down temperature sensor
P2	Power down $I_{SENSE}2$
P1	Power down $I_{SENSE}1$
P0	DAC outputs set to high impedance (set automatically if die temperature >150°C)

$DATA_{HIGH}$/$DATA_{LOW}$ REGISTER

The $DATA_{HIGH}$ / $DATA_{LOW}$ registers for a channel are 16-bit, read/write registers. General alert is flagged by the MSB, D15. D14 – D12 are not used in the register and are read as 0s. The remaining 12-bits set the high/low limits for the relevant channel. With respect to Channels 1 to 4, for Single Ended mode, 000 and FFF are the defaults values. For differential mode on Channels 1 to 4, the default values for $DATA_{HIGH}$ & $DATA_{LOW}$ are 7FF and 800. Note that if the part is configured in Single Ended mode and the limits are changed, the user must re-program limits when changing to a different mode. Channels 5 to 6, $I_{SENSE}1$ and $I_{SENSE}2$, are two's complement format and so the default limits will also be in this format. The limit registers can be used to monitor the conversion results on one or both channels. The AD7294 signals an alert (in either hardware or software or both, depending on the configuration) if the result moves outside the upper or lower limit set by the user.

Table 20. Default values for $DATA_{HIGH}$ and $DATA_{LOW}$ REGISTERS

ADC Channel	Single Ended	Differential
CH1	000 and FFF	7FF and 800
CH2	000 and FFF	7FF and 800
CH3	000 and FFF	7FF and 800
CH4	000 and FFF	7FF and 800
$I_{SENSE}1$	7FF and 800 (2's Complement)	N/A
$I_{SENSE}2$	7FF and 800 (2's Complement)	N/A
$T_{SENSE}1$	3FF and 400 (2's Complement)	N/A
$T_{SENSE}2$	3FF and 400 (2's Complement)	N/A
$T_{SENSE}INT$	3FF and 400 (2's Complement)	N/A

The $DATA_{HIGH}$ register stores the upper limit that activates the ALERT output and/or the Alert_Flag bit in the conversion result register. If the value in the conversion result register is greater than the value in the $DATA_{HIGH}$ register, an alert occurs. When the conversion result returns to a value of at least N LSB below the $DATA_{HIGH}$ register value, the ALERT output pin and Alert_Flag bit are reset. The value of N is taken from the 12-bit hysteresis register associated with that channel. For the T_{SENSE} limit registers D11 is equal to 0, as this denotes the diode open-circuit flag in the T_{SENSE} registers.

The $DATA_{LOW}$ register stores the lower limit that activates the ALERT output and/or the Alert_Flag bit in the conversion result register. If the value in the conversion result register is less than the value in the $DATA_{LOW}$ register, an alert occurs. When the conversion result returns to a value of at least N LSB above the $DATA_{LOW}$ register value, the ALERT output pin and Alert_Flag bit are reset. The value of N is taken from the hysteresis register associated with that channel.

The ALERT pin can also be reset by writing to Bits D2 and D1 in the configuration register. The four standard voltage inputs (CH1 to CH4), two I_{SENSE} channels (CH5 to CH6), and three T_{SENSE} channels (CH7 to CH9) utilize the high/low limit registers.

Table 21. AD7294 $DATA_{HIGH}$/$_{LOW}$ Register (First R/W)

MSB							LSB
D15	D14	D13	D12	D11	D10	D9	D8
Alert_Flag	0	0	0	B11	B10	B9	B8

Table 22. AD7294 $DATA_{HIGH}$/$_{LOW}$ Register (Second R/W)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
B7	B6	B5	B4	B3	B2	B1	B0

HYSTERESIS REGISTERS

Each hysteresis register is a 16-bit read/write register; only the 12 LSBs of the register are used, with the MSB signaling the alert event. The hysteresis

register stores the hysteresis value, N, when using the limit registers. Each pair of limit registers has a dedicated hysteresis register. The hysteresis value determines the reset point for the ALERT pin/Alert_Flag if a violation of the limits occurs. For example, if a hysteresis value of 8 LSB is required on the upper and lower limits of Channel 1, the 16-bit word 0000 0000 0000 1000 should be written to the hysteresis register of CH1 (see Table 11). On power-up, the hysteresis registers contain a value of 8 LSB for non-temperature result registers and 8 °C, or 32 LSB, for the T_{SENSE} registers. If a different hysteresis value is required, that value must be written to the hysteresis register for the channel in question. For the TSENSE register D11, in **Error! Reference source not found.** is 0.

Table 23. Hysteresis Register (First Read/Write)

MSB							LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Alert_Flag	0	0	0	B11	B10	B9	B8

Table 24. Hysteresis Register (Second Read/Write)

MSB							LSB
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
B7	B6	B5	B4	B3	B2	B1	B0

Using the Limit Registers to Store Min/Max Conversion Results

If full scale—that is, all 1s—is written to the hysteresis register for a particular channel, the $DATA_{HIGH}$ and $DATA_{LOW}$ registers for that channel no longer act as limit registers as previously described, but act as storage registers for the maximum and minimum conversion results returned from conversions on a channel over any given period of time. This function is useful in applications where the widest span of actual conversion results is required rather than using the ALERT to signal that an intervention is necessary. Note that on power-up, the contents of the $DATA_{HIGH}$ register for each channel are full scale, whereas the contents of the $DATA_{LOW}$ registers are zero scale by default. Therefore, minimum and maximum conversion values being stored in this way are lost if power is removed or cycled.

SERIAL BUS INTERFACE

Control of the AD7294 is carried out via the I²C-compatible serial bus. The AD7294 is connected to this bus as a slave device under the control of a master device.

GENERAL I²C TIMING

Figure 36 shows the timing diagram for general read and write operations using an I²C-compliant interface. The master initiates a data transfer by establishing a start condition, defined as a high-to-low transition on the serial data line (SDA) while the serial clock line (SCL) remains high. This indicates that a data stream follows. The master sends a 7-bit slave address (MSB first) and an R/W bit that determines the direction of the data transfer—that is, whether data is written to or read from the slave device (0 = written, 1 = read).

The slave responds by pulling the data line low during the low period before the ninth clock pulse, known as the acknowledge bit, and holding it low during the high period of this clock pulse. All other devices on the bus remain idle while the selected device waits for data to be read from or written to it. If the R/W bit is 0, the master writes to the slave device. If the R/W bit is 1, the master reads from the slave device.

Data is sent over the serial bus in sequences of nine clock pulses—eight bits of data followed by an acknowledge bit, which can be from the master or slave device. Data transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, because a low-to-high transition when the clock is high may be interpreted as a stop signal. If the operation is a write operation, the first data byte after the slave address is a command byte. This tells the slave device what to expect next. It may be an instruction telling the slave device to expect a block write, or it may be a register address that tells the slave where subsequent data is to be written. Because data can flow in only one direction, as defined by the R/W bit, it is not possible to send a command to a slave device during a read operation. Before performing a read operation, it is sometimes necessary to perform a write operation to tell the slave what sort of read operation to expect and/or the address from which data is to be read.

When all data bytes have been read or written, stop conditions are established. In write mode, the master pulls the data line high during the 10th clock pulse to assert a stop condition. In read mode, the master device releases the SDA line during the low period before the ninth clock pulse, but the slave device does not pull it low. This is known as a no acknowledge (NACK). The master takes the data line low during the low period before the 10th clock pulse, and then high during the 10th clock pulse to assert a stop condition.

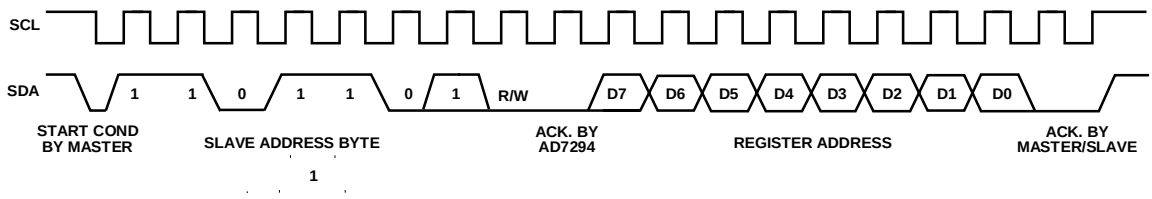


Figure 36. General I²C Timing

SERIAL BUS ADDRESS BYTE

The first byte the user writes to the device is the Serial Bus Address Byte. Like all I²C-compatible devices the AD7294 has a 7-bit serial address. The 5 LSBs are user programmable by the 3 three-state input pins as shown in Table 25 where Z refers to a pin left floating.

Table 25. Serial Address control using 3-State Input Pins

AS2	AS1	AS0	A4	A3	A2	A1	A0
0	0	0	0	0	0	0	1
0	0	1	0	0	0	1	0
0	0	Z	0	0	0	1	1
0	1	0	0	0	1	0	0
0	1	1	0	0	1	0	1
0	1	Z	0	0	1	1	0
0	Z	0	0	0	1	1	1
0	Z	1	0	1	0	0	0
0	Z	Z	0	1	0	0	1
1	0	0	0	1	0	1	0
1	0	1	0	1	0	1	1
1	0	Z	0	1	1	0	0
1	1	0	0	1	1	0	1
1	1	1	0	1	1	1	0
1	1	Z	0	1	1	1	1
1	Z	0	1	0	0	0	0
1	Z	1	1	0	0	0	1
1	Z	Z	1	0	0	1	0
Z	0	0	1	0	0	1	1
Z	0	1	1	0	1	0	0
Z	0	Z	1	0	1	0	1
Z	1	0	1	0	1	1	0
Z	1	1	1	0	1	1	1
Z	1	Z	1	1	0	0	0
Z	Z	0	1	1	0	0	1
Z	Z	1	1	1	0	1	0
Z	Z	Z	1	1	0	1	1

WRITING/READING TO THE AD7294

The AD7294 uses the following I²C protocols:

Writing to the Address Pointer Register for a Subsequent Read

In the AD7294, to read from a particular register, the address pointer register must first contain the address of that register. If the address pointer is not set, the correct address must be written to the address pointer register by performing a single byte write operation, as shown in Figure 37. In this operation, the slave device receives a single byte from a master as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write (low) bit.
3. The addressed slave device asserts ACK on SDA.
4. The slave receives a data byte.
5. The slave asserts ACK on SDA.
6. The master asserts a stop condition on SDA, and the transaction ends.

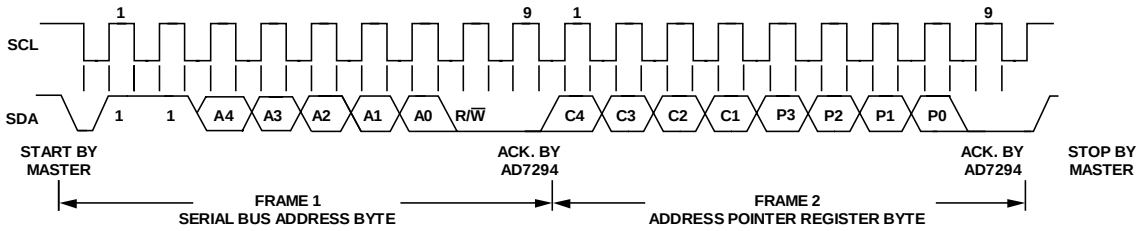


Figure 37. Writing to the Address Pointer Register to Select a Register for a Subsequent Read Operation

Reading Data from an 8-Bit Register

Reading the contents from any of the 8-bit registers is a single-byte read operation, as shown in Figure 38. This protocol assumes that the particular register address has been set up by a single-byte write operation to the address pointer register (see Figure 38). Once the register address has been set up, any number of reads can be performed from that particular register without having to write to the address pointer register again. If a read from a different address is required, the relevant register address has to be written to the address pointer register, and again any number of reads from this register can then be performed. In this operation, the master device receives a single byte from a slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the read bit (high).
3. The addressed slave device asserts ACK on SDA.
4. The master receives a data byte.
5. The master asserts NACK on SDA so that the slave knows the data transfer is complete.
6. The master asserts a stop condition on SDA, and the transaction ends.

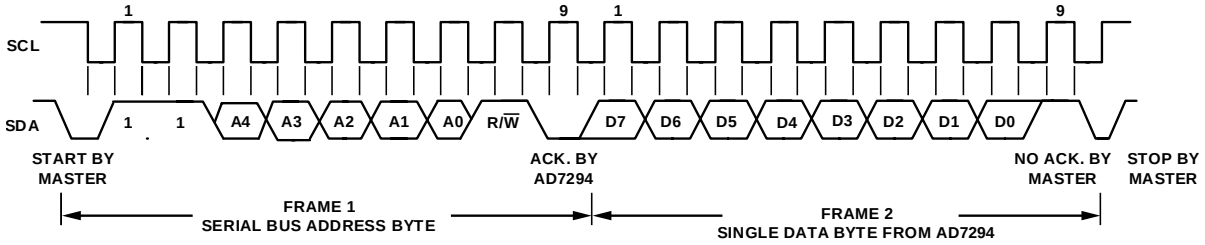


Figure 38. Reading a Single Byte of Data from a Selected Register

Reading Two Bytes of Data from a 16-Bit Register

In this operation, the master device reads two bytes of data from a slave device. This protocol assumes that the particular register address has been set up by a single-byte write operation to the address pointer register, see Figure 39.

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the read bit (high).
3. The addressed slave device asserts ACK on SDA.
4. The master receives a data byte.
5. The master asserts ACK on SDA.
6. The master receives a second data byte.
7. The master asserts NACK on SDA, so the slave knows that the data transfer is complete.
8. The master asserts a stop condition on SDA to end the transaction.

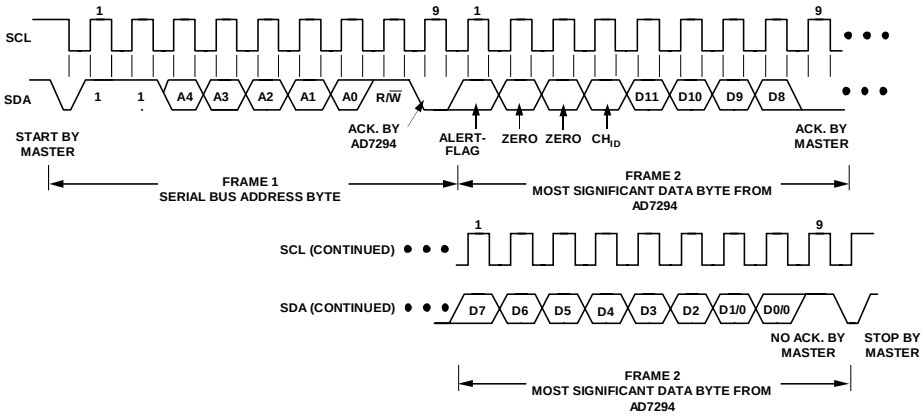


Figure 39. Reading Two Bytes of Data from the Conversion Result Register

Reading Two Bytes of Data from a Result Register

The result register, $T_{SENSE}1$ result register and the $T_{SENSE}2$ register are 16-bit registers used to store the conversion results from the ADC. The master must first write to the command register to determine which multiplexed channel to convert on. The address pointer register is then pointed towards the register to which to enter the converted data. The master sends a repeated start to the frame and then enters the two bytes of converted data into the desired result register. :

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a register address of all 0s in order to write to the command register.
5. The addressed slave device asserts ACK on SDA.
6. The master writes to the command register.
7. The slave asserts ACK on SDA.
8. The master sends a register address.
9. The slave asserts ACK on SDA.
10. The master device asserts a repeated start condition on SDA.
11. The master sends the 7-bit slave address followed by the read bit (high).
12. The slave asserts ACK on SDA.
13. The master sends the most significant data byte.
14. The master asserts ACK on SDA.
15. The master sends the least significant data byte.
16. The master asserts NACK on SDA, so the slave knows that the data transfer is complete.
17. The master asserts a stop condition on SDA to end the transaction.

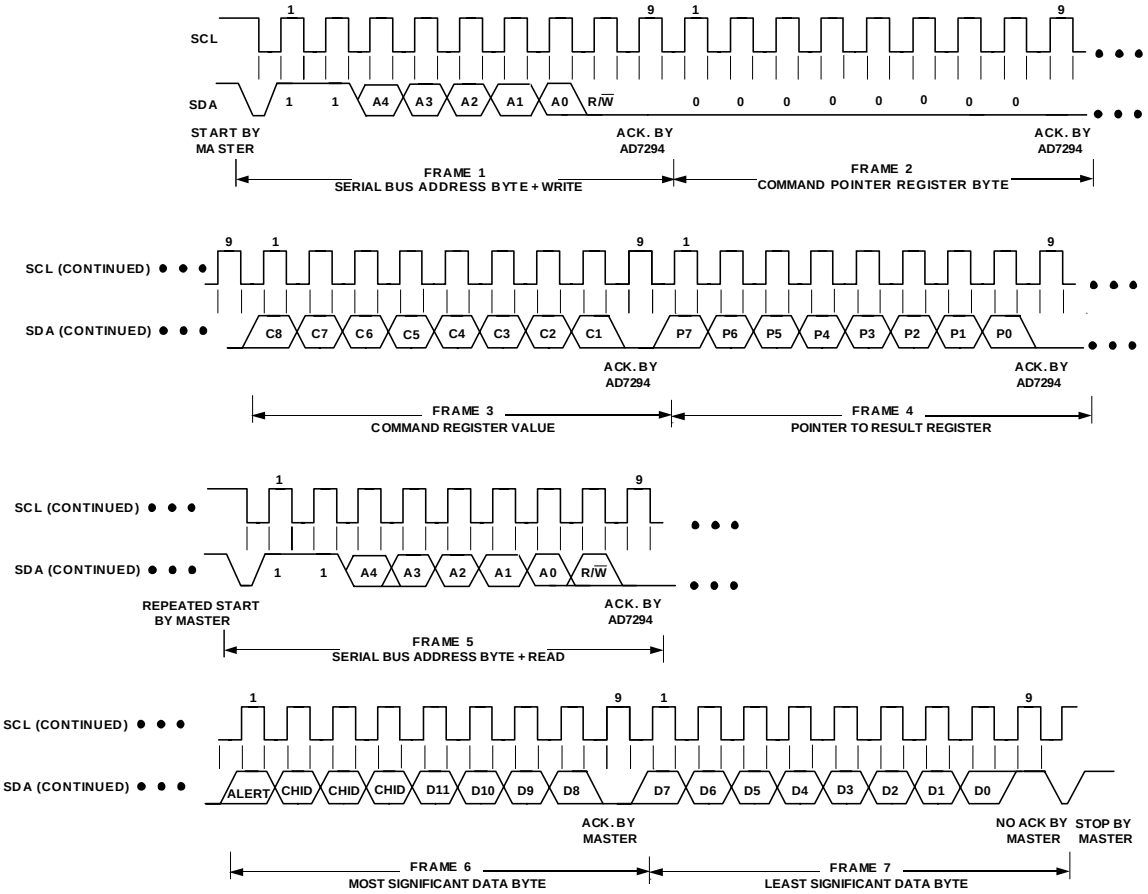


Figure 40.

Writing a Single Byte of Data to an 8-Bit Register

The alert registers, power down register, channel sequence register, offset registers, and the command register are 8-bit registers; therefore, only one byte of data can be written to each. In this operation, the master device sends a byte of data to the slave device. To write data to the register, the command sequence is as follows:

18. The master device asserts a start condition on SDA.
19. The master sends the 7-bit slave address followed by the write bit (low).
20. The addressed slave device asserts ACK on SDA.
21. The master sends a register address.
22. The slave asserts ACK on SDA.
23. The master sends a data byte.
24. The slave asserts ACK on SDA.
25. The master asserts a stop condition on SDA to end the transaction.

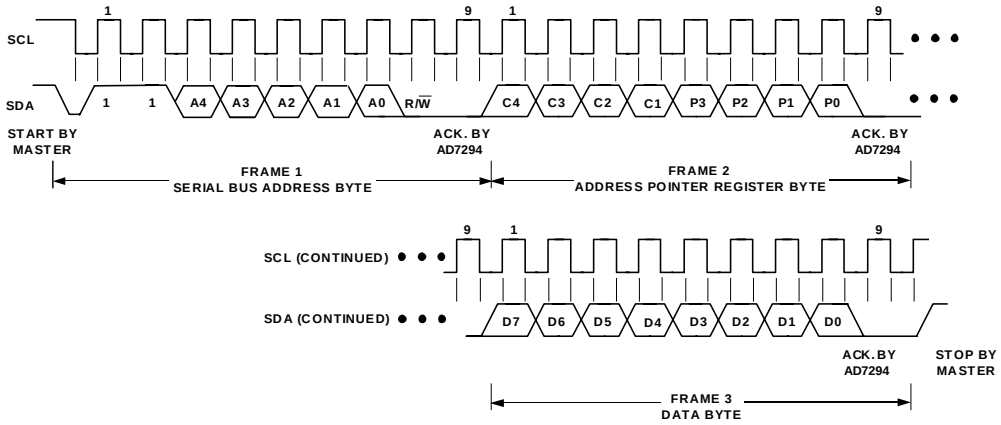


Figure 41. Single-Byte Write Sequence

Writing Two Bytes of Data to a 16-Bit Register

Both types of limit registers, the hysteresis registers, the result register, the T_{SENSE} result registers, the configuration register, and the fuse registers are 16-bit registers; therefore, two bytes of data are required to write a value to any one of these registers. Writing two bytes of data to one of these registers consists of the following:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a register address. The slave asserts ACK on SDA.
5. The master sends the first data byte
6. The slave asserts ACK on SDA.
7. The master sends the second data byte.
8. The slave asserts ACK on SDA.
9. The master asserts a stop condition on SDA to end the transaction.

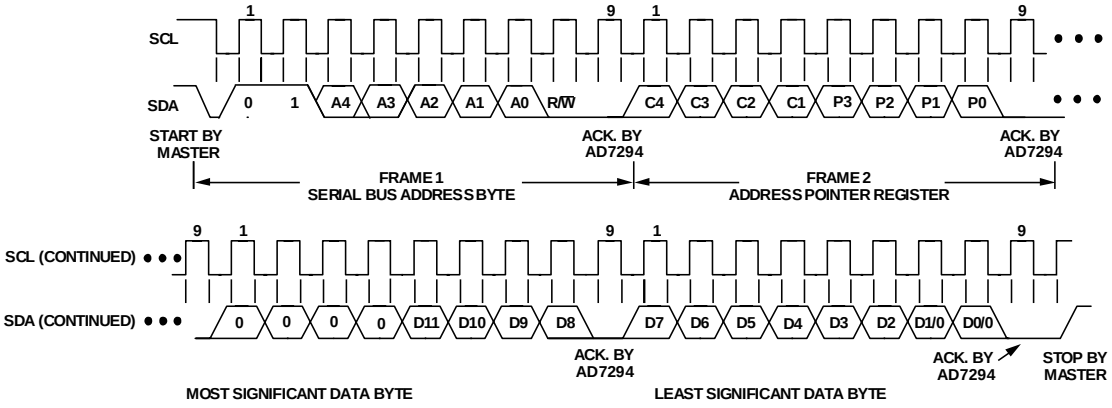


Figure 42. 2-Byte Write Sequence

MODES OF OPERATION

When supplies are first applied to the AD7294 the ADC powers up in sleep mode and normally rmains in this shutdown state while not converting. There are two different methods of initiating a conversion on the AD7294.

MODE 1 – COMMAND MODE

In this mode the part cycles through the selected channels on each subsequent read. To setup the command mode the command register must first be told which ADC channels to convert on, see Table 7 . In the case of $T_{SENSE}1$, $T_{SENSE}2$ and $T_{SENSE}INT$, the command mode is not actually requesting a conversion but outputting the last automatic conversion in sequence. In the case of the internal temperature sensor $T_{SENSE}INT$, it is not possible to read the result via the ADC result register. The result is stored in the $T_{SENSE}INT$ result register

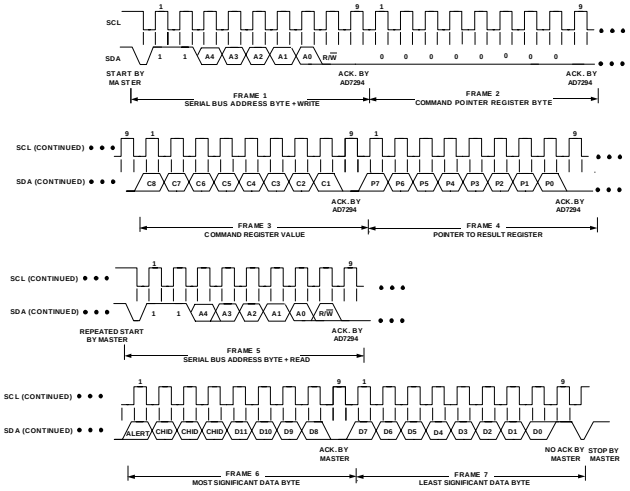


Figure 43. Command Mode Operation

Figure 44 illustrates a 2–byte read operation from the result register. Prior to the read operation, ensure that the address pointer is pointing to the command register. In the command register choose the sequence of conversions required. At this point the ADC will power up and begin channel conversions. Also take note that the address pointer must be re-addressed to the result register to read the conversions results. For each channel conversion in the sequence, the frame is re-addressed to the result register to synchronize the frames. When more then one channel is selected in the command register. The first read accesses the data from the conversion on channel1. While this read takes place, a conversion occurs on channel 2. The second read accesses this data from channel 2 and so on.

The wake-up and conversion time together should take approximately 5 µs, and the conversion begins when the last bit in the command register has been clocked in.

MODE 2 – AUTOCYCLE MODE

An automatic conversion cycle can be selected and enabled by initially selecting the enable autocycle mode option in the configuration register. The desired sequence of the autocycle mode is controlled using the channel sequence register. The automatic cycle mode can be set on the four uncommitted analog input channels along with the two I_{SENSE} channels. When the 6 LSBs of this register are programmed with any configuration other than all 0s, a conversion takes place every 5 ms. In autocycle mode the sample delay and bit trial delay are two configuration options which can be used to maintain ADC performance when I^2C bus activity is taking place during a conversion.

If more than one channel bit is set in the channel sequence register, the ADC automatically cycles through the channel sequence, starting with the lowest channel. Once the sequence is complete, the ADC starts converting on the lowest channel again, continuing to loop through the sequence until the cycle timer register contents are set to all 0s. This mode is useful for monitoring signals, such as signal power and current sensing, alerting only when the limits are violated. To exit the autocycle mode the user must write all zeroes to the channel sequence register or disable the autocycle mode in the configuration register. Figure 45 shows the autocycle mode where only one channel is chosen from the channel sequence register. Depending on the controller of the I^2C interface, it is also possible to break the long write frame into two shorter frames, where a second frame can begin after writing to the configuration register. After writing to the configuration register, the user can stop the frame, re-address the part and write to the channel sequence.

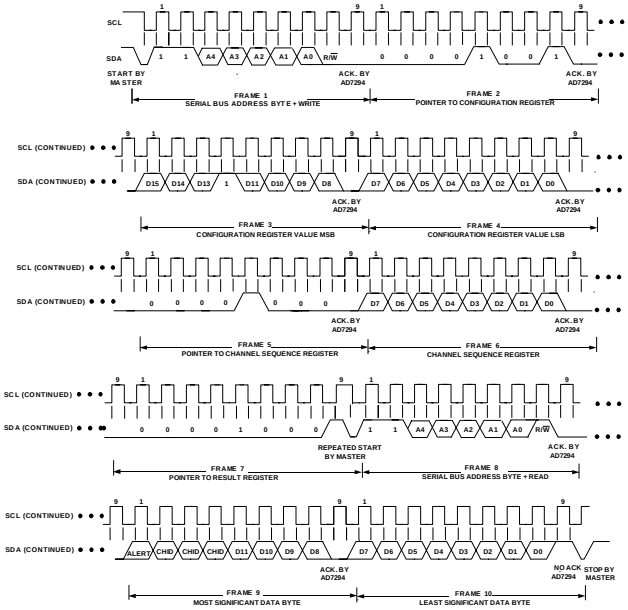


Figure 45. Autocycle Mode Operation

LAYOUT AND CONFIGURATION

POWER SUPPLY BYPASSING AND GROUNDING

When accuracy is important in a circuit, carefully consider the power supply and ground return layout on the board. The printed circuit board containing the AD7294 should have separate analog and digital sections, each having its own area of the board. If the AD7294 is in a system where other devices require an AGND-to-DGND connection, the connection should be made at one point only. This ground point should be as close as possible to the AD7294.

The power supply to the AD7294 should be bypassed with 10 µF and 0.1 µF capacitors. The capacitors should physically be as close as possible to the device, with the 0.1 µF capacitor ideally right up against the device. The 10 µF capacitors are the tantalum bead type. It is important that the 0.1 µF capacitor has low effective series resistance (ESR) and low effective series inductance (ESI); common ceramic types of capacitors are suitable. The 0.1 µF capacitor provides a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching.

The power supply line should have as large a trace as possible to provide a low impedance path and reduce glitch effects on the supply line. Clocks and other components with fast switching digital signals should be shielded from other parts of the board by a digital ground. Avoid crossover of digital and analog signals if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects on the board. The best board layout technique is the microstrip technique where the component side of the board is dedicated to the ground plane only and the signal traces are placed on the solder side; however, this is not always possible with a 2-layer board.

EVALUATION BOARD FOR THE AD7294

The AD7294 evaluation board consists of the AD7294 LFCSP package along with two R_{SENSE} resistors and a number of SMB sockets and jumpers, which allow access to the various on-chip functionalities of the AD7294. Other on-board components are used to interface the part to the PC, such as an EEPROM, a USB Microcontroller and a voltage regulator. More information, on the AD7294 evaluation board, is available in the EVAL-AD7294EB application note and should be consulted when evaluating the board.

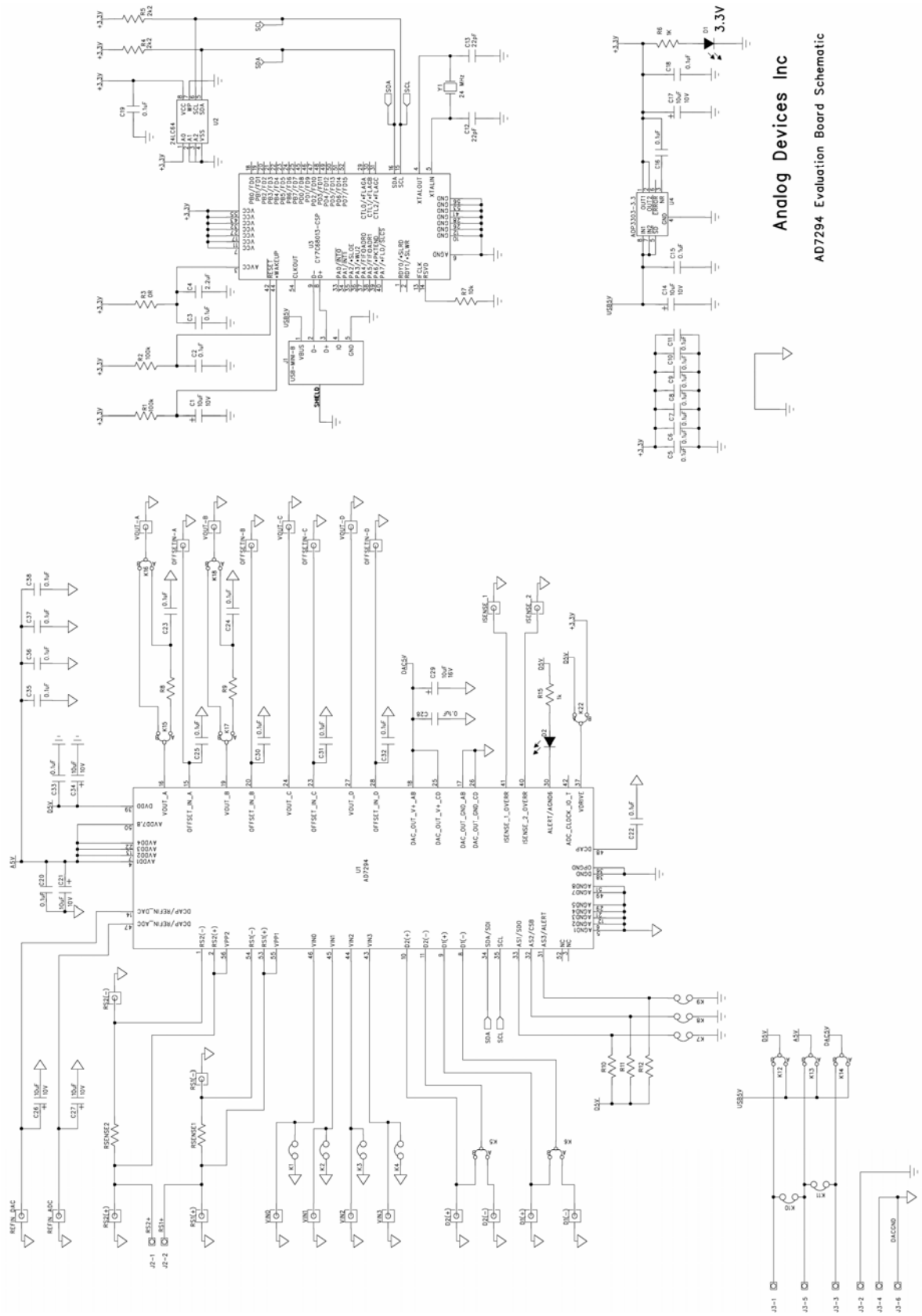


Figure 46. Evaluation Board Schematic

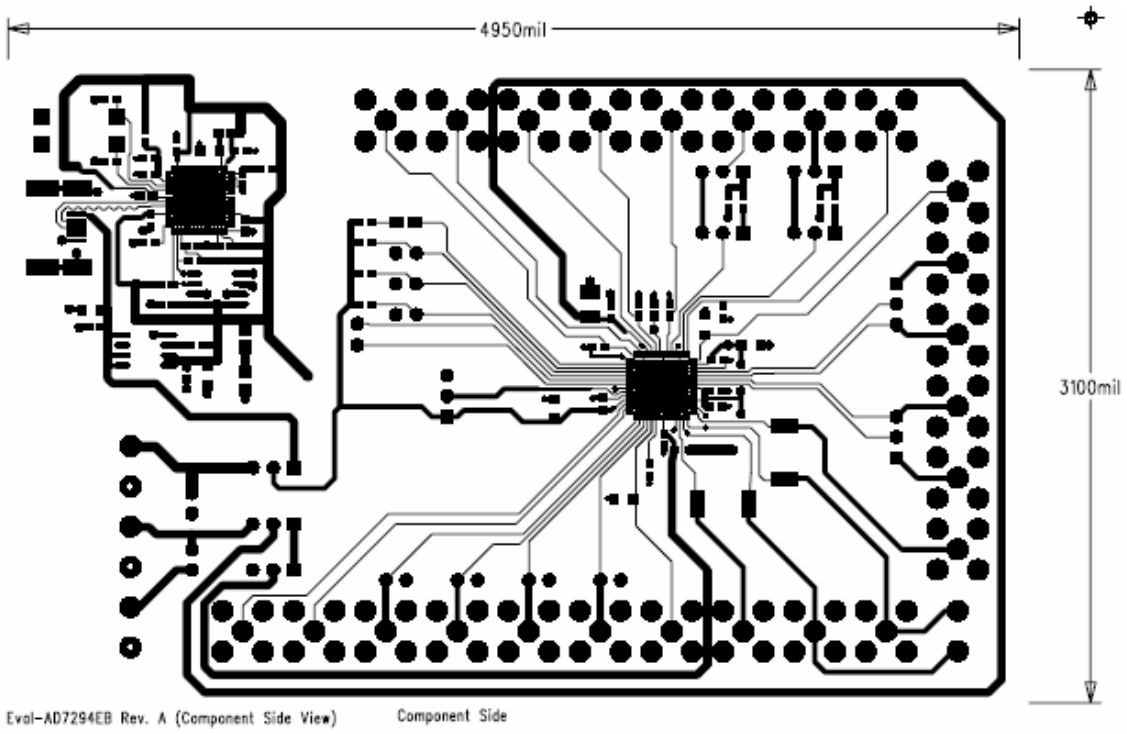


Figure 47. Component Side Artwork

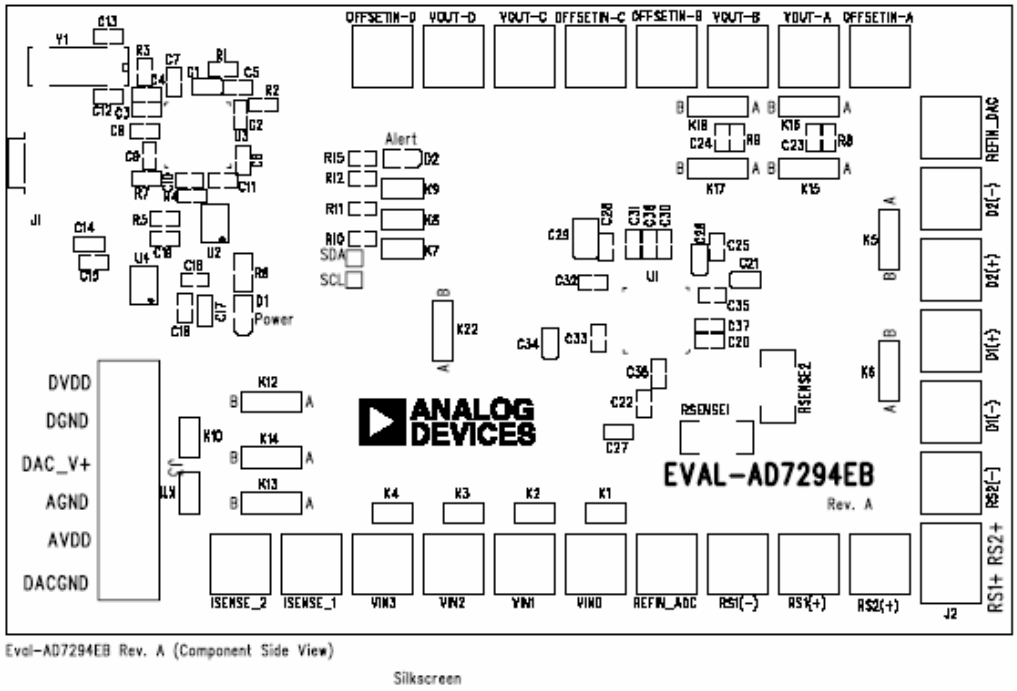


Figure 48. Component Side SilkScreen

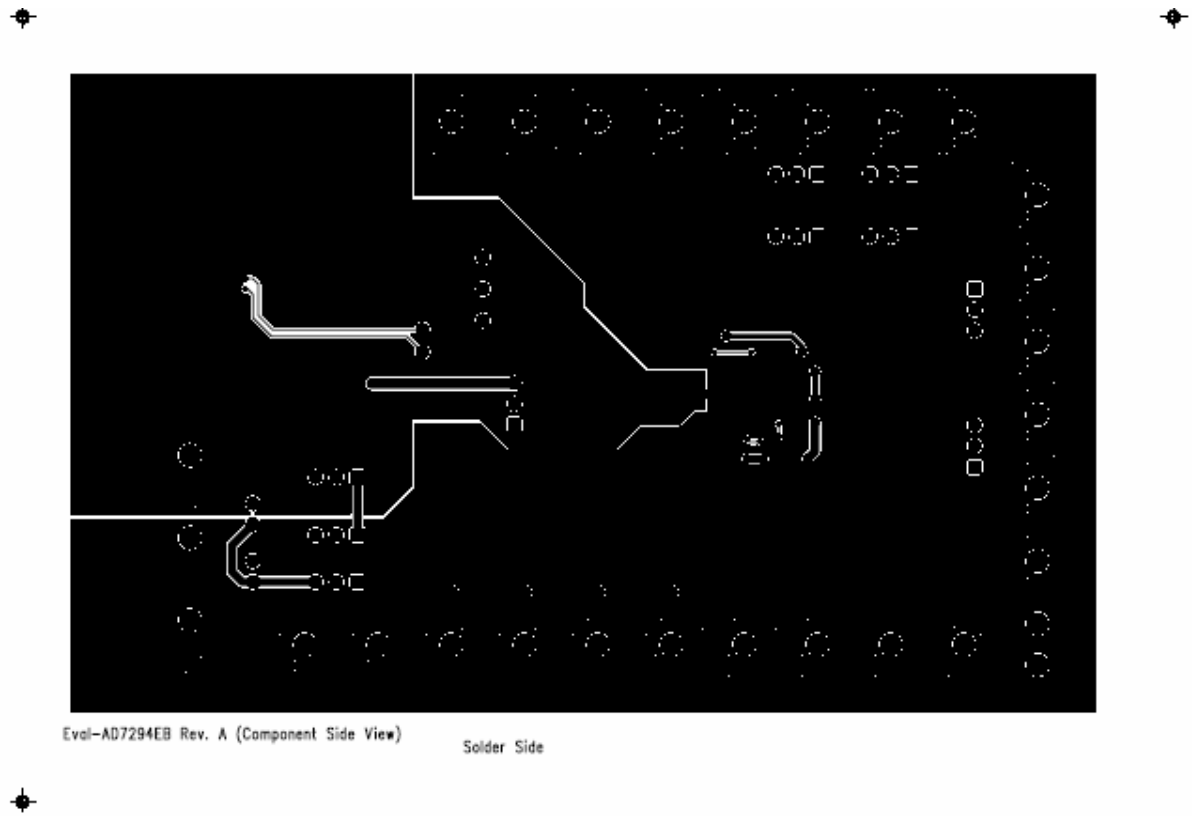
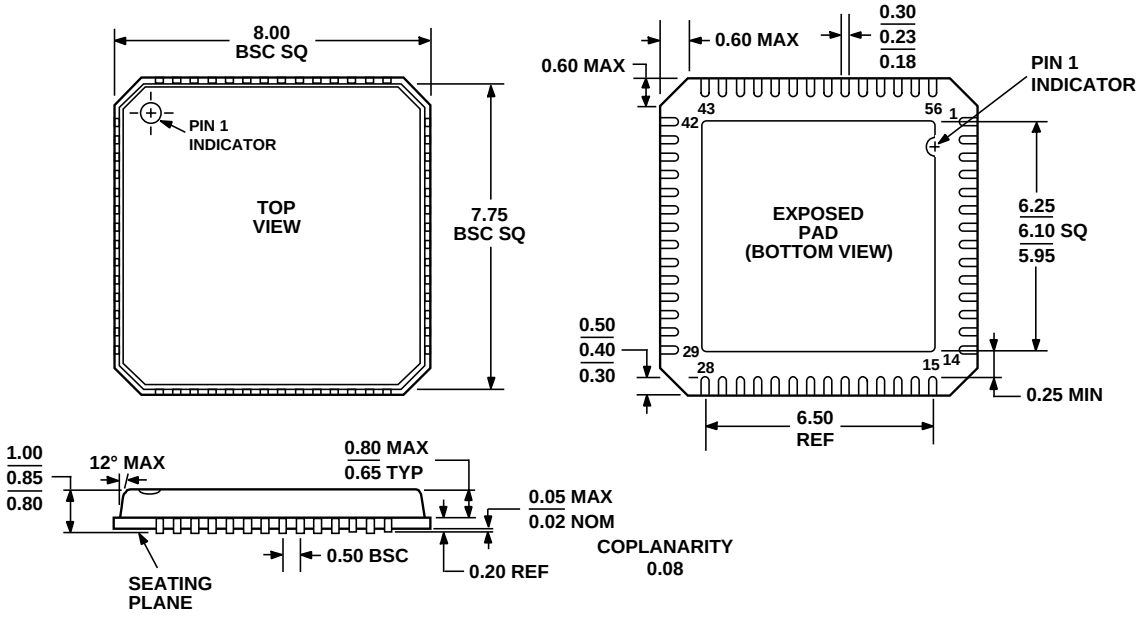


Figure 49. Solder-Side Artwork

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VLLD-2

Figure 50. LFCSP-56 Pin Package

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