DATA SHEET

LF398
Sample-and-hold amplifier

Product data
Replaces LF198/LF298/LF398 of 1994 Aug 31
IC11

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Philips
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Sample-and-hold amplifier LF398

DESCRIPTION

The LF398 is a monolithic sample-and-hold circuit which utilizes high-voltage ion-implant JFET technology to obtain ultra-high DC accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, DC gain accuracy is 0.002% typical and acquisition time is as low as 6 μs to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin and does not degrade input offset drift. The wide bandwidth allows the LF398 to be included inside the feedback loop of 1 MHz op amps without having stability problems. Input impedance of $10^{10}\Omega$ allows high source impedances to be used without degrading accuracy.

P-channel junction FETs are combined with bipolar devices in the output amplifier to give droop rates as low as 5 mV/min with a 1 μF hold capacitor. The JFETs have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design guarantees no feedthrough from input to output in the hold mode even for input signals equal to the supply voltages.

Logic inputs are fully differential with low input current, allowing direct connection to TTL, PMOS, and CMOS; differential threshold is 1.4 V. The LF398 will operate from ±5 V to ±18 V supplies. It is available in 8-pin plastic DIP and 14-pin plastic SO packages.

FEATURES

- Operates from ±5 V to ±18 V supplies
- Less than 10 μs acquisition time
- TTL, PMOS, CMOS compatible logic input
- 0.5 mV typical hold step at C_H = 0.01 μF
- Low input offset
- 0.002% gain accuracy
- Low output noise in hold mode
- Input characteristics do not change during hold mode
- High supply rejection ratio in sample or hold
- Wide bandwidth

PIN CONFIGURATIONS

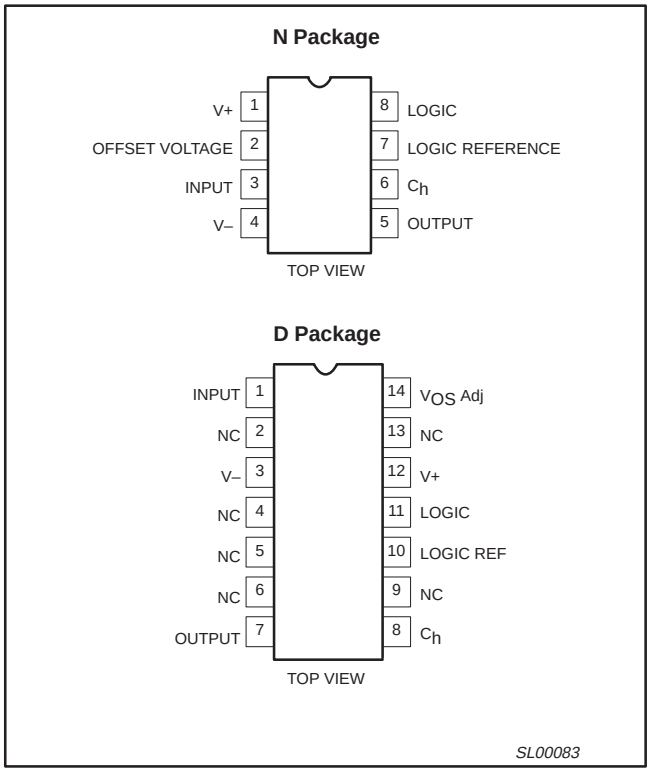


Figure 1. Pin Configurations

APPLICATION

- The LF398 is ideally suited for a wide variety of sample-and-hold applications, including data acquisition, analog-to-digital conversion, synchronous demodulation, and automatic test setup.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Small Outline (SO) Package	0 to +70°C	LF398D	SOT108-1
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	LF398N	SOT97-1

FUNCTIONAL DIAGRAM

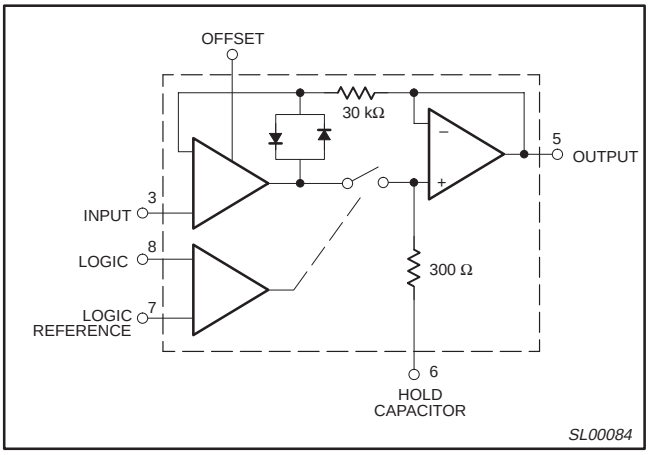


Figure 2. Functional Diagram

TYPICAL APPLICATIONS

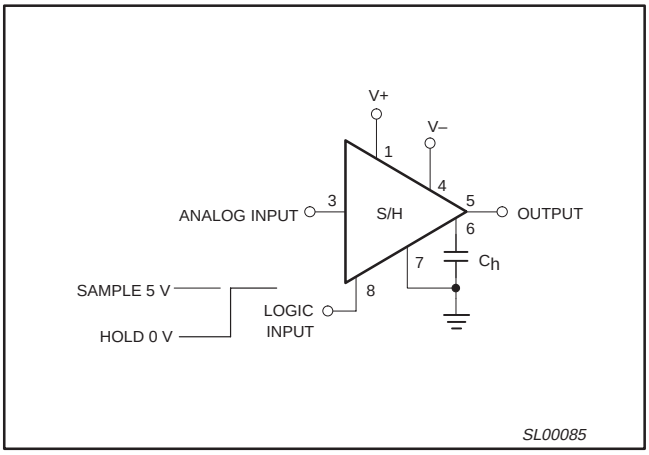


Figure 3. Typical Applications

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage	±18	V
	Maximum power dissipation T_{amb} = 25 °C (still-air)[3] N package D package	 1160 1040	 mW mW
T_{amb}	Operating ambient temperature range	0 to +70	°C
T_{stg}	Storage temperature range	-65 to +150	°C
V_{IN}	Input voltage	Equal to supply voltage	
	Logic-to-logic reference differential voltage[2]	+7, -30	V
	Output short-circuit duration	Indefinite	
	Hold capacitor short-circuit duration	10	sec
T_{SOLD}	Lead soldering temperature (10 sec max)	230	°C

NOTES:

1. The maximum junction temperature of the LF398 is 150 °C. When operating at elevated ambient temperature, the packages must be derated based on the thermal resistance specified.
2. Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins must always be at least 2V below the positive supply and 3 V above the negative supply.
3. Derate above 25 °C, at the following rates:
   N package at 9.3 mW/°C
   D package at 8.3 mW/°C

DC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following conditions apply: unit is in "sample" mode; $V_S = \pm 15$ V; $T_j = 25$ °C; –11.5 V3 $V_{IN} \leq +11.5$ V; $C_H = 0.01$ µF; and $R_L = 10$ kΩ. Logic reference voltage = 0 V and logic voltage = 2.5 V.

SYMBOL	PARAMETER	TEST CONDITIONS	Min	Typ	Max	UNIT
V_{OS}	Input offset voltage[4]	$T_j = 25$ °C Full temperature range		2	7 10	mV
I_{BIAS}	Input bias current[4]	$T_j = 25$ °C Full temperature range		10	50 100	nA
	Input impedance	$T_j = 25$ °C		10^{10}		Ω
	Gain error	$T_j = 25$ °C, R_L=10 kΩ Full temperature range		0.004	0.01 0.02	%
	Feedthrough attenuation ratio at 1 kHz	$T_j = 25$ °C, $C_h = 0.01$ µF	80	90		dB
	Output impedance	$T_j = 25$ °C, "HOLD" mode Full temperature range		0.5	4 6	Ω
	"HOLD" step[2]	$T_j = 25$ °C, $C_h = 0.01$ µF, $V_{OUT} = 0$ V		1.0	2.5	mV
I_{CC}	Supply current[4]	$T_j \leq 25$ °C		4.5	6.5	mA
	Logic and logic reference input current	$T_j = 25$ °C		2	10	µA
	Leakage current into hold capacitor[4]	$T_j = 25$ °C, "HOLD" mode		30	200	pA
t_{AC}	Acquisition time to 0.1%	$\Delta V_{OUT} = 10$ V, $C_h = 1000$ pF $C_h = 0.01$ µF		4 20		µs
	Hold capacitor charging current	$V_{IN}–V_{OUT} = 2$ V		5		mA
	Supply voltage rejection ratio	$V_{OUT} = 0$ V	80	110		dB
	Differential logic threshold	$T_j = 25$ °C	0.8	1.4	2.4	V

NOTES:

1. Unless otherwise specified, the following conditions apply. Unit is in "sample" mode, $V_S = \pm 15$ V, $T_j = 25$ °C, $-11.5 \text{ V} \leq V_{IN} \leq +11.5$ V, $C_h = 0.01$ µF, and $R_L = 10$ kΩ. Logic reference voltage = 0 V and logic voltage = 2.5 V.
2. Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1 pF, for instance, will create an additional 0.5 mV step with a 5 V logic swing and a 0.01 µF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.
3. Leakage current is measured at a junction temperature of 25 °C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25 °C value for each 11 °C increase in chip temperature. Leakage is guaranteed over full input signal range.
4. The parameters are guaranteed over a supply voltage of ±5 to ±18 V.

TYPICAL DC PERFORMANCE CHARACTERISTICS

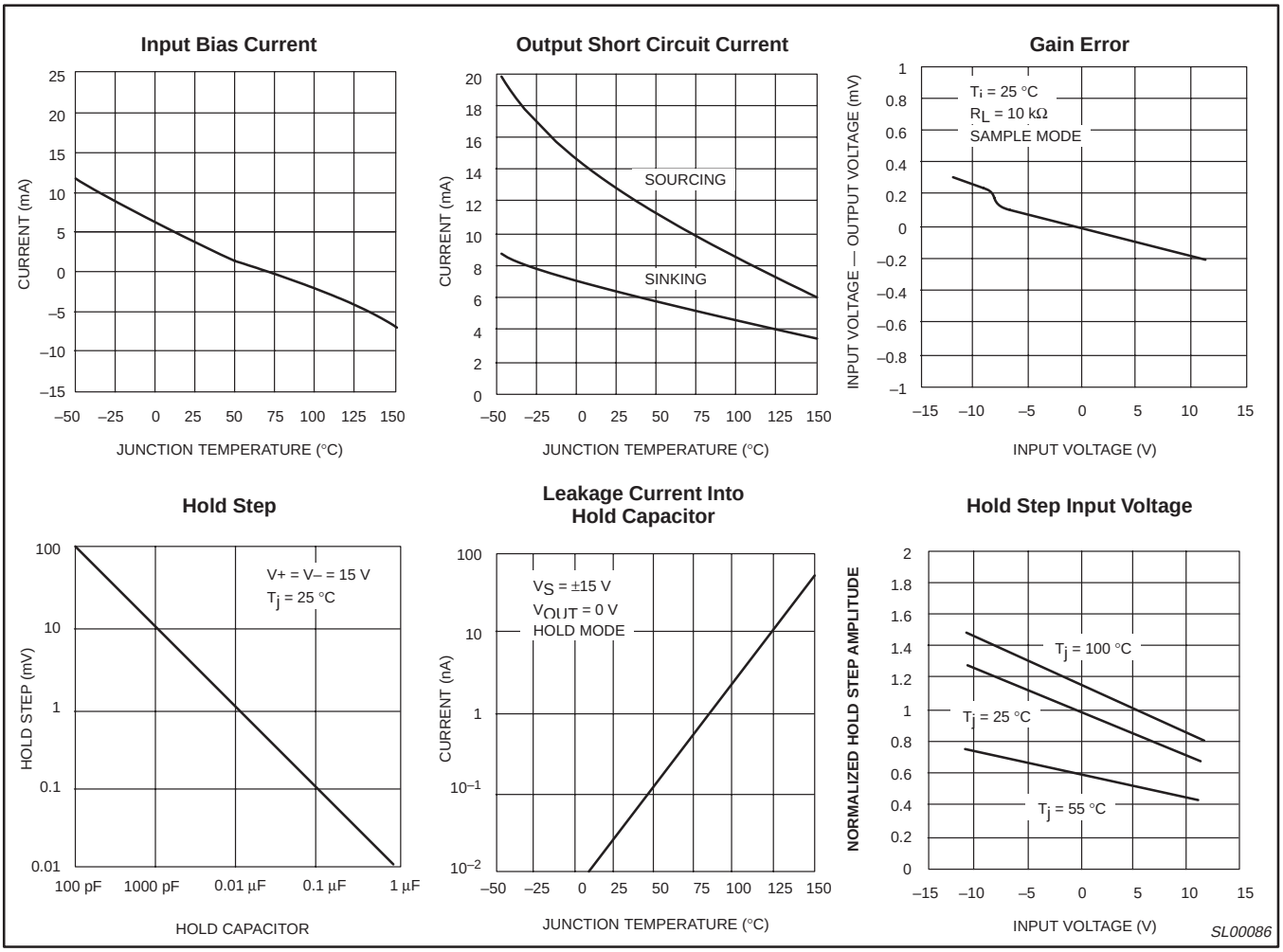


Figure 4. Typical DC Performance Characteristics

TYPICAL AC PERFORMANCE CHARACTERISTICS

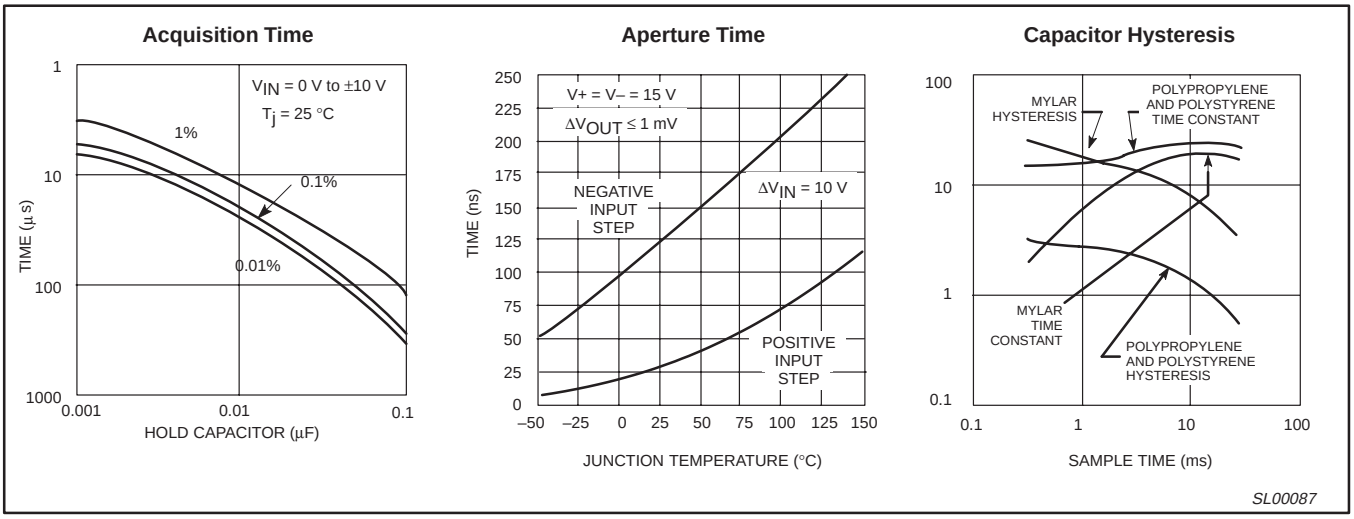


Figure 5. Typical AC Performance Characteristics

TYPICAL AC PERFORMANCE CHARACTERISTICS (Continued)

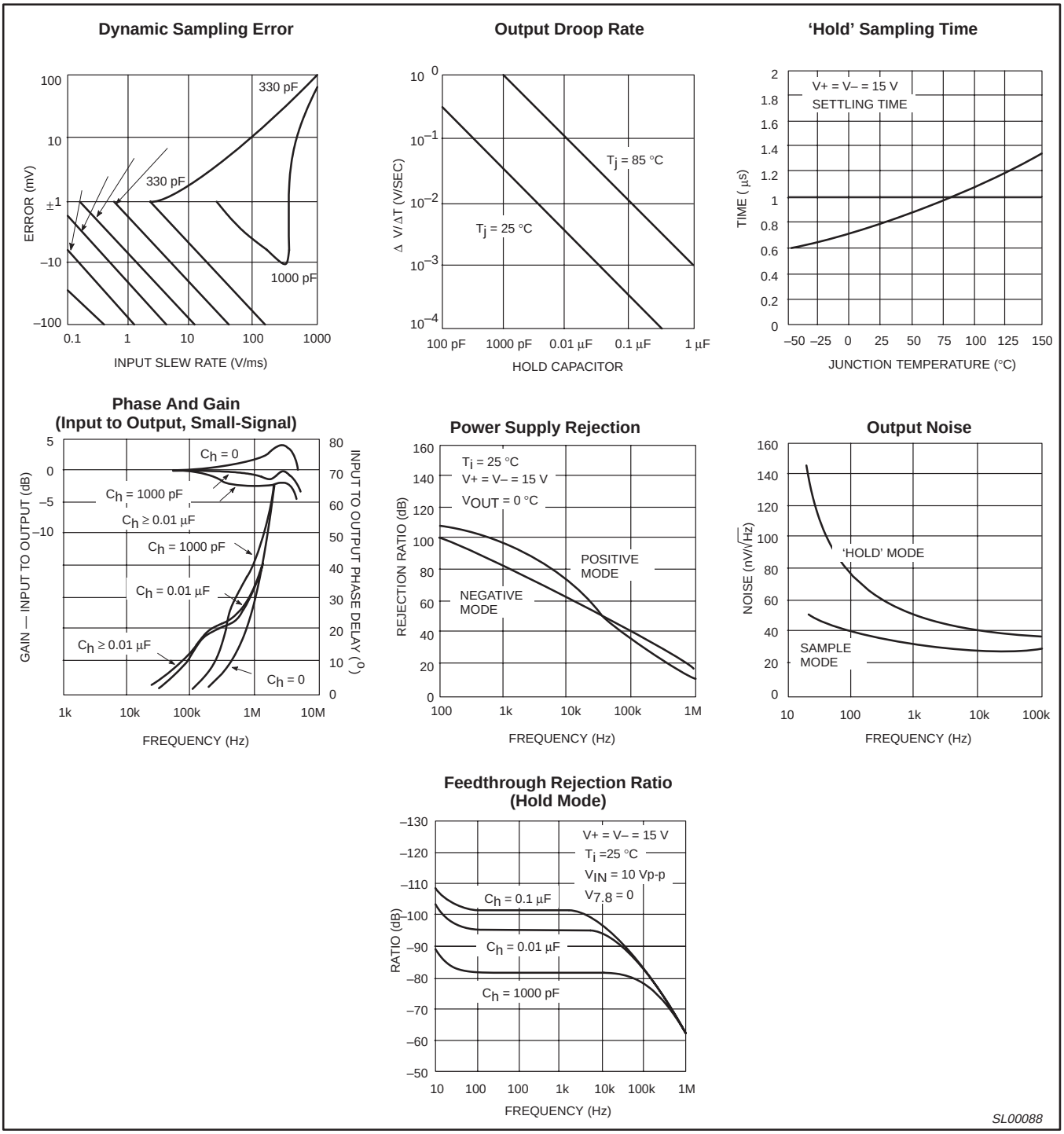
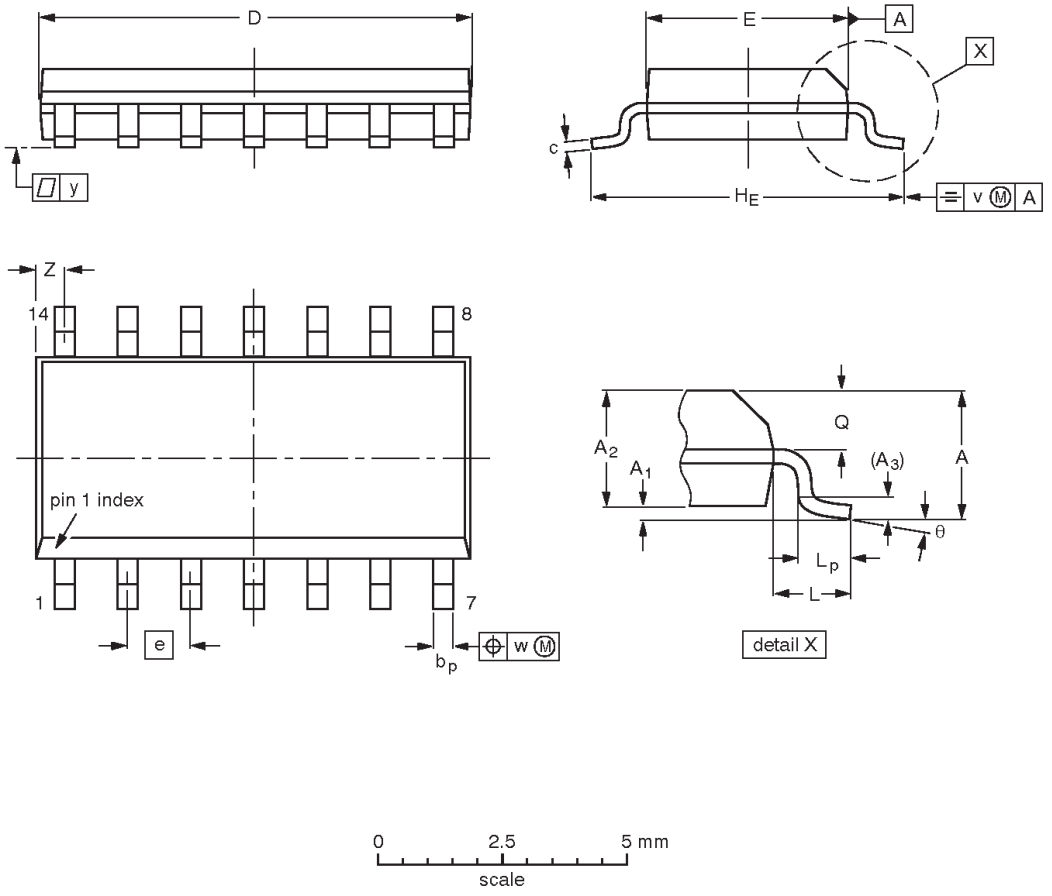


Figure 6. Typical AC Performance Characteristics (cont.)

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

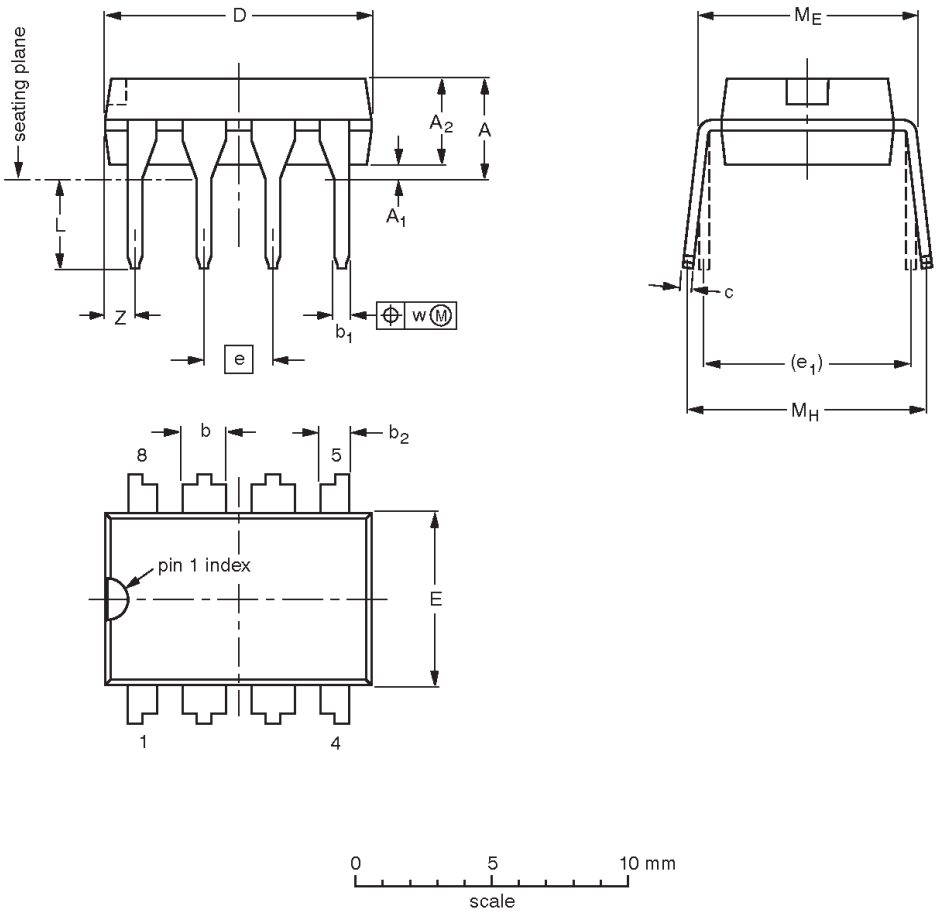
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06	MS-012				~~97-05-22~~ 99-12-27

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001	SC-504-8			~~95-02-04~~ 99-12-27

NOTES

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Data sheet status [1]	Product status [2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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