

Dual 10-bit D-type flip-flop; positive-edge trigger (3-State)

MB2821

FEATURES

- 20-bit positive-edge triggered register
- Multiple V_{CC} and GND pins minimize switching noise
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The MB2821 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The MB2821 has two 10-bit, edge triggered registers, with each register coupled to ten 3-State output buffers. The two sections of each register are controlled independently by the clock (nCP) and Output Enable (nOE) control gates.

Each register is fully edge triggered. The state of each D input, one set-up time before

the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors.

The active Low Output Enable (nOE) controls all ten 3-State buffers independent of the register operation. When nOE is Low, the data in the register appears at the outputs. When nOE is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

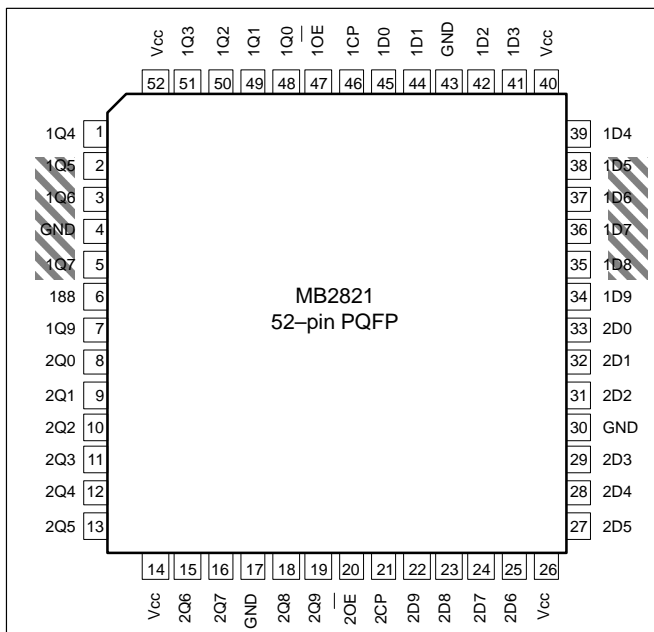
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T _{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t _{PLH} t _{PHL}	Propagation delay nCP to nQx	C _L = 50pF; V _{CC} = 5V	4.6	ns
C _{IN}	Input capacitance	V _I = 0V or V _{CC}	4	pF
C _{OUT}	Output capacitance	V _O = 0V or V _{CC} ; 3-State	7	pF
I _{CCZ}	Total supply current	Outputs disabled; V _{CC} = 5.5V	120	μA

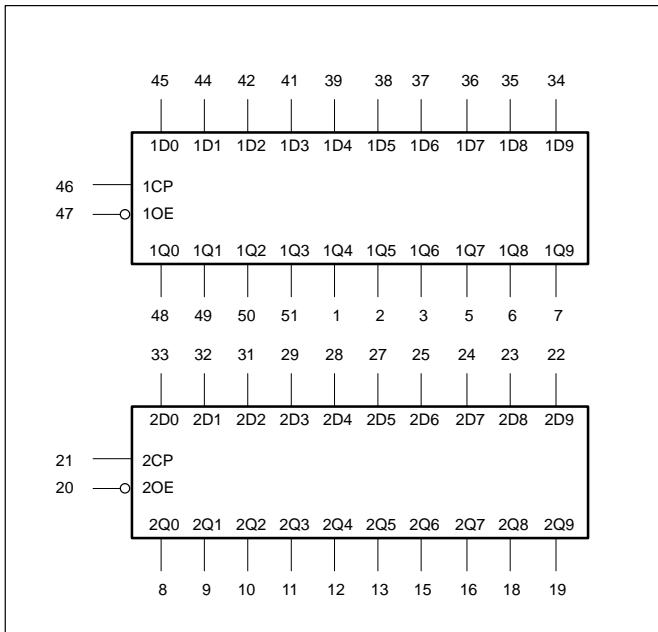
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
52-pin plastic Quad Flat Pack	-40°C to +85°C	MB2821BB	1418B

PIN CONFIGURATION



LOGIC SYMBOL



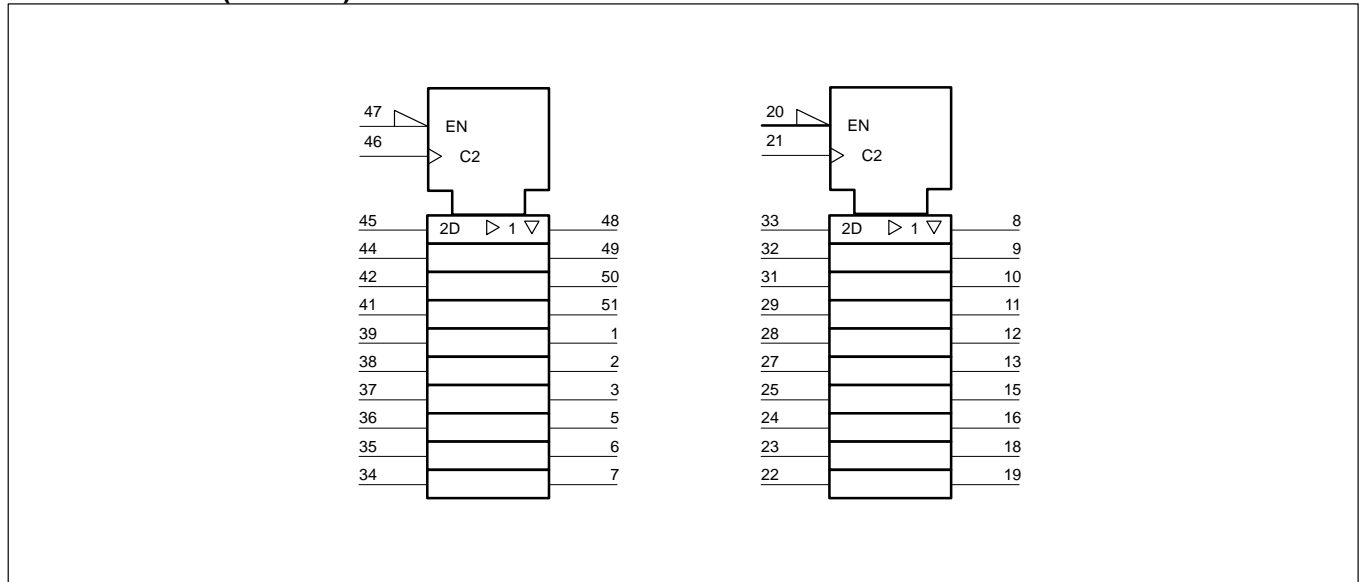
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PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
45, 44, 42, 41, 39, 38, 37, 36, 35, 34, 33, 32, 31, 29, 28, 27, 25, 24, 23, 22	1D0 – 1D9 2D0 – 2D9	Data inputs
48, 49, 50, 51, 1, 2, 3, 5, 6, 7, 8, 9, 10, 11, 12, 13, 15, 16, 18, 19	1Q0 – 1Q9 2Q0 – 2Q9	Data outputs
47, 20	1 \overline{OE} , 2 \overline{OE}	Output enable inputs (active-Low)
46, 21	1CP, 2CP	Clock pulse inputs (active rising edge)
4, 17, 30, 43	GND	Ground (0V)
14, 26, 40, 52	V _{CC}	Positive supply voltage

LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

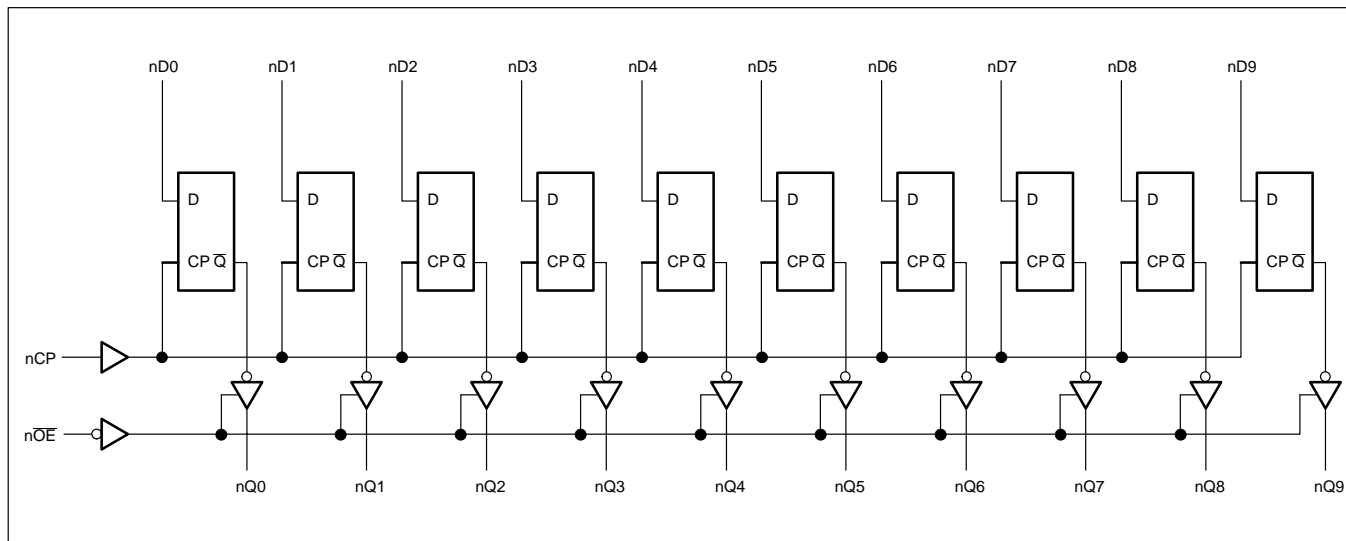
INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
n \overline{OE}	nCP	nDx		nQ0 – nQ9	
L	↑	l	L	L	Load and read register
L	↑	h	H	H	
L	↑	X	NC	NC	Hold
H	↑	X	NC	Z	Disable outputs
H	↑	Dn	Dn	Z	

- H = High voltage level
- h = High voltage level one set-up time prior to the Low-to-High clock transition
- L = Low voltage level
- l = Low voltage level one set-up time prior to the Low-to-High clock transition
- NC = No change
- X = Don't care
- Z = High impedance "off" state
- ↑ = Low to High clock transition
- ↑ = Not a Low-to-High clock transition

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LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +7.0	V
I _{IK}	DC input diode current	V _I < 0	-18	mA
V _I	DC input voltage ³		-1.2 to +7.0	V
I _{OK}	DC output diode current	V _O < 0	-50	mA
V _{OUT}	DC output voltage ³	output in Off or High state	-0.5 to +5.5	V
I _{OUT}	DC output current	output in Low state	128	mA
T _{stg}	Storage temperature range		-65 to 150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V _{CC}	DC supply voltage	4.5	5.5	V
V _I	Input voltage	0	V _{CC}	V
V _{IH}	High-level input voltage	2.0		V
V _{IL}	Low-level Input voltage		0.8	V
I _{OH}	High-level output current		-32	mA
I _{OL}	Low-level output current		64	mA
Δt/Δv	Input transition rise or fall rate	0	5	ns/V
T _{amb}	Operating free-air temperature range	-40	+85	°C

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T _{amb} = +25°C			T _{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V _{IK}	Input clamp voltage	V _{CC} = 4.5V; I _{IK} = -18mA		-0.9	-1.2		-1.2	V
V _{OH}	High-level output voltage	V _{CC} = 4.5V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH}	2.5	2.9		2.5		V
		V _{CC} = 5.0V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH}	3.0	3.4		3.0		V
		V _{CC} = 4.5V; I _{OH} = -32mA; V _I = V _{IL} or V _{IH}	2.0	2.4		2.0		V
V _{OL}	Low-level output voltage	V _{CC} = 4.5V; I _{OL} = 64mA; V _I = V _{IL} or V _{IH}		0.42	0.55		0.55	V
V _{RST}	Power-up output voltage NO TAG	V _{CC} = 5.5V; I _O = 1mA; V _I = GND or V _{CC}		0.13	0.55		0.55	V
I _I	Input leakage current	V _{CC} = 5.5V; V _I = GND or 5.5V		±0.01	±1.0		±1.0	μA
I _{OFF}	Power-off leakage current	V _{CC} = 0.0V; V _O or V _I ≤ 4.5V		±5.0	±100		±100	μA
I _{PU/PD}	Power-up/down 3-State output current ⁴	V _{CC} = 2.1V; V _O = 0.5V; V _I = GND or V _{CC} ; V _{OE} = Don't care		±5.0	±50		±50	μA
I _{OZH}	3-State output High current	V _{CC} = 5.5V; V _O = 2.7V; V _I = V _{IL} or V _{IH}		5.0	50		50	μA
I _{OZL}	3-State output Low current	V _{CC} = 5.5V; V _O = 0.5V; V _I = V _{IL} or V _{IH}		-5.0	-50		-50	μA
I _{CEX}	Output High leakage current	V _{CC} = 5.5V; V _O = 5.5V; V _I = GND or V _{CC}		5.0	50		50	μA
I _O	Output current ¹	V _{CC} = 5.5V; V _O = 2.5V	-50	-70	-180	-50	-180	mA
I _{CCH}	Quiescent supply current	V _{CC} = 5.5V; Outputs High, V _I = GND or V _{CC}		120	250		250	μA
I _{CCL}		V _{CC} = 5.5V; Outputs Low, V _I = GND or V _{CC}		54	76		76	mA
I _{CCZ}		V _{CC} = 5.5V; Outputs 3-State; V _I = GND or V _{CC}		120	250		250	μA
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 5.5V; one input at 3.4V, other inputs at V _{CC} or GND		0.5	1.5		1.5	mA

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
- This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V a transition time of up to 100μsec is permitted.

AC CHARACTERISTICS

GND = 0V, t_r = t_f = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V			T _{amb} = -40 to +85°C V _{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
f _{MAX}	Maximum clock frequency	1	160	250		160		MHz
t _{PLH} t _{PHL}	Propagation delay nCP to nQx	1	2.5 2.7	4.4 4.6	5.6 6.0	2.5 2.7	6.4 6.7	ns
t _{PZH} t _{PZL}	Output enable time to High and Low level	3 4	1.2 2.2	3.3 3.8	4.2 5.1	1.2 2.2	5.0 5.8	ns
t _{PHZ} t _{PLZ}	Output disable time from High and Low level	3 4	1.3 1.5	3.2 3.0	4.6 4.2	1.3 1.5	5.0 4.7	ns

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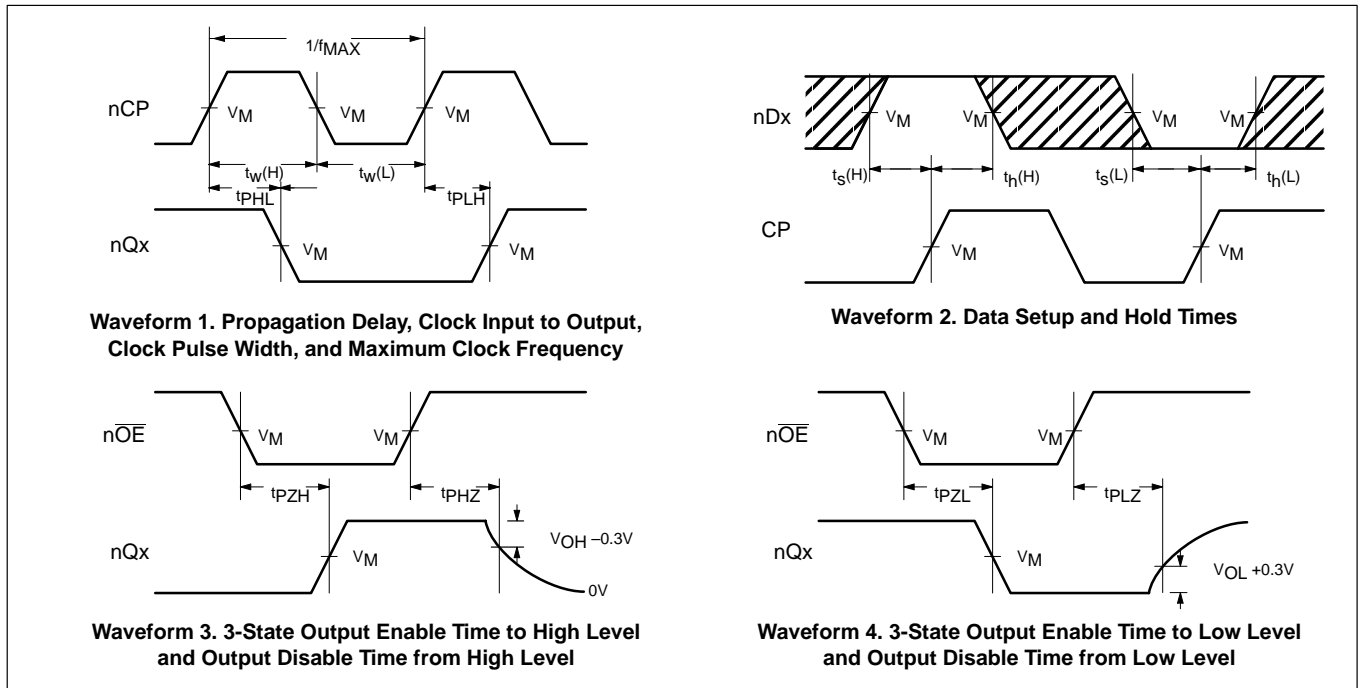
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AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			$T_{\text{amb}} = +25^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V}$			$T_{\text{amb}} = -40$ to $+85^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 0.5\text{V}$		
			MIN	TYP	MAX	MIN	MAX	
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, High or Low nDx to nCP	2	1.5 1.0	0.6 -0.2		1.5 1.0		ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, High or Low nDx to nCP	2	1.0 1.0	0.3 -0.4		1.0 1.0		ns
$t_w(\text{H})$ $t_w(\text{L})$	nCP pulse width High or Low	1	3.5 3.0	2.2 1.6		3.5 3.0		ns

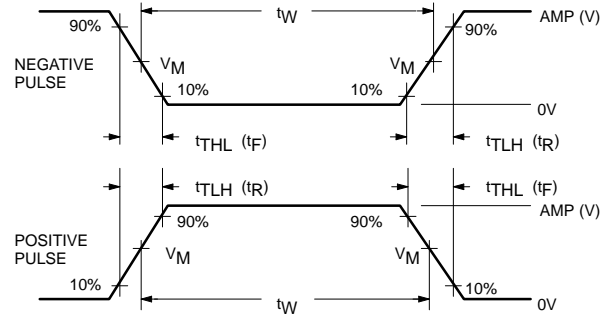
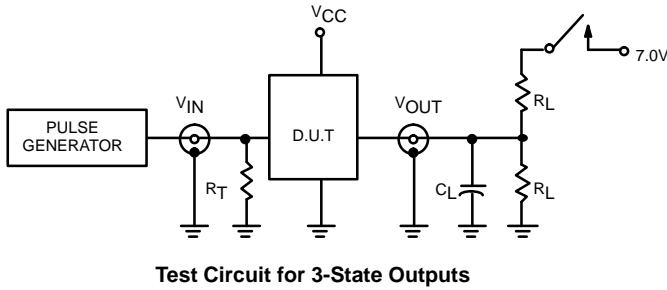
AC WAVEFORMS



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TEST CIRCUIT AND WAVEFORM



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t _{PLZ}	closed
t _{pZL}	closed
All other	open

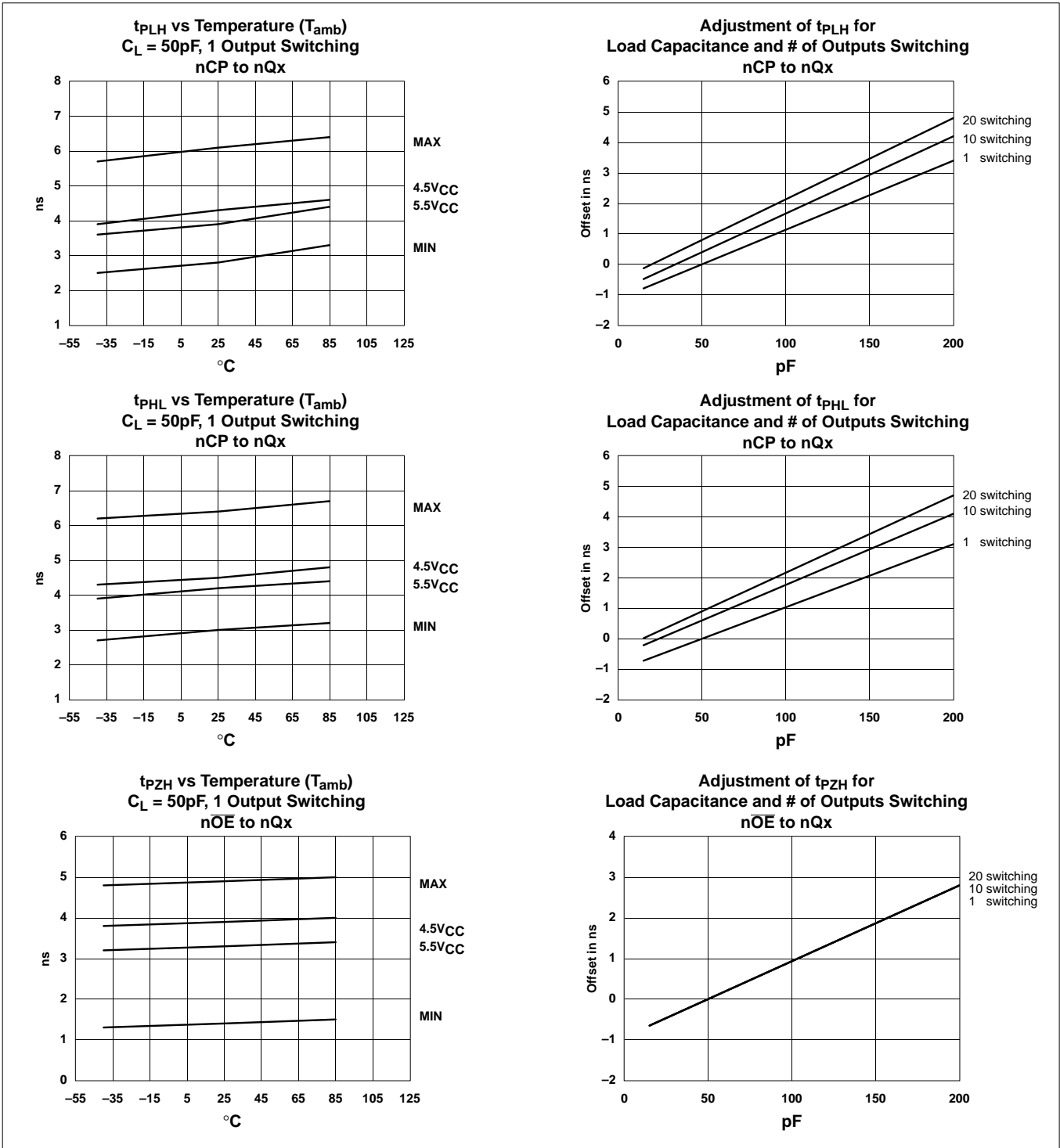
DEFINITIONS

- R_L = Load resistor; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t _w	t _r	t _f
MB	3.0V	1MHz	500ns	2.5ns	2.5ns

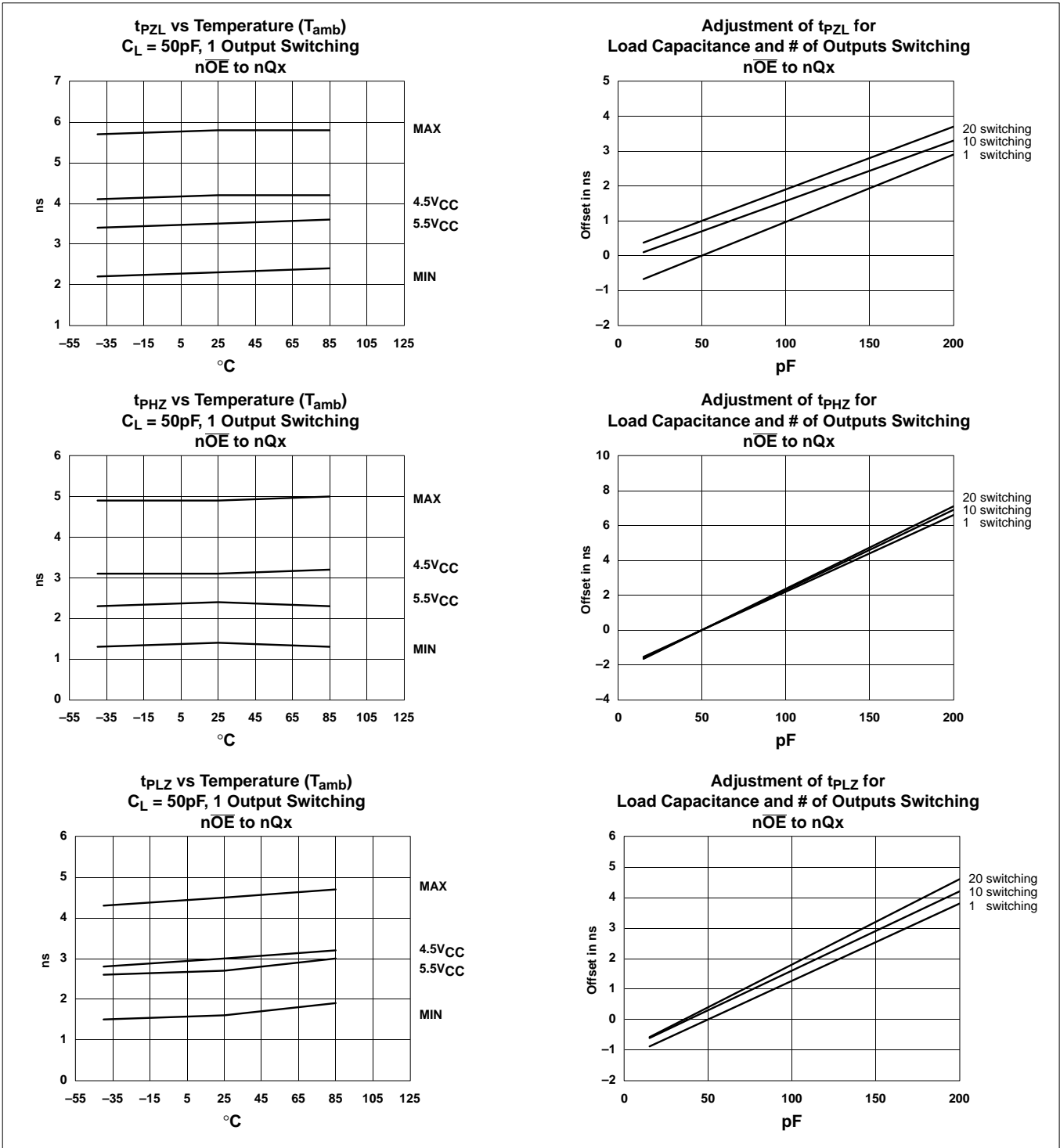
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