MOTOROLA
SEMICONDUCTOR MOTOROLA SC (TELECOM)
TECHNICAL DATA

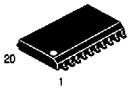
MC145030

Advance Information

Remote Control Encoder/ Decoder

CMOS

P SUFFIX
PLASTIC DIP
CASE 738



DW SUFFIX
SOG
CASE 751D

ORDERING INFORMATION

MC145030P	Plastic DIP
MC145030DW	SOG Package

The MC145030 encodes and decodes nine bits of information, which allows 512 different codes.

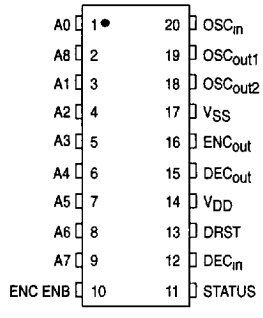
The encoder section samples the 9-bit parallel address input, encodes the bits into Manchester Code, and sends the serial information via the ENC_{out} pin. The address is issued twice per encoding sequence; initialization occurs with a rising edge on ENC ENB.

The decoder accepts serial information at the DEC_{in} pin, and decodes the Manchester information. The decoded address is compared with the local address. If a match occurs, DEC_{out} toggles once per sequence. The active-high DRST input is used to clear DEC_{out}.

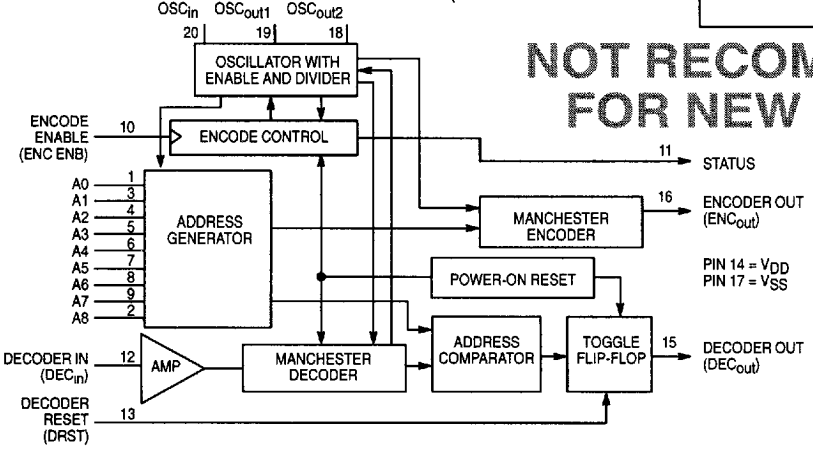
The Status pin, when high, indicates the device is encoding. During decoding or standby, Status is low.

- Applications:
  Cordless Phones and Half-Duplex Remote Control
- Interfaces with RF, Ultrasonic, or Infrared Modulators and Demodulators
- Operating Temperature Range: – 40 to 85°C
- Operating Voltage Range: 2 to 6 V
- Standby Supply Current: 20 µA Maximum @ 2.0 V
- Operating Supply Current: 700 µA Maximum @ 2.5 V
- Address Inputs Have On-Chip Pull-Up Devices
- RC Oscillator, No Crystal Required
- On-Chip Amplifier in Decode Section
- Power-On Reset Forces DEC_{out} Low and Initializes the Decoder and Encoder Sections
- See Application Notes AN1016 and AN1126 and Article Reprint AR255

PIN ASSIGMENT



BLOCK DIAGRAM



NOT RECOMMENDED FOR NEW DESIGN

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	− 0.5 to + 7.0	V
V_{in}	DC Input Voltage	− 0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage	− 0.5 to V_{DD} + 0.5	V
I_{in}	DC Input Current, per Pin	± 10	mA
I_{out}	DC Output Current, per Pin	± 10	mA
I_{DD}	DC Supply Current, V_{DD} and V_{SS} Pins	± 30	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	− 65 to + 150	°C
T_L	Lead Temperature (10-Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

† Power Dissipation Temperature Derating: − 12 mW/°C from 65 to 85°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Except for the Address Inputs, unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). The Address inputs may be left open; see Pin Descriptions. Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, Voltages Referenced to V_{SS})

Symbol	Parameter	Test Condition	V_{DD} V	Guaranteed Limit	Unit
V_{DD}	Power Supply Voltage Range		—	2.0 to 6.0	V
V_{IL}	Maximum Low-Level Input Voltage (Except DEC_{in})		2.5 6.0	0.3 1.2	V
V_{IH}	Minimum High-Level Input Voltage (Except DEC_{in})		2.5 6.0	1.9 4.5	V
V_{sig}	Minimum Output Voltage of Signal Source Driving DEC_{in}	Square-Wave Source See Figure 1	2.5 6.0	200 200	mV_{p-p}
V_{OL}	Maximum Low-Level Output Voltage	I_{out} = 0 µA I_{out} = 0.4 mA	2.5	0.15 0.4	V
		I_{out} = 0 µA I_{out} = 1.0 mA	6.0	0.15 0.4	
V_{OH}	Minimum High-Level Output Voltage	I_{out} = 0 µA I_{out} = − 0.4 mA	2.5	2.35 2.0	V
		I_{out} = 0 µA I_{out} = − 1.0 mA	6.0	5.85 5.5	
I_{in}	Maximum Input Current DEC_{in} ENC ENB, DRST, OSC_{in}	V_{in} = V_{DD} or V_{SS}	6.0	± 60 ± 0.3	µA
I_{IH}	Maximum High-Level Input Leakage Current A0–A8	V_{in} = V_{DD}	6.0	0.3	µA
I_{IL}	Maximum Low-Level Pull-Up Current A0–A8	V_{in} = V_{SS}	6.0	− 100	µA
I_{OZ}	Maximum Three-State Leakage Current ENC_{out}	V_{out} = V_{DD} or V_{SS}	6.0	± 500	nA
I_{DD}	Maximum Quiescent Supply Current	Device in Standby Mode V_{in} = V_{SS} or V_{DD} for ENC ENB, DEC_{in}, DRST, OSC_{in} V_{in} = V_{SS}, V_{DD}, or Open for A0–A8 I_{out} = 0 µA	2.0 6.0	20 100	µA
I_{dd}	Maximum RMS Operating Supply Current	Oscillator Frequency = 500 kHz V_{in} = V_{SS} or V_{DD} for ENC ENB, DEC_{in}, DRST, OSC_{in} V_{in} = V_{SS}, V_{DD}, or Open for A0–A8 I_{out} = 0 µA	2.5 6.0	700 2500	µA

AC ELECTRICAL CHARACTERISTICS (T_A = 25°C, C_L = 50 pF, V_{DD} = 2.5 to 6 V unless otherwise stated)

Symbol	Parameter	Figure #	V_{DD} V	Guaranteed Limit	Unit
f_{osc}	Maximum Oscillator Frequency (≈ 50% Duty Cycle)*	2	—	500	kHz
t_{PLH}, t_{PHL}	System Propagation Delay, ENC ENB (of an encoding device) to DEC_{out} (of a decoding device)	3, 5	—	384–608	OSC Cycles
t_d	Debounce Time, ENC ENB (guarantees 1 encoding sequence)		—	608	OSC Cycles
t_w	Minimum Input Pulse Width, ENC ENB or DRST	4	2.5 6.0	200 80	ns
C_{in}	Maximum Input Capacitance		—	10	pF

*See Pin Descriptions and Application Example for component tolerances.

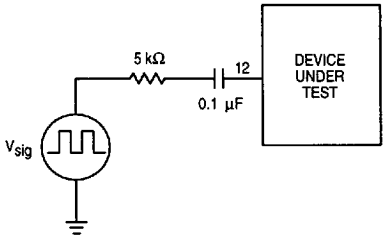


Figure 1. Decoder Input Sensitivity Test

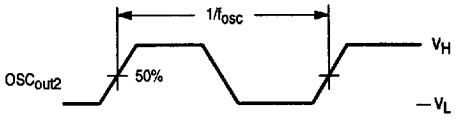


Figure 2. Switching Waveform

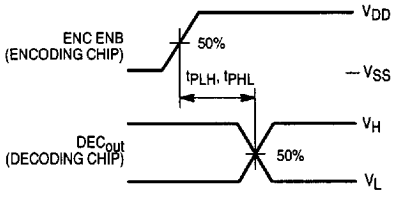


Figure 3. Switching Waveforms

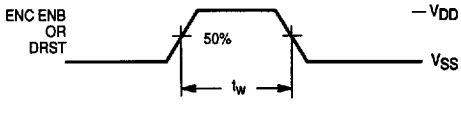
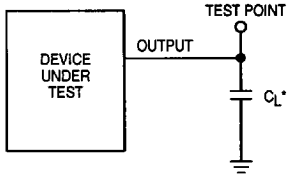


Figure 4. Switching Waveform



*Includes all probe and fixture capacitance.

Figure 5. Test Circuit

PIN DESCRIPTIONS

INPUT PINS

A0–A8
Local Address Inputs (Pins 1, 3–9, 2)

These binary inputs provide the address for both the encoder and decoder; 512 addresses are possible. The local address is sent serially from ENC_{out} with 2 sync bits appearing first, followed by A0. The decoder compares the local address with the received address stream.

On-chip pullup devices are provided on the address inputs to facilitate interface to SPST switches or jumpers to V_{SS}. During standby, A0–A8 are in the high-impedance state (i.e., the pull-up devices are inactive to minimize standby power consumption).

The inputs are left open (or tied to V_{DD}) for a high level and tied to V_{SS} for a low level.

ENC ENB
Edge-Sensitive Encode Enable (Pin 10)

A low-to-high transition on this pin aborts any decoding sequence in progress and initiates an encoding sequence. This input is debounced 608 oscillator cycles. See Figures 8 and 9.

DEC_{in}
Decoder In (Pin 12)

Decoder In is the input to the on-chip amplifier. The incoming signal is usually capacitively-coupled to this pin. Direct coupling may be used if the signal level is rail-to-rail (V_{SS} to V_{DD}).

DRST
Level-Sensitive Decoder Reset (Pin 13)

When this input is taken high, DEC_{out} is cleared to a low level. This pin may be used to override a response from a DEC_{in} data stream.

OUTPUT PINS

STATUS
Encode/Decode Status (Pin 11)

This pin is high during the encoding sequence and low during decoding or idle.

When Status is low, the ENC_{out} pin is in the high-impedance state.

DEC_{out}
Toggle Flip-Flop Decoder Output (Pin 15)

The encoder sends the same address twice to complete a sequence. If one or both of the decoded addresses matches the local address, DEC_{out} toggles once per sequence (unless overridden by DRST). See Figures 6 and 7.

ENC_{out}
Three-State Encoder Output (Pin 16)

This is the serial output of the Manchester-encoded local address. A0 appears before A8 in the bit stream. The local address is sent twice to complete a sequence which is initialized by ENC ENB. When a sequence is complete, ENC_{out} returns to the high-impedance state. See Figures 8 and 9.

OSCILLATOR PINS

OSC_{in}, OSC_{out1}, OSC_{out2}
Oscillator Input, Oscillator Outputs 1/2 (Pins 20, 19, 18)

As shown in Figure 10, these pins are used in conjunction with external resistors and a capacitor to form an oscillator. Polystyrene or mylar capacitors are recommended. Susceptibility to externally induced noise signals may occur if resistors utilized are greater than 1 MΩ. See Figure 10 for component tolerances.

When the on-chip oscillator is used, the frequency may be up to 500 kHz. The oscillator is active only during encoding or decoding.

When an external frequency source is used to drive OSC_{in}, OSC_{out1} and OSC_{out2} may be left floating. The signal applied to OSC_{in} should swing rail-to-rail and may be dc to 500 kHz.

POWER SUPPLY PINS

V_{SS}
Negative Power Supply (Pin 17)

This pin is the negative supply potential and is usually ground.

V_{DD}
Positive Power Supply (Pin 14)

This pin is the positive supply potential and may range from + 2 to + 6 V with respect to V_{SS}.

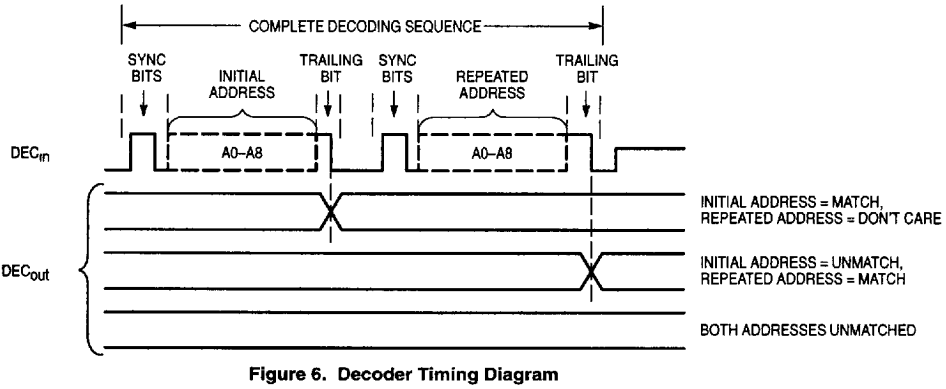


Figure 6. Decoder Timing Diagram

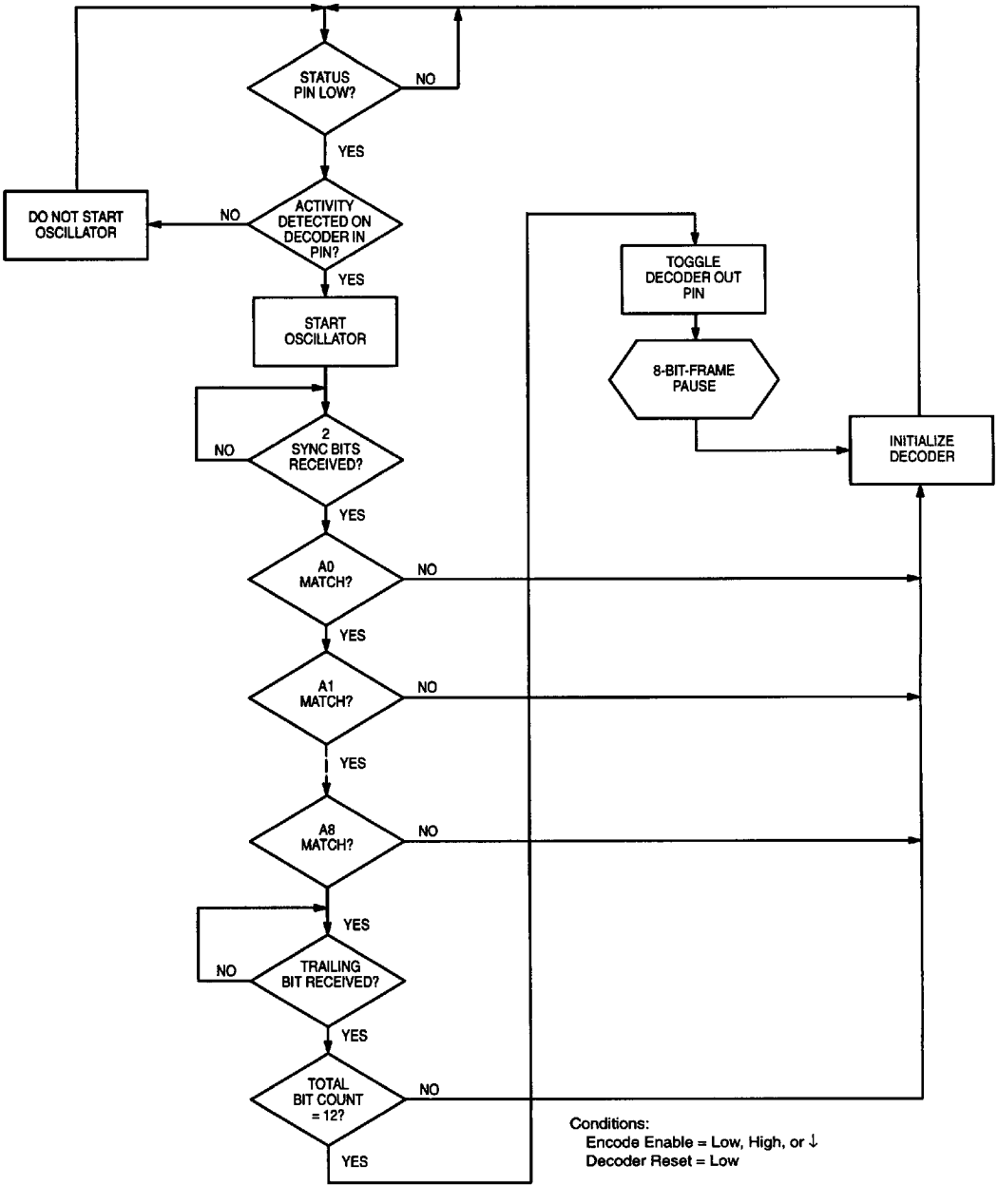


Figure 7. Decoder Flowchart

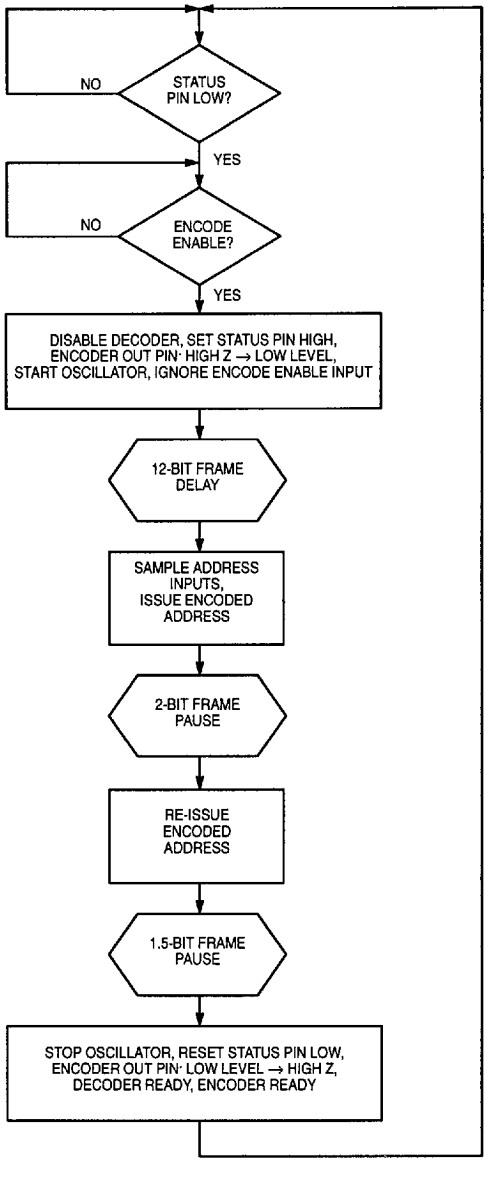


Figure 8. Encoder Flowchart

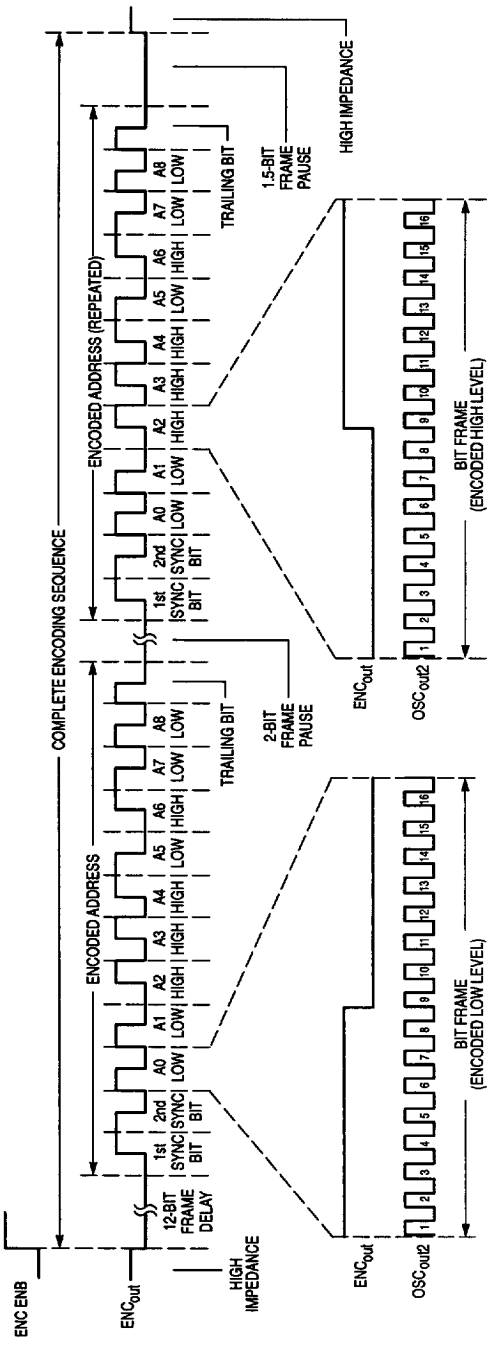
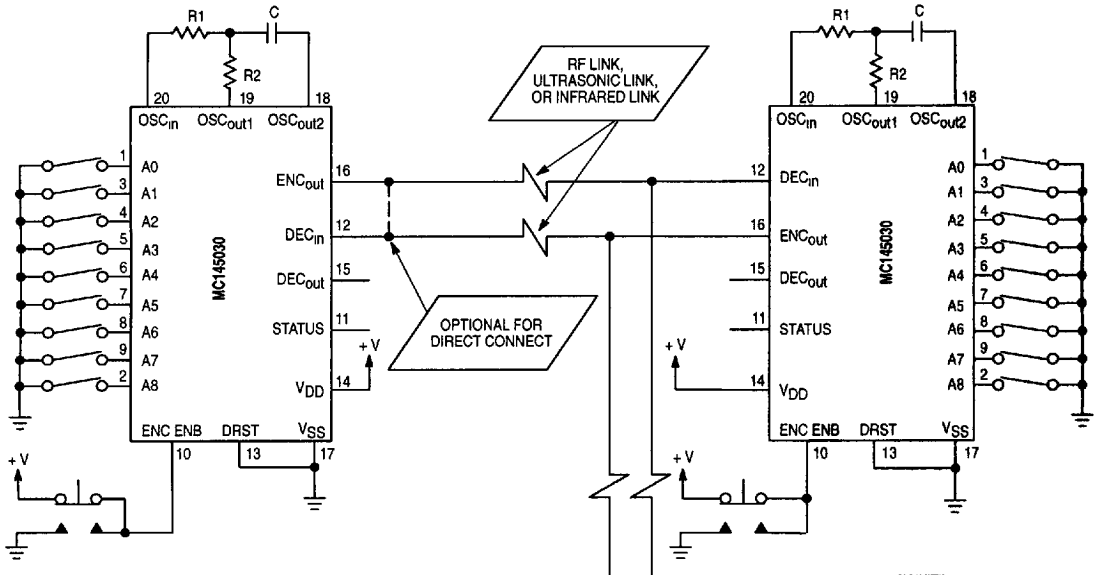


Figure 9. Encoder Timing Diagram



EXAMPLE R/C VALUES

f_{OSC} (APPROX.)	R1	R2	C	ENCODE ENABLE SWITCH DEBOUNCE TIME (APPROX.)
452 kHz	30 kΩ	5.6 kΩ	100 pF	1.3 ms
220 kHz	47 kΩ	10 kΩ	100 pF	2.8 ms
70 kHz	47 kΩ	10 kΩ	510 pF	8.7 ms
4.1 kHz	330 kΩ	47 kΩ	2200 pF	148 ms

GUIDELINES: 100 pF ≤ C ≤ 0.1 μF
2 (R2) < R1 < 10 (R2)
10 kΩ ≤ R2 ≤ 500 kΩ
R1 ≤ 1 MΩ

The maximum oscillator frequency difference allowable from encoding IC to decoding IC is ± 11%. The ambient temperature and supply voltage differences between ICs affect this frequency difference. Therefore, the tolerances of the frequency-determining components R2 and C are determined by the rule of thumb:

$$[\Delta R2 + \Delta C + \Delta f_{IC} + \Delta f_{temp} + \Delta f_{sup}] \leq \pm 11\%,$$

where

R2 = tolerance of R2 in percent
C = tolerance of C in percent
f_{IC} = IC frequency variation from part to part (expected value: ± 4%)
f_{temp} = IC frequency variation over temperature (expected value: ± 2% @ 25°C ± 40°)
f_{sup} = IC frequency variation with supply (expected value: ± 2% @ 5 V ± 0.5 V)

For the above variances: $[\Delta R2 + \Delta C + (\pm 4\%) + (\pm 2\%) + (\pm 2\%)] \leq \pm 11\%$

$[\Delta R2 + \Delta C] \leq \pm 3\%$

Choose R2 with a ± 1% tolerance and C2 with a ± 2% tolerance. R1 may be ± 5%.

Figure 10. Application Example