SILICON LABORATORIES

Si532

PRELIMINARY DATA SHEET

DUAL FREQUENCY XO (10 MHZ TO 1.4 GHZ)

Features

- Available with any-rate output frequencies from 10 to 945 MHz and selected frequencies to 1.4 GHz
- Two selectable output frequencies
- Industry standard 7x5 mm package
- Available CMOS, LVPECL, LVDS & CML outputs
- 3.3, 2.5, and 1.8 V supply options
- 3x better frequency stability than SAW based oscillators
- 3rd generation DSPLL® with superior jitter performance
- Internal fixed crystal frequency ensures high reliability and low aging
- Lead-free/RoHS-compliant

Ordering Information:

See page 7.

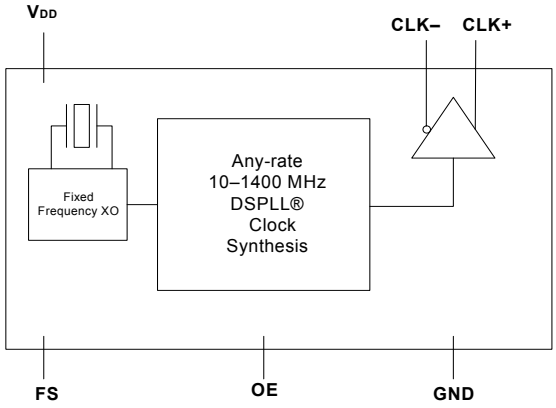
Applications

- SONET/SDH
- xDSL
- 10 GbE LAN/WAN
- Low jitter clock generation
- Optical modules
- Test and measurement

Description

The Si532 dual frequency XO utilizes Silicon Laboratories advanced DSPLL® circuitry to provide a very low jitter clock for all output frequencies. The Si532 is available with any-rate output frequency from 10 to 945 MHz and selected frequencies to 1400 MHz. Unlike traditional XOs where a different crystal is required for each output frequency, the Si532 uses one fixed crystal frequency to provide a wide range of output frequencies. This IC based approach allows the crystal resonator to be optimized for superior frequency, stability, and reliability. In addition, DSPLL clock synthesis provides superior supply noise rejection, simplifying the task of generating low jitter clocks in noisy environments often found in communication systems. The Si532 IC based XO is factory configurable for a wide variety of user specifications including frequency, supply voltage, and output format. Specific configurations are factory programmed into the Si532 at the time of shipment, thereby eliminating the long lead times associated with custom oscillators.

Functional Block Diagram



1. Electrical Specifications

Table 1. Si532 Electrical Specifications

Parameter	Min	Typ	Max	Units	Notes
Frequency					
Nominal Frequency LVDS/CML/LVPECL CMOS	 10 10	 — —	 945 160	MHz	Specified at time of order by P/N. Also available in bands from 970 to 1134 MHz and 1213 to 1417 MHz.
Initial Accuracy	–1.5	—	1.5	ppm	Measured at +25 °C at time of shipping
Temperature Stability	–20 –50	— —	+20 +50	ppm	Selectable option by P/N. See Section 4. "Ordering Information" on page 7.
Aging	—	—	±10	ppm	Frequency drift over projected 15 year life
Outputs					
Symmetry	45	—	55	%	LVPECL: V_{DD} – 1.3 V (differential) LVDS: 1.25 V (differential) CMOS: V_{DD}/2
RMS Jitter for $F_{OUT} \geq$ 500 MHz 12 kHz to 20 MHz 50 kHz to 80 MHz	 — —	 0.27 0.30	 — —	ps	$F_{OUT} \geq$ 500 MHz Differential Modes: LVPECL/LVDS/CML
RMS Jitter for F_{OUT} of 125 to 500 MHz 12 kHz to 20 MHz	 —	 0.5	 —	ps	125 < F_{OUT} < 500 MHz Differential Modes: LVPECL/LVDS/CML
Period Jitter for $F_{OUT} \leq$160 MHz Peak-to-Peak RMS	 — —	 5 1	 — —	ps	Any output N = 1000 cycles
LVPECL Output Option mid-level swing (diff) swing (single-ended)	 V_{DD} – 1.42 1.1 0.50	 — — —	 V_{DD} – 1.25 1.9 0.93	 V V_{PP} V_{PP}	50 Ω to V_{DD} – 2.0 V
LVDS Output Option mid-level swing (diff)	 1.125 0.32	 1.2 0.40	 1.275 0.50	 V V_{PP}	R_{term} = 100 Ω (differential)
CML Output Option mid-level swing	 — 0.70	 V_{DD} – 0.75 0.95	 — 1.20	 V V_{PP}	Rterm = 100 Ω (differential)

Table 1. Si532 Electrical Specifications (Continued)

Parameter	Min	Typ	Max	Units	Notes
CMOS Output Option V_{OH} V_{OL}	 0.8xV_{DD} —	 — —	 V_{DD} 0.4	 V	 C_L = 15 pF
Rise/Fall time	— —	— 1	350 —	ps ns	CML/LVPECL/LVDS at 20% / 80% CMOS with CL = 15 pF
Inputs					
Voltage (V_{DD}) 3.3 V option 2.5 V option 1.8 V option	 2.97 2.25 1.71	 3.3 2.5 1.8	 3.63 2.75 1.89	V	Optional parameter specified by P/N
Current Output enabled TriState mode	 — —	 90 60	 — —	 mA	
Frequency Select (FS) V_{IH} V_{IL}	 0.75 x V_{DD} 0	 — —	 V_{DD} 0.5	 V	 FS = “0” selects F0 FS = “1” selects F1
Output Enable V_{IH} V_{IL}	 0.75 x V_{DD} —	 — —	 V_{DD} 0.5	 V	

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Supply Voltage	V_{DD}	–0.5 to +3.8	V
Storage Temperature	T_S	–55 to +125	°C

Table 3. Environmental Conditions

Parameter	Conditions/Test Method
Operating Temperature	–40 to +85 °C
Mechanical Shock	MIL-STD-883F, Method 2002.3 B
Mechanical Vibration	MIL-STD-883F, Method 2007.3 A
Solderability	MIL-STD-883F, Method 203.8
Gross & Fine Leak	MIL-STD-883F, Method 1014.7
Resistance to Solvents	MIL-STD-883F, Method 2016

Table 4. Pinout

Pin	Symbol	Function
1	FS	Frequency Select
2	OE	Output Enable
3	GND	Ground
4	CLK+	Oscillator Output
5	CLK– (N/A for CMOS)	Complementary Output (N/C for CMOS)
6	V_{DD}	Power Suppy Voltage

2. Outline Diagram and Suggested Pad Layout

Figure 1 illustrates the package details for the Si532. Table 5 lists the values for the dimensions shown in the illustration.

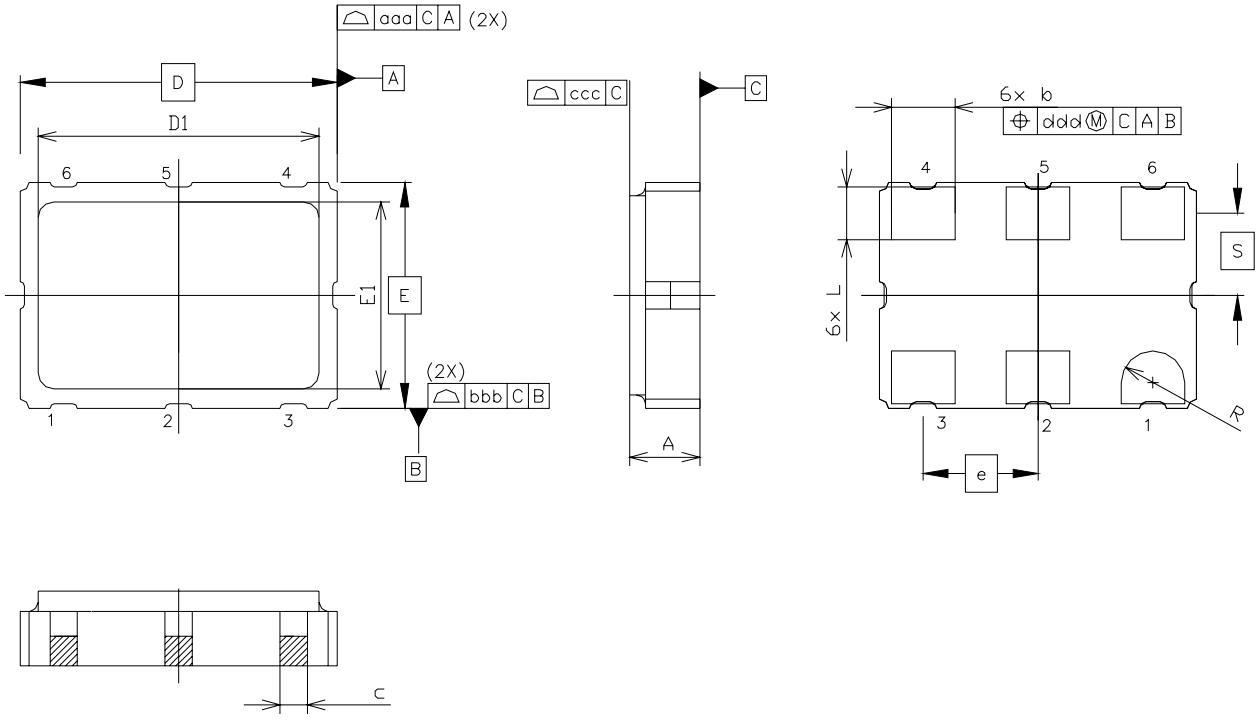


Figure 1. Si532 Outline Diagram

Table 5. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max
A	1.45	1.65	1.85
b	1.2	1.4	1.6
c		0.60 TYP.	
D		7.00 BSC.	
D1	6.10	6.2	6.30
e		2.54 BSC.	
E		5.00 BSC.	
E1	4.30	4.40	4.50
L	1.07	1.27	1.47
S		1.815 BSC.	
R		0.7 REF.	
aaa	—	—	0.15
bbb	—	—	0.15
ccc	—	—	0.10
ddd	—	—	0.10

3. 6-Pin PCB Land Pattern

Figure 2 illustrates the 6-pin PCB land pattern for the Si532. Table 6 lists the values for the dimensions shown in the illustration.

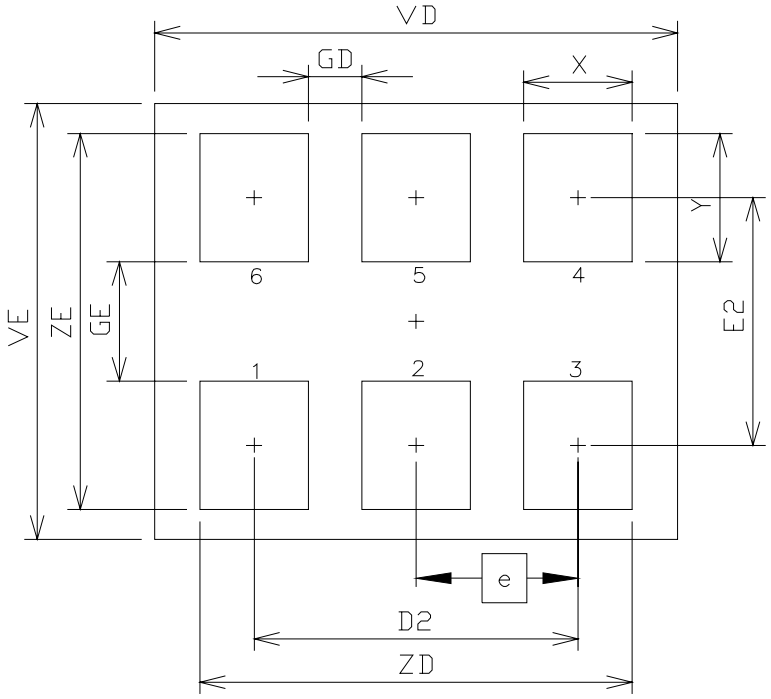


Figure 2. Si530 PCB Land Pattern

Table 6. PCB Land Pattern Dimensions (mm)

Dimension	Min	Max
D2	5.08 REF	
e	2.54 BSC	
E2	4.15 REF	
GD	0.84	—
GE	2.00	—
VD	8.20 REF	
VE	7.30 REF	
X	1.70 TYP	
Y	2.15 REF	
ZD	—	6.78
ZE	—	6.30

Notes:
1. Dimensioning and tolerancing per the ANSI Y14.5M-1994 specification.
2. Land pattern design based on IPC-7351 guidelines.
3. All dimensions shown are at maximum material condition (MMC).
4. Controlling dimension is in millimeters (mm).

4. Ordering Information

The Si532 was designed to support a variety of options including frequency, tuning slope, output format, and V_{DD}. Specific device configurations are programmed into the Si532 at time of shipment. A unique part number associated with these options and frequencies will be assigned. The Si532 XO series is supplied in an industry-standard, 7x5 mm package.

Part numbers for the Si532 Dual Frequency XO are determined by following configuration tables. Silicon Labs provides a web browser-based part number configuration tool to simplify this process. Refer to www.silabs.com/VCXO to access this tool and for further ordering instructions.

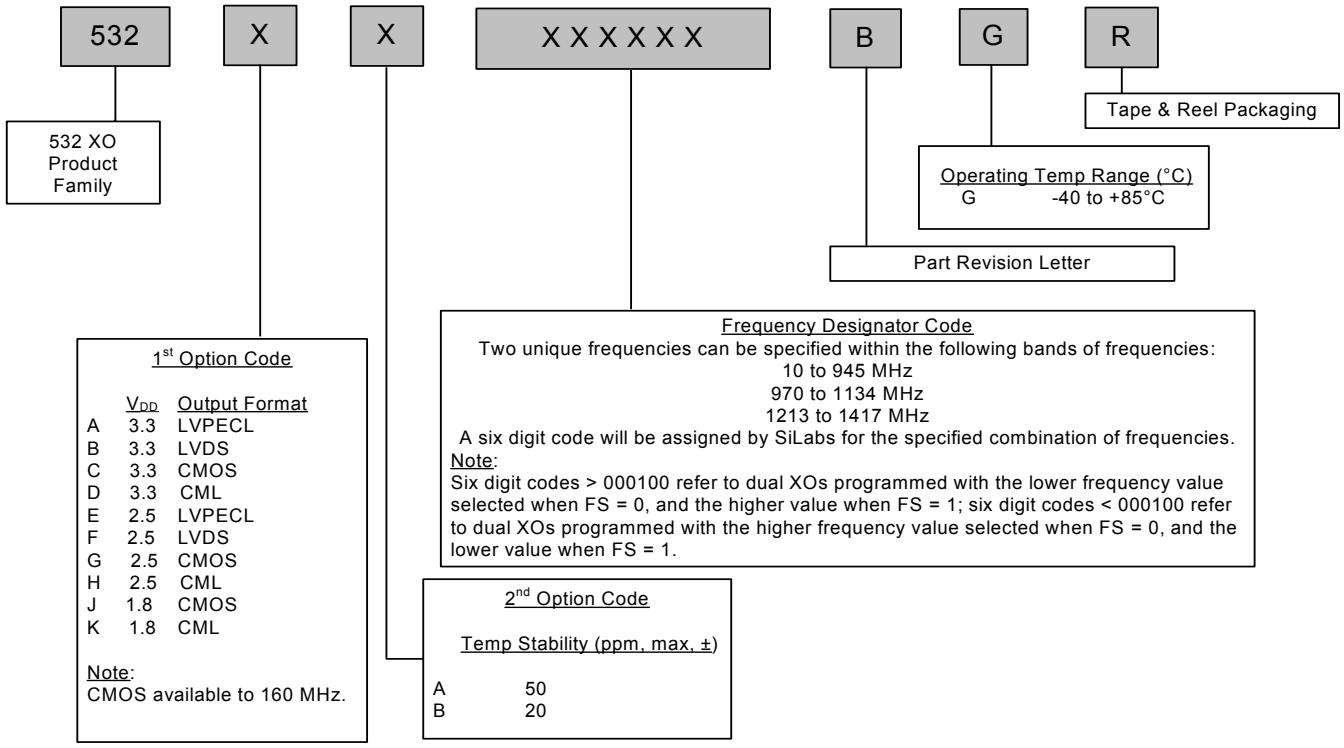


Figure 3. Part Number Convention

DOCUMENT CHANGE LIST

Revision 0.2 to Revision 0.3

- Updated the “Features” section.
- Updated Table 1, “Si532 Electrical Specifications,” on page 2.
  - Updated LVDS, CML, and CMOS electric specifications.
- Updated Figure 1, “Si532 Outline Diagram,” on page 5.
- Updated 4. "Ordering Information" on page 7.
  - Updated Figure 3, “Part Number Convention,” on page 7.

NOTES:

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