Low Dropout Regulator Driver

FEATURES

- **Low Cost Solution for High Current, Low Dropout Regulators**
- **Fast Transient Response Needs Much Less Bulk Capacitance**
- **Latching Overload Protection Minimizes Heat Sink Size**
- **Single Supply Operation: V_{IN} = 10V to 2.8V**
- Precision Output Voltage (1%)
- Small Surface Mount Package
- Capable of Very Low Dropout Voltage (<0.2V)
- Fixed or Adjustable Outputs
- Shutdown

APPLICATIONS

- 3.3V to 2.5V Regulator
- Microprocessor Power Source
- Post Regulator for Switching Supplies
- High Efficiency Linear Regulators
- Ultralow Dropout Regulators
- Low Voltage Linear Regulators

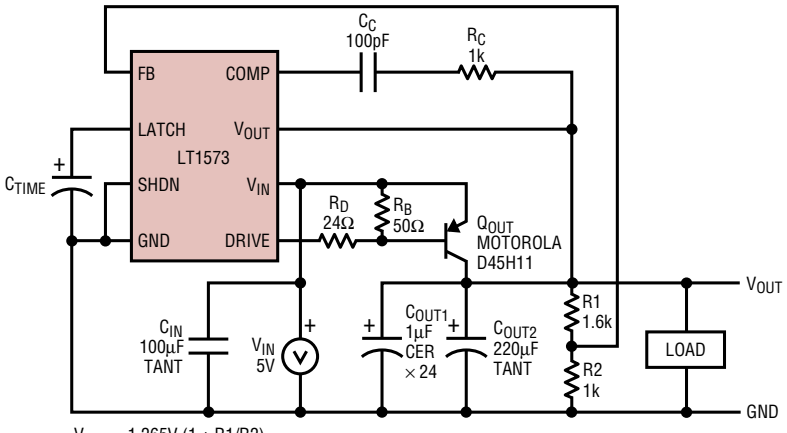
DESCRIPTION

The LT®1573 is a regulator driver IC designed to provide a low cost solution to applications requiring high current, low dropout and fast transient response. When combined with an external PNP power transistor, this device provides load current up to 5A with dropout voltages as low as 0.35V. The LT1573 circuitry is designed for extremely fast transient response. This greatly reduces bulk storage capacitance when the regulator is used in applications with fast, high current load transients.

To keep cost and complexity low, the LT1573 uses a new time-delayed latching current protection technique that requires no external current sense resistor. Base drive is limited for instantaneous protection, and a time-delayed latch protects the regulator from continuous short circuits.

The LT1573 is available as an adjustable regulator with an output range of 1.27V to 6.8V and with fixed output voltages of 2.5V, 2.8V and 3.3V. Output accuracy is better than 1% to meet the critical regulation requirement of fast microprocessors. A special 8-pin, fused-lead surface mount package is used to minimize regulator footprint and provide adequate heat sinking.

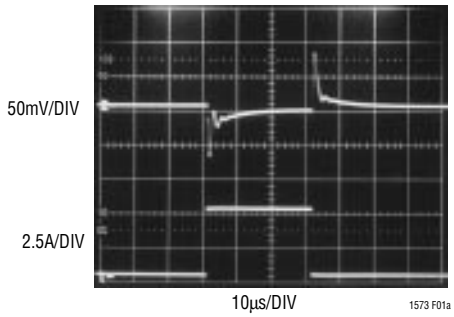
TYPICAL APPLICATION



V_{OUT} = 1.265V (1 + R1/R2)
FOR T < 45°C, C_{OUT1} = 24 × 1µF Y5V CERAMIC SURFACE MOUNT CAPACITORS.
FOR T > 45°C, C_{OUT1} = 24 × 1µF X7R CERAMIC SURFACE MOUNT CAPACITORS.
PLACE C_{OUT1} IN THE MICROPROCESSOR SOCKET CAVITY

Figure 1. 3.3V, 5A Microprocessor Supply

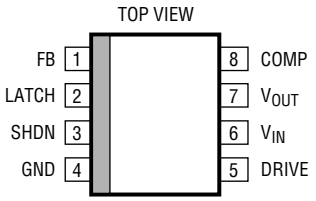
Transient Response for 0.2A to 5A Output Load Step



ABSOLUTE MAXIMUM RATINGS

Input Pin Voltage (V_{IN} to GND) 10V
Drive Pin Voltage (V_{DRIVE} to GND) 10V
Output Pin Voltage (V_{OUT} to GND) 10V
Shutdown Pin Voltage (V_{SHDN} to GND) 10V
Operating Junction Temperature Range .... 0°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 85°C/W

ORDER PART NUMBER
LT1573CS8 LT1573CS8-2.5 LT1573CS8-2.8 LT1573CS8-3.3
S8 PART MARKING
1573 157328 157325 157333

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, V_{DRIVE} = 3V, T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC Characteristics						
LT1573 Reference Voltage (Adjustable)(Note 1)	I_{DRIVE} = 20mA, T_J = 25°C		1.252	1.265	1.278	V
	5mA < I_{DRIVE} < 250mA, 3V < V_{IN} < 7V, 1.5V < V_{DRIVE} < 7V	●	1.240	1.265	1.290	V
LT1573-3.3 Output Voltage (Note 1)	I_{DRIVE} = 20mA. T_J = 25°C		3.267	3.3	3.333	V
	5mA < I_{DRIVE} < 250mA, 3.5V < V_{IN} < 7V, 1.5V < V_{DRIVE} < 7V	●	3.234	3.3	3.366	V
LT1573-2.8 Output Voltage (Note 1)	I_{DRIVE} = 20mA, T_J = 25°C		2.772	2.8	2.828	V
	5mA < I_{DRIVE} < 250mA, 3V < V_{IN} < 7V, 1.5V < V_{DRIVE} < 7V	●	2.744	2.8	2.856	V
LT1573-2.5 Output Voltage (Note 1)	I_{DRIVE} = 20mA, T_J = 25°C		2.475	2.5	2.525	V
	5mA < I_{DRIVE} < 250mA, 3V < V_{IN} < 7V, 1.5V < V_{DRIVE} < 7V	●	2.450	2.5	2.550	V
Line Regulation						
LT1573 (V_{FB})	I_{DRIVE} = 20mA, 3V < V_{IN} < 7V	●		0.17	2	mV
LT1573-3.3 (V_{OUT})	I_{DRIVE} = 20mA, 3.5V < V_{IN} < 7V	●		0.34	5	mV
LT1573-2.8 (V_{OUT})	I_{DRIVE} = 20mA, 3V < V_{IN} < 7V	●		0.34	4	mV
LT1573-2.5 (V_{OUT})	I_{DRIVE} = 20mA, 3V < V_{IN} < 7V	●		0.25	4	mV
Load Regulation						
LT1573 (V_{FB})	ΔI_{DRIVE} = 20mA to 250mA	●		7	15	mV
LT1573-3.3 (V_{OUT})	ΔI_{DRIVE} = 20mA to 250mA	●		18	40	mV
LT1573-2.8 (V_{OUT})	ΔI_{DRIVE} = 20mA to 250mA	●		15	34	mV
LT1573-2.5 (V_{OUT})	ΔI_{DRIVE} = 20mA to 250mA	●		13	30	mV
FB Pin Bias Current (Adjustable Only)	V_{FB} = 1.265V	●		0.8	5	µA
DRIVE Pin Current	V_{FB} = 1.35V, V_{DRIVE} = 7V	●			2	mA
	V_{FB} = 1.15V, V_{DRIVE} = 1.5V	●	250	440		mA
DRIVE Pin Saturation Voltage	I_{DRIVE} = 20mA, V_{FB} = 1.15V	●		0.12	0.3	V
	I_{DRIVE} = 250mA, V_{FB} = 1.15V	●		0.73	1.4	V
SHDN Pin Threshold Voltage		●	1.0	1.33	1.6	V
SHDN Pin Current	V_{SHDN} = 5V			200		µA

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, V_{DRIVE} = 3V, T_A = 25°C, unless otherwise noted.

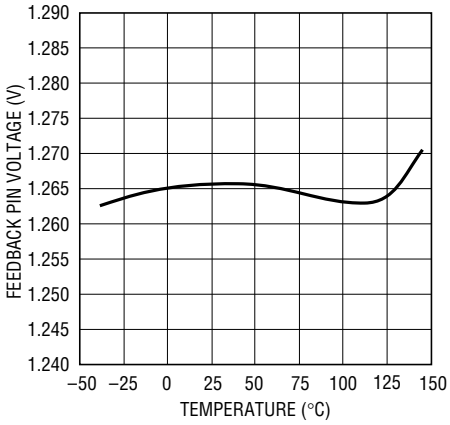
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LATCH Pin Latch-Off Threshold Voltage		●	0.8	1.4	2.2	V
LATCH Pin Charging Current				7		µA
LATCH Pin Latching Current				0.65		mA
$V_{IN} – V_{OUT}$ Differential Threshold for Latch Disable		●	0.4	0.7	1.0	V
Input Quiescent Current	V_{IN} = 7V	●		1.7	3.5	mA
Minimum Input Voltage for Bias Operation		●	2.8			V

The ● denotes specifications that apply over the full operating temperature range.

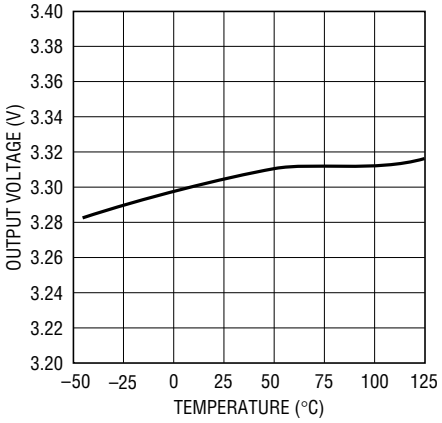
Note 1: Operating conditions are limited by maximum junction temperature. The regulated feedback or output voltage specification will not apply for all possible combinations of input voltage, drive voltage and drive current. When operating at maximum drive current, the drive voltage range must be limited. When operating at maximum input and drive voltage, the drive current must be limited.

TYPICAL PERFORMANCE CHARACTERISTICS

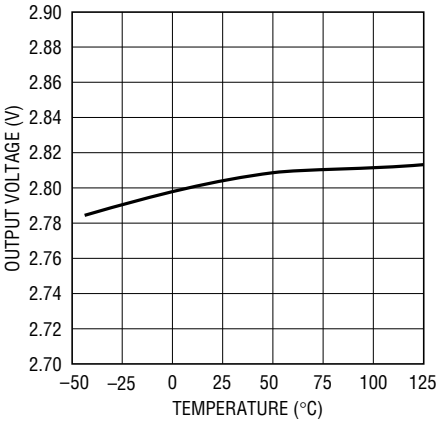
LT1573 Feedback Pin Voltage vs Temperature



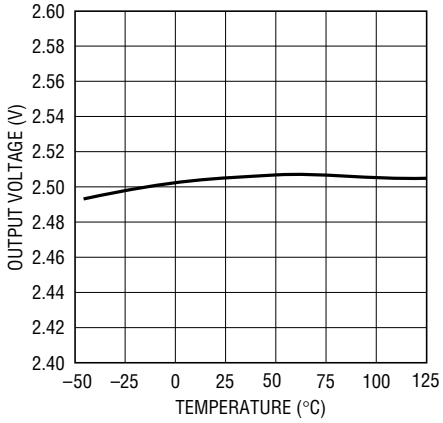
LT1573-3.3V Output Voltage vs Temperature



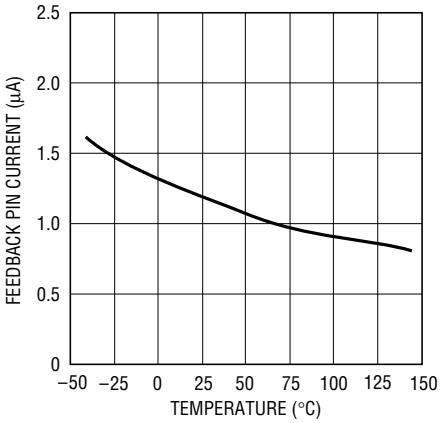
LT1573-2.8V Output Voltage vs Temperature



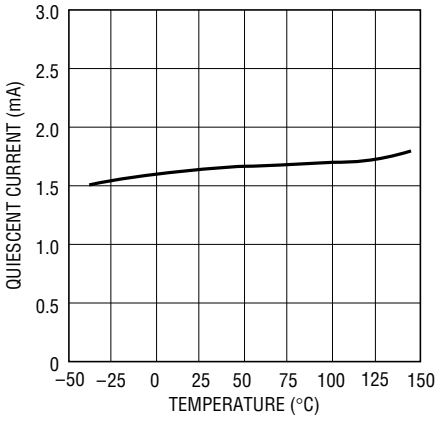
LT1573-2.5V Output Voltage vs Temperature



Feedback Pin Bias Current vs Temperature

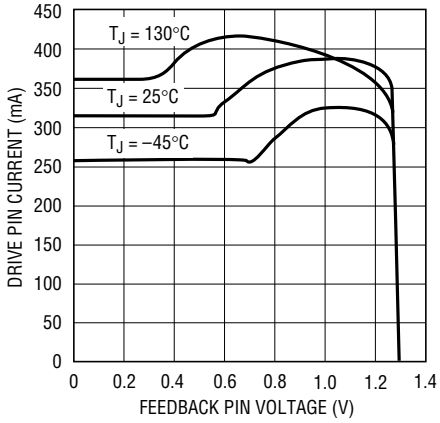


Quiescent Current vs Temperature



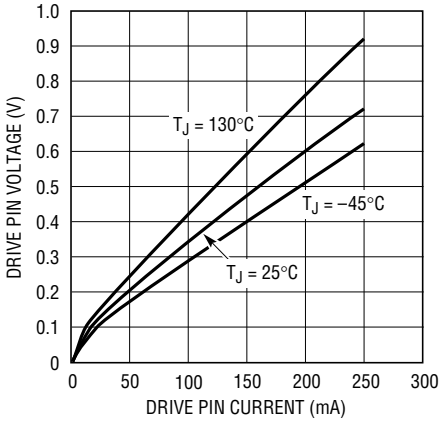
TYPICAL PERFORMANCE CHARACTERISTICS

Drive Pin Current vs Feedback Pin Voltage



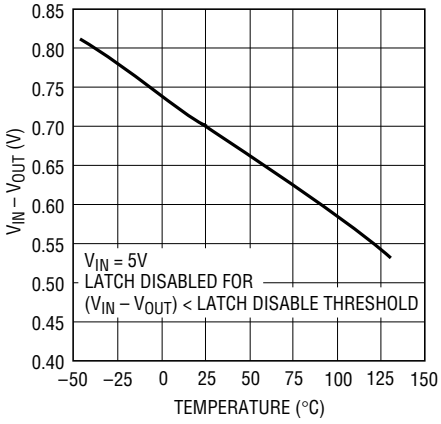
1573 G07

Drive Pin Saturation Voltage vs Drive Pin Current



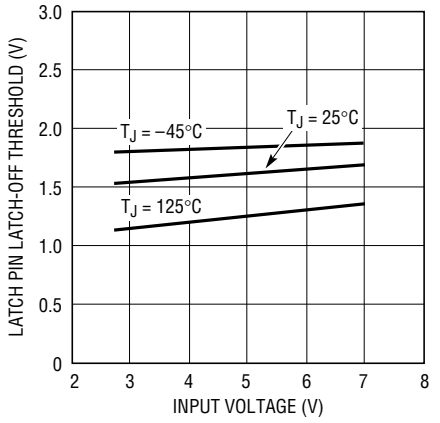
1573 G08

Latch-Disable Threshold ($V_{IN} – V_{OUT}$) vs Temperature



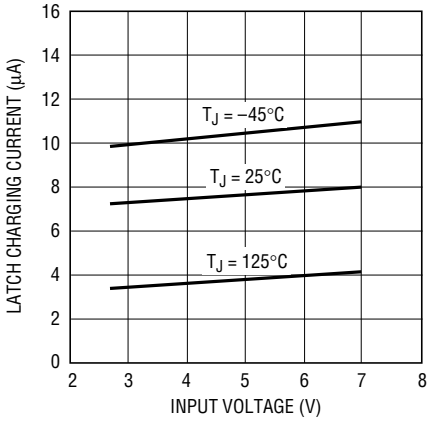
1573 G09

Latch Pin Latch-Off Threshold vs Input Voltage



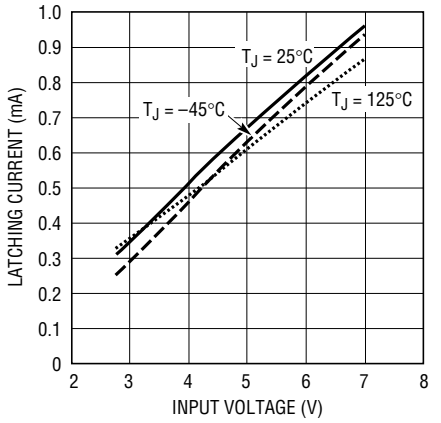
1573 G10

Latch Charging Current vs Input Voltage



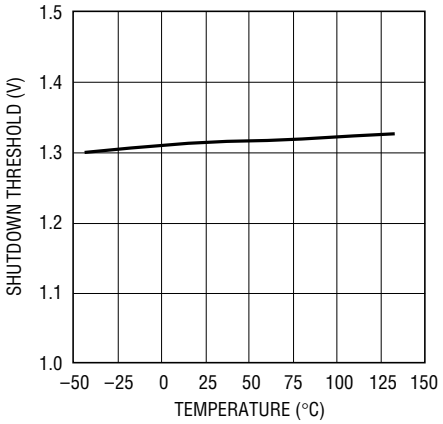
1573 G11

Latching Current vs Input Voltage



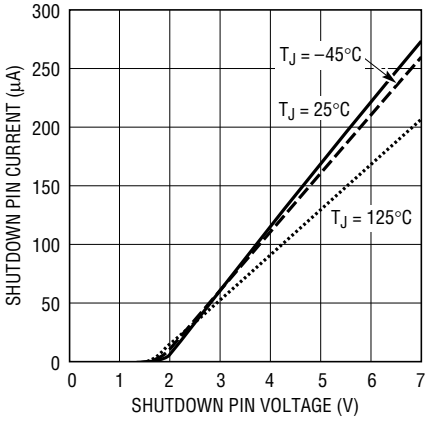
1573 G12

Shutdown Voltage Threshold vs Temperature



1573 G13

Shutdown Pin Current vs Shutdown Pin Voltage



1573 G14

PIN FUNCTIONS

FB (Pin 1): The feedback pin is the inverting input of the error amplifier. The noninverting input of the error amplifier is internally connected to a 1.265V reference. The error amplifier will servo the drive to the output transistor, Q_{OUT} in Figure 1, to force the voltage at the feedback pin to be 1.265V. Output voltage is set by a resistor divider as shown in Figure 1. For adjustable devices an external resistor divider is used to set the output voltage. For fixed voltage devices the resistor divider is internal and the top of the resistor divider is connected to the V_{OUT} pin.

LATCH (Pin 2): The LT1573 provides overcurrent protection with a timed latch-off circuit. The latch-off time out is triggered when the DRIVE pin is pulled below the saturation voltage of the drive transistor. The saturation voltage is a function of the drive current and is equal to approximately 130mV at 20mA rising to 780mV at 250mA (see typical performance curves). The time out is set by the latch charging current and the value of a capacitor connected between the LATCH pin and ground. If the overcurrent condition persists at the end of the timing cycle the regulator will latch off until either the latch is reset or power is cycled off and back on. The latch can be reset by either pulling the SHDN pin high, pulling current out of the LATCH pin greater than latching current or grounding the LATCH pin. Exceeding the thermal limit temperature will trigger the latch with no timing delay. Under normal condition, the DC voltage at the LATCH pin is zero. When the system is latched off, the DC voltage at theLATCH pin is two V_{BE} above ground.

SHDN (Pin 3): The SHDN pin has two functions. It can be used to turn off the output voltage by disabling the drive to the output transistor. It can also be used to reset the current limit latch. The shutdown/reset functions are activated by applying a voltage > 1.3V to the SHDN pin. The output voltage will restart as soon as the SHDN pin is pulled below the shutdown threshold. If the shutdown/reset function is not used, the pin should be grounded. The voltage applied to the SHDN pin can be higher than the input voltage. When the SHDN pin voltage is higher than 2V, the SHDN pin current increases and is limited by an internal 20k resistor.

GND (Pin 4): Circuit Ground.

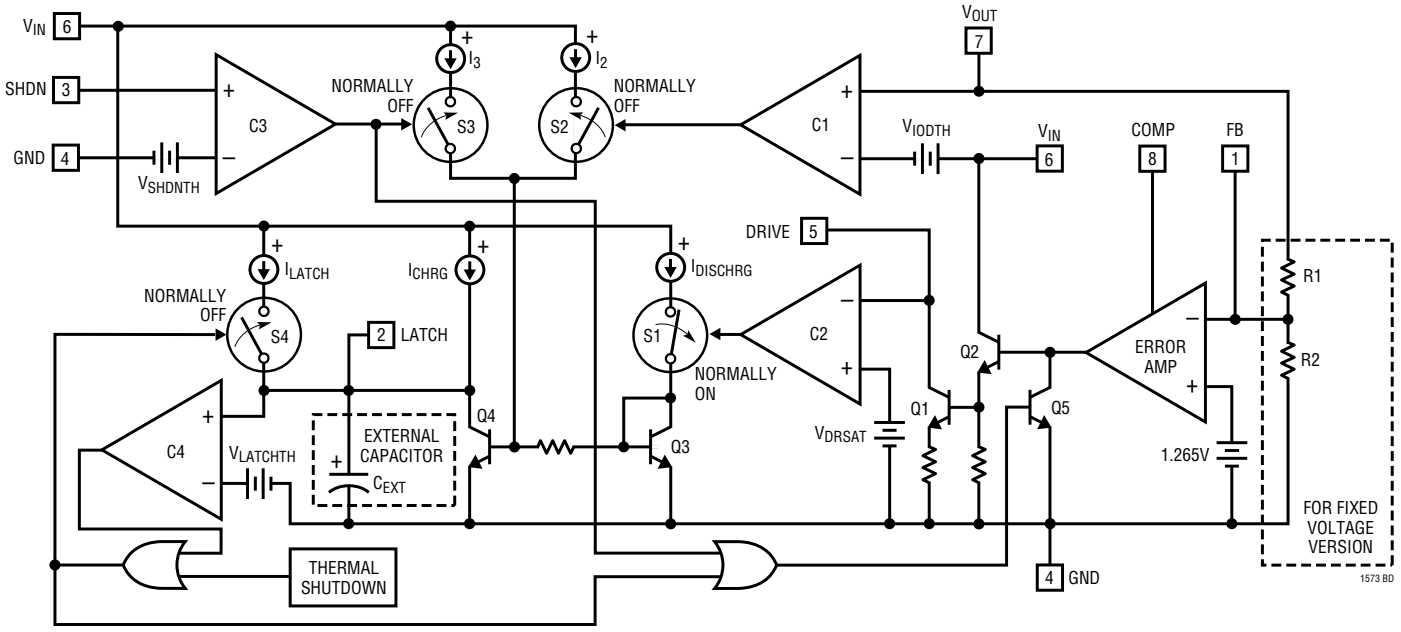
DRIVE (Pin 5): The DRIVE pin is connected to the collector of the main drive transistor of the LT1573. This drive transistor sinks the base current of the external PNP output transistor. A resistor is normally inserted between the base of the external PNP output transistor and the DRIVE pin. This resistor is sized to allow the LT1573 to sink the appropriate amount of base current for a given application and to activate the overcurrent latch in a fault condition.

V_{IN} (Pin 6): This pin provides power to all internal circuitry of the LT1573 including bias, start-up, thermal limit, error amplifier and all overcurrent latch circuitry.

V_{OUT} (Pin 7): The V_{OUT} pin is the input to comparator C1 shown in Block Diagram. This pin is normally connected to the output. The comparator C1 is used to disable the overcurrent latch during start-up when the output transistor is saturated. For fixed voltage devices the top of the internal resistor divider that sets the output voltage is connected to this pin.

COMP (Pin 8): A compensation network is inserted between the V_{OUT} and COMP pins to obtain optimal transient response. Under normal condition, the DC voltage of the COMP pin sits at one V_{BE} above ground.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The basic block diagram of the LT1573 is shown above. The regulating loop consists of a 1.265V reference, an error amplifier, a Darlington driver and an external PNP pass transistor. The 1.265V reference feeds the noninverting input of the error amplifier. The error amplifier drives the Darlington connected transistor pair Q1 and Q2. The collector of Q1 comes out to the DRIVE pin and is used to drive the base of an external PNP power transistor as shown in Figure 1. The error amplifier will adjust the drive current to the external PNP power transistor to maintain the feedback pin voltage at 1.265V. The LT1573 provides overcurrent protection by means of a timed latch function. Base current to the external PNP transistor is limited by placing a resistor between the base of the transistor and the DRIVE pin. When the DRIVE pin drops below V_{DRSAT} (the DRIVE pin saturation voltage) the output of the comparator C2 switches high; S1, which is normally closed, opens and the external capacitor connected to the LATCH pin is allowed to charge. Discharge current $I_{DISCHRG}$ is equal to approximately 28μA and charging current I_{CHRG} is equal to approximately 7μA. If the fault condition goes away before C_{EXT} charges to the latch threshold, C2 will switch back low, S1 will close and Q4 will discharge C_{EXT}. If the fault condition persists long enough for C_{EXT} to charge up to the latch threshold ($V_{LATCHTH}$), comparator C4 will switch high and S4 will close and latch the output off. The device will stay latched because latching current I_{LATCH} is greater than the pull-down current of Q4. Thermal shutdown circuitry will close S4 and latch the device off with no timing delay. Comparator C1 is used to override the latching function during start-up. If the difference between the output voltage and the input voltage is less than the input-output differential threshold (V_{IODTH}), comparator C1 output goes high which closes S2. Current source I_2 then drives base of Q4 which prevents C_{EXT} from charging. Comparator C3 is used for system shutdown and latch reset. If SHDN pin voltage is higher than shutdown threshold V_{SDTH}, the comparator C3 output goes high, shutting down the regulator and closing switch S3. Current I_3 will drive Q4 to discharge C_{EXT}, resetting the latch.

APPLICATIONS INFORMATION

The LT1573 is designed to be used in conjunction with an external PNP transistor. The overall specifications of a regulator circuit using the LT1573 and an external PNP will be heavily dependent on the specifications of the external PNP. While there are a wide variety of PNP transistors available that can be used with the LT1573, the specifications given in a typical transistor data sheet are of little use in determining overall circuit performance. In the following discussion the critical requirements of the PNP transistors are noted. Design equations are given and examples are shown using a readily available discrete PNP transistor. This device is inexpensive, available from multiple sources and can be used for a wide range of applications. For applications using other PNP transistors, the regulator specifications can be derived by the same method.

Basic Regulator Circuit

The basic regulator circuit is shown in Figure 2. The adjustable output LT1573 senses the regulator output voltage from its feedback pin via the output voltage divider, R1 and R2, and drives the base of the external PNP transistor to maintain the regulator output at the desired value. For fixed output versions of the LT1573, the regulator output voltage is sensed from the feedback pin via an internal voltage divider. The resistor R_D is required for the overcurrent latch-off function. R_D is also used to limit the drive current available to the external PNP transistor and to limit the power dissipation in the LT1573. Limiting the drive current to the external PNP transistor will limit the output current of the regulator which minimizes the stress on the regulator circuit under overload conditions. The resistor R_D is chosen based on the operating requirements of the circuit, primarily the dropout voltage and the output current. The dropout voltage of an LT1573-based regulator circuit is determined by the V_{CE} saturation voltage of the discrete external PNP transistor when it is driven with a base current equal to the available drive current of the LT1573.

External PNP Transistor Selection Criteria

The selection of an appropriate external PNP transistor depends on the regulator application specifications. The critical PNP transistor selection criteria include:

1. The maximum output current of the PNP transistor
2. The dropout voltage at the maximum output current
3. The gain-bandwidth product f_T of the transistor

The PNP transistor must be able to supply the specified maximum regulator output current to be qualified for the regulator application. The V_{CE} saturation voltage of the transistor at the maximum output current determines the dropout voltage of the circuit. The dropout voltage determines the minimum regulator input voltage for a certain specified output voltage. The gain-bandwidth product f_T of the transistor determines how fast the voltage regulator can follow an output load change without losing voltage regulation.

The D45H11 from Motorola and the KSE45H11TU from Samsung can be used in all LT1573 regulator circuits with current ratings up to 5A. The D45H11 can supply 5A of

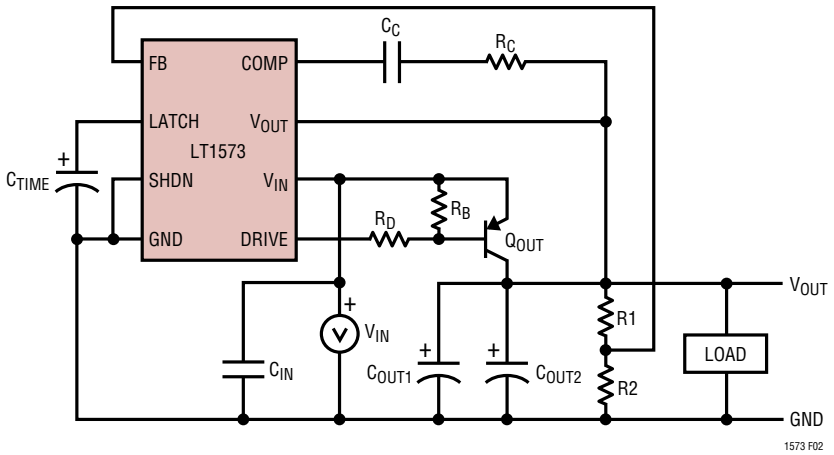


Figure 2. Basic Regulator Circuit

APPLICATIONS INFORMATION

output current with dropout voltage as low as 0.35V. The gain-bandwidth product f_T of the D45H11 is typically 40MHz which enables the regulator, composed of this PNP transistor and the LT1573, to handle the load changes of several amps in a few hundred nanoseconds with a minimum amount of output capacitance.

The following sections describe how specifications can be determined for the basic regulator based on the LT1573 and D45H11 from Motorola. To determine the specifications for regulators formed by the LT1573 and other PNP transistors, a similar method can be used.

Dropout Voltage

The dropout voltage of an LT1573-based regulator circuit is determined by the V_{CE} saturation voltage of the discrete external PNP transistor when it is driven with a base current equal to the available drive current of the LT1573. The LT1573 is guaranteed to sink 250mA of base current (440mA typ). The available drive current of the LT1573 can be reduced by adding a resistor (R_D in Figure 2) in series with the DRIVE pin. Table 1 lists some useful operating points for the D45H11. These points were empirically determined using a sampling of devices.

Table 1. D45H11 Dropout Voltage

DRIVE CURRENT (mA)	OUTPUT CURRENT (A)	TYPICAL DROPOUT VOLTAGE (V)
20	1	0.20
20	2	0.50
40	2	0.25
40	3	0.50
60	3	0.25
60	4	0.70
80	4	0.45
100	4	0.35
100	5	0.70
150	5	0.40
200	5	0.35
150	6	0.65
200	6	0.45
250	7	0.50

Current Limit

For regulator circuits using the LT1573, current limiting is achieved by limiting the base drive current to the external PNP pass transistor. This means that the actual system current limit will be a function of both the current limit of the LT1573 and the Beta of the external PNP. Motorola provides the following Beta information for the D45H11. The minimum Beta of the D45H11 is 60 when V_{CE} = 1V and I_C = 2A. The minimum Beta is 40 when V_{CE} = 1V and I_C = 4A. For other PNP transistors, the user should first find out the Beta information from the external PNP transistor manufacturer to determine the appropriate LT1573 base drive current limit. The current limit of the regulator system then can be achieved by selecting the appropriate amount of resistance R_D in Figure 2.

Selecting R_D

Resistor R_D can be used to limit the available drive current to the external PNP transistor. In order to select R_D, the user should first choose the value of the drive current that will give the required value of output current and dropout voltage. For a circuit using the D45H11 as a pass transistor this can be done using Table 1. For circuits using transistors other than D45H11, the user must characterize the transistor to determine the drive current requirements for the specified output current and dropout voltage. In general, it is recommended that the user choose the lowest value of drive current that will satisfy the output current requirements. This will minimize the stress on circuit components during overload conditions.

The formula used to determine the resistor R_D is:

$$R_D = (V_{IN} - V_{BE} - V_{DRIVE})/(I_{DRIVE} + I_{RB}) \quad (1)$$

where,

V_{IN} = the minimum input voltage to the circuit
V_{BE} = the maximum emitter/base voltage of the PNP pass transistor
I_{DRIVE} = the minimum PNP base current required
I_{RB} = the current through $R_B = V_{BE}/R_B$
V_{DRIVE} = the DRIVE pin saturation voltage when the DRIVE pin current equals ($I_{DRIVE} + I_{RB}$)

APPLICATIONS INFORMATION

Resistor R_B helps to turn off the PNP (Q_{OUT} in Figure 2). Smaller values for R_B turn off the PNP faster but will increase input current. The recommended value for R_B is 50Ω. For circuits that do not require high output current or fast transient response, the value of R_B can be increased up to 200Ω. For the D45H11, the emitter-base voltage is a function of base and collector current. Table 2 lists some useful operating points for the D45H11. These points were empirically determined using a sampling of devices.

Table 2. D45H11 V_{BE}

I_B (mA)	I_C (A)	V_{BE} AT 25°C (V)
1	0.2	0.65
7	1	0.75
23	2	0.80
45	3	0.85
66	4	0.90
100	5	0.95

Design Example

Given the following operating requirements:

$4.5V < V_{IN} < 5.5V$
$I_{OUT(MAX)} = 5A$
$V_{OUT} = 3.3V$

1. The first step is to determine the required drive current for the D45H11. Dropout voltage must be less than 1.2V at 5A output current. From Table 1, a drive current of 100mA will give 0.7V dropout voltage at an output current of 5A. This satisfies the operating requirements.

2. The next step is to determine the value of R_D. Assume R_B is 50Ω. From Table 2, the maximum emitter-base voltage for this design is 0.95V. The current through R_B is:

   $I_{RB} = V_{BE}/R_B = 0.95/50 = 19mA$

   V_{DRIVE} is the DRIVE pin saturation voltage when the DRIVE pin current equals 119mA, which can be read from the typical performance characteristics curve to be 0.39V. Resistor R_D now can be calculated from Eq (1):

   $R_D = (4.5 – 0.95 – 0.39)V/(100 + 19)mA = 26.6Ω$

   The next lowest 5% value is 24Ω.

Overcurrent Latch-Off

In addition to limiting the base drive current, the resistor R_D is included in the circuit for the overcurrent protection latch-off function. There is a minimum value for this resistance. It is calculated by Equation 1 with the drive current I_{DRIVE} set to the minimum available drive current (= 250mA) from the LT1573. At high currents, R_D also limits the power dissipation in the LT1573. In some conditions, resistor R_D can be replaced with a short. This is possible in circuits where an overload is unlikely and the input voltage and drive requirements are low. If resistor R_D is not included in the circuit, the regulator is protected against the overcurrent condition only by the thermal shutdown function. After the resistor R_D is determined, a certain amount of base drive current is available to the external PNP transistor. An overcurrent or output short condition will demand a base drive current greater than the LT1573 can supply. The internal drive transistor will saturate. A time-out latch will be triggered by this overcurrent condition to turn off the regulator system. The time-out period is determined by an external capacitor connected between the LATCH and GND pins. The time-out period is equal to the time it takes for the capacitor to charge from 0V to the latch threshold which is equal to $2V_{BE}$. The latch charging current is set by an internal current source and is a function of input voltage and temperature as shown in the typical performance characteristics curve. At 25°C, the typical latch charging current ranges from 7.2μA with 3V input to 8μA with 7V input. If the overcurrent or output short condition persists longer than the time-out period, the regulator will be shut down. Otherwise, the regulator will function normally. In the latch-off mode, some extra current is drawn from the input to maintain the latch. The latching current is a function of input voltage and temperature as shown in the typical performance characteristic curve. At 25°C, the typical latching current ranges from 0.3mA with 3V input to 9.5mA with 7V input. The latch can be reset by recycling input power, by grounding the LATCH pin or by putting the device into shutdown.

APPLICATIONS INFORMATION

Thermal Considerations

The thermal characteristics of several components need to be considered; the LT1573, the pass transistor and resistor R_D. Power dissipation should be calculated based on the worst-case conditions seen by each component during normal operation.

1. **Power Dissipation of the LT1573:** The worst-case power dissipation in the LT1573 is a function of drive current, supply voltage and the value of R_D. Worst-case dissipation for the LT1573 occurs when the drive current is equal to approximately one half of its maximum value. The worst-case power dissipation in the LT1573 can be calculated by the following formula:

$$P_D = \frac{\left(V_{IN} - V_{BE}\right)^2}{4R_D} \quad (2)$$

$R_D >$ minimum R_D for latch-off function

where,

V_{IN} = the maximum input voltage to the circuit
V_{BE} = the minimum emitter/base voltage of the PNP pass transistor

Following the previous design example for selecting resistor R_D, the power dissipation of LT1573 is calculated from Eq (2):

$$P_D = \frac{\left(5.5 - 0.65\right)^2}{4\left(24\right)} = 0.25W$$

For some operating conditions R_D may be replaced with a short. This is possible in applications where the operating requirements (input voltage and drive current) are at the low end and the output will not be shorted. For $R_D = 0$, the following formula may be used to calculate the maximum power dissipation in the LT1573:

$$P_D = (V_{IN} - V_{BE})(I_{DRIVE}) \quad (3)$$

where,

V_{IN} = the maximum input voltage
V_{BE} = the minimum emitter/base voltage of the PNP
I_{DRIVE} = the required maximum drive current

2. **Power Dissipation of the Resistor R_D:** The worst-case power dissipation in resistor R_D needs to be calculated so that the power rating of the resistor can be determined. The worst-case power dissipation in this resistor will occur when the drive current is at a maximum. The power dissipation can be calculated from the following formula:

$$P_{RD} = \frac{\left(V_{IN} - V_{BE} - V_{DRIVE}\right)^2}{R_D} \quad (4)$$

where,

V_{IN} = the maximum input voltage
V_{BE} = the minimum emitter/base voltage of the PNP
V_{DRIVE} = the voltage at the LT1573 DRIVE pin
= V_{SAT} of the DRIVE pin in the worst case

Following the previous design example, the power dissipation of resistor R_D is calculated from Eq (4):

$$P_{RD} = \frac{\left(5.5 - 0.65 - 0.39\right)^2}{24} = 0.83W$$

3. **Power Dissipation of the PNP Transistor:** The worst-case power dissipation in the PNP pass transistor is simply equal to:

$$P_{PNP} = (V_{IN} - V_{OUT})(I_{OUT}) \quad (5)$$

where,

V_{IN} = the maximum input voltage
I_{OUT} = the maximum output current

Following the previous design example, the power dissipation of PNP transistor is calculated from Eq (5):

$P_{PNP} = (5.5 - 3.3)(5) = 11W$

The LT1573 series regulators have internal thermal limiting designed to protect the device during overload conditions. For continuous normal load conditions, the maximum junction temperature rating of 125°C must not be exceeded. It is important to give careful consideration to all sources of thermal resistance from junction to ambient. For surface mount devices, heat sinking is accomplished by using the heat spreading

APPLICATIONS INFORMATION

capabilities of the PC board and its copper traces. Table 3 lists some typical values for the thermal resistance of the LT1573. Measured values of thermal resistance for a specific board size with different copper areas are listed. All measurements were taken in still air on 3/32" FR-4 board with 2oz copper. It is possible to achieve significantly lower values with thinner multilayer boards.

Table 3. LT1573 Thermal Resistance

COPPER AREA			THERMAL RESISTANCE
TOPSIDE*	BACKSIDE	BOARD AREA	(JUNCTION-TO-AMBIENT)
2500mm^2	2500mm^2	2500mm^2	80°C/W
1000mm^2	2500mm^2	2500mm^2	80°C/W
225mm^2	2500mm^2	2500mm^2	85°C/W

*Device is mounted on topside.

We can find out the maximum junction temperature of the LT1573 during normal load operation after we calculate the maximum power dissipation of the LT1573 from Eq (2). From the previous design example, the maximum power dissipation of the LT1573 is 0.2W. From Table 3, we know the thermal resistance from junction-to-ambient is around 85°C/W. The temperature difference between junction and ambient is:

(0.25W)(85°C/W) = 21.25°C

If the maximum ambient temperature is specified at 50°C, the maximum junction temperature will be:

T_{JMAX} = 50°C + 21.25°C = 71.25°C

The maximum junction temperature must not exceed the specified 125°C for safe continuous regulator operation.

Thermal Limiting

The thermal shutdown temperature of the LT1573 is approximately 150°C. The thermal limit of the LT1573 can be used to protect both the LT1573 and the external PNP pass transistor. This is accomplished by thermally coupling the LT1573 to the PNP power transistor by locating the LT1573 as close to the PNP transistor as possible. In this case, the power dissipation of the power transistor must be considered in the LT1573 maximum junction temperature calculation.

Compensation

In order to improve the transient response to regulator output load variation, a capacitor in series with a resistor can be inserted between the V_{OUT} and COMP pins. For the microprocessor power supply regulator system based on the LT1573 and the PNP transistor D45H11 with 24 1µF surface mount ceramic capacitors in parallel with one 220µF surface mount tantalum capacitor at the output as shown in Figure 1, a 100pF capacitor in series with a 1k resistor is recommended. In theory, the output capacitor forms the dominant pole of the regulator system. An internal compensation capacitor forms another pole. The external compensation capacitor and resistor form a zero which adds phase margin to the regulator system to prevent high frequency oscillation. The LT1573 has an internal pole at approximately 5kHz. An external compensation zero between 10kHz and 100kHz is usually required to stabilize the regulator. The zero frequency is primarily determined by the compensation capacitor and can be roughly calculated by the following equation:

$$f_{ZERO} = (40kHz)\frac{30(pF)}{C_{COMP}(pF)}, 10 \le C_{COMP} \le 100$$

A compensation resistor between 1k and 10k is suggested. A compensation resistor of 5k works for most cases. In some cases, a greater compensation resistor is needed to stop oscillation above 1MHz. In some cases, the output capacitor may have enough equivalent series resistance (ESR) to generate the required zero and the external compensation zero may not be needed.

Output Capacitor

The LT1573 is designed to be used with an external PNP transistor with a high gain-bandwidth product f_T to make a regulator with a very fast transient response, which can minimize the size of the output capacitor. For a regulator made of an LT1573 and a D45H11, only one 10µF surface mount ceramic capacitor at the output is enough for the regulator to handle the output load varying up to 5A in a few hundred nanoseconds interval and to remain stable with a 30pF capacitor in series with a 7.5k resistor between the V_{OUT} and COMP pins. If tighter voltage regulation is

APPLICATIONS INFORMATION

needed during output transients, more capacitance can be added to the regulator output. If more capacitance is added to the output, the bandwidth of the regulator is lowered. A large value compensation capacitor may be needed to lower the frequency of the compensation zero to avoid high frequency oscillation. Equal value output capacitors with different ESR can have different output transient response. High frequency performance will be strongly affected by parasitics in the output capacitor and board layout. Some experimentation with the external compensation will be required for optimum results.

Shutdown Function

The regulator can be shut down by pulling the SHDN pin voltage higher than the shutdown threshold (about 1.3V). The regulator will restart itself if the SHDN is pulled below the shutdown threshold.The SHDN pin should be tied to ground if it is not used. The SHDN pin voltage can be higher than the input voltage. When the SHDN pin voltage is higher than 2V, the SHDN pin current increases and is limited by a 20k resistor. Momentarily putting the device into shutdown also resets the overcurrent latch.

Lower Dropout Voltage or Higher Output Current Capability

Lower dropout voltage or higher output current capability can be achieved by paralleling several output PNP transistors as shown in Figure 3. By paralleling output PNP transistors, the equivalent resistance between the emitters (V_{IN}) and collectors (V_{OUT}) is lowered or each PNP transistor sharing the output current now runs at a lower collector current, which causes the dropout voltage to decrease. Because the PNP transistors are running at a lower collector current where the transistor beta is higher, much more output current can be obtained at a given base drive current. When paralleling two or more output transistors, a separate resistor is needed for R_B and R_D for each output transistor. This allows the base drive current to be split evenly between output transistors, which promotes equal output current sharing. In the specific example drawn in Figure 3 with two output transistors, the resistance of R_{B1} and R_{B2} is now twice the value of the resistance of R_B in Figure 2, and the resistance of R_{D1} and R_{D2} is twice the value of the resistance of R_D in Figure 2. In case of n PNP transistors in parallel, the resistance R_B

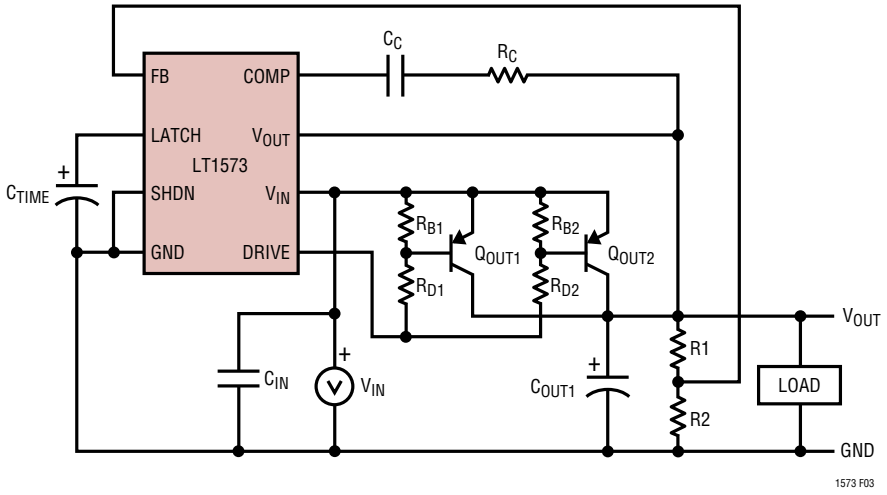


Figure 3. Reduced Dropout Voltage or Increased Output Current by Paralleling Output PNP Transistors

APPLICATIONS INFORMATION

equals the resistance of R_{B1}, R_{B2}, ..., and R_{Bn} in parallel, and the resistance R_D equals the resistance of R_{D1}, R_{D2}, ..., and R_{Dn} in parallel.

Voltage Feedback Resistor Divider Table

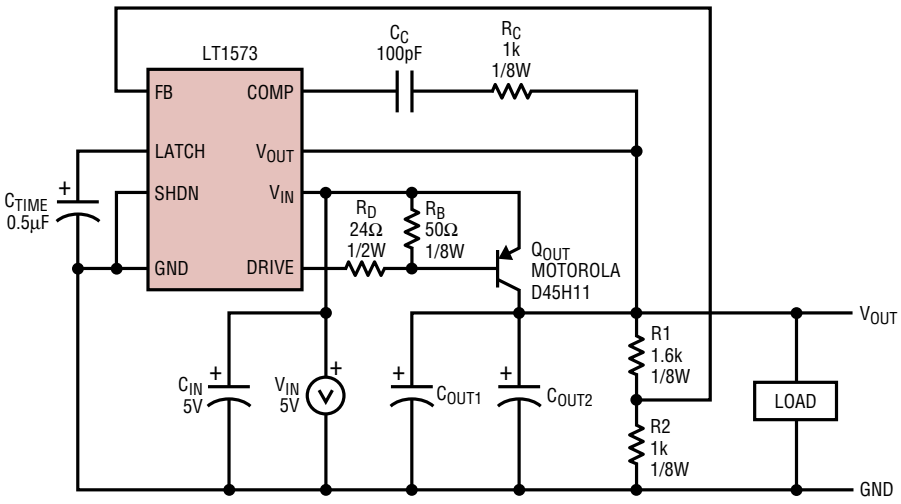
Voltage feedback resistor divider is provided for convenience for the most possibly used output voltages in Table 4.

Table 4. LT1573 Thermal Resistance

OUTPUT VOLTAGE (V)	R2 (Ω)	R1 (Ω) (NEAREST 1%)
1.5	1k	187
1.8	1k	422
2.0	1k	576
2.2	1k	732
2.5	1k	976
2.8	1k	1210
3.0	1k	1370
3.3	1k	1620
3.5	1k	1780
3.8	1k	2000
4.0	1k	2150
4.5	1k	2550
5.0	1k	2940

TYPICAL APPLICATIONS

3.3V/5A Microprocessor Supply

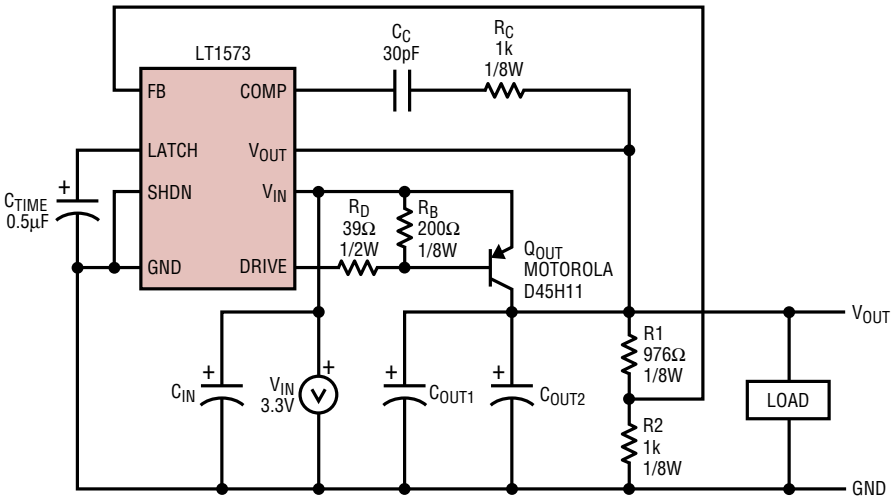


1573 TA01

C_{OUT1} = 24 × 1µF SURFACE MOUNT CERAMIC CAPACITOR
(FOR T < 45°C, C_{OUT1} = 24 × 1µF Y5V CERAMIC SURFACE MOUNT CAPACITORS,
FOR T > 45°C, C_{OUT1} = 24 × 1µF X7R CERAMIC SURFACE MOUNT CAPACITORS)
PLACE C_{OUT1} IN THE MICROPROCESSOR SOCKET CAVITY
C_{IN}, C_{OUT2} = 220µF SURFACE MOUNT TANTALUM CAPACITOR
C_{TIME} = 0.5µF FOR 100ms TIME OUT AT ROOM TEMPERATURE
SHDN (ACTIVE HIGH) PIN SHOULD BE TIED TO GROUND IF IT IS NOT USED

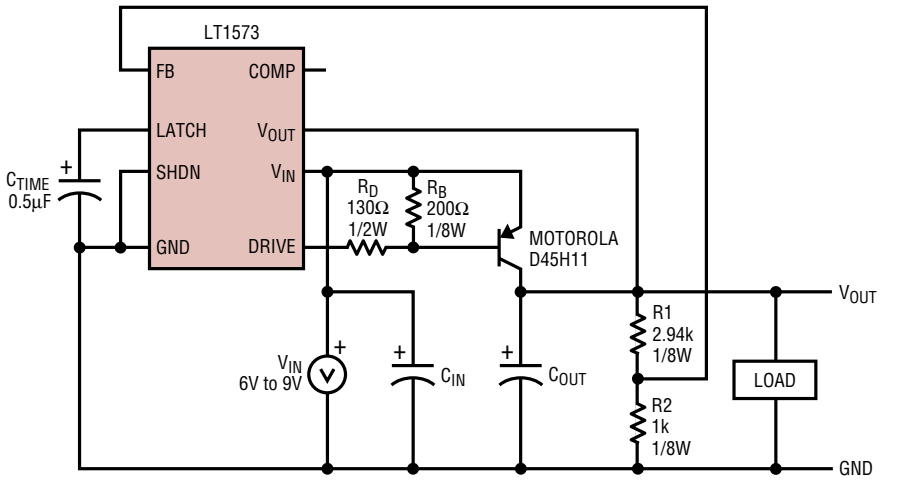
TYPICAL APPLICATIONS

3.3V to 2.5/2A Voltage Regulator



C_{IN} = 22µF SURFACE MOUNT TANTALUM CAPACITOR
C_{OUT1} = 10µF SURFACE MOUNT CERAMIC CAPACITOR
C_{OUT2} = 15µF SURFACE MOUNT TANTALUM CAPACITOR
C_{TIME} = 0.5µF FOR 100ms TIME OUT AT ROOM TEMPERATURE
SHDN (ACTIVE HIGH) PIN SHOULD BE TIED TO GROUND IF IT IS NOT USED

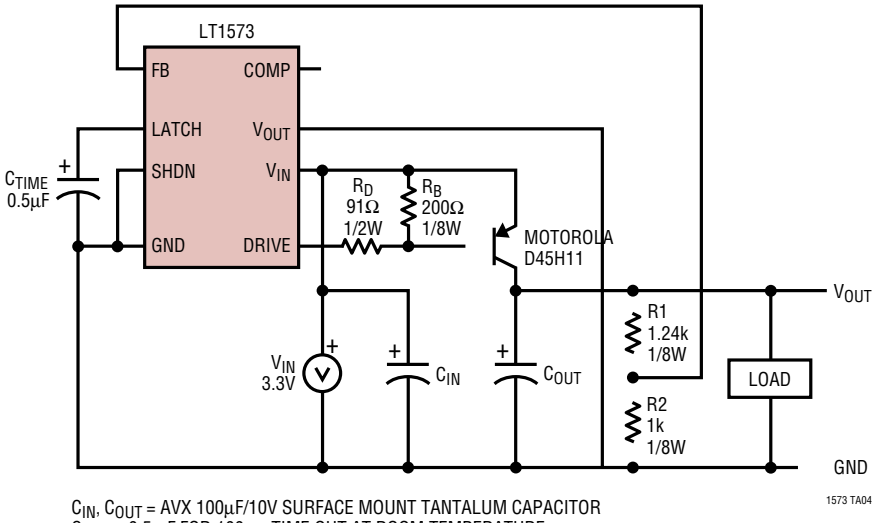
5V/2A Output from 6V to 9V Wall Adapter Input



C_{IN} = 150 µF (SANYO SURFACE MOUNT ELECTROLYTIC, 10V, PART #10CV150BS)
OR 10 µF LOW ESR TANTALUM CAPACITOR
C_{OUT} = 47 µF (SANYO SURFACE MOUNT ELECTROLYTIC, 25V, PART #25CV47BS)
OR 150 µF (SANYO SURFACE MOUNT ELECTROLYTIC, 10V, PART #10CV150BS)
C_{TIME} = 0.5 µF FOR 100ms TIME OUT AT ROOM TEMPERATURE
SHDN (ACTIVE HIGH) PIN SHOULD BE TIED TO GROUND IF IT IS NOT USED

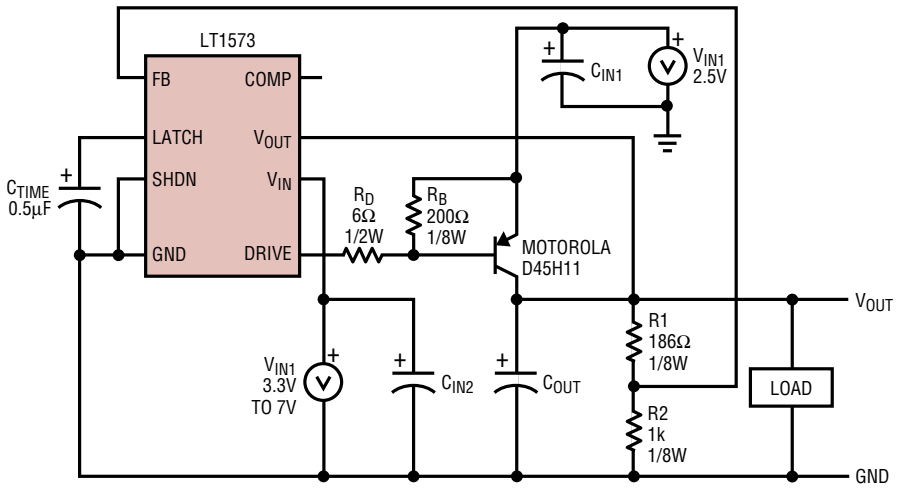
TYPICAL APPLICATIONS

3.3V to 2.85V/1A Voltage Regulator



C_{IN}, C_{OUT} = AVX 100µF/10V SURFACE MOUNT TANTALUM CAPACITOR
C_{TIME} =0.5 µF FOR 100ms TIME OUT AT ROOM TEMPERATURE
SHDN (ACTIVE HIGH) PIN SHOULD BE TIED TO GROUND IF IT IS NOT USED

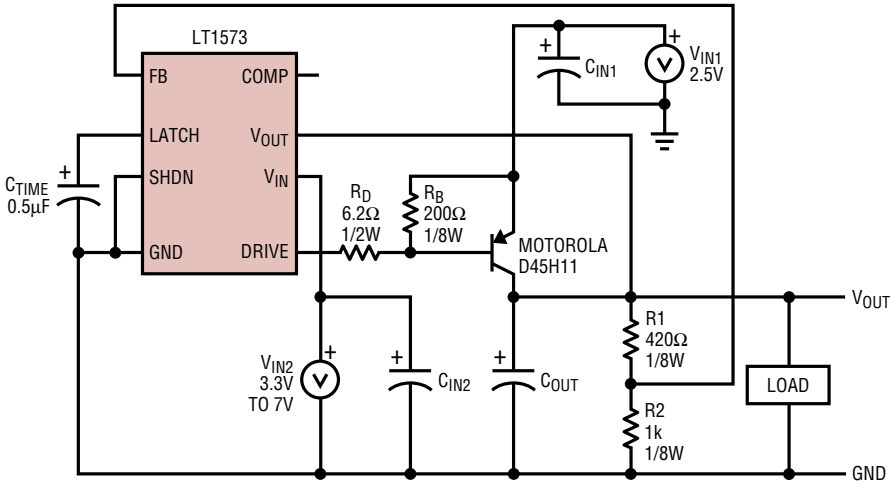
High Efficiency 2.5V to 1.5V Converter at 6A Output Current



C_{IN1}, C_{OUT} = AVX 100µF/10V SURFACE MOUNT TANTALUM CAPACITOR
C_{IN2} =AVX 15 µF/10V SURFACE MOUNT TANTALUM CAPACITOR
C_{TIME} =0.5 µF FOR 100ms TIME OUT AT ROOM TEMPERATURE
SHDN (ACTIVE HIGH) PIN SHOULD BE TIED TO GROUND IF IT IS NOT USED

TYPICAL APPLICATIONS

High Efficiency 2.5V to 1.8V Converter at 5A Output Current

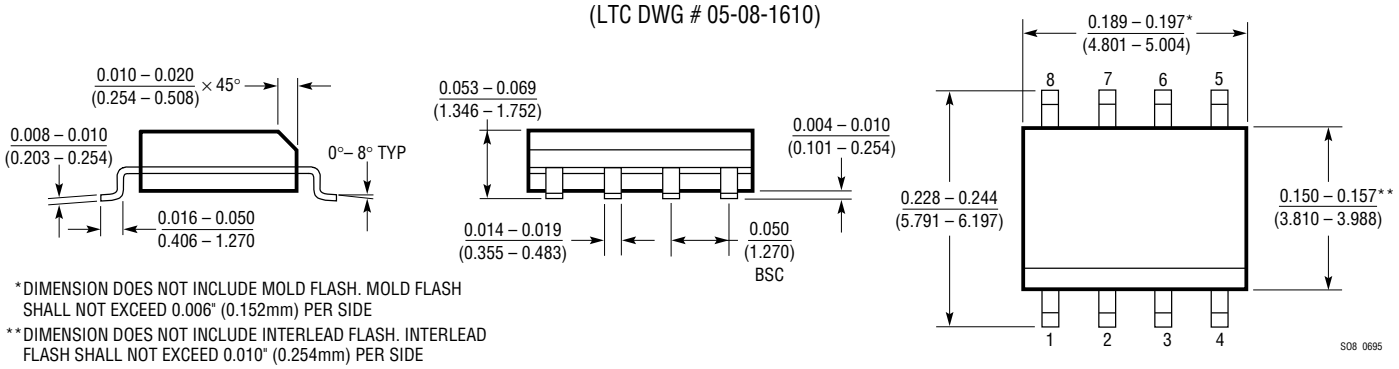


C_{IN1}, C_{OUT} = AVX 100µF/10V SURFACE MOUNT TANTALUM CAPACITOR
C_{IN2} =AVX 15 µF/10V SURFACE MOUNT TANTALUM CAPACITOR
C_{TIME} =0.5 µF FOR 100ms TIME OUT AT ROOM TEMPERATURE
SHDN (ACTIVE HIGH) PIN SHOULD BE TIED TO GROUND IF IT IS NOT USED

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1083/LT1084/LT1085	7.5A/5A/3A Low Dropout Regulators	Maximum 1.5V Dropout, Adjustable and Fixed Outputs
LT1529	3A Micropower Low Dropout Regulator	50µA Quiescent Current, 0.5V Dropout, Shutdown
LT1553	5-Bit Programmable Synchronous Switching Regulator	1.8V to 3.5V Fixed Output Voltage, Meets Intel VRM 8.1
LT1575	Low Dropout N-Channel MOSFET Regulator Driver	Ultrafast Transient, Adjustable/Fixed Output, Current Limiting
LT1580/LT1581	7A, 10A Very Low Dropout Linear Regulators	For High Current 3.3V to 2.xV Applications
LT1584/LT1585/LT1587	7A/4.6A/3A Low Dropout, Fast Response Regulators	For High Performance Microprocessors

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