PM7350

DSLAM WAN CARD REFERENCE DESIGN ERRATA

ISSUE 1: NOVEMBER 1999

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1 INTRODUCTION

This document is the errata notice for Issue 1 of the PM7350 DSLAM WAN Card Reference Design Board (document number PMC-990474).

2 CHANGES TO THE DSLAM WAN CARD REFERENCE DESIGN

This document describes changes required on the reference board for correct operation of the DSLAM WAN Card. The following modifications are required:

Problem: The DSLAM WAN Card had originally been designed with an added feature of meeting the specification for DS3 WAN jitter transfer. (Bellcore GR-499-CORE) This was to be accomplished using 4 FIFOs to synchronize upstream (destined for the WAN) data to a jitter-free clock, provided by 4 PLLs. (See figure 1). It has since been decided that this feature will be removed from the WAN Card due to complications in ensuring proper functionality of 4 PLLs in close proximity to each other.

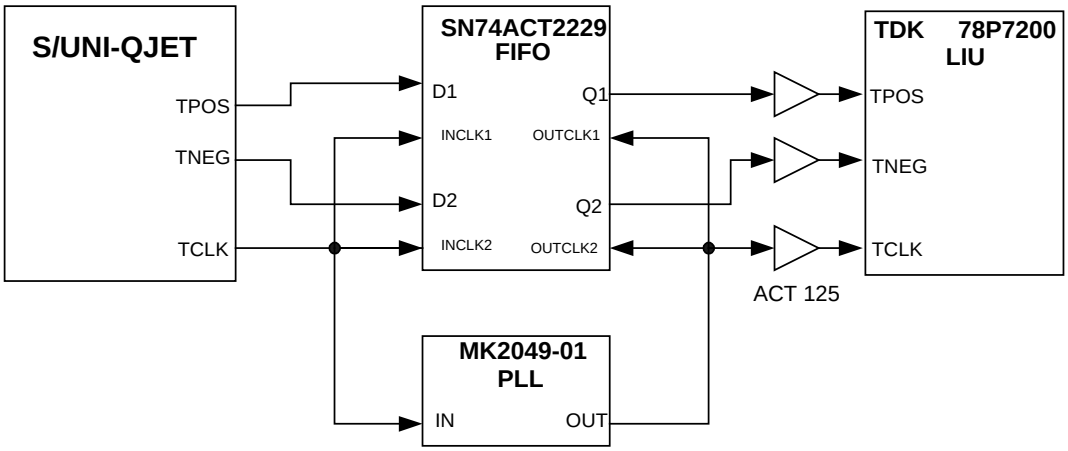
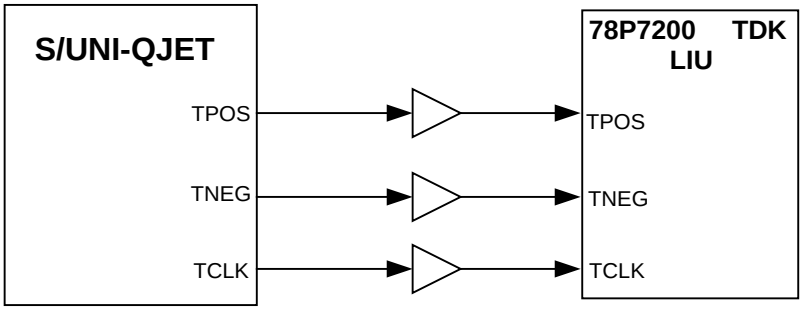


Figure 1. Original jitter attenuation circuitry design. (Upstream data path for 1 out of 4 identical channels shown).

Fix: The 4 PLLs used to de-jitter 44.736 MHz clocks & the 4 FIFOs should be removed from the design. The TPOS, TNEG, and TCLK signals from the S/UNI-QJET should be connected directly to the ACT125 buffers leading to the TDK LIUs. (See Figure 2). All code within the FPGA dealing with FIFO control should be removed.



ACT 125

Figure 2. Revised design (no jitter attenuation circuitry).

Problem: The 44.736 MHz oscillator (Y4) used by the FPGA has its output enable pin pulled low, disabling the oscillator.

Fix: Remove R58, leaving the output enable pin unconnected (active).

Problem: The RCLK output pin of the TDK78P7200 Line Interface Units (U3, U4, U6, U9) has been ANDed with the LOWSIGB output pin. The result is that when the input signal (from the WAN) to the LIUs is below threshold, the LOWSIGB signal activates, causing the QJET to lose its RCLK signal. This essentially disables the QJET receiver.

Fix: Remove the AND gate with RCLK and LOWSIGB as inputs on all 4 LIUs. Connect the 4 LIU RCLK output pins directly to the 4 QJET RCLK input pins through R151, R154, R157, R160 (respectively).

Problem: On the AT27C4096 ROM (U15) both the Chip Enable and Output Enable pins are connected to CS0 from the microprocessor. This results in the ROM switching between active and standby conditions during every read cycle. This can cause transient voltage excursions at the output of the ROM. Only the Output Enable pin of the ROM should be connected to CS0.

Fix Connect pin 3 (CE) of the ROM (U15) directly to GND.

Problem: On the LT1528 Voltage Regulator (U36) pins 1 & 2 are not connected. These pins should be shorted together when a 3.3V output is desired.

Fix: Connect pins 1 & 2 on U36.

Problem: Pins LTXD[3] (N1) and LTXD[0] (N12) on the S/UNI-DUPLEX (U27) have been left unconnected. The LTXD pins on the S/UNI-DUPLEX are used as outputs when the device is operating with its 16 port serial interface. When using the SCI-PHY/Utopia/Any-PHY bus, the LTXD pins become inputs. In this mode LTXD[0] and LTXD[3] are the only 2 LTXD pins with no alternate function associated. In accordance with proper design technique, leaving these 2 input pins floating is not recommended.

Fix: Pull pins LTXD[0] (N12) and LTDX[3] (N1) of the S/UNI-DUPLEX (U27) high or low through a pull up or pull down resistor.

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PM-991505 ref PMC-990474 Issue date: November 1999