Quad Clock Recovery and Synthesis Unit for 2488 Mbit/s

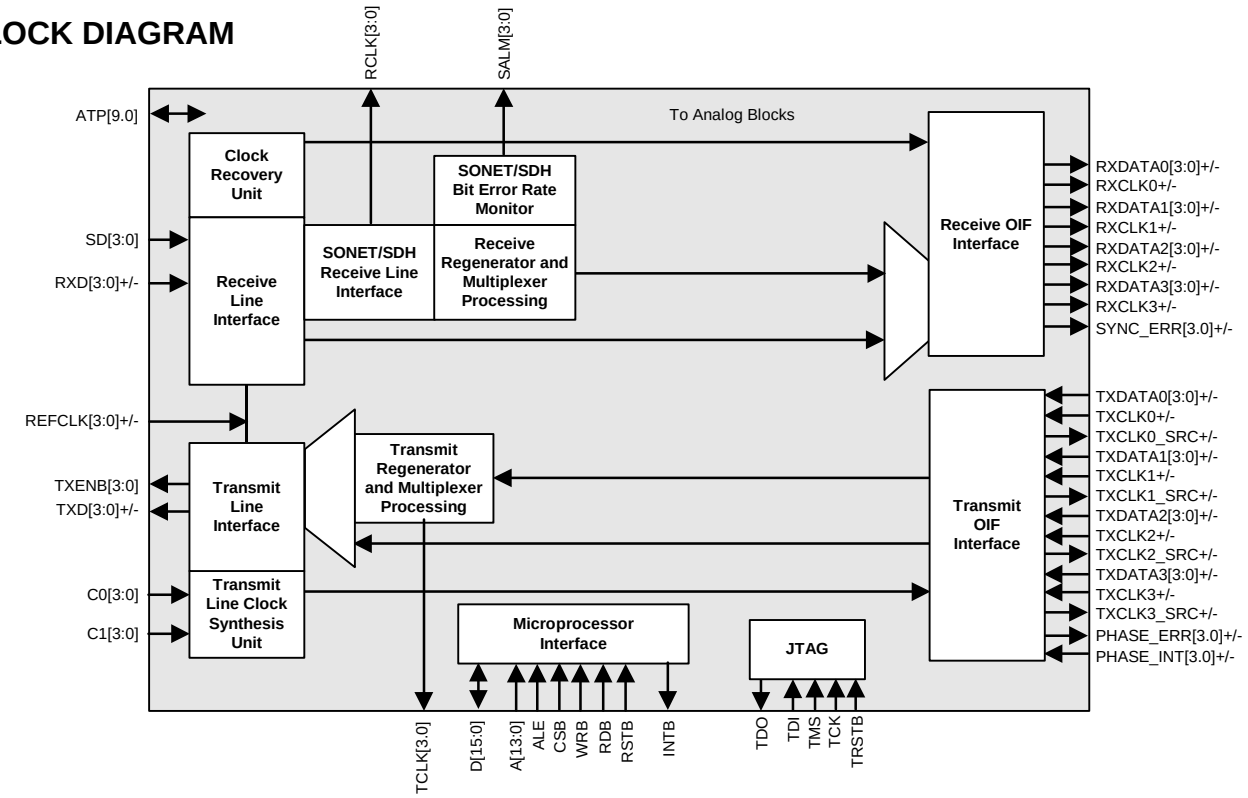
FEATURES

- Processes four independent bit-serial 2488.32 Mbit/s STS-48 (STM-16) data streams with on-chip clock and data recovery and clock synthesis.
- Complies with ITU-T G.958, Telcordia GR-253-CORE and ANSI-T1.105.03-1994 jitter tolerance, jitter transfer and intrinsic jitter criteria.
- Interfaces with downstream SONET/SDH framer devices over a set of four 4-bit 622 MHz ports that conforms to the timing and AC characteristics defined in the Optical Internetworking Forum, contribution OIF1999.102.8.
- Supports Internal Channel-to-Channel Loopback Function (Serial In/Serial Out). Channel 1 can be internally connected to Channel 2, and Channel 3 can be connected to Channel 4.
- Provides performance monitoring of SONET Section and Line layer entities or SDH Regenerator Section and Multiplex Section entities.
- Supports data streams between 2.4 and 2.7 Gbit/s with arbitrary format in pure Serializer-Deserializer (SERDES) mode.
- Supports line loopback from the line side receive stream to the transmit stream and diagnostic loopback from the system side transmit interface to the system side receive stream interface.
- Supports loop-timing of the transmit stream from the associated receive stream.
- Provides a standard 5 signal IEEE 1149.1 JTAG test port for boundary scan board test purposes.
- Provides a generic 16-bit microprocessor bus interface for configuration, control, and status monitoring.
- Low power 1.8 V CMOS core logic with 3.3 V CMOS/TTL compatible digital inputs and digital outputs. PECL inputs and outputs are 3.3 V compatible.
- Industrial temperature range (-40 °C to +85 °C Ambient, 105 °C Maximum Junction Temperature).
- 580-pin UBGA package.

SONET SECTION AND LINE/SDH REGENERATOR AND MUX SECTION

- Frames to the SONET/SDH receive stream and inserts the framing bytes (A1, A2) into the transmit stream; unscrambles the received stream and scrambles the transmit stream.
- Calculates and compares the bit interleaved parity (BIP) error detection codes (B1, B2) for the receive stream. Calculates and inserts B1 in the transmit stream. Accumulates near end errors (B1, B2) and far end errors (M1).
- Extracts and filters the automatic protection switch (APS) channel (K1, K2) bytes into internal registers.
- Extracts and filters the synchronization status message (S1) byte into an internal register for the receive stream.
- Detects loss of signal (LOS), out of frame (OOF), loss of frame (LOF), line remote defect indication (RDI-L), line alarm indication signal (AIS-L), and protection switching byte failure alarms on the receive stream.
- Provides automatic line AIS insertion following detection of various received

BLOCK DIAGRAM



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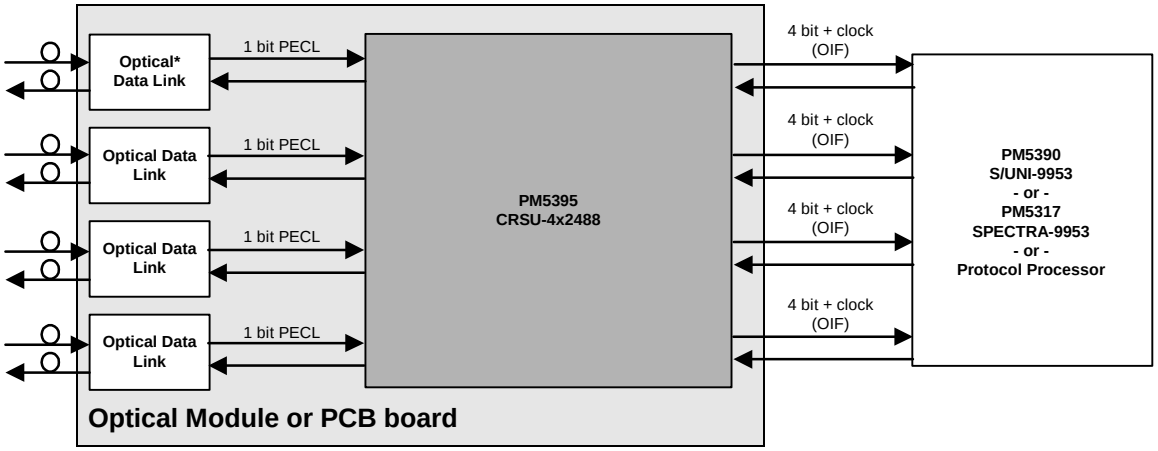
alarms (LOS, LOF, AIS-L) on the OIF receive interface.
- Configurable to force line AIS in the transmit stream.

APPLICATIONS

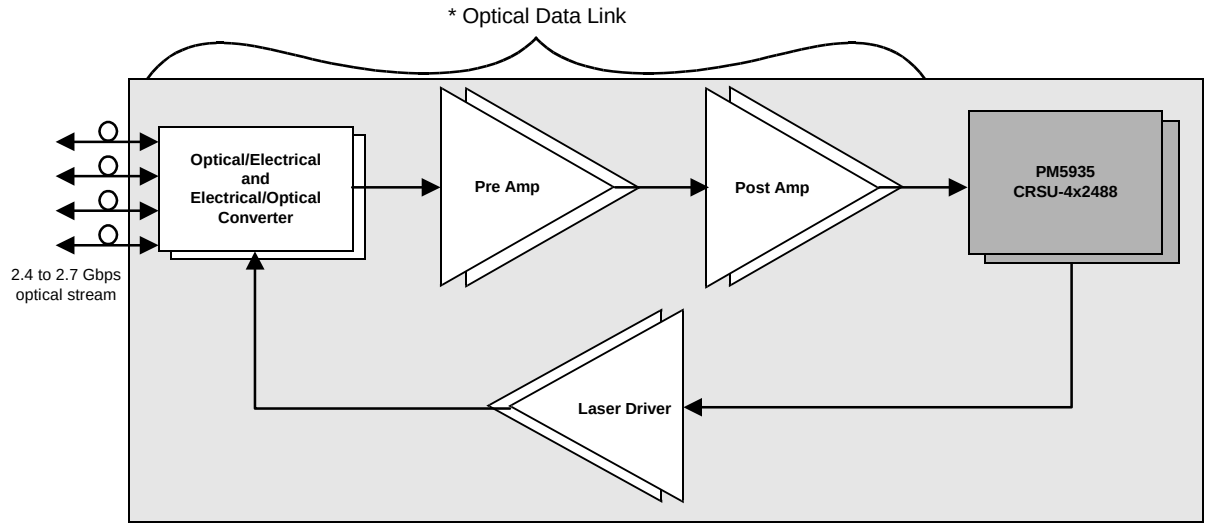
- Analog Front End for PM5317 SPECTRA-9953 SONET/SDH Framer or PM5390 S/UNI-9953 ATM/POS PHY in 4xOC-48 mode.
- High Density OC-48 Serial In/Serial Out Regenerators with optional SONET/SDH performance monitoring and termination, or Optical Overhead Transparency.
- Optical Modules requiring Quad Channel Clock Recovery, Clock Synthesis and SERDES to/from an OIF interface with optional SONET/SDH performance monitoring.

TYPICAL APPLICATIONS

QUAD CHANNEL 2.4 TO 2.7 GBPS TO OIF SERDES



QUAD CHANNEL 2.4 TO 2.7 GBPS REGENERATOR



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PMC-2001500 (P4)