

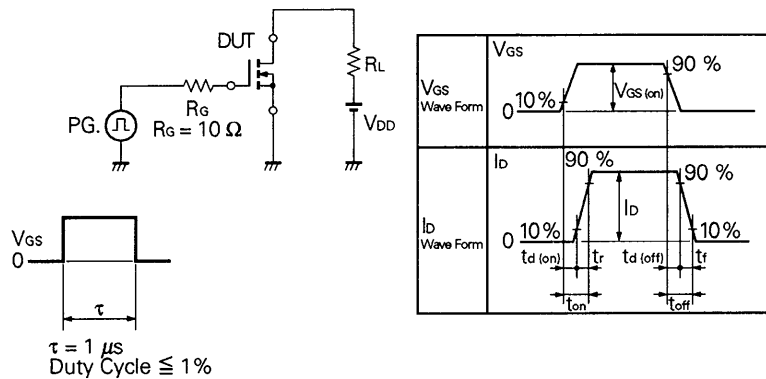
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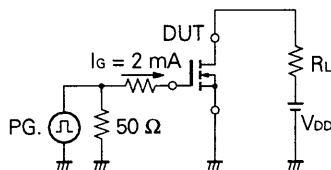
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R _{DS(on)}		14	20	mΩ	V _{GS} = 10 V, I _D = 20 A
Drain to Source On-state Resistance	R _{DS(on)}		20	30	mΩ	V _{GS} = 4 V, I _D = 20 A
Gate to Source Cutoff Voltage	V _{GS(off)}	1.0		2.5	V	V _{DS} = 10 V, I _D = 1 mA
Forward Transfer Admittance	y _{fs}	20	35		S	V _{DS} = 10 V, I _D = 20 A
Drain Leakage Current	I _{DSS}			10	μA	V _{DS} = 30 V, V _{GS} = 0
Gate to Source Leakage Current	I _{GSS}			±10	μA	V _{GS} = ±20 V, V _{DS} = 0
Input Capacitance	C _{iss}		3 400		pF	V _{DS} = 10 V V _{GS} = 0 f = 1 MHz
Output Capacitance	C _{oss}		1 800		pF	
Reverse Transfer Capacitance	C _{rss}		960		pF	
Turn-On Delay Time	t _{d(on)}		80		ns	V _{GS(on)} = 10 V V _{DD} = 15 V I _D = 20 A, R _G = 10 Ω R _L = 0.75 Ω
Rise Time	t _r		1 000		ns	
Turn-Off Delay Time	t _{d(off)}		210		ns	
Fall Time	t _f		230		ns	
Total Gate Charge	Q _G		100		nC	V _{GS} = 10 V I _D = 40 A V _{DD} = 24 V
Gate to Source Charge	Q _{GS}		12		nC	
Gate to Drain Charge	Q _{GD}		32		nC	
Diode Forward Voltage	V _{SD}		1.1		V	I _{SD} = 40 A, V _{GS} = 0
Reverse Recovery Time	t _{rr}		80		ns	I _{SD} = 40 A, V _{GS} = 0 di/dt = 50 A/μs

Test Circuit 1: Switching Time

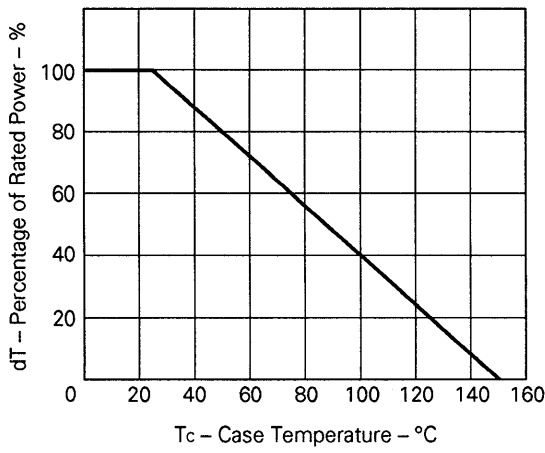


Test Circuit 2: Gate Charge

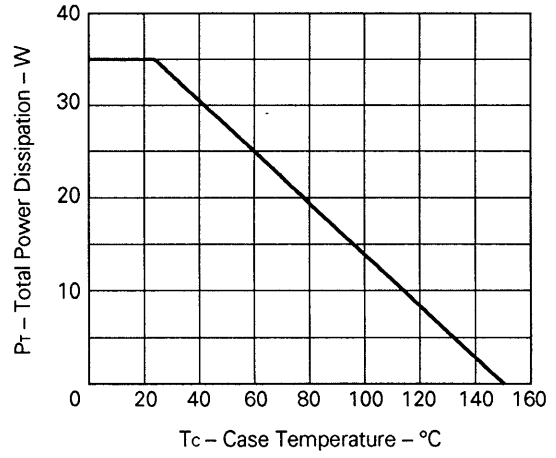


TYPICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

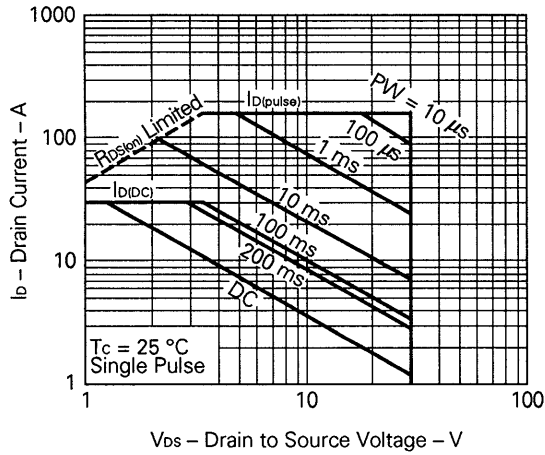
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



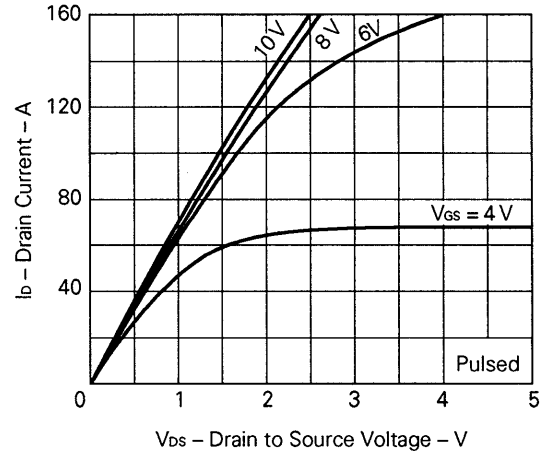
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



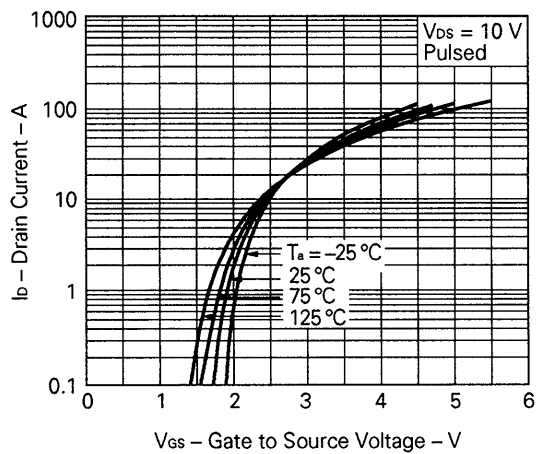
FORWARD BIAS SAFE OPERATING AREA

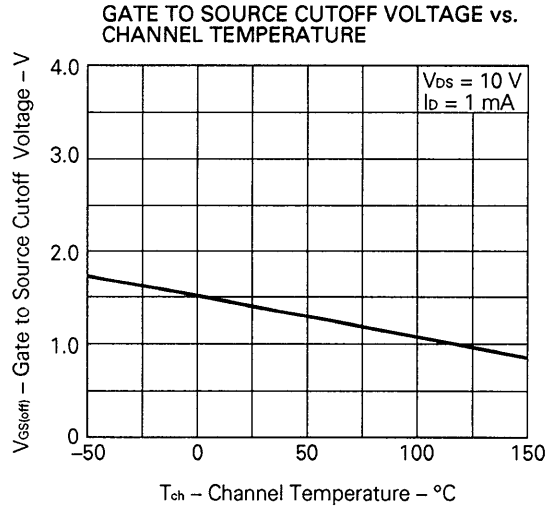
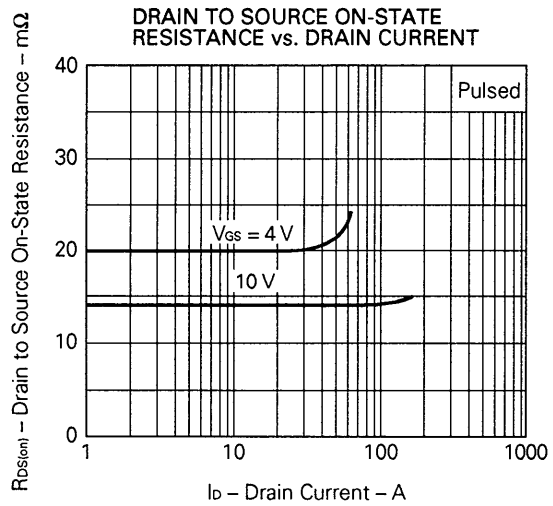
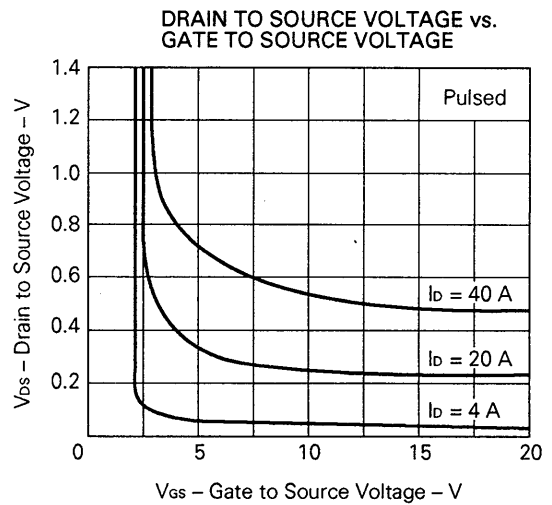
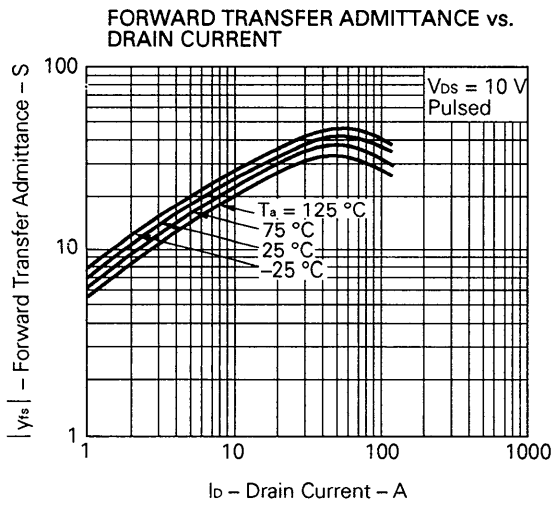
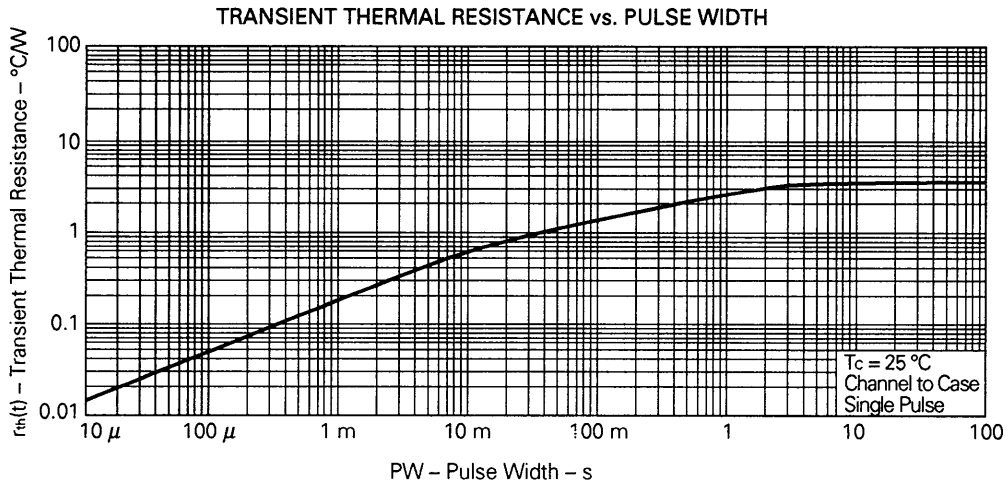


DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

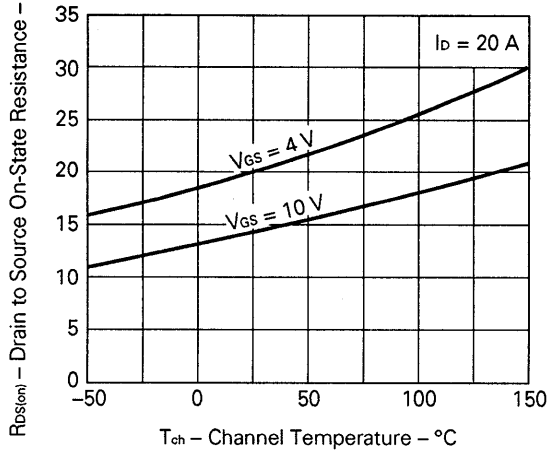


TRANSFER CHARACTERISTICS

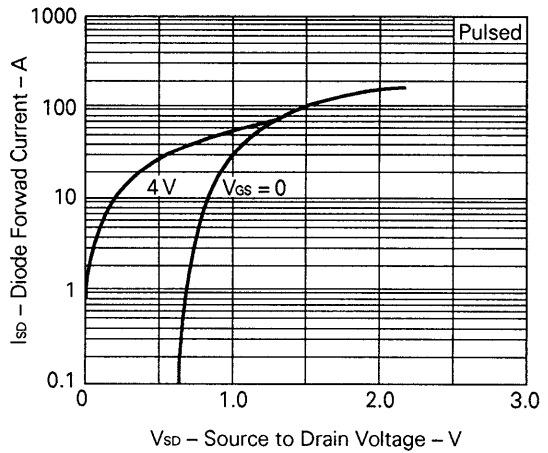




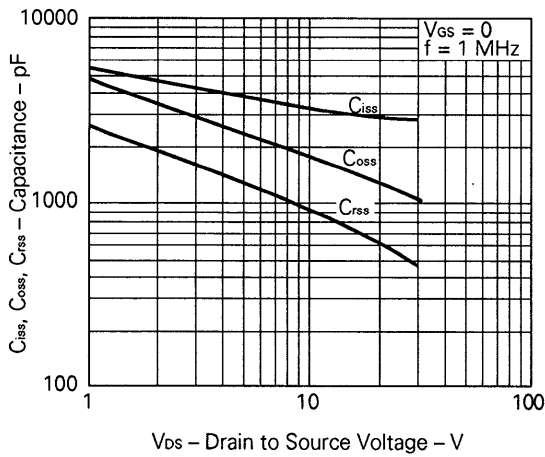
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



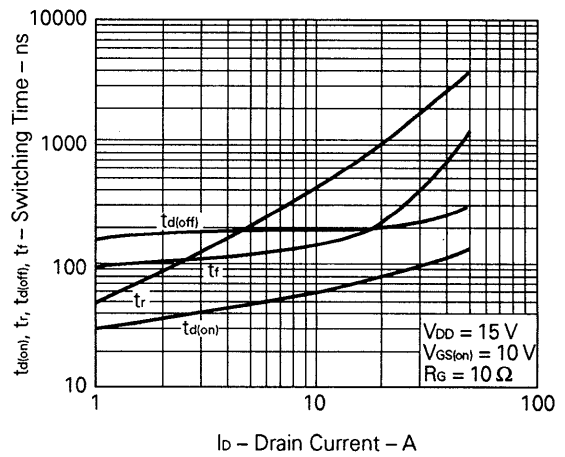
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



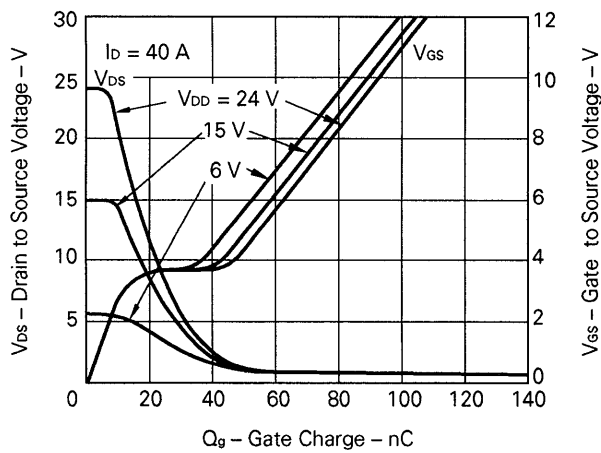
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



SWITCHING CHARACTERISTICS



DYNAMIC INPUT CHARACTERISTICS



Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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