

74ABT16952

16-Bit Registered Transceiver with 3-STATE Outputs

General Description

The ABT16952 is a 16-bit registered transceiver. Two 8-bit back to back registers store data flowing in both directions between two bidirectional buses. Separate clock, clock enable and 3-STATE output enable signals are provided for each register. The output pins are guaranteed to source 32 mA and to sink 64 mA.

Features

- Separate clock, clock enable and 3-STATE output enable provided for each register
- A and B output sink capability of 64 mA source capability of 32 mA
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability

Ordering Code:

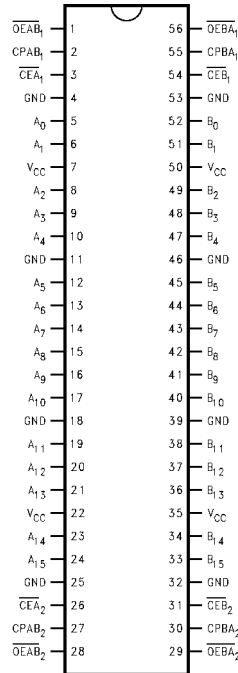
Order Number	Package Number	Package Description
74ABT16952CSSC	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74ABT16952CMTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the letter suffix "X" to the ordering code.

Pin Descriptions

Pin Names	Description
A ₀ -A ₁₅	Data Register A Inputs/ B-Register 3-STATE Outputs
B ₀ -B ₁₅	Data Register B Inputs/ A-Register 3-STATE Outputs
CPAB _n , CPBA _n	Clock Pulse Inputs
CEA _n , CEB _n	Clock Enable
OEAB _n , OEBA _n	Output Enable Inputs

Connection Diagram



Output Control

OE	Internal Q	Output	Function
H	X	Z	Disable Outputs
L	L	L	Enable Outputs
L	H	H	

Register Function Table

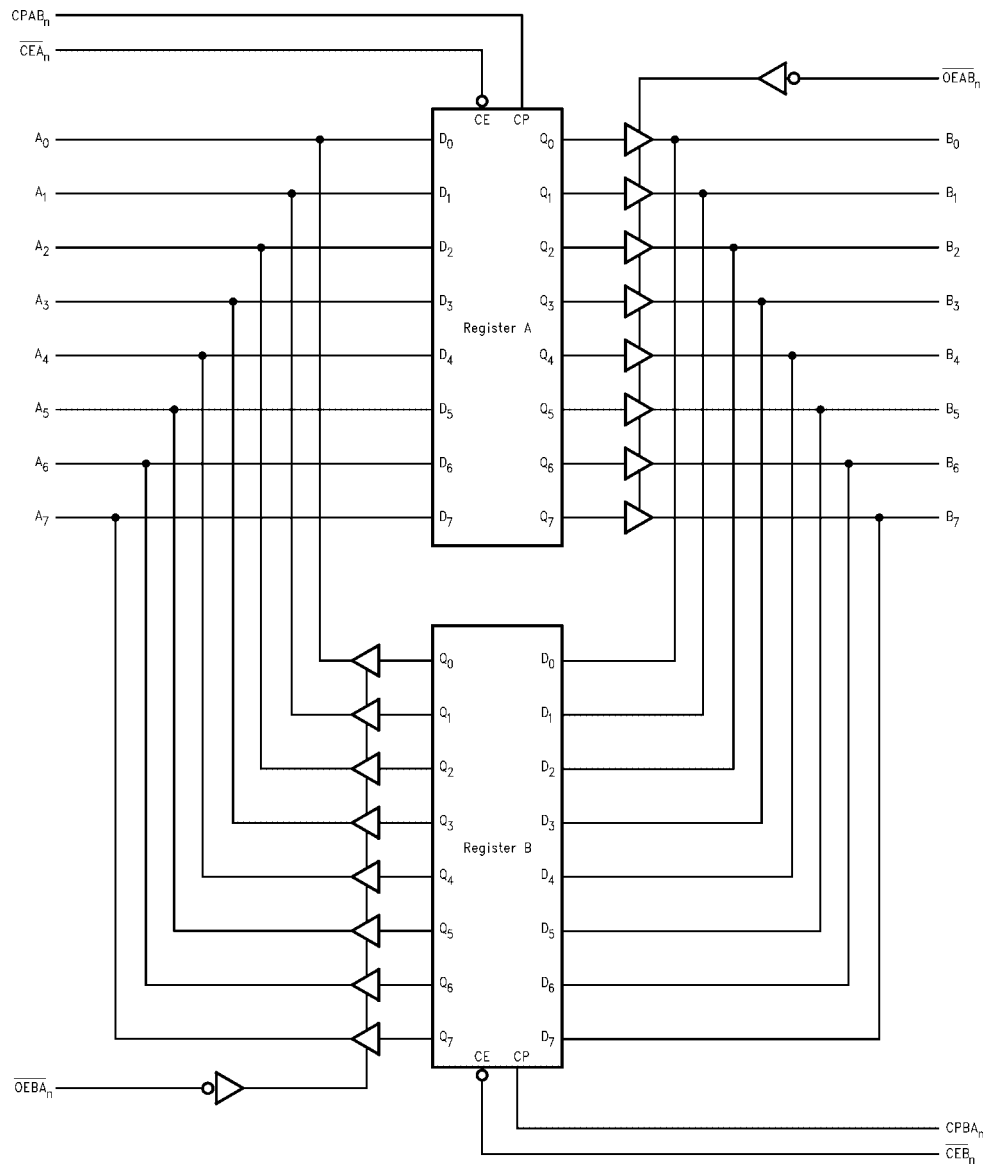
(Applies to A or B Register)

Inputs			Internal Q	Function
D	CP	CE		
X	X	H	NC	Hold Data
L	↗	L	L	Load Data
H	↗	L	H	

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance
↗ = LOW-to-HIGH Transition
NC = No Change

74ABT16952 16-Bit Registered Transceiver with 3-STATE Outputs

Block Diagram

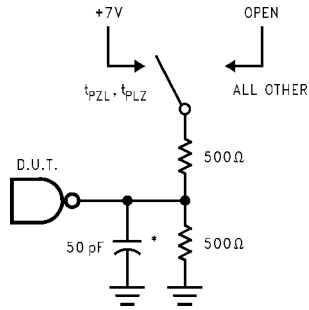


n for either byte 1 or byte 2

Absolute Maximum Ratings ^(Note 1)				Recommended Operating Conditions			
Storage Temperature	-65°C to +150°C			Free Air Ambient Temperature	-40°C to +85°C		
Ambient Temperature under Bias	-55°C to +125°C			Supply Voltage	+4.5V to +5.5V		
Junction Temperature under Bias	-55°C to +150°C			Minimum Input Edge Rate ($\Delta V/\Delta t$)			
V_{CC} Pin Potential to Ground Pin	-0.5V to +7.0V			Data Input	50 mV/ns		
Input Voltage (Note 2)	-0.5V to +7.0V			Enable Input	20 mV/ns		
Input Current (Note 2)	-30 mA to +5.0 mA			Clock Input	100 mV/ns		
Voltage Applied to Any Output in the Disable or Power-Off State	-0.5V to +5.5V						
in the HIGH State	-0.5V to V_{CC}						
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)			Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.			
DC Latchup Source Current	-500 mA			Note 2: Either voltage limit or current limit is sufficient to protect inputs.			
Over Voltage Latchup (I/O)	10V						
DC Electrical Characteristics							
Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage			-1.2	V	Min	$I_{IN} = -18$ mA (Non I/O Pins)
V_{OH}	Output HIGH Voltage	2.5 2.0			V	Min	$I_{OH} = -3$ mA (A_n, B_n) $I_{OH} = -32$ mA (A_n, B_n)
V_{OL}	Output LOW Voltage			0.55	V	Min	$I_{OL} = 64$ mA (A_n, B_n)
V_{ID}	Input Leakage Test	4.75			V	0.0	$I_{ID} = 1.9$ μ A (Non-I/O Pins) All Other Pins Grounded
I_{IH}	Input HIGH Current			1 1	μ A	Max	$V_{IN} = 2.7$ V (Non-I/O Pins) (Note 4) $V_{IN} = V_{CC}$ (Non-I/O Pins)
I_{BVI}	Input HIGH Current Breakdown Test			7	μ A	Max	$V_{IN} = 7.0$ V (Non-I/O Pins)
I_{BVIIT}	Input HIGH Current Breakdown Test (I/O)			100	μ A	Max	$V_{IN} = 5.5$ V (A_n, B_n)
I_{IL}	Input LOW Current			-1 -1	μ A	Max	$V_{IN} = 0.5$ V (Non-I/O Pins) (Note 4) $V_{IN} = 0.0$ V (Non-I/O Pins)
$I_{IH} + I_{OZH}$	Output Leakage Current			10	μ A	0V-5.5V	$V_{OUT} = 2.7$ V (A_n, B_n); $\overline{OE}A$ or $\overline{OE}B = 2.0$ V
$I_{IL} + I_{OZL}$	Output Leakage Current			-10	μ A	0V-5.5V	$V_{OUT} = 0.5$ V (A_n, B_n); $\overline{OE}A$ or $\overline{OE}B = 2.0$ V
I_{OS}	Output Short-Circuit Current	-100		-275	mA	Max	$V_{OUT} = 0$ V (A_n, B_n)
I_{CEX}	Output HIGH Leakage Current			50	μ A	Max	$V_{OUT} = V_{CC}$ (A_n, B_n)
I_{ZZ}	Bus Drainage Test			100	μ A	0.0V	$V_{OUT} = 5.5$ V (A_n, B_n); All Others GND
I_{CCH}	Power Supply Current			1.0	mA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current			60	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current			1.0	mA	Max	Outputs 3-STATE; All Others GND
I_{CCT}	Additional I_{CC} /Input			2.5	mA	Max	$V_I = V_{CC} - 2.1$ V; All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC} (Note 4)	No Load		0.18	mA/ MHz	Max	Outputs OPEN $\overline{OE}A$ or $\overline{OE}B =$ GND, Non-I/O = GND or V_{CC} One Bit toggling, 50% duty cycle (Note 3)
Note 3: For 8-bit toggling, $I_{CCD} < 1.4$ mA/MHz.							
Note 4: Guaranteed, but not tested.							

AC Electrical Characteristics						
(SSOP Package)						
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V to } 5.5\text{V}$ $C_L = 50\text{ pF}$		Units
		Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	200		200		MHz
t_{PLH}	Propagation Delay	1.5	5.3	1.5	5.3	ns
t_{PHL}	\overline{CPAB}_n or \overline{CPBA}_n to A_n or B_n	1.5	5.3	1.5	5.3	
t_{PZH}	Output Enable Time	1.5	5.5	1.5	5.5	ns
t_{PZL}	\overline{OEAB}_n or \overline{OEBA}_n to A_n or B_n	1.5	5.5	1.5	5.5	
t_{PHZ}	Output Disable Time	1.5	6.0	1.5	6.0	ns
t_{PLZ}	\overline{OEAB}_n or \overline{OEBA}_n to A_n or B_n	1.5	6.0	1.5	6.0	
AC Operating Requirements						
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V to } 5.5\text{V}$ $C_L = 50\text{ pF}$		Units
		Min	Max	Min	Max	
$t_S(H)$	Setup Time, HIGH	2.5		2.5		ns
$t_S(L)$	or LOW A_n or B_n to \overline{CPAB}_n or \overline{CPBA}_n	2.5		2.5		
$t_H(H)$	Hold Time, HIGH	1.5		1.5		ns
$t_H(L)$	or LOW A_n or B_n to \overline{CPAB}_n or \overline{CPBA}_n	1.5		1.5		
$t_S(H)$	Setup Time, HIGH	2.5		2.5		ns
$t_S(L)$	or LOW \overline{CEA}_n or \overline{CEB}_n to \overline{CPAB}_n or \overline{CPBA}_n	2.5		2.5		
$t_H(H)$	Hold Time, HIGH	1.5		1.5		ns
$t_H(L)$	or LOW \overline{CEA}_n or \overline{CEB}_n to \overline{CPAB}_n or \overline{CPBA}_n	1.5		1.5		
$t_W(H)$	Pulse Width, HIGH	3.0		3.0		ns
$t_W(L)$	or LOW to \overline{CPAB}_n or \overline{CPBA}_n	3.0		3.0		
Capacitance						
Symbol	Parameter	Typ	Units	Conditions $T_A = 25^\circ\text{C}$		
C_{IN}	Input Capacitance	5	pF	$V_{CC} = 0\text{V}$ (Non I/O Pins)		
C_{IO} (Note 5)	Output Capacitance	11	pF	$V_{CC} = 5.0\text{V}$ (A_n , B_n)		
Note 5: C_{IO} is measured at frequency $f = 1\text{ MHz}$, per MIL-STD-883, Method 3012.						

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

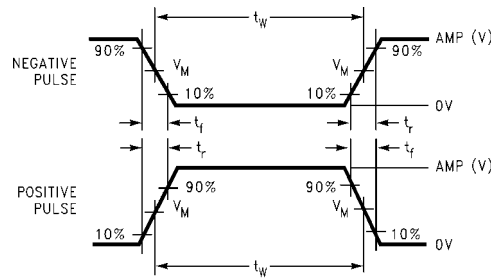


FIGURE 2. Test Input Signal Levels

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Input Signal Requirements

AC Waveforms

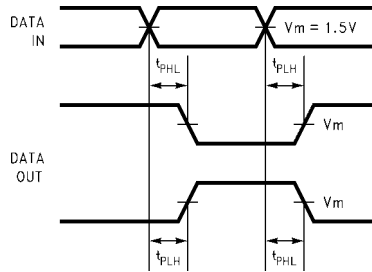


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

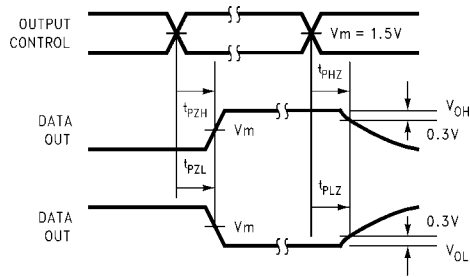


FIGURE 6. 3-STATE Output HIGH and LOW Enable and Disable Times

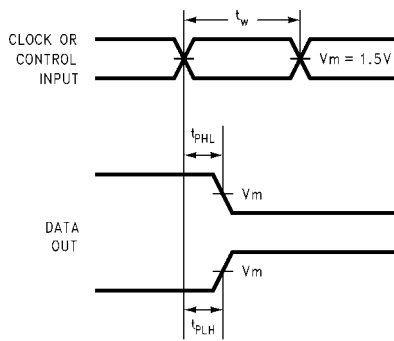


FIGURE 5. Propagation Delay, Pulse Width Waveforms

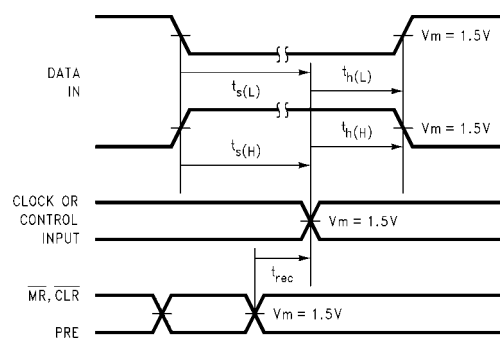
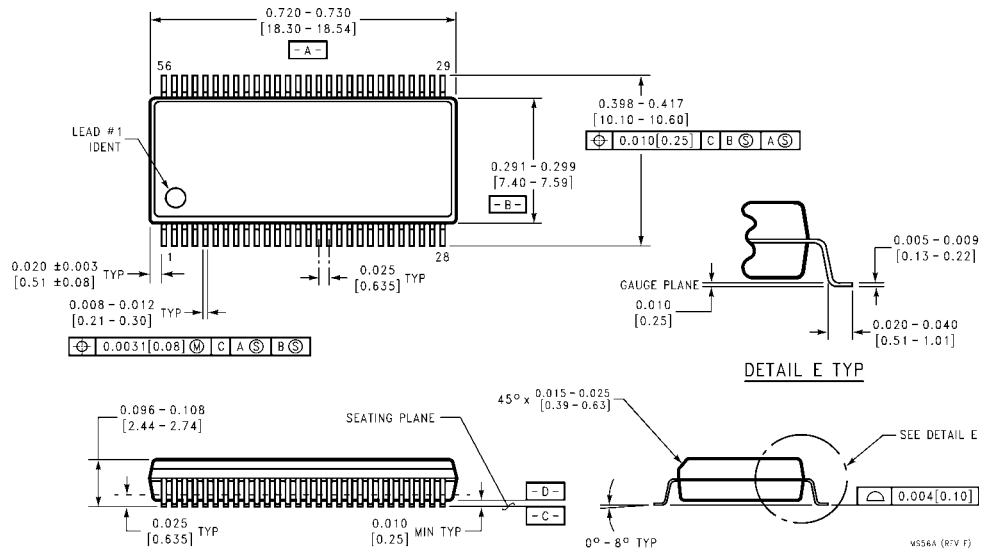


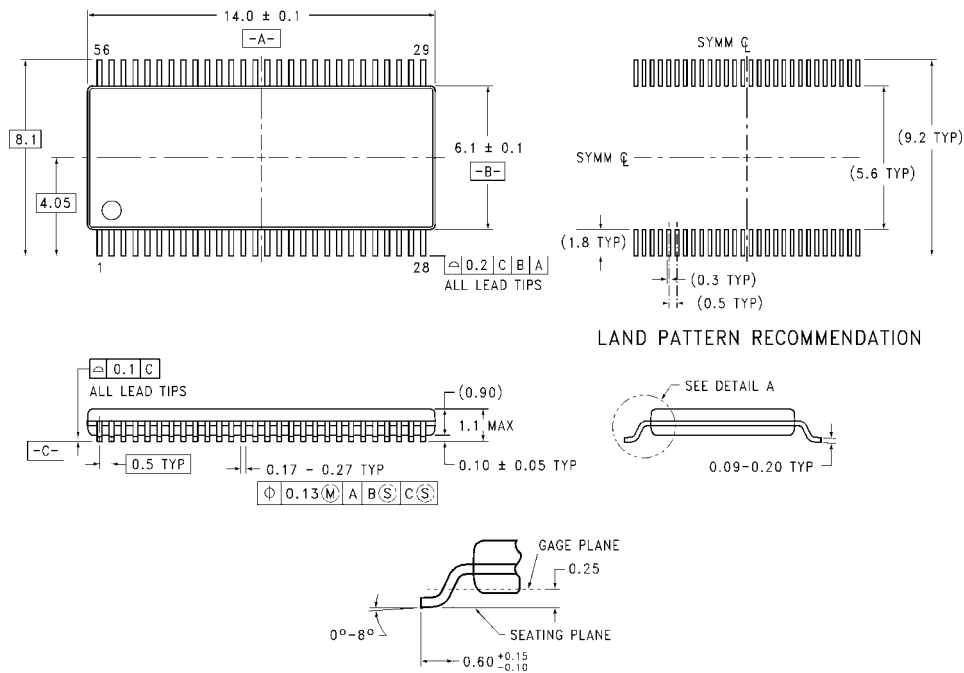
FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



**56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS56A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56**

MTD56 (REV B)

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