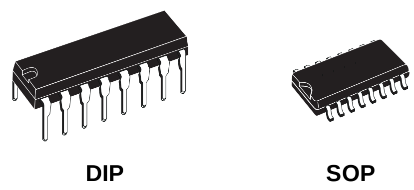
HCF40160B

SYNCHRONOUS PROGRAMMABLE 4-BIT DECADE COUNTER WITH ASYNCHRONOUS CLEAR

- INTERNAL LOOK-AHEAD FOR FAST COUNTING
- CARRY OUTPUT FOR CASCADING
- SYNCHRONOUSLY PROGRAMMABLE
- LOW-POWER TTL COMPATIBILITY
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIF. UP TO 20V
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT I_I = 100nA (MAX) AT V_{DD} = 18V T_A = 25°C
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



ORDER CODES

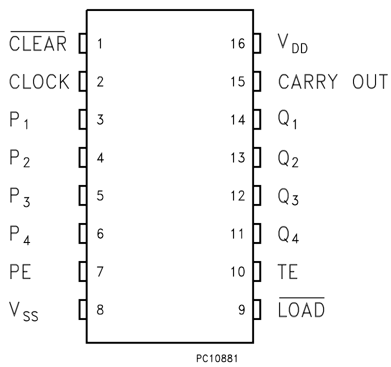
PACKAGE	TUBE	T & R
DIP	HCF40160BEY	
SOP	HCF40160BM1	HCF40160M013TR

DESCRIPTION

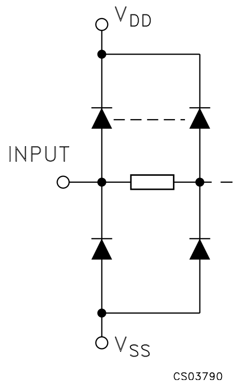
HCF40160B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages.

HCF40160B is 4-bit synchronous programmable counters. The $\overline{\text{CLEAR}}$ function is asynchronous. A low level at the $\overline{\text{CLEAR}}$ input sets all four outputs low regardless of the state of the CLOCK, $\overline{\text{LOAD}}$ and ENABLE inputs. A low level at the $\overline{\text{LOAD}}$ inputs disables the counter and causes the output to agree with the set-up data after the following CLOCK pulse regardless of the condition of the ENABLE inputs. Two count-enable inputs and a carry output (COUT) are instrumental in accomplishing this function. The carry look-ahead circuitry provides for cascading counter for n-bit synchronous application without additional gating. Counting is enabled when both the PE and TE inputs are high. The TE input is fed forward to enable COUT. This enable output produces a positive output pulse with a duration approximately equal to the positive portion of the Q1 output. This positive overflow carry pulse can be used to enable successive cascaded stages. Logic transitions at the PE and TE inputs may occur when the clock is either high or low.

PIN CONNECTION



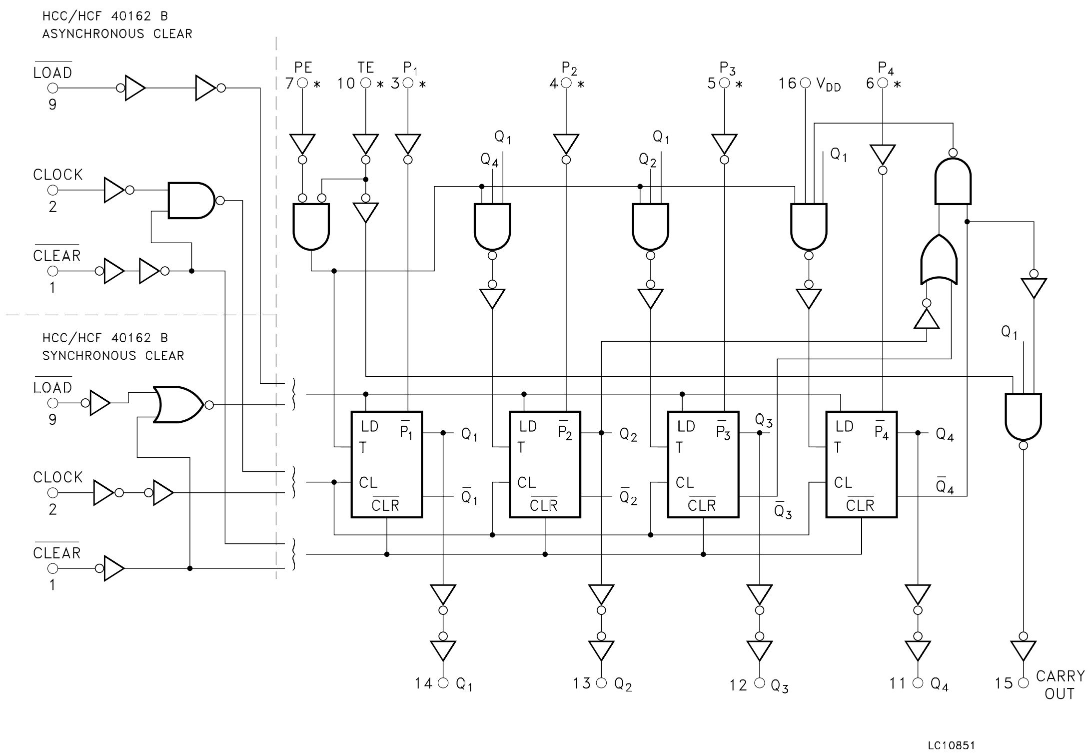
IINPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{\text{CLEAR}}$	Asynchronous Master Reset
2	CLOCK	Clock Input (LOW to HIGH, Edge-triggered)
3, 4, 5, 6	P1 to P4	Data Inputs
7	PE	Count Enable Input
10	TE	Count Enable Carry Input
9	$\overline{\text{LOAD}}$	Parallel Enable Input
14, 13, 12, 11	Q1 to Q4	Flip Flop Outputs
15	CARRY OUT	Terminal Count Output
8	V_{SS}	Negative Supply Voltage
16	V_{DD}	Positive Supply Voltage

LOGIC DIAGRAM

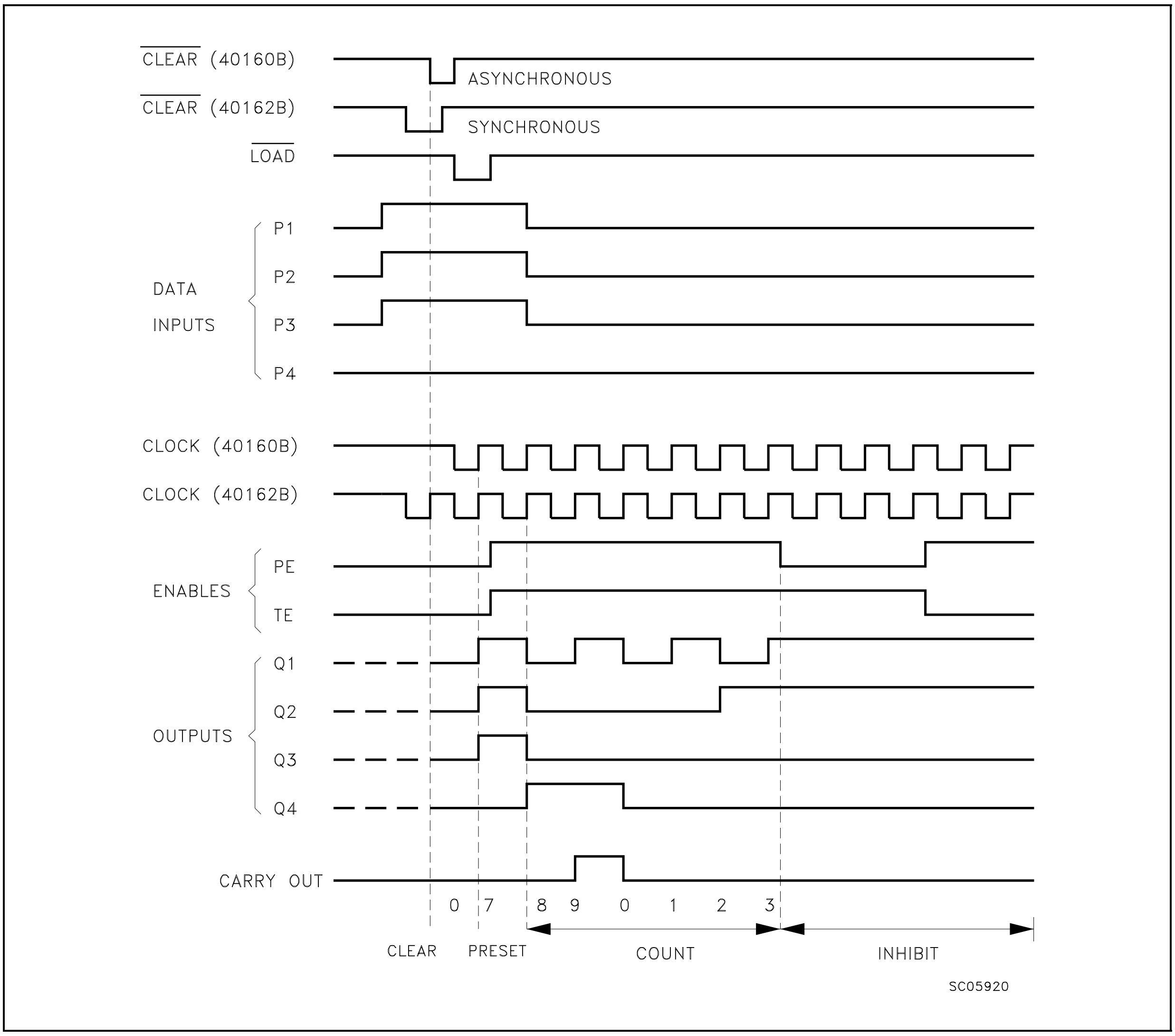


TRUTH TABLE

CLOCK	$\overline{CLR}$	$\overline{LOAD}$	PE	TE	OPERATION
⎍ (rising edge)	H	L	X	X	PRESET
⎍ (rising edge)	H	H	L	X	NC
⎍ (rising edge)	H	H	X	L	NC
⎍ (rising edge)	H	H	H	H	COUNT
X	L	X	X	X	RESET

(X) : Don't Care
NC : No Change

TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +22	V
V_I	DC Input Voltage	-0.5 to V_{DD} + 0.5	V
I_I	DC Input Current	± 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 20	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value							Unit
		V_I (V)	V_O (V)	$\lvert I_O \rvert$ (µA)	V_{DD} (V)	T_A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_L	Quiescent Current	0/5			5		0.04	5		150		150	µA
		0/10			10		0.04	10		300		300	
		0/15			15		0.04	20		600		600	
		0/20			20		0.08	100		3000		3000	
V_{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V_{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V_{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V_{IL}	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I_{OH}	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.1		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I_{OL}	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I_I	Input Leakage Current	0/18	Any Input		18		$\pm 10^{-5}$	±0.1		±1		±1	µA
C_I	Input Capacitance		Any Input				5	7.5					pF

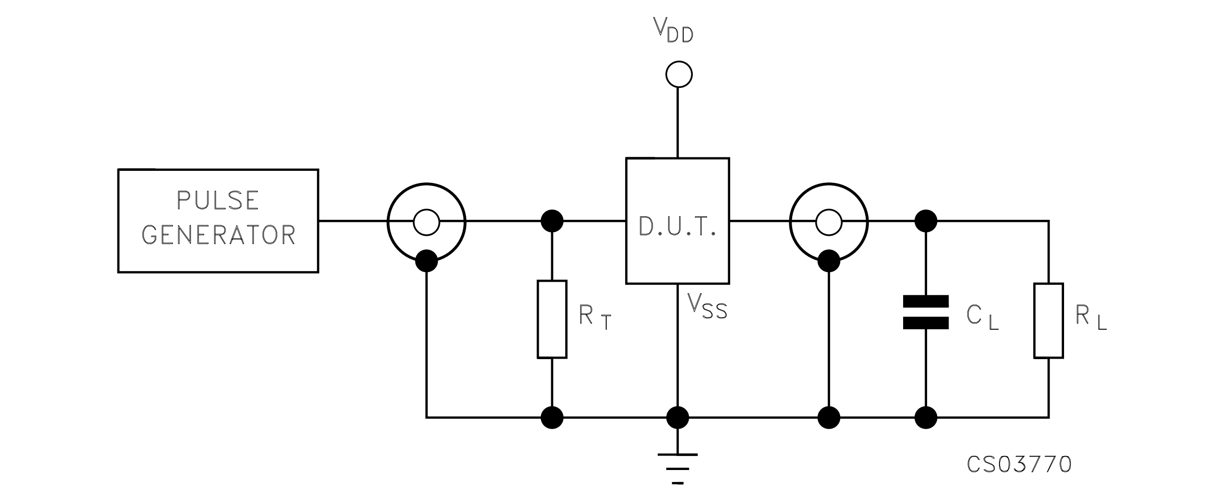
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50pF, R_L = 200KΩ, t_r = t_f = 20 ns)

Symbol	Parameter	Test Condition		Value (*)			Unit
		V_{DD} (V)		Min.	Typ.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time Clock to Q	5			200	400	ns
		10			80	160	
		15			60	120	
t_{PLH} t_{PHL}	Propagation Delay Time Clock to C_{OUT}	5			225	450	ns
		10			95	190	
		15			70	140	
t_{PLH} t_{PHL}	Propagation Delay Time TE to C_{OUT}	5			125	250	ns
		10			55	110	
		15			40	80	
t_{setup}	Setup Time Data to Clock	5		240	120		ns
		10		90	45		
		15		60	30		
t_{setup}	Setup Time $\overline{\text{Load}}$ to Clock	5		240	120		ns
		10		90	45		
		15		60	30		
t_{setup}	Setup Time PE or TE to Clock	5		340	170		ns
		10		140	70		
		15		100	50		
t_{hold}	Hold Time	5		0			ns
		10		0			
		15		0			
t_{THL} t_{TLH}	Transition Time	5			100	200	ns
		10			50	100	
		15			40	80	
t_W	Clock Input Pulse Width	5		170	85		ns
		10		70	35		
		15		50	25		
f_{CL}	Maximum Clock Input Frequency	5		2	3		MHz
		10		5.5	8.5		
		15		8	12		
t_r t_f	Clock Input Rise or Fall Time	5				200	ns
		10				70	
		15				15	
t_{PHL}	Proagation Delay Time $\overline{\text{Clear}}$ to Q	5			250	500	ns
		10			110	220	
		15			80	160	
t_W	$\overline{\text{Clear}}$ Input Pulse Width Low Level	5		170	85		ns
		10		70	35		
		15		50	25		

(*) Typical temperature coefficient for all V_{DD} value is 0.3 %/°C.

TEST CIRCUIT

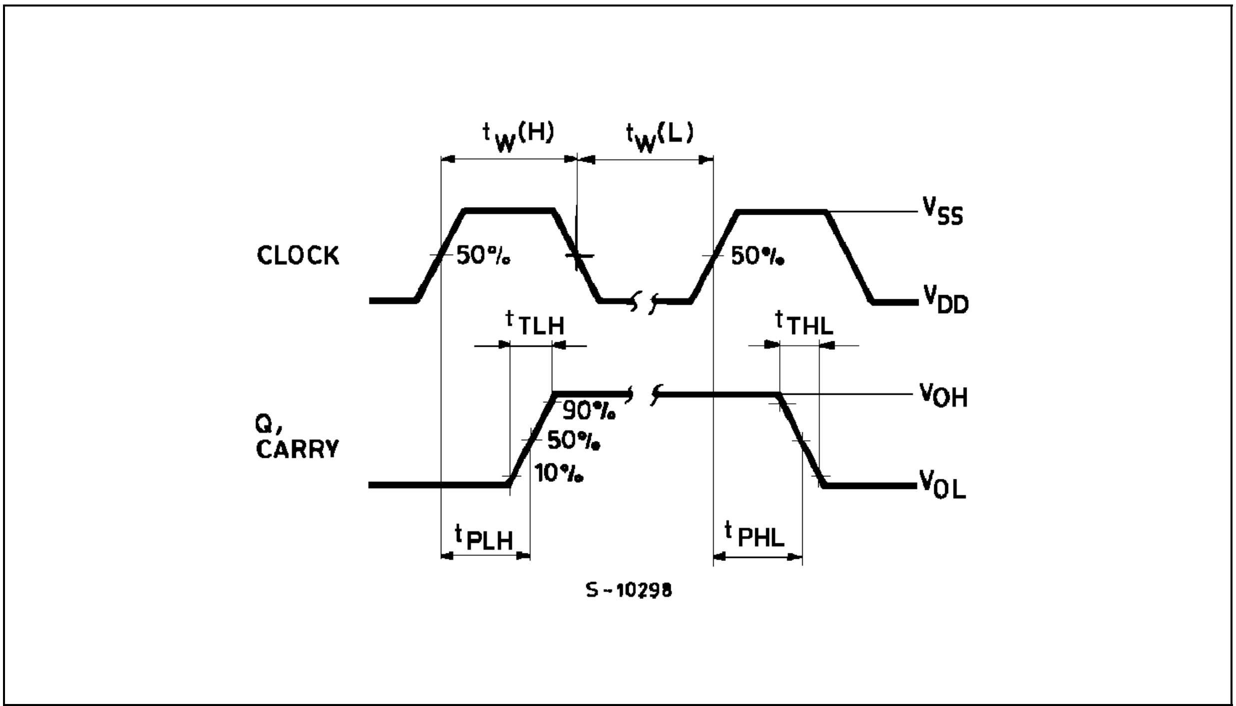


C_L = 50pF or equivalent (includes jig and probe capacitance)

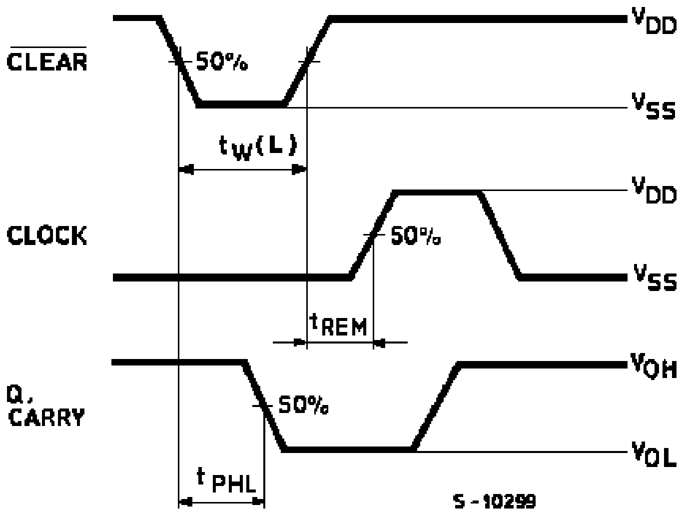
R_L = 200KΩ

R_T = Z_{OUT} of pulse generator (typically 50Ω)

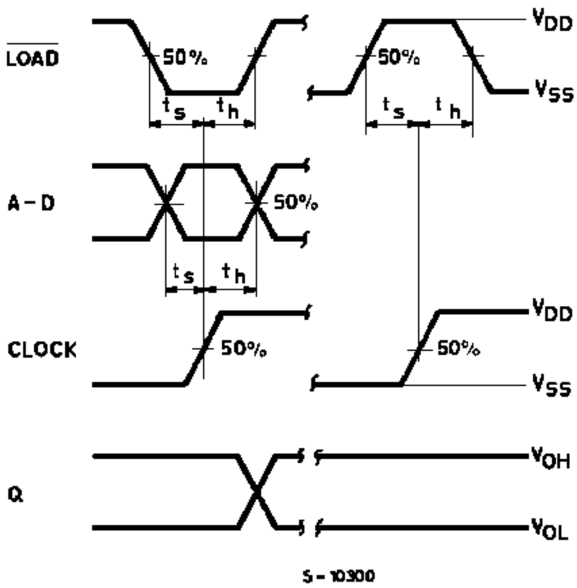
WAVEFORM 1 : PROPAGATION DELAY TIMES, MINIMUM PULSE WIDTH (CLOCK),(COUNT MODE)
(f=1MHz; 50% duty cycle)



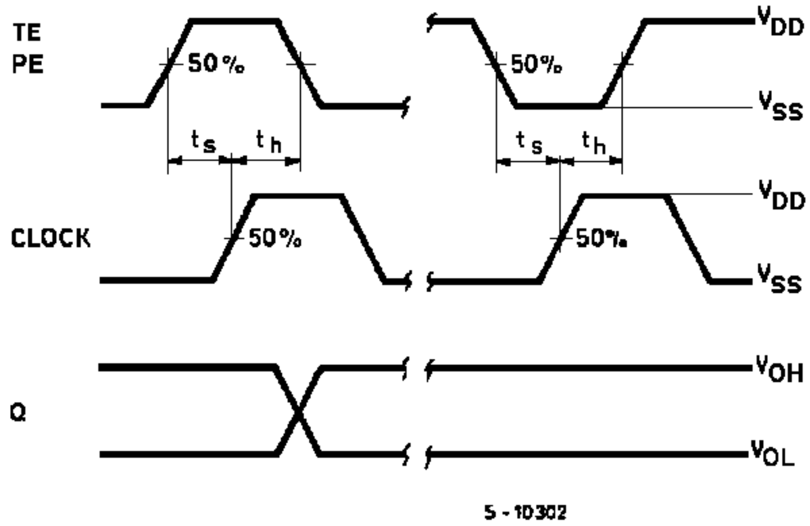
WAVEFORM 2 : MINIMUM PULSE WIDTH ($\overline{\text{CLEAR}}$), REMOVAL TIME ($\overline{\text{CLEAR}}$ to CLOCK) (PRESET MODE) (f=1MHz; 50% duty cycle)



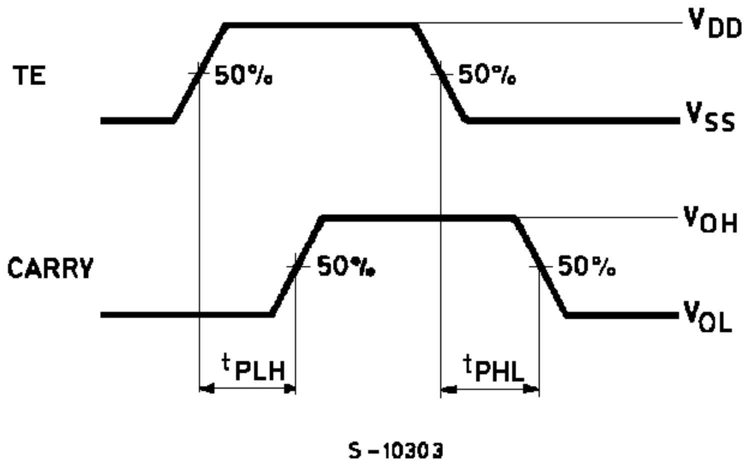
WAVEFORM 3 : SETUP AND HOLD TIMES (CLEAR MODE) (f=1MHz; 50% duty cycle)



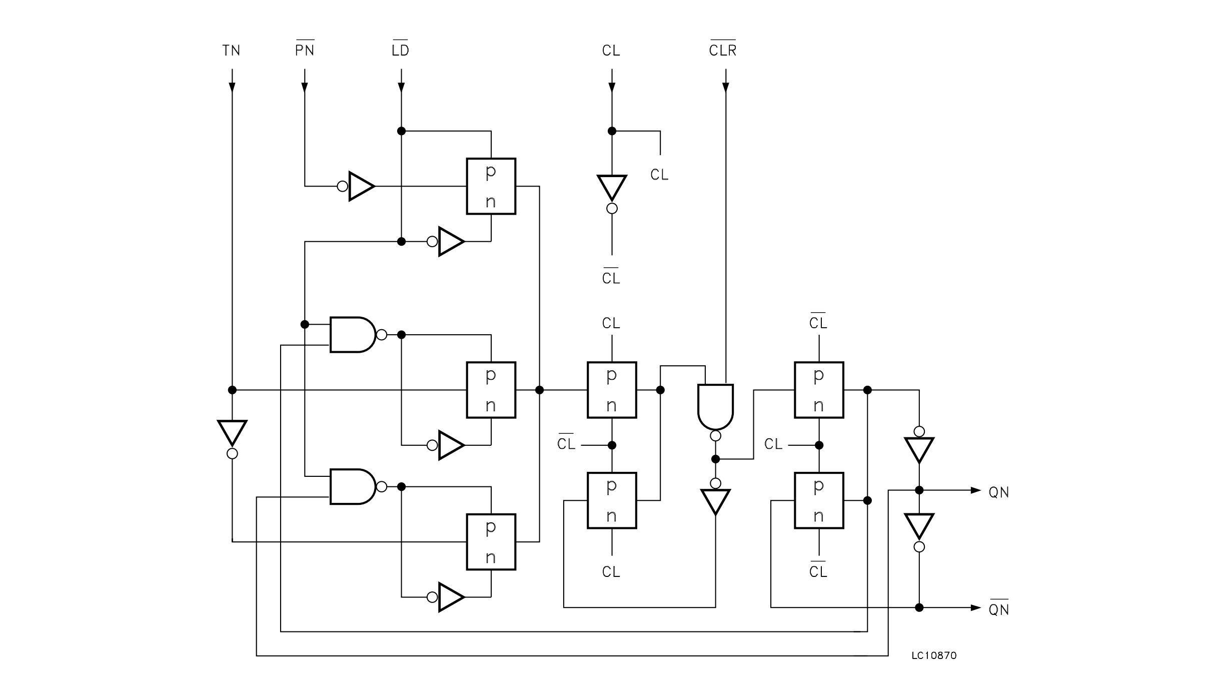
WAVEFORM 4 : SETUP AND HOLD TIMES (COUNTENABLE MODE) (f=1MHz; 50% duty cycle)



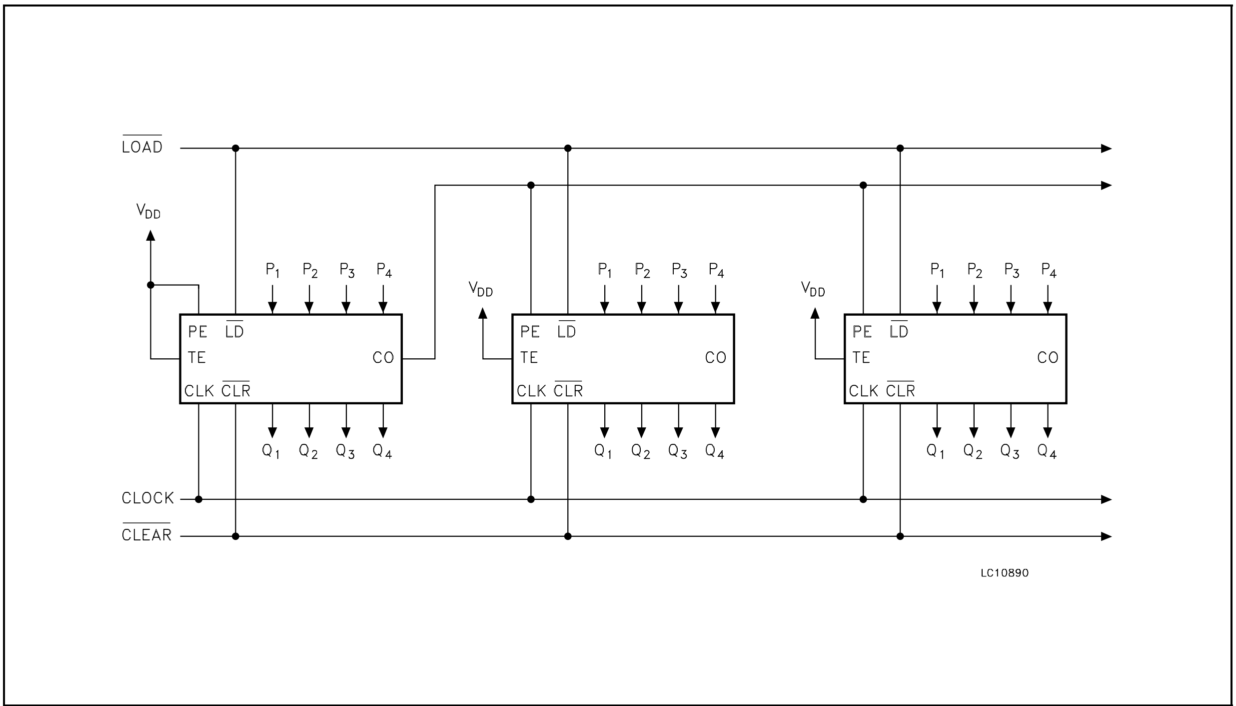
WAVEFORM 5 : PROPAGATION DELAY TIMES (CASCADE MODE) (f=1MHz; 50% duty cycle)



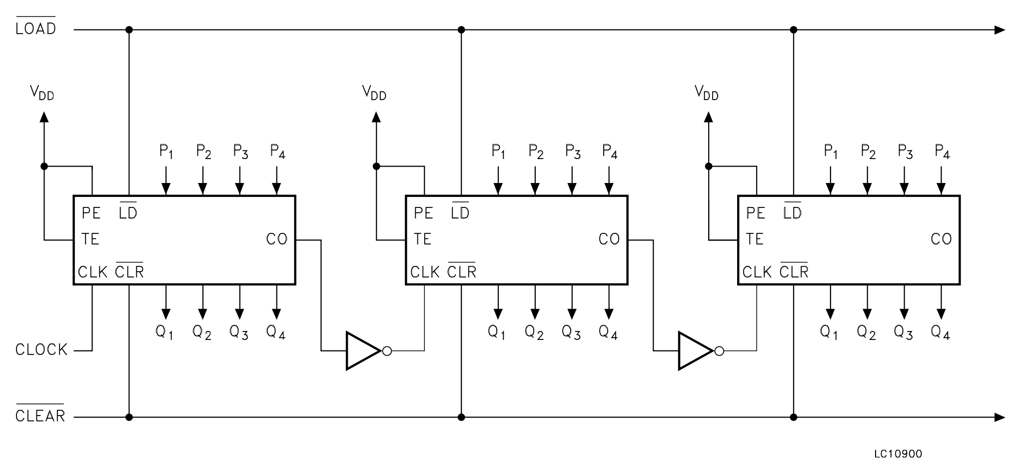
TYPICAL APPLICATION: DETAIL OF FLIP-FLOPS (Asynchronous Clear)



TYPICAL APPLICATION: CASCADING COUNTER PACKAGES IN THE PARALLEL-CLOCKED MODE

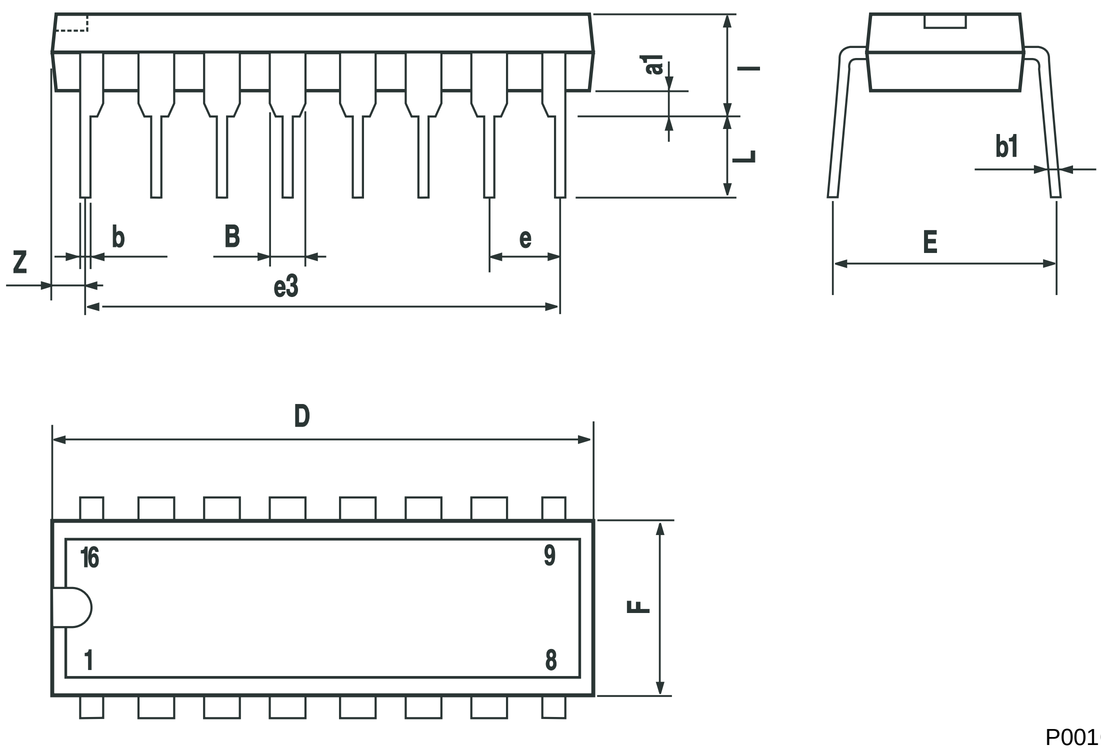


TYPICAL APPLICATION: CASCADING COUNTER PACKAGES IN THE RIPPLE-CLOCKED MODE



Plastic DIP-16 (0.25) MECHANICAL DATA

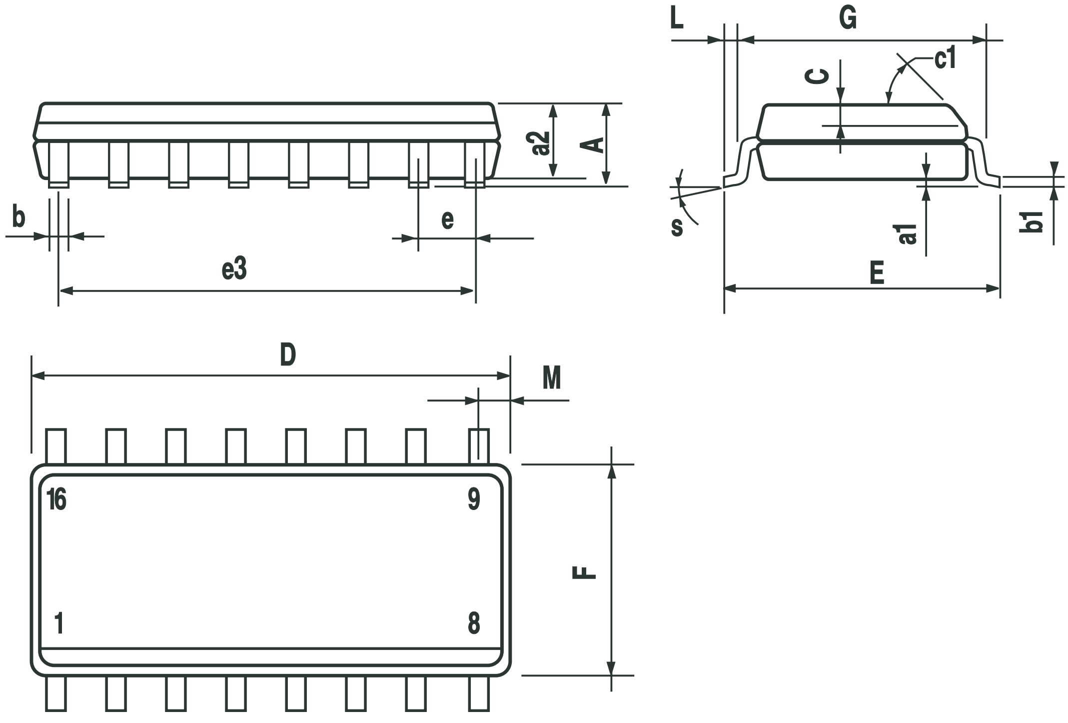
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H