HM66WP18512/HM66WP36256

9M Pipelined Zero Bus Latency (ZBL) SRAM

(HM66WP18512) 512-Kword × 18-bit
(HM66WP36256) 256-Kword × 36-bit

HITACHI

ADE-203-1284D (Z)
Preliminary
Rev. 0.4
Jun. 21, 2002

Description

The HM66WP18512 is a synchronous fast static RAM organized as 512-Kword × 18-bit. The HM66WP36256 is a synchronous fast static RAM organized as 256-Kword × 36-bit. It has realized high speed access time by employing the most advanced CMOS process and high speed circuit designing technology. It is most appropriate for the application which requires high speed, high density memory and wide bit width configuration, such as cache and buffer memory in system. It is packaged in standard 100-pin LQFP.

Note: All power supply (V_{DD}, V_{DDQ}) and ground (V_{SS}) pins must be connected for proper operation of the device.

ZBL: Zero Bus Latency and compatible ZBT™ SRAM. ZBT™ is trademark of Integrated Device Technology, Inc.,

Features

- 3.3 V or 2.5V power supply, 3.3 V or 2.5 V I/O supply voltage
- Clock frequency: 250/166 MHz
- Fast clock access time: 2.6/3.5 ns (max)
- Low operating current: 250/200 mA (max)
- Address data pipeline capability
- Internal input registers (Address, Data, Control)
- Internal self-timed write cycle
- ADV/$\overline{LD}$ burst control pins
- Internally synchronized registered outputs eliminate the need to control $\overline{OE}$
- Individual byte write control
- Power down state via ZZ
- Common data inputs and data outputs
- High board density 100-pin LQFP package
- Burst control selected pin $\overline{LBO}$ (Interleave or linear burst order)

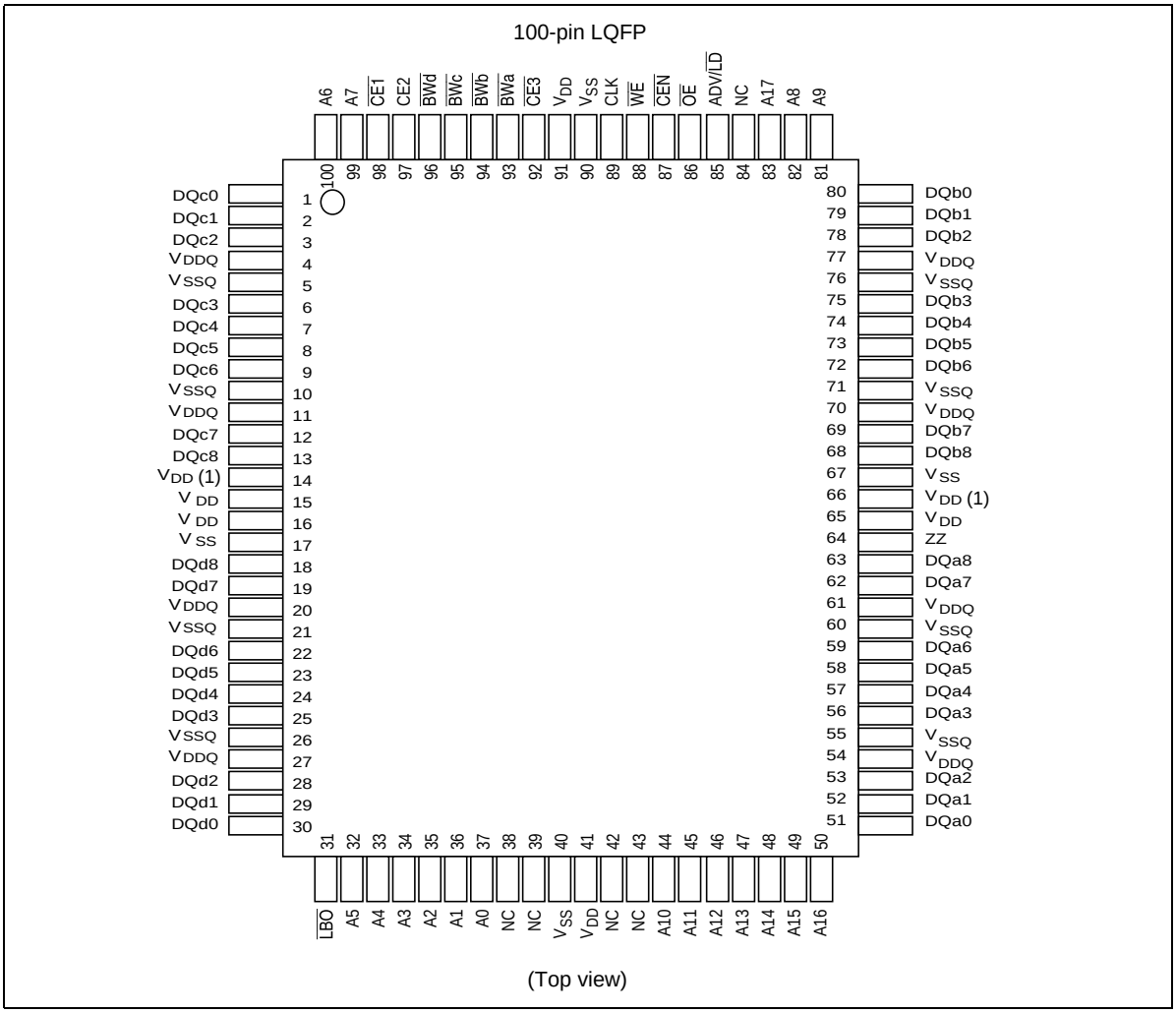
Preliminary: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

Shaping intelligence
HITACHI SEMICONDUCTOR

Ordering Information

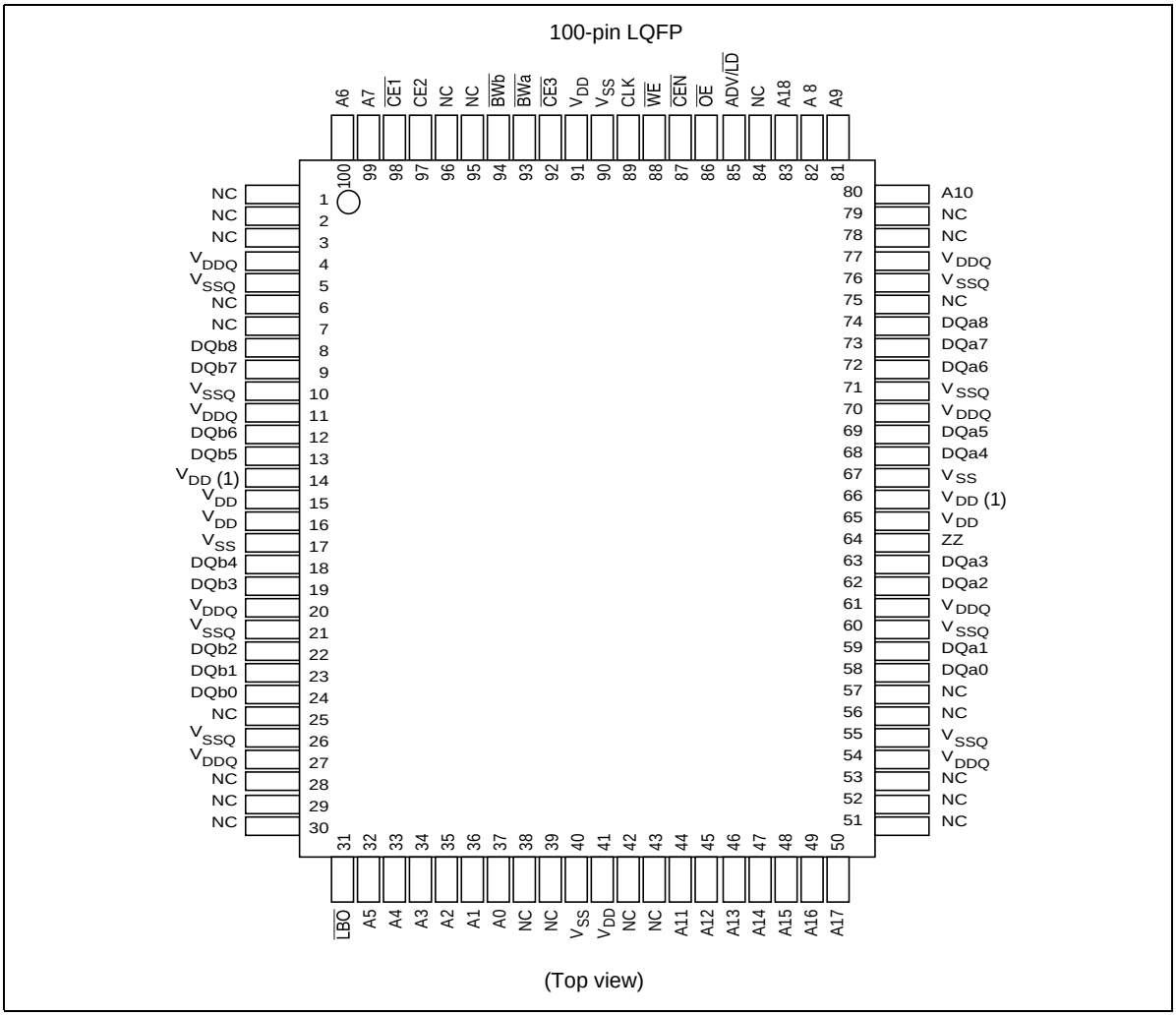
Type No.	Access time	CPU clock rate	Package
HM66WP18512FP-40	2.6 ns	250 MHz	LQFP 100-pin (FP-100H)
HM66WP18512FP-60	3.5 ns	166 MHz	
HM66WP36256FP-40	2.6 ns	250 MHz	
HM66WP36256FP-60	3.5 ns	166 MHz	

Pin Arrangement (HM66WP36256) 100PIN-LQFP



Note: Pins 14 and 66 are not V_{DD} Supply, but have to be connected V_{DD}.

Pin Arrangement (HM66WP18512) 100PIN-LQFP



Note: Pins 14 and 66 are not V_{DD} Supply, but have to be connected V_{DD}.

Pin Description (See Detailed Pin Description)

Name	I/O type	Description	Notes
A0, A1 and A2-17 (HM66WP36256)	Input	18 address inputs	
A0, A1 and A2-18 (HM66WP18512)	Input	19 address inputs	
$\overline{BWm}$	Input	Byte write enables $\overline{BWa}$ controls DQa0 to DQa8 $\overline{BWb}$ controls DQb0 to DQb8 $\overline{BWc}$ controls DQc0 to DQc8 $\overline{BWd}$ controls DQd0 to DQd8	m = a, b, c, d (HM66WP36256) m = a, b (HM66WP18512)
$\overline{WE}$	Input	Write enable	
CLK	Input	Clock	
$\overline{CE1}$, $\overline{CE3}$, CE2	Input	Chip enable	
$\overline{OE}$	Input	Output enable	
ADV/$\overline{LD}$	Input	Address load control	
$\overline{CEN}$	Input	Clock enable control	
ZZ	Input	Power down	
$\overline{LBO}$	Input	Burst mode control	
NC	—	No connection	
DQmn n = 0 – 8	Input/Output	Data input/output	m = a, b, c, d (HM66WP36256) m = a, b (HM66WP18512)
V_{DD}	Supply	Power supply	
V_{DDQ}	Supply	I/O power supply	
V_{SS}	Supply	Ground	

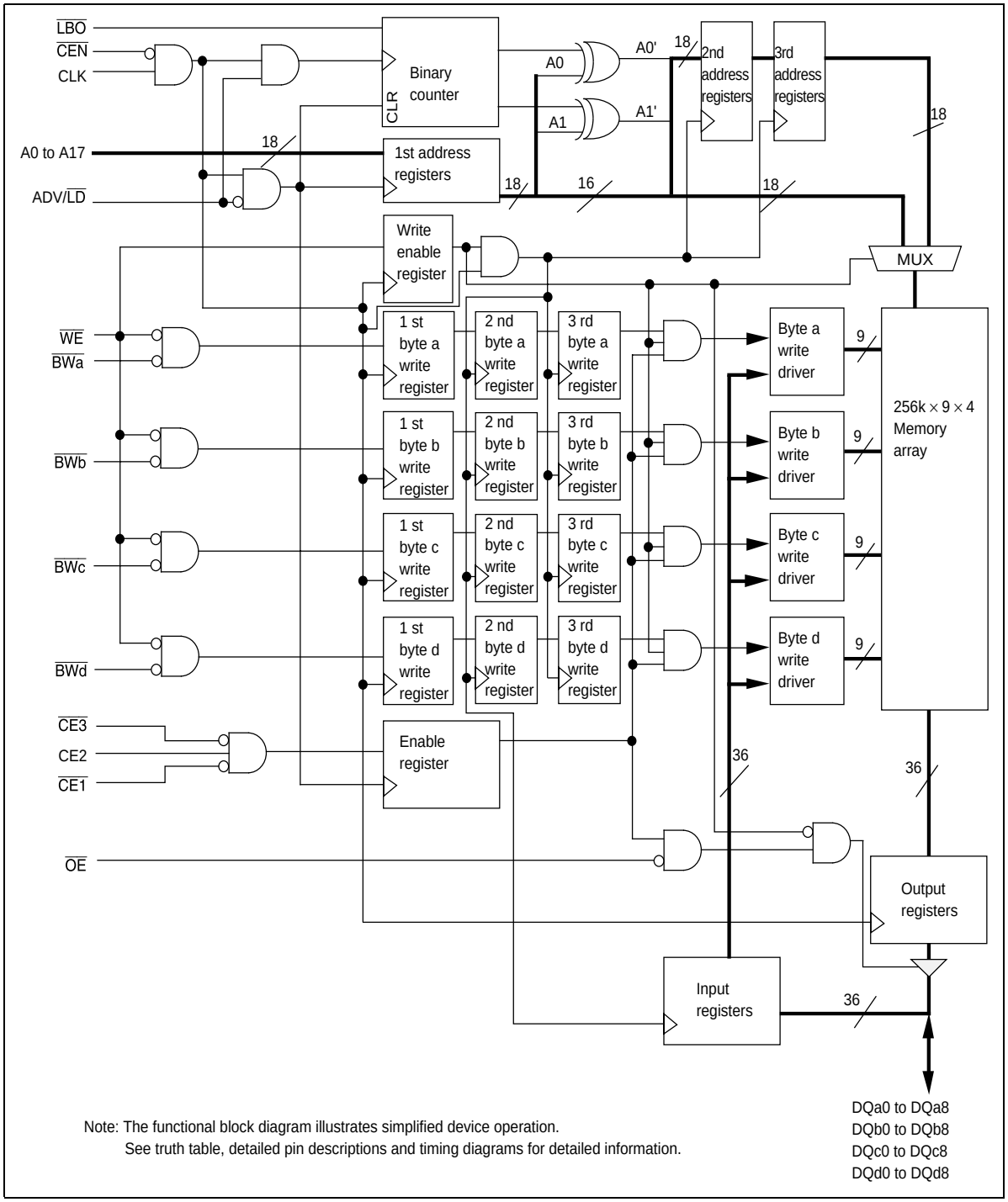
Detailed Pin Description

Pin number(s) LQFP	Symbol	Type	Description
35, 34, 33, 32, 44, 45, 46, 47, 48, 49, 50, 81, 82, 83, 99, 100	A ($\times$ 36-bit $\times$ 18-bit common)	Input	Synchronous address inputs: These inputs are registered and must meet setup and hold times around the rising edge of CLK.
37, 36	A0, A1		Burst address inputs
80	A ($\times$ 18-bit)		
93, 94, 95, 96	$\overline{BWa}$, $\overline{BWb}$ $\overline{BWc}$, $\overline{BWd}$ ($\times$ 36-bit)	Input	Synchronous byte write enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{BWa}$ controls DQa0 to DQa8. $\overline{BWb}$ controls DQb0 to DQb8. $\overline{BWc}$ controls DQc0 to DQc8. $\overline{BWd}$ controls DQd0 to DQd8. Data I/O are tristated if any of these four inputs are LOW.
93, 94	$\overline{BWa}$, $\overline{BWb}$ ($\times$ 18-bit)		
87	$\overline{CEN}$	Input	Synchronous clock enable: This active LOW internal clock signal is active.
88	$\overline{WE}$	Input	Synchronous write enable: This active LOW input permits write operations and must meet the setup and hold times around the rising edge of CLK.
89	CLK	Input	Clock: This signal latches the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
98	$\overline{CE1}$	Input	Synchronous chip enable: This active LOW input is used to enable the device. This input is sampled only when an external address is loaded. This input can be used for memory depth expansion.
92	$\overline{CE3}$	Input	
97	CE2	Input	Synchronous chip enable: This active HIGH input is used to enable the device. This input sampled only when a new external address is load. This input can be used for memory depth expansion.
86	$\overline{OE}$	Input	Output enable: This active LOW asynchronous input enables the data I/O output drivers.
85	ADV/$\overline{LD}$	Input	Synchronous address advance or load control: This active HIGH input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A LOW input is caused a new external address to be latched.

Detailed Pin Description (cont)

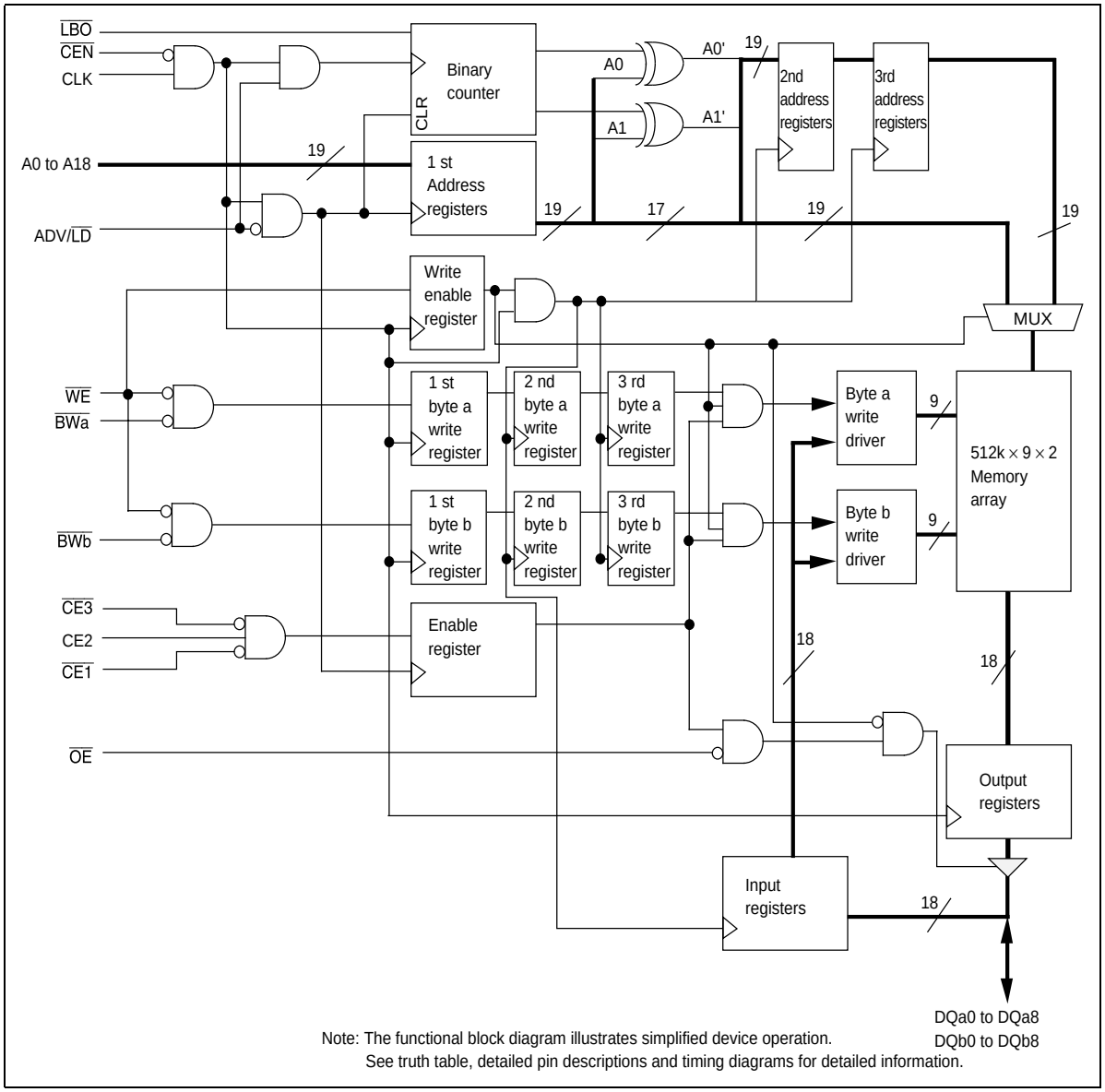
Pin number(s) LQFP	Symbol	Type	Description
38, 39, 42, 43, 84,	NC (× 36-bit)	—	No Connect: These signals are internally not connected.
1, 2, 3, 6, 7, 25, 28, 29, 30, 38, 39, 42, 43, 51, 52, 53, 56, 57, 75, 78, 79, 84, 95, 96	NC (× 18-bit)	—	No Connect: These signals are internally not connected.
51, 52, 53, 56, 57, 58, 59, 62, 63, 68, 69, 72, 73, 74, 75, 78, 79, 80, 1, 2, 3, 6, 7, 8, 9, 12, 13, 18, 19, 22, 23, 24, 25, 28, 29, 30	DQmn m = a, b, c, d n = 0 – 8 (× 36-bit)	Input/ Output	SRAM data I/O: Byte a is DQa0 to DQa8; Byte b is DQb0 to DQb8; Byte c is DQc0 to DQc8; Byte d is DQd0 to DQd8. Input data must meet setup and hold times around the rising edge of CLK.
58, 59, 62, 63, 68, 69, 72, 73, 74, 8, 9, 12, 13, 18, 19, 22, 23, 24	DQmn m = a, b n = 0 – 8 (× 18-bit)	Input/ Output	SRAM data I/O: Byte a is DQa0 to DQa8; Byte b is DQb0 to DQb8. Input data must meet setup and hold times around the rising edge of CLK.
14, 15, 16, 41, 65, 66, 91	V_{DD}	Supply	Power supply: 3.3 V (+5%/–5%) or 2.5 V (+5%/–5%)
4, 11, 20, 27, 54 61, 70, 77	V_{DDQ}	Supply	I/O power supply: 3.3 V (+5%/–5%) or 2.5 V (+5%/–5%)
17, 40, 67, 90, 5, 10, 21, 26, 55, 60, 71, 76	V_{SS}	Supply	Ground: GND
64	ZZ	Input	Asynchronous power-down (Snooze): This active HIGH input enables SRAM to enter a power-down (Snooze) state with data retention. During Snooze state, data retention is guaranteed. At this time, internal state of the SRAM is not preserved. After Snooze state, SRAM must be initiated with $\overline{CEN}$ or ADV/$\overline{LD}$ using a new external address. This pin must be connected to V_{SS} in systems that do not use ZZ feature.
31	$\overline{LBO}$	Input	Burst order (Interleave burst or linear burst) select pin (DC) This pin must connect V_{DD} or V_{DDQ} or V_{SS}.

Block Diagram (HM66WP36256)



Note: The functional block diagram illustrates simplified device operation.
See truth table, detailed pin descriptions and timing diagrams for detailed information.

Block Diagram (HM66WP18512)



Note: The functional block diagram illustrates simplified device operation.
See truth table, detailed pin descriptions and timing diagrams for detailed information.

Synchronous Truth Table

Operation	Address	$\overline{CE1}$	$\overline{CE3}$	CE2	ADV/$\overline{LD}$	$\overline{CEN}$	$\overline{WE}$	$\overline{BWm}$	$\overline{OE}$	CLK	DQ
Deselected cycle, power-down	None	H	×	×	L	L	×	×	×	L-H	High-Z
Deselected cycle, power-down	None	×	H	×	L	L	×	×	×	L-H	High-Z
Deselected cycle, power-down	None	×	×	L	L	L	×	×	×	L-H	High-Z
WRITE cycle, begin burst	External	L	L	H	L	L	L	L	×	L-H	D
NOP/WRITE Abort, begin burst	External	L	L	H	L	L	L	H	×	L-H	High-Z
READ cycle, begin burst	External	L	L	H	L	L	H	×	L	L-H	Q
Dummy READ cycle, begin burst	External	L	L	H	L	L	H	×	H	L-H	High-Z
WRITE cycle, continue burst	Next	×	×	×	H	L	×	L	×	L-H	D
WRITE Abort, continue burst	Next	×	×	×	H	L	×	H	×	L-H	High-Z
READ cycle, continue burst	Next	×	×	×	H	L	×	×	L	L-H	Q
Dummy READ cycle, continue burst	Next	×	×	×	H	L	×	×	H	L-H	High-Z
WRITE cycle, suspend	Current	×	×	×	×	H	×	×	×	L-H	-
READ cycle, suspend	Current	×	×	×	×	H	×	×	L	L-H	Q
Dummy READ cycle, suspend	Current	×	×	×	×	H	×	×	H	L-H	High-Z

Notes: 1. H means logic HIGH, L means logic LOW. × means H or L. $B\overline{Wm}$ = L means any one or more byte write enable signals ($\overline{BWa}$, $\overline{BWb}$, $\overline{BWc}$ or $\overline{BWd}$) are LOW. $B\overline{Wm}$ = H means all byte write enable signals are HIGH.

2. $\overline{BWa}$ enables write to Bytea (DQa0 to DQa8). $\overline{BWb}$ enables write to Byteb (DQb0 to DQb8). $\overline{BWc}$ enables write to Bytec (DQc0 to DQc8). $\overline{BWd}$ enables write to Byted (DQd0 to DQd8).
3. All inputs except $\overline{OE}$ and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. A WRITE is performed by setting one or more byte write enable signals and $\overline{WE}$ LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.
5. The status for DQ described in this synchronous truth table appears two clocks after the cycle in which the Read or Write command is asserted.
6. If ADV/$\overline{LD}$ is sampled High that it is continue burst cycle follows before the operation cycle.
7. Wait states are inserted by $\overline{CEN}$ = High. When $\overline{CEN}$ is sampled High after Read cycle, the Read data is maintain as output data. When $\overline{CEN}$ is sampled High after Write cycle, the Write Input Data is ignored and is maintained High-Z. Refer to Timing diagram for clarification.

Asynchronous Truth Table

Operation	ZZ	$\overline{OE}$	I/O status
Read	L	L	Data out
Read	L	H	High-Z
Write	L	×	High-Z, Data in
Deselect	L	×	High-Z
Power down (Snooze)	H	×	High-Z

Note: H means logic HIGH. L means logic LOW. × means H or L.

Partial Truth Table for Writes

Operation	$\overline{WE}$	$\overline{BWa}$	$\overline{BWb}$	$\overline{BWc}$	$\overline{BWd}$
Read	H	×	×	×	×
No write	L	H	H	H	H
Write byte a	L	L	H	H	H
Write all bytes	L	L	L	L	L

Note: H means logic HIGH. L means logic LOW. × means H or L.

Interleave Sequence Table ($\overline{LBO} = V_{DD}$ or V_{DDQ})

Parameter	Sequence 1 (A1, A0)	Sequence 2 (A1, A0)	Sequence 3 (A1, A0)	Sequence 4 (A1, A0)
External address	0 0	0 1	1 0	1 1
1st internal address	0 1	0 0	1 1	1 0
2nd internal address	1 0	1 1	0 0	0 1
3rd internal address	1 1	1 0	0 1	0 0

Note: Each sequence wraps around to its initial state upon completion.

Linear Sequence Table ($\overline{LBO} = V_{SS}$)

Parameter	Sequence 1 (A1, A0)	Sequence 2 (A1, A0)	Sequence 3 (A1, A0)	Sequence 4 (A1, A0)
External address	0 0	0 1	1 0	1 1
1st internal address	0 1	1 0	1 1	0 0
2nd internal address	1 0	1 1	0 0	0 1
3rd internal address	1 1	0 0	0 1	1 0

Note: Each sequence wraps around to its initial state upon completion.

Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Supply voltage		V_{DD}	–0.5 to +4.6	V
Voltage on any pins relative to V_{SS}	(DQ)	V_T	–0.5 to V_{DDQ} + 0.5	V
Except V_{DD}	(Others)	V_T	–0.5 to V_{DD} + 0.5	V
Power dissipation		P_T	1.6	W
Operating temperature		Topr	0 to +70	°C
Storage temperature range (with bias)		Tstg (bias)	–10 to +85	°C
Storage temperature range		Tstg	–55 to +125	°C

Recommended DC Operating Conditions (3.3V Power supply)

(Ta = 0 to +70°C)

Parameter		Symbol	Min	Typ	Max	Unit	Note
Supply voltage (Operating voltage range)		V_{DD}	3.135	3.3	3.465	V	
Supply I/O voltage (3.3 V I/O)		V_{DDQ}	3.135	3.3	3.465	V	
Supply I/O voltage (2.5 V I/O)		V_{DDQ}	2.375	2.5	2.625	V	
Supply voltage to V_{SS}		V_{SS}	0.0	0.0	0.0	V	
Input high voltage (3.3 V I/O)	(DQ)	V_{IH}	2.0	-	V_{DDQ} + 0.3	V	
	(Others)	V_{IH}	2.0	-	V_{DD} + 0.3	V	
Input high voltage (2.5 V I/O)	(DQ)	V_{IH}	1.7	-	V_{DDQ} + 0.3	V	
	(Others)	V_{IH}	1.7	-	V_{DD} + 0.3	V	
Input low voltage (3.3 V I/O)		V_{IL}	–0.3	-	0.8	V	1
Input low voltage (2.5 V I/O)		V_{IL}	–0.3	-	0.7	V	1

Note: 1. –2.0 V for undershoot pulse width ≤ 20% t_{CYC}.

Recommended DC Operating Conditions (2.5V Power supply)

(Ta = 0 to +70°C)

Parameter		Symbol	Min	Typ	Max	Unit	Note
Supply voltage (Operating voltage range)		V_{DD}	2.375	2.5	2.625	V	
Supply I/O voltage (2.5 V I/O)		V_{DDQ}	2.375	2.5	2.625	V	
Supply voltage to V_{SS}		V_{SS}	0.0	0.0	0.0	V	
Input high voltage (2.5 V I/O)	(DQ)	V_{IH}	1.7	-	V_{DDQ} + 0.3	V	
	(Others)	V_{IH}	1.7	-	V_{DD} + 0.3	V	
Input low voltage (2.5 V I/O)		V_{IL}	–0.3	-	0.7	V	1

Note: 1. –2.0 V for undershoot pulse width ≤ 20% t_{CYC}.

DC Characteristics

(Ta = 0 to +70°C, V_{DD} = 3.3 V +5%/–5% or 2.5 V +5%/–5%)

		HM66WP18512/HM66WP36256					
		-40		-60			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**
Input leakage current	I_{LI}	–2	2	–2	2	µA	All inputs Vin = V_{SS} to V_{DD}
Output leakage current	I_{LO}	–5	5	–5	5	µA	$\overline{OE}$ = V_{IH}, Vout = V_{SS} to V_{DDQ}
Operating current	I_{DD}	—	250	—	200	mA	Device selected, Iout = 0 mA, all inputs = V_{IH} or V_{IL}, cycle time = t_{CYC} min.
Standby current	I_{SB}	—	100	—	80	mA	Device deselected all inputs = fixed and all inputs ≥ V_{DD} – 0.2 V or ≤ 0.2 V, cycle time = t_{CYC} min.
	I_{SB1}	—	30	—	30	mA	Device deselected all inputs = fixed and all inputs ≥ V_{DD} – 0.2 V or ≤ 0.2 V, Frequency = 0 MHz.
	I_{SBZZ}	—	10	—	10	mA	Device deselected all inputs = fixed and all inputs ≥ V_{DD} – 0.2 V or ≤ 0.2 V, ZZ ≥ V_{DD} – 0.2 V, Frequency = 0 MHz.
Output low voltage (3.3 V I/O)	V_{OL}	—	0.4	—	0.4	V	I_{OL} = 8 mA
Output high voltage (3.3 V I/O)	V_{OH}	2.4	—	2.4	—	V	I_{OH} = –4 mA
Output low voltage (2.5 V I/O)	V_{OL}	—	0.4	—	0.4	V	I_{OL} = 1 mA
Output high voltage (2.5 V I/O)	V_{OH}	2.0	—	2.0	—	V	I_{OH} = –1 mA

Note: 1. $\overline{LBO}$ pin has an internal pull-up, ZZ pin has an internal pull-down, and input leakage current < |5µA|.

Capacitance

(Ta = +25°C, f = 1.0 MHz, V_{DD} = 3.3 V and 2.5 V)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Input capacitance	Cin	—	4	5	pF	1
Input/output capacitance	$C_{I/O}$	—	6	7	pF	1

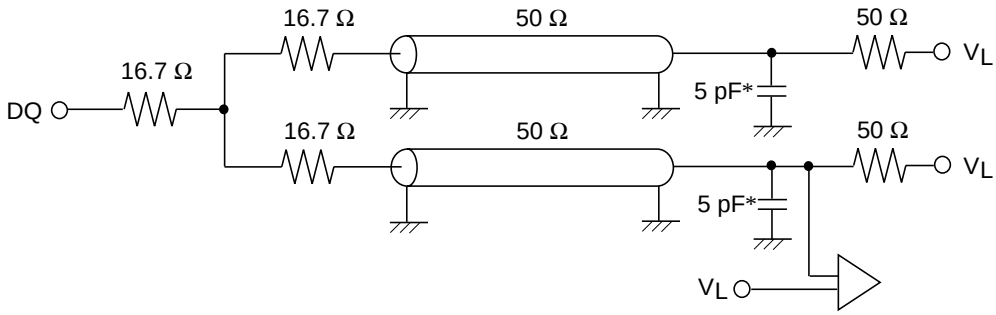
Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics

(Ta = 0 to +70°C, V_{DD} = 3.3 V +5%/–5% and 2.5 V +5%/–5%, V_{SS} = 0 V)

Test Conditions

- Input timing measurement reference level :1.4 V (3.3 V I/O)
  :1.2 V (2.5 V I/O)
- Input pulse levels : 0 V to 2.8 V (3.3 V I/O)
  : 0 V to 2.4 V (2.5 V I/O)
- Input rise and fall time: 2 V/ns (10% – 90%)
- Output timing reference level : 1.4 V (3.3 V I/O)
  : 1.2 V (2.5 V I/O)
- Output load: See figure



V_L = 1.4 V (3.3 V I/O) or 1.2 V (2.5 V I/O)

*(Including scope and jig)

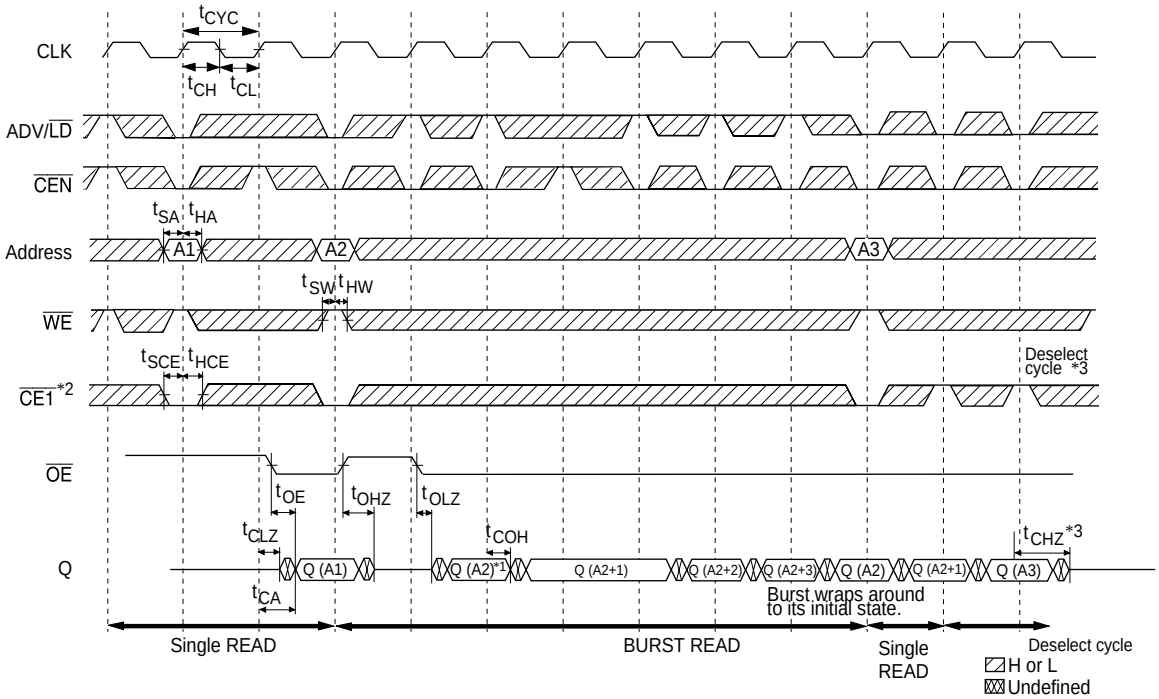
	Symbol		HM66WP18512/HM66WP36256 -40		-60			
Parameter	**Standard**	**Alternate**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Cycle time	t_{KHKH}	t_{CYC}	4.0	—	6.0	—	ns	
Clock access time	t_{KHQV}	t_{CA}	—	2.6	—	3.5	ns	
Output enable to output valid	t_{GLQV}	t_{OE}	—	2.6	—	3.5	ns	
Clock high to output active	t_{KHQX2}	t_{CLZ}	0.8	—	1.5	—	ns	1
Clock high to output change	t_{KHQX}	t_{COH}	0.8	—	1.5		ns	
Output enable to output active	t_{GLQX}	t_{OLZ}	0	—	0	—	ns	1
Output disable to Q High-Z	t_{GHQZ}	t_{OHZ}	—	2.6	—	3.5	ns	1
Clock high to Q High-Z	t_{KHQZ}	t_{CHZ}	—	2.6	—	3.5	ns	1
Clock high pulse width	t_{KHKL}	t_{CH}	1.7	—	2.2	—	ns	
Clock low pulse width	t_{KLKH}	t_{CL}	1.7	—	2.2	—	ns	
Setup Times:			1.2	—	1.5	—	ns	
Address	t_{AVKH}	t_{SA}						
Clock Enable	t_{CENVKH}	t_{SCEN}						
Input Data	t_{DVKH}	t_{SD}						
Write ($\overline{WE}$, $\overline{BWa\text{-}d}$)	t_{WVKH}	t_{SW}						
Address Advance	t_{ADVVK}	t_{SADV}						
Chip Enable	t_{EVKH}	t_{SCE}						
Hold Times:			0.3	—	0.5	—	ns	
Address	t_{KHAX}	t_{HA}						
Clock Enable	t_{KHCENX}	t_{HCEN}						
Input Data	t_{KHDX}	t_{HD}						
Write ($\overline{WE}$, $\overline{BWa\text{-}d}$)	t_{KHWX}	t_{HW}						
Address Advance	t_{KHADVX}	t_{HADV}						
Chip Enable	t_{KHEX}	t_{HCE}						
ZZ Active to input ignored		t_{PDS}	2	—	2	—	cycle	4
ZZ Inactive to input Sampled		t_{PUS}	2	—	2	—	cycle	4
ZZ Active to sleep current		t_{ZZI}	—	2	—	2	cycle	4
ZZ Inactive to exit sleep current		t_{RZZI}	0	—	0	—	cycle	4

Notes: 1. Transition is measured ± 100 mV from steady-state voltage. This parameter is sampled.

2. A READ cycle is defined by $\overline{WE}$ HIGH for the required setup and hold times. A WRITE cycle is defined by $\overline{WE}$ LOW for the required setup and hold times.
3. This is a synchronous device. All address must meet the specified setup and hold times for all rising edges of CLK when chip enabled. All other Synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when chip is enabled. Chip enable must be valid at each rising edge of CLK to remain enabled.
4. Data-output is not guaranteed during the cycle when transition of ZZ from low to high occurs.

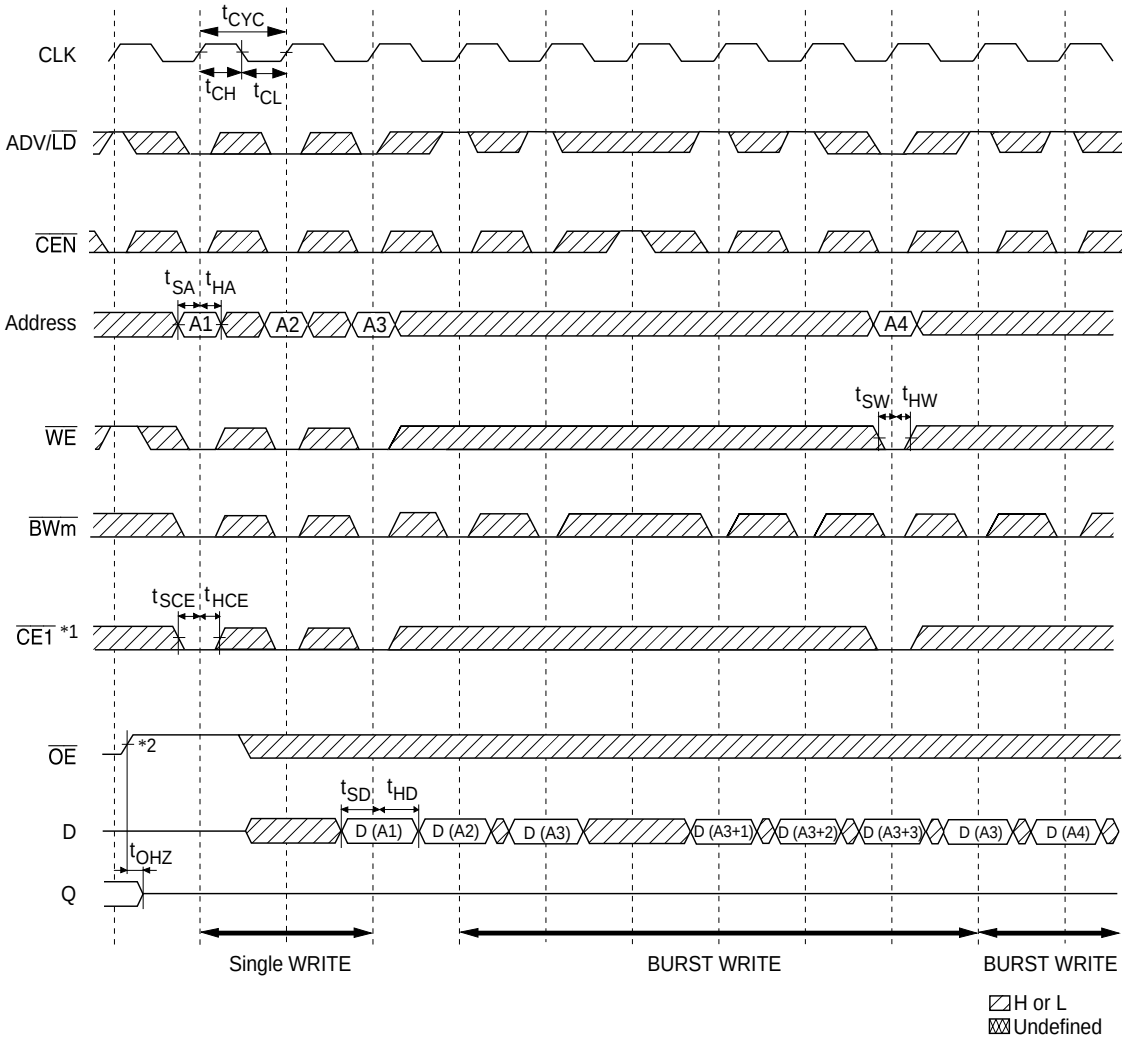
Timing Waveforms

Read Cycle



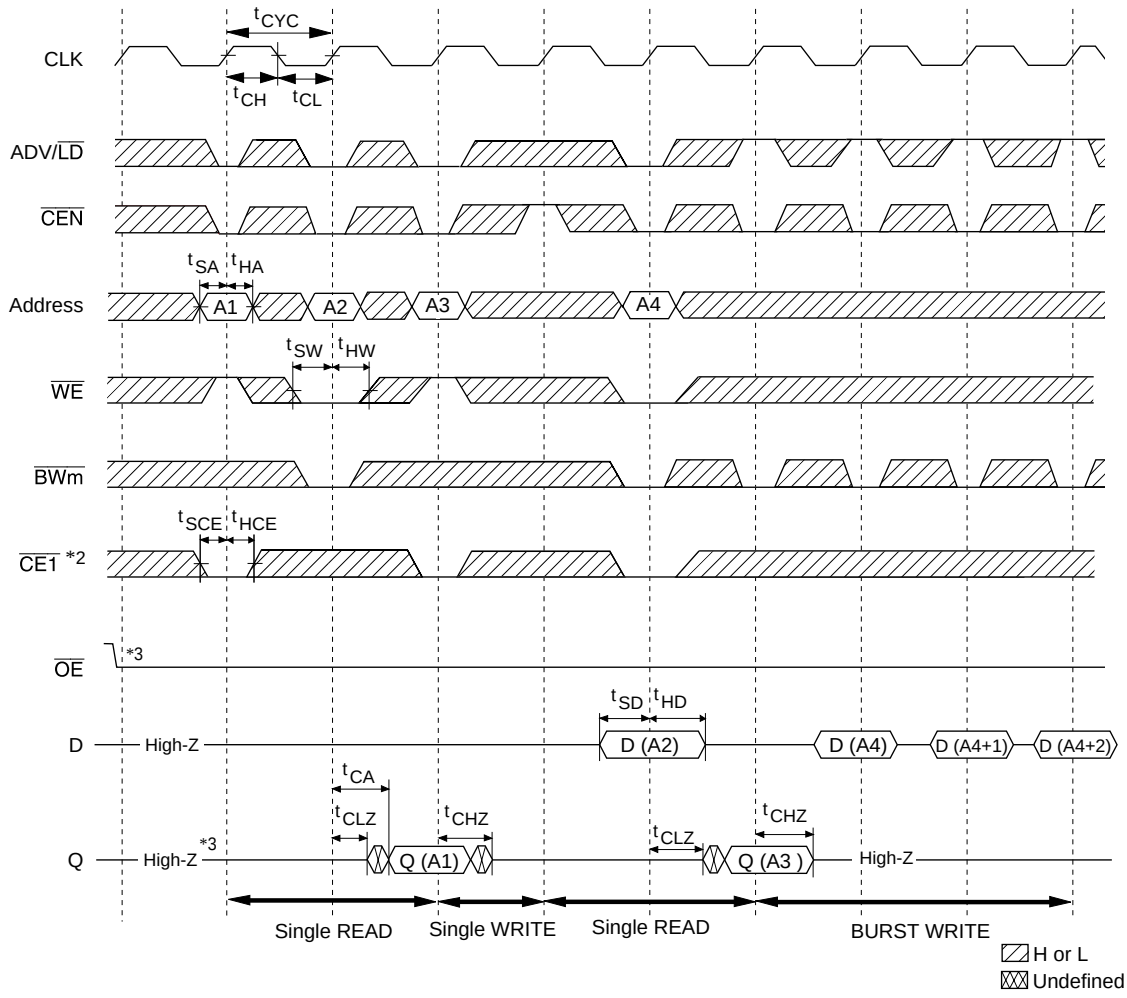
Notes: 1. Q (A2) refers to output from address A2. Q (A2 + 1) refers to output from next internal burst address following A2.
2. $\overline{CE3}$ and CE2 have timing identical to $\overline{CE1}$. On this diagram, when $\overline{CE1}$ is LOW, $\overline{CE3}$ is LOW and CE2 is HIGH. When $\overline{CE1}$ is HIGH, $\overline{CE3}$ is HIGH and CE2 is LOW.
3. Outputs are disabled within one clock cycle after deselect.
4. ZZ is LOW.

Write Cycle



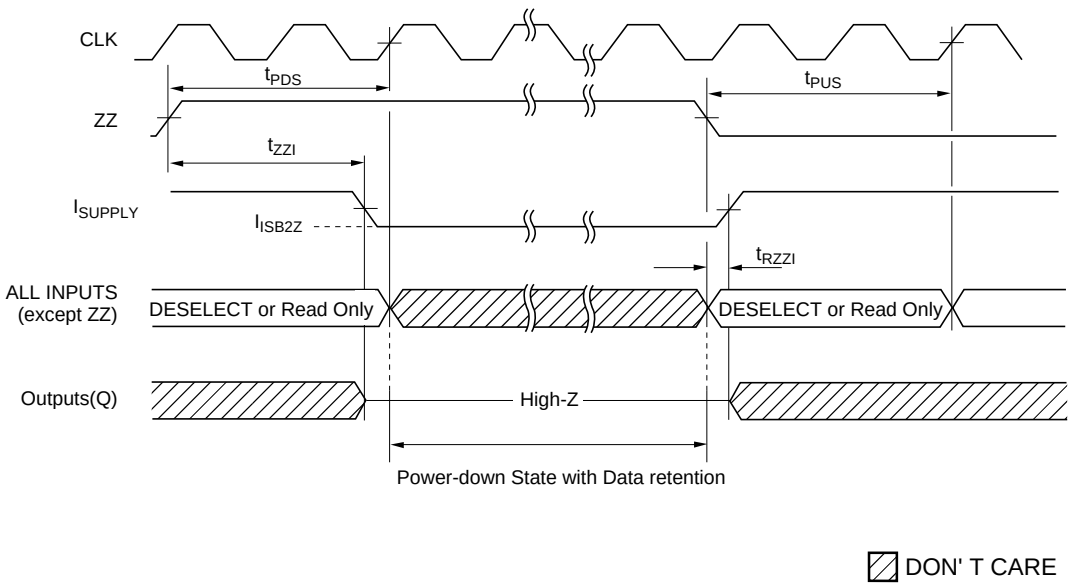
Notes: 1. $\overline{CE3}$ and CE2 have timing identical to $\overline{CE1}$. On this diagram, when $\overline{CE1}$ is LOW, $\overline{CE3}$ is LOW and CE2 is HIGH. When $\overline{CE1}$ is HIGH, $\overline{CE3}$ is HIGH and CE2 is LOW.
2. $\overline{OE}$ must be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
3. Full width WRITE can be initiated by $\overline{WE}$, $\overline{BWa}$ to $\overline{BWd}$ are LOW.
4. ZZ is LOW.

Read-Write Cycle



Notes: 1. Q (A3) refers to output from address A3.
2. $\overline{CE3}$ and CE2 have timing identical to $\overline{CE1}$. On this diagram, when $\overline{CE1}$ is LOW, $\overline{CE3}$ is LOW and CE2 is HIGH. When $\overline{CE1}$ is HIGH, $\overline{CE3}$ is HIGH and CE2 is LOW.
3. Timing is shown assuming that the device was not enabled before entering into this sequence. $\overline{OE}$ does not cause Q to be driven until after the following clock rising edge.
4. ZZ is LOW.

Power-down State



Notes: 1. The terms of t_{PDS} and t_{PUS} have to be that $\overline{CEN}$ is LOW.
2. Data-output is not guaranteed during the cycle when transition of ZZ from low to high occurs.

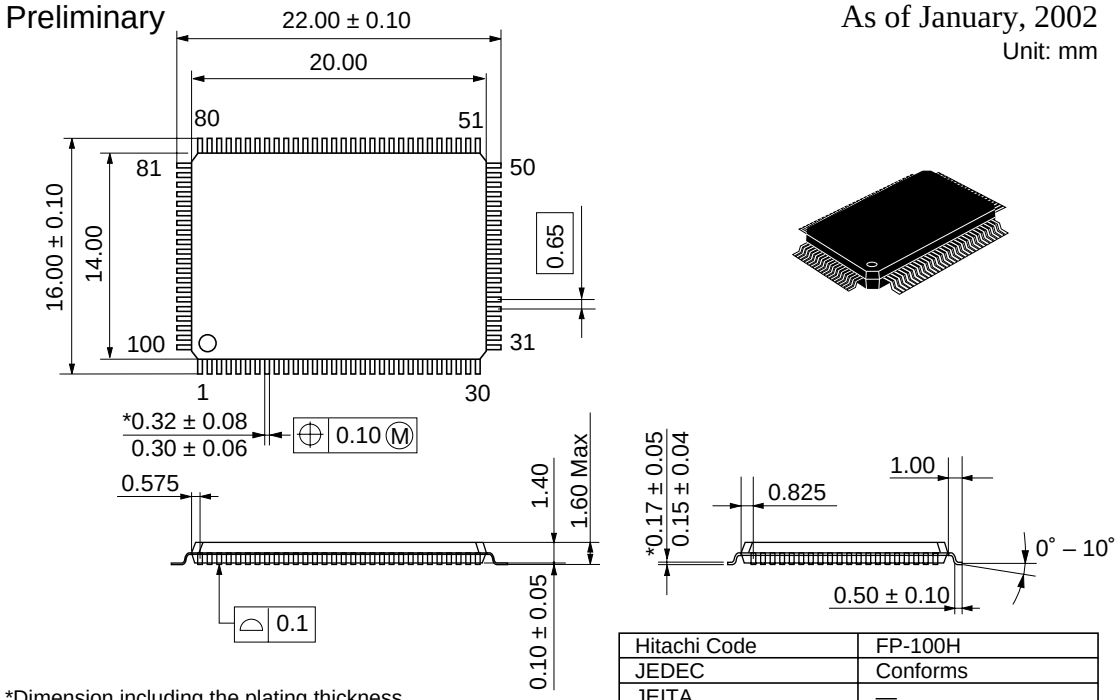
Package Dimensions

HM66WP18512FP, HM66WP36256FP Series (FP-100H)

Preliminary

As of January, 2002

Unit: mm



Hitachi Code	FP-100H
JEDEC	Conforms
JEITA	—
Mass (reference value)	0.95 g

*Dimension including the plating thickness
Base material dimension

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