Ordering number : ENN8095

SANYO Semiconductors

DATA SHEET

Monolithic Digital IC

LB11693 — Three-Phase Brushless Motor Driver for 24 V Fan Motors

Overview

The LB11693 reduces motor noise by imparting a slope to the output current when switching the phase to which power is applied. This motor driver includes an automatic recovery constraint protection circuit and is optimal for driving 24 V fan motors.

Functions and Features

- Soft phase switching + direct PWM drive
- PWM control based on both a DC voltage input (the CTL voltage) and a pulse input
- Provides a 5 V regulator output
- One Hall-effect sensor FG output
- Integrating amplifier
- Automatic recovery constraint protection circuit (on/off = 1/14), RD output
- Current limiter circuit
- LVSD circuit
- Thermal protection circuitt

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC} max		30	V
Output current	IO max	T ≤ 500 ms	1.8	A
Allowable power dissipation 1	Pd max1	Independent IC	3	W
Allowable power dissipation 2	Pd max2	With an infinite heat sink	20	W
Operating temperature	Topr		–30 to +100	°C
Storage temperature	Tstg		–55 to +150	°C

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Allowable Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range	V_{CC}		9.5 to 28	V
Constant voltage output current	IREG		0 to –30	mA
RD output current	IRD		0 to 10	mA
FG output current	IFG		0 to 10	mA

Electrical Characteristics at Ta = 25°C, V_{CC} = VM = 24 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain 1	$I_{CC}1$			10	13.5	mA
Current drain 2	$I_{CC}2$	Stop mode		4.0	5.5	mA
Output Block						
Output saturation voltage 1	$V_O$sat1	I_O = 0.7 A, V_O (SINK) + V_O (SOURCE)		1.5	2.05	V
Output saturation voltage 2	$V_O$sat2	I_O = 1.5 A, V_O (SINK) + V_O (SOURCE)		2.2	2.9	V
Output leakage current	$I_O$leak				100	µA
High side diode forward voltage 1	VD1	ID = 0.7 A		1.25	1.65	V
High side diode forward voltage 2	VD2	ID = 1.5 A		1.9	2.5	V
5 V Constant Voltage Output						
Output voltage	VREG	I_O = –5 mA	4.7	5.0	5.3	V
Line regulation	ΔVREG1	V_{CC} = 9.5 to 28 V		30	100	mV
Load regulation	ΔVREG2	I_O = –5 to –20 mA		20	100	mV
Hall Sensor Amplifier						
Input bias current	IB (HA)			2	10	µA
Differential-mode input voltage range	VHIN	Sine wave input	50		350	mVp-p
Common-mode input voltage range	VICM	Differential input, 50 mVp-p	1.5		VREG – 1.0	V
Input offset voltage	VIOH	Design target value	–20		20	mV
CSD Pin						
High-level output voltage	VOH (CSD)		2.75	3.0	3.25	V
Low-level output voltage	VOL (CSD)		0.85	1.0	1.15	V
External capacitor charge current	ICSD1		–3.3	–2.4	–1.4	µA
External capacitor discharge current	ICSD2		0.09	0.17	0.23	µA
Charge/discharge current ratio	RCSD	Charge current/discharge current		14		times
Undervoltage Protection Circuit (LVS pin)						
Operating voltage	VSDL		3.6	3.8	4.0	V
Release voltage	VSDH		4.1	4.3	4.5	V
Hysteresis	ΔVSD		0.35	0.5	0.65	V
Current Limiter Circuit (RF pin)						
Limit voltage	VRF	V_{CC} – VM	0.45	0.5	0.55	V
Thermal Protection Operation						
Thermal protection operating temperature	TSD	Design target value (junction temperature)	150	170		°C
Hysteresis	ΔTSD	Design target value (junction temperature)		40		°C
CTL Amplifier						
Input offset voltage	VIO (CTL)		–10		+10	mV
Input bias current	IB (CTL)		–1		+1	µA
Common-mode input voltage range	VICM		0		VREG – 1.7	V
High-level output voltage	VOH (CTL)	ITOC = –0.2 mA	VREG – 1.2	VREG – 0.8		V
Low-level output voltage	VOL (CTL)	ITOC = 0.2 mA		0.8	1.05	V
Open-loop gain	G (CTL)	f (CTL) = 1 kHz	45	51		dB
PWM Oscillator Circuit						
High-level output voltage	VOH (PWM		2.75	3.0	3.25	V
Low-level output voltage	VOL (PWM)		1.1	1.3	1.4	V
Amplitude	V (PWM)		1.5	1.7	2.0	Vp-p
External capacitor charge current	ICHG	VPWM = 2.1 V	–125	–90	–70	µA
Oscillator frequency	f (PWM)	C = 2200 pF	15.5	19.5	27.0	kHz
TOC Pin						
Input voltage 1	VTOC1	Output duty: 100%	2.72	3.0	3.30	V
Input voltage 2	VTOC2	Output duty: 0%	1.07	1.3	1.45	V
Input voltage 1L	VTOC1L	Design target value, when VREG = 4.7 V, 100%	2.72	2.80	2.90	V
Input voltage 2L	VTOC2L	Design target value, when VREG = 4.7 V, 0%	1.07	1.17	1.27	V
Input voltage 1H	VTOC1H	Design target value, when VREG = 5.3 V, 100%	3.08	3.20	3.30	V
Input voltage 2H	VTOC2H	Design target value, when VREG = 5.3 V, 0%	1.21	1.33	1.45	V

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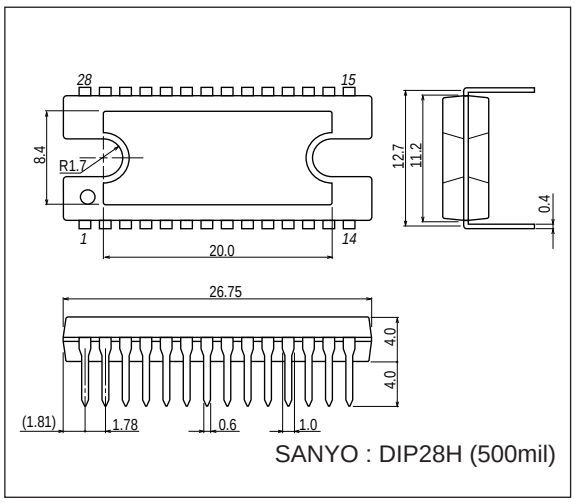
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
RD Pin						
Low-level output voltage	VOL (RD)	IRD = 5 mA		0.1	0.3	V
Output leakage current	IL (RD)	VRD = 28 V			10	µA
FG Pin						
Low-level output voltage	VOL (FG)	IFG = 5 mA		0.1	0.3	V
Output leakage current	IL (FG)	VFG = 28 V			10	µA
FGFIL Pin						
Charge current	IFGFIL1		–7	–5	–3	µA
Discharge current	IFGFIL2		3	5	7	µA
FG Amplifier Schmitt Block (IN1)						
Amplifier gain	G (FG)	Design target value		7		times
Hysteresis	VIS (FG)	Design target value, input equivalent		8		mV
S/S Pin						
High-level input voltage range	VIH (SS)		2.0		VREG	V
Low-level input voltage range	VIL (SS)		0		1.0	V
Input open voltage	VIO (SS)		2.6	2.9	3.2	V
Hysteresis	VIS (SS)		0.16	0.25	0.34	V
High-level input current	IIH (SS)	VS/S = VREG		100	130	µA
Low-level input current	IIL (SS)	VS/S = 0 V	–170	–130		µA
PWMIN Pin						
Input frequency range	f (PI)				50	kHz
High-level input voltage range	VIH (PI)		2.0		VREG	V
Low-level input voltage range	VIL (PI)		0		1.0	V
Input open voltage	VIO (PI)		2.6	2.9	3.2	V
Hysteresis	VIS (PI)		0.16	0.25	0.34	V
High-level input current	IIH (PI)	VPWMIN = VREG		100	130	µA
Low-level input current	IIL (PI)	VPWMIN = 0 V	–170	–130		µA
F/R Pin						
High-level input voltage range	VIH (FR)		2.0		VREG	V
Low-level input voltage range	VIL (FR)		0		1.0	V
Input open voltage	VIO (FR)		VREG – 0.5		VREG	V
Hysteresis	VIS (FR)		0.16	0.25	0.34	V
High-level input current	IIH (FR)	VF/R = VREG	–10	0	+10	µA
Low-level input current	IIL (FR)	VF/R = 0 V	–165	–115		µA

Package Dimensions

unit : mm

3147C



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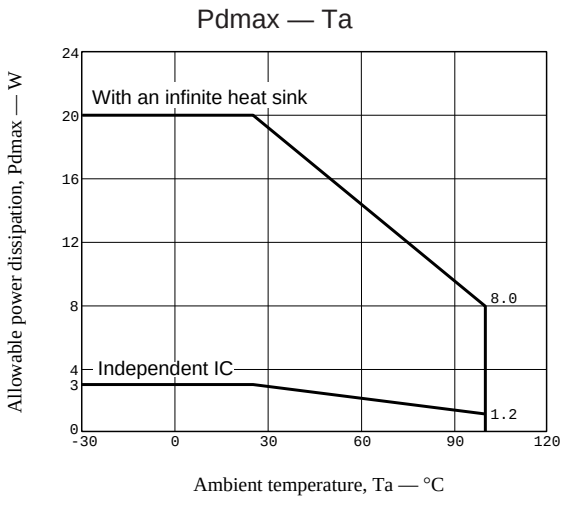
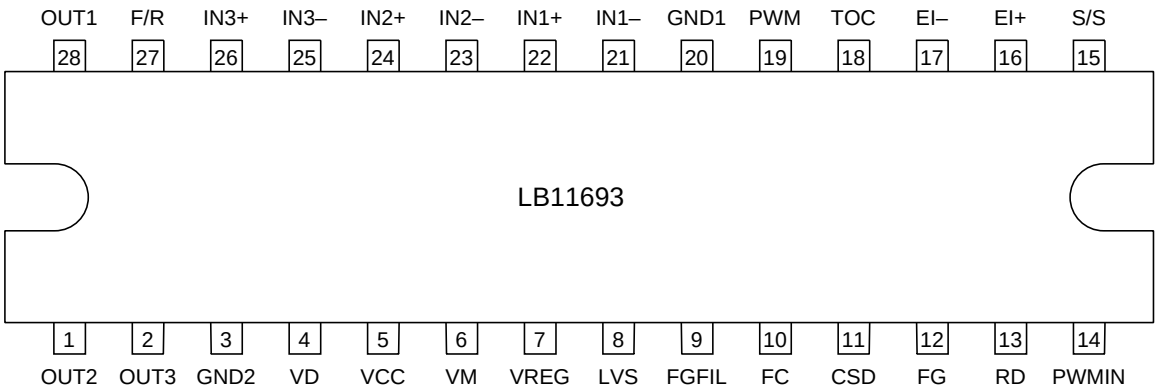


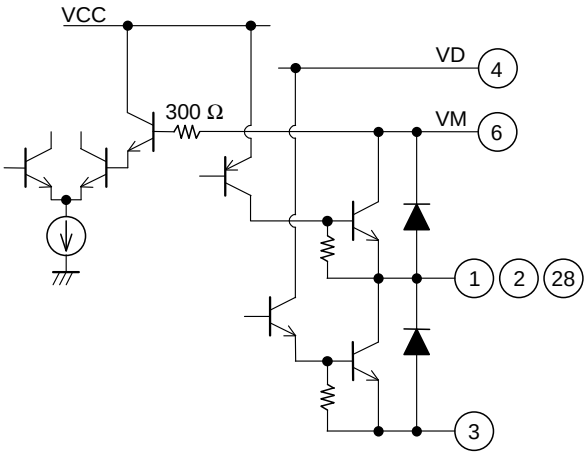
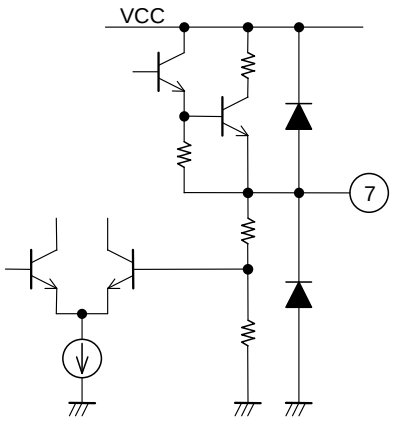
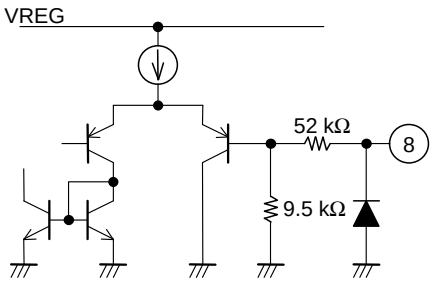
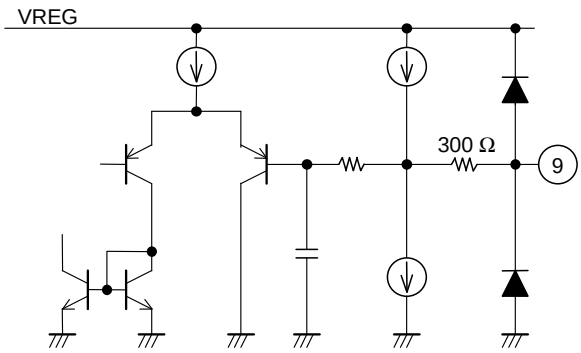
Truth Table

	Source → Sink	F/R = L			F/R = H		
		IN1	IN2	IN3	IN1	IN2	IN3
1	OUT2 → OUT1	H	L	H	L	H	L
2	OUT3 → OUT1	H	L	L	L	H	H
3	OUT3 → OUT2	H	H	L	L	L	H
4	OUT1 → OUT2	L	H	L	H	L	H
5	OUT1 → OUT3	L	H	H	H	L	L
6	OUT2 → OUT3	L	L	H	H	H	L

Pin Assignment



Pin Functions

Pin No.	Symbol	Function	Equivalent circuit
28 1 2	OUT1 OUT2 OUT3	Motor drive outputs	
3	GND2	Motor drive output system ground	
4	VD	Low side output transistor drive current supply	
6	VM	Motor drive output power supply and output current detection Connect the resistor Rf between this pin and V_{CC}. The output current will be limited to the current value set by the equation IOUT = VRF/Rf.	
5	V_{CC}	Power supply for systems other than the motor drive output	
7	VREG	5 V regulator output Insert a capacitor (about 0.1 µF) between this pin and ground for stabilization.	
8	LVS	Undervoltage protection voltage detection To detect VREG, connect this pin to VREG. To detect V_{CC}, set the detection voltage by inserting a zener diode in series.	
9	FGFIL	FG filter connection This pin is normally left open. If noise on the FG signal is a problem, insert a capacitor between this pin and ground.	

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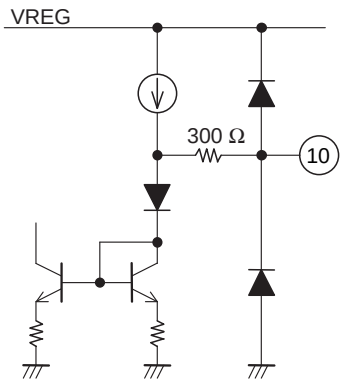
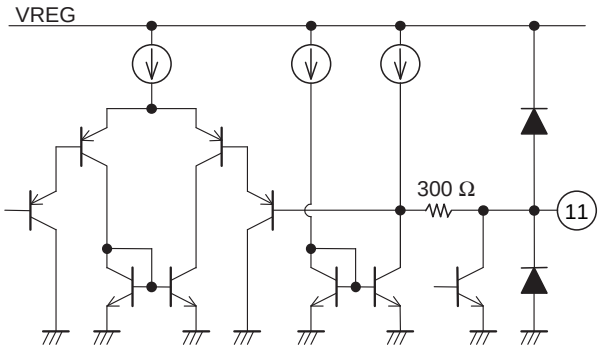
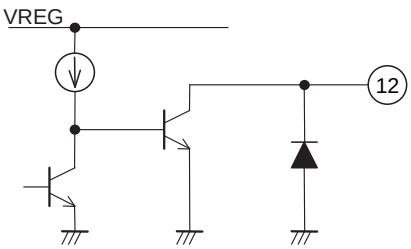
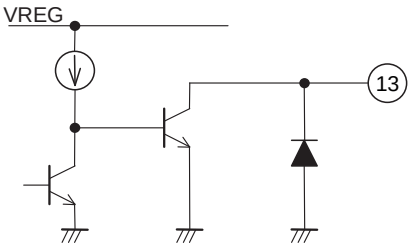
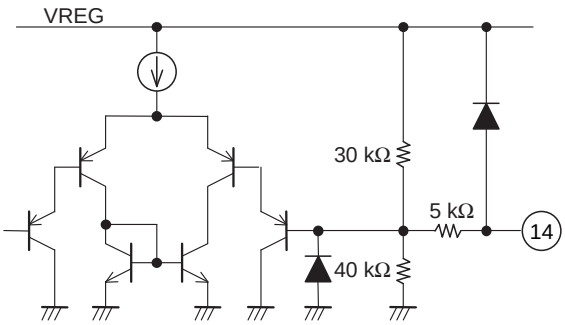
Pin No.	Pin Name	Pin Description	Equivalent circuit
10	FC	Control loop frequency characteristics correction Insert a capacitor between this pin and ground.	
11	CSD	Sets the operating time constant for the constraint protection circuit.	
12	FG	Hall sensor FG output (This is an open-collector output.)	
13	RD	Motor constraint state detection (This is an open-collector output.) This pin outputs a high level if the motor is mechanically constrained, and it outputs a low level when the motor is turning.	
14	PWM IN	PWM pulse input When low, the outputs are turned on, and when high or open, the outputs are turned off. When these pins are used for control, connect the EI– pin to ground and the EI+ pin to the TOC pin.	

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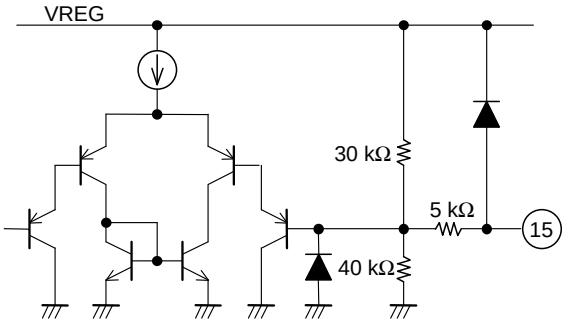
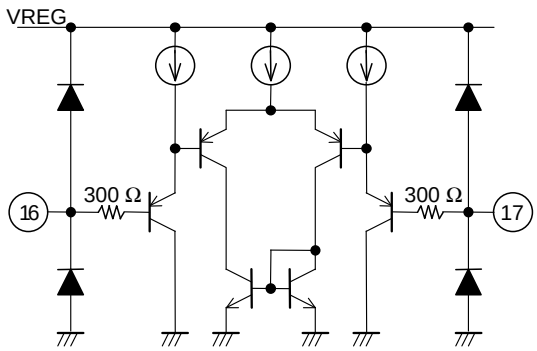
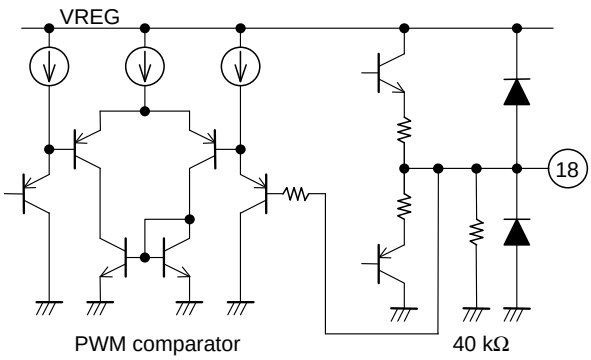
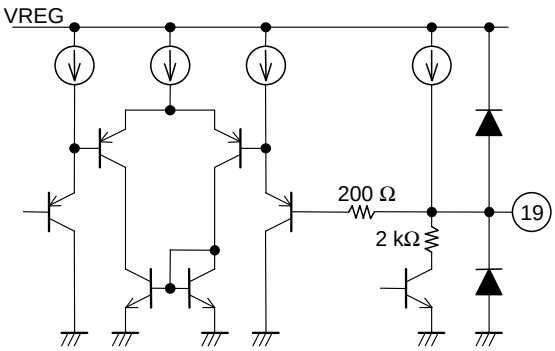
Pin No.	Pin Name	Pin Description	Equivalent circuit
15	S/S	Motor start/stop control A low level selects start mode, and a high level or open selects stop mode.	
16 17	EI+ EI–	Control amplifier noninverting input Control amplifier inverting input	
18	TOC	PWM waveform comparison (Control amplifier output)	
19	PWM	Sets the PWM oscillator frequency. Insert a capacitor between this pin and ground. A value of C = 2200 pF sets the frequency to be about 20 kHz.	

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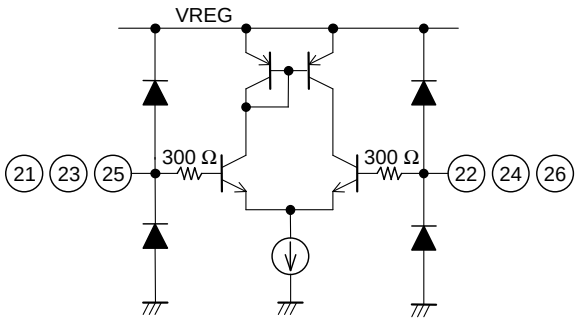
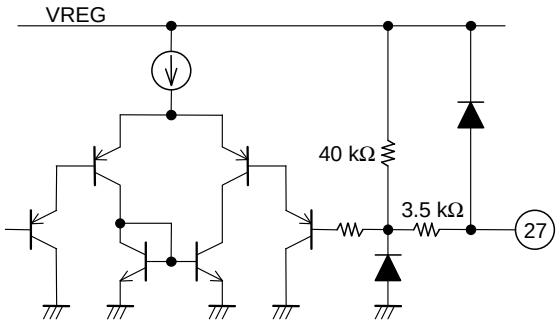
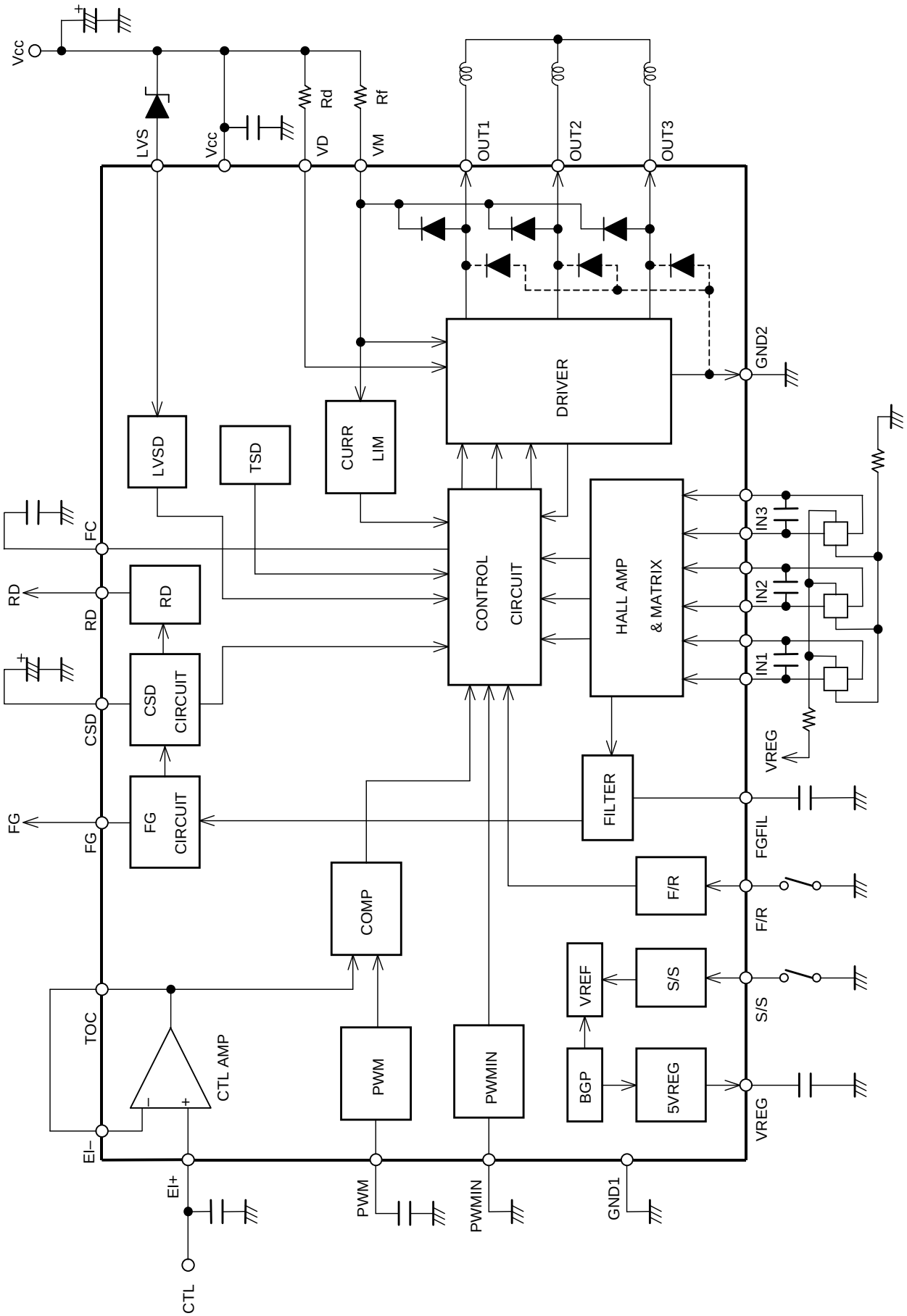
Pin No.	Pin Name	Pin Description	Equivalent circuit
20	GND1	Ground for systems other than the motor drive output	
22 21 24 23 26 25	IN1+ IN1– IN2+ IN2– IN3+ IN3–	Hall-effect sensor inputs When IN+ > IN–, the input is seen as a high level, and when the reverse condition is true, it is seen as a low level. An amplitude of over 50 mVp-p (differential) is desirable as the Hall input signal. If noise on the Hall signals is a problem, insert capacitors between the IN+ and IN- inputs.	
27	F/R	Forward/reverse control A low level specifies forward and a high level or open specifies reverse.	

Equivalent Circuit Block Diagram



Functional Description

1. Output Drive Circuit

This IC reduces motor vibration and noise by smoothly switching the output current when switching phases. Since control of the change (slope) in the output current during phase switching uses the slope of the Hall sensor input waveform, if the slope of the Hall sensor input waveform is too steep, the changes in the output current during phase switching will also be too steep. This will reduce the noise and vibration minimizing effect of this design. Thus care is required with regard to the slope of the Hall sensor input waveform.

Motor speed control is implemented by PWM switching of the low side output transistor. The drive output is adjusted by changing the duty. The LB11693 includes the diode between OUT and VM used for the regenerative current when the PWM signal is off.

When the slope (amplitude) of the Hall sensor input waveform is large, if the circuit is used with a large current, the parasitic diode between OUT and ground will operate due to the low side kickback during phase switching. If waveform disruptions or other problems occur, add an external rectifying diode or Schottky diode between OUT and ground.

2. Power Supply Stabilization

Since this IC uses a PWM switching technique, the power supply line level can be disturbed easily. Electrolytic capacitors with adequate capacitance to stabilize the power supply lines must be inserted between V_{CC} and ground. The power supply lines will be especially subject to disturbance if diodes are inserted in the power supply lines to prevent damage if the power supply is connected with reversed polarity. Here, even larger capacitances should be used. The connected electrolytic capacitors must be placed as close to the IC pins (V_{CC}, VM, and the two ground pins) as possible. If the heat sink or some other obstacle prevents the electrolytic capacitors from being connected close to the IC, ceramic capacitors with a capacitance of about 0.1 μF must be connected near the pins.

3. VREG Pin

The VREG pin is both the 5 V regulator output and the power supply for the IC's internal control circuits. Therefore, a capacitor with a capacitance of at least 0.1 μF must be connected between VREG and ground. The ground side of the connected capacitor must be connected to the GND1 pin with a line that is as short as possible.

4. FC Pin

The capacitor connected to the FC pin is required to correct the control loop frequency characteristics. (Use a value of about 0.1 μF.)

5. VD Pin

The VD pin supplies the low side output transistor drive current (about 0.1 A, maximum).

The IC internal power consumption can be suppressed by connecting a resistor between the V_{CC} and VD pins to divide the power consumption due to the low side transistor drive current. The IC internal power consumption due to the drive current can be made smaller to the extent the VD pin voltage is lowered. However, a voltage of 4 V or higher must be assured for the VD pin voltage. When used with V_{CC} = 24 V, insert a resistor of between 50 Ω (0.5 W) and 100 Ω (1 W) between the V_{CC} and VD pins.

6. Hall Input Signals

A signal input with an amplitude (differential) of 50 mVp-p or higher is required for the Hall inputs. If disturbances in the output waveform occur due to noise, capacitors must be connected across the Hall input pins (the + and – sides).

7. Current Limiter Circuit

The current limiter circuit limits the output current peak value to a level determined by the equation I = VRF/Rf (VRF = 0.5 V typical, Rf: current detection resistor). This circuit limits the current by controlling the low side output transistor PWM at the PWM frequency determined by the PWM pin external capacitor. In particular, it reduces the on duty of the PWM signal.

8. Forward/Reverse Direction Switching

This IC is designed with the assumption that the motor direction (forward or reverse) will not be switched while the motor is turning. We recommend operating this IC with the F/R pin held fixed at either the low or high level. When this pin is left open, the internal pull-up resistor (about 40 kΩ) will set the pin to the high level. However, if there are large fluctuations in signal levels in the circuit, this pull-up resistor should be strengthened by adding an external resistor.

If a direction switching operation is performed while the motor is turning, large currents will flow due to the braking operation. However, this IC's current limiter circuit cannot limit these braking currents. Thus direction switching is only

possible if the braking current is limited to be under Iomax (1.8 A) by the motor coil resistance or other factors. Also, since a transient through current will flow at the instant the direction is switched if the direction switching operation is performed just from the F/R pin, a period where drive is turned off must be provided when switching directions. Through currents must be prevented by setting the IC to the stop state with the S/S pin or TOC pin to provide a drive off period where the duty due to the PWMIN pin is set to 0% and switching the F/R pin during that period.

9. Power Saving Circuit

This IC goes to a low-power mode (power saving state) when set to the stop state with the S/S pin. In the power saving state, the bias currents in most of the circuits are cut off. However, the 5 V regulator output is still provided in the power saving state.

10. Notes on the PWM Frequency

The PWM frequency is determined by the capacitor C (F) connected to the PWM pin.

$$f_{PWM} \approx 1/(23400 \times C)$$

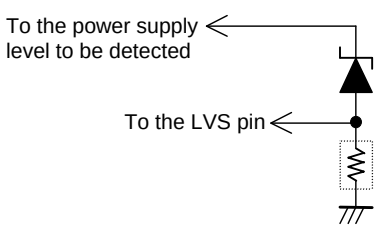
It is preferable to use a frequency in the range 15 kHz to 25 kHz for the PWM frequency. The connected capacitor must be connected to the GND1 pin with a line as short as possible.

11. Control Methods

The output duty can be controlled by either of the following methods

- Control based on comparing the TOC pin voltage to the PWM oscillator waveform
  The low side output transistor duty is determined according to the result of comparing the TOC pin voltage to the PWM oscillator waveform. When the TOC pin voltage is 1.3 V or lower, the duty will be 0%, and when it is 3.0 V or higher, the duty will be 100%.
  Since the TOC pin is the output of the control amplifier (CTL), a control voltage cannot be directly input to the TOC pin. Normally, the control amplifier is used as a full feedback amplifier (with the EI– pin connected to the TOC pin) and a DC voltage is input to the EI+ pin (the EI+ pin voltage will become equal to the TOC pin voltage). When the EI+ pin voltage becomes higher, the output duty increases. Since the motor will be driven when the EI+ pin is in the open state, a pull-down resistor must be connected to the EI+ pin if the motor should not operate when EI+ is open.
  When TOC pin voltage control is used, a low-level input must be applied to the PWMIN pin or that pin connected to ground.
- Control based on a pulse signal input to the PWMIN pin
  A pulse signal with a frequency in the range 15 to 25 kHz can be input to the PWMIN pin, and the duty of the low side output transistor can be controlled based on the duty of that input signal. Note that the output is on when a low level is input to the PWMIN pin, and off when a high level is input. When the PWMIN pin is open it goes to the high level input and the output is be turned off.
  When controlling motor operation from the PWMIN pin, the EI– pin must be connected to ground, and the EI+ pin must be connected to the TOC pin.

12. Undervoltage Protection Circuit



The undervoltage protection circuit turns the low side output transistor off when the LVS pin voltage falls below the minimum operation voltage (about 3.8 V). The operating voltage detection level is set up for 5 V systems. The detected voltage level can be increased by shifting the voltage by inserting a zener diode in series with the LVS pin. The LVS influx current during detection is about 65 μA. To minimize the effect of sample-to-sample variations in the zener voltage, the current flowing in the zener diode must be increased thus stabilizing the rise in the zener diode voltage. If this is required, insert a resistor between the LVS pin and ground.
If the LVS pin is left open, the internal pull-down resistor will result in the IC seeing a ground level input, and the output will be turned off. Therefore, a voltage in excess of the LVS circuit clear voltage (about 4.3 V) must be applied to the LVS pin if the application does not use the undervoltage protection circuit. The maximum rating for the LVS pin applied voltage is 30 V.

13. Constraint Protection Circuit

When the motor is physically constrained (held stopped), the CSD pin external capacitor is charged (to about 3.0 V) by a constant current of about 2.4 μA and is then discharged (to about 1.0 V) by a constant current of about 0.17 μA. This process is repeated, generating a sawtooth waveform. The constraint protection circuit turns motor drive (the low side

output transistor) on and off repeatedly based on this sawtooth waveform. Motor drive is on during the period the CSD pin external capacitor is being charged from about 1.0 V to about 3.0 V, and motor drive is off during the period the CSD pin external capacitor is being discharged from about 3.0 V to about 1.0 V. The IC and the motor are protected by this repeated drive on/off operation when the motor is physically constrained. When a 0.47 µF capacitor is connected to the CSD pin, this repeated operation will turn motor drive on for about 0.4 seconds and off for about 5.5 seconds.

When the motor is turning, the CSD pin is held at a certain fixed voltage (which varies depending on the motor speed) by the CSD pin external capacitor being charged and discharged by two processes. One is the constant current (about 2.4 µA) charge current, and the other is a roughly 10 µs discharge pulse generated internal in the IC when the Hall sensor input IN1 changes state (on rising and falling edges on the FG output).

Since the Hall sensor input IN1 does not change state when the motor is not turning, discharge pulses are not generated, and the CSD pin external capacitor is charged by the approximately 2.4 µA constant current until it reaches about 3.0 V. At that point, the constraint protection circuit operates. The constraint protection state is cleared if the motor constraint is released.

When the motor turns at an extremely low rate, the CSD pin voltage during this motor rotation will be held at a relatively high voltage, and the constraint protection circuit will operate if this reaches the roughly 3.0 V threshold level. Since the constraint protection circuit may operate if the Hall sensor input IN1 frequency falls below about 10 Hz, care is required when using the constraint protection circuit with a motor that turns slowly.

Connect the CSD pin to ground if the constraint protection circuit is not used.