

DESCRIPTION

The M66257FP is a high-speed line memory with a FIFO (First In First Out) structure of 5120-word × 8-bit double configuration which uses high-performance silicon gate CMOS process technology.

It allows simultaneous output of 1-line delay data and 2-line delay data, and is most suitable for data correction over multiple lines.

It has separate clock, enable and reset signals for write and read, and is most suitable as a buffer memory between devices with different data processing throughput.

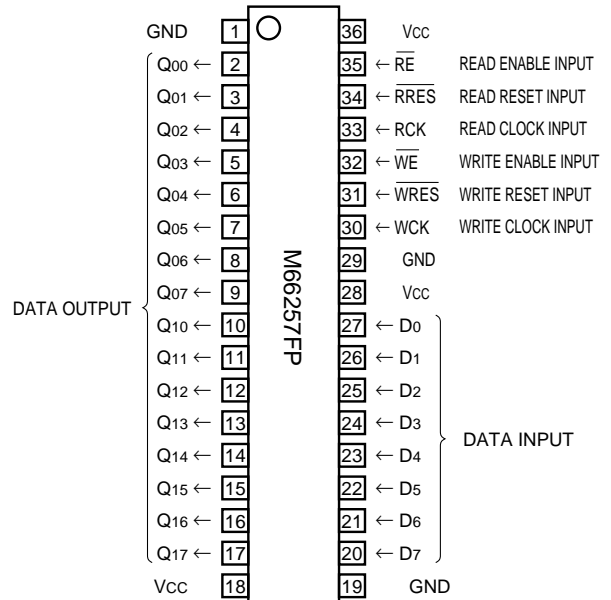
FEATURES

- Memory configuration of 5120 words × 8 bits × 2 (dynamic memory)
- High-speed cycle 25ns (Min.)
- High-speed access 18ns (Max.)
- Output hold 3ns (Min.)
- Fully independent, asynchronous write and read operations
- Output 3 states
- Q00 to Q07 1-line delay
- Q10 to Q17 2-line delay

APPLICATION

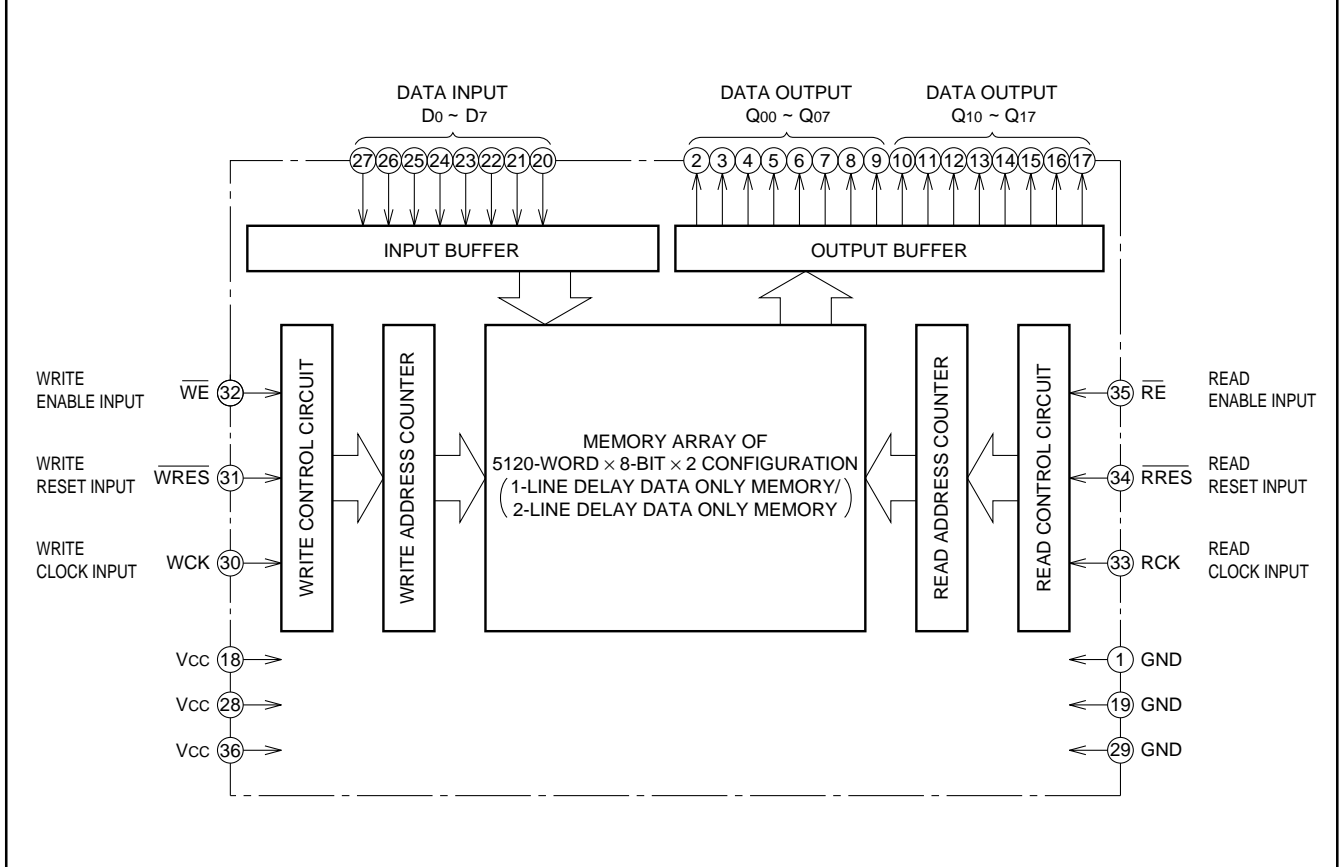
Digital photocopiers, high-speed facsimile, laser beam printers.

PIN CONFIGURATION (TOP VIEW)



Outline 36P2R-A

BLOCK DIAGRAM



FUNCTION

When write enable input \overline{WE} is "L", the contents of data inputs D0 to D7 are written into 1-line delay data only memory in synchronization with rise edge of write clock input WCK. At this time, the write address counter of 1-line delay data only memory is also incremented simultaneously.

The write functions given below are also performed in synchronization with rise edge of WCK.

When \overline{WE} is "H", a write operation to 1-line delay data only memory is inhibited and the write address counter of 1-line delay data only memory is stopped.

When write reset input \overline{WRES} is "L", the write address counter of 1-line delay data only memory is initialized.

When read enable input \overline{RE} is "L", the contents of 1-line delay data only memory are output to data outputs Q00 to Q07 and those of 2-line delay data only memory to data outputs Q10 to Q17 in synchronization with the rise of read clock input RCK. At this time, the read address counters of 1-line and 2-line delay data only memories is also incremented simultaneously.

Moreover, data of Q00 to Q07 are written into 2-line delay data only memory in synchronization with rise edge of RCK. At this time, the write address of 2-line delay data only memory is incremented.

The read functions given below are also performed in synchronization with rise edge of RCK.

When \overline{RE} is "H", a read operation from both of 1-line delay data only memory and 2-line delay data only memory is inhibited and the read address counter of each memory is stopped. The outputs of Q00 to Q07 and Q10 to Q17 are in the high impedance state.

Moreover, a write operation to 2-line delay data only memory is inhibited and the write address counter of 2-line delay data only memory is stopped.

When read reset input \overline{RRES} is "L", the read address counter of 1-line delay data only memory, and the write address counter and read address counter of 2-line delay data only memory are initialized.

ABSOLUTE MAXIMUM RATINGS (Ta = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
VCC	Supply voltage	A value based on GND pin	-0.5 ~ +7.0	V
VI	Input voltage		-0.5 ~ VCC + 0.5	V
VO	Output voltage		-0.5 ~ VCC + 0.5	V
Pd	Maximum power dissipation	Ta = 25°C	660	mW
Tstg	Storage temperature		-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
VCC	Supply voltage	4.5	5	5.5	V
GND	Supply voltage		0		V
Topr	Operating ambient temperature	0		70	°C

ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 70°C, VCC = 5V ± 10%, GND = 0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min.	Typ.	Max.		
VIH	"H" input voltage		2.0			V	
VIL	"L" input voltage				0.8	V	
VOH	"H" output voltage	IOH = -4mA	VCC-0.8			V	
VOL	"L" output voltage	IOL = 4mA			0.55	V	
IiH	"H" input current	VI = VCC	WE, WRES, WCK, RE, RRES, RCK, Do ~ D7			1.0	μA
IiL	"L" input current	VI = GND	WE, WRES, WCK, RE, RRES, RCK, Do ~ D7			-1.0	μA
IoZH	Off state "H" output current	VO = VCC			5.0	μA	
IoZL	Off state "L" output current	VO = GND			-5.0	μA	
Icc	Operating mean current dissipation	VI = VCC, GND, Output open twCK, tRCK = 25ns			120	mA	
CI	Input capacitance	f = 1MHz			10	pF	
Co	Off state output capacitance	f = 1MHz			15	pF	

SWITCHING CHARACTERISTICS (Ta = 0 ~ 70°C, Vcc = 5V ± 10%, GND = 0V, unless otherwise noted)

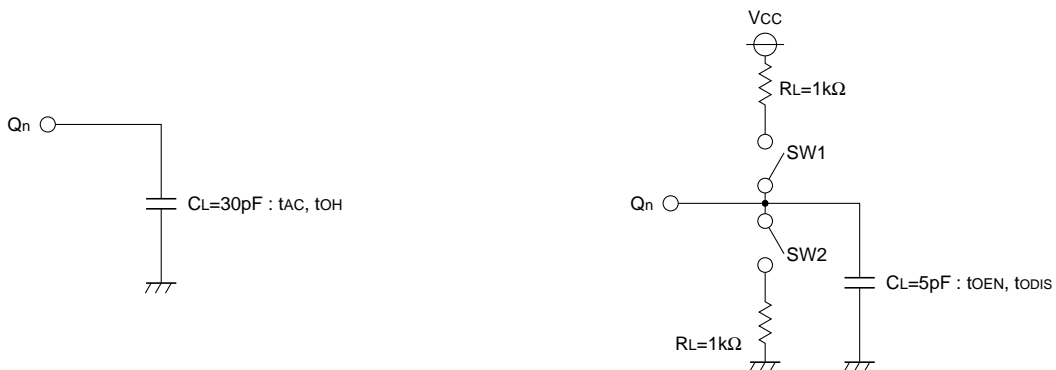
Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tAC	Access time			18	ns
tOH	Output hold time	3			ns
tOEN	Output enable time	3		18	ns
tODIS	Output disable time	3		18	ns

TIMING CONDITIONS (Ta = 0 ~ 70°C, Vcc = 5V ± 10%, GND = 0V, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tWCK	Write clock (WCK) cycle	25			ns
tWCKH	Write clock (WCK) "H" pulse width	11			ns
tWCKL	Write clock (WCK) "L" pulse width	11			ns
tRCK	Read clock (RCK) cycle	25			ns
tRCKH	Read clock (RCK) "H" pulse width	11			ns
tRCKL	Read clock (RCK) "L" pulse width	11			ns
tDS	Input data setup time to WCK	7			ns
tDH	Input data hold time to WCK	3			ns
tRESS	Reset setup time to WCK or RCK	7			ns
tRESH	Reset hold time to WCK or RCK	3			ns
tNRESS	Reset nonselect setup time to WCK or RCK	7			ns
tNRESH	Reset nonselect hold time to WCK or RCK	3			ns
tWES	WE setup time to WCK	7			ns
tWEH	WE hold time to WCK	3			ns
tNWES	WE nonselect setup time to WCK	7			ns
tNWEH	WE nonselect hold time to WCK	3			ns
tRES	RE setup time to RCK	7			ns
tREH	RE hold time to RCK	3			ns
tNRES	RE nonselect setup time to RCK	7			ns
tNREH	RE nonselect hold time to RCK	3			ns
tr, tf	Input pulse rise/fall time			20	ns
tH	Data hold time (Note 1)			20	ms

Note 1: For 1-line access, the following should be satisfied:
 WE "H" level period < 20ms – 5120 twck – WRES "L" level period
 RE "H" level period < 20ms – 5120 trck – RRES "L" level period
 2: Reset the IC after power is turned on.

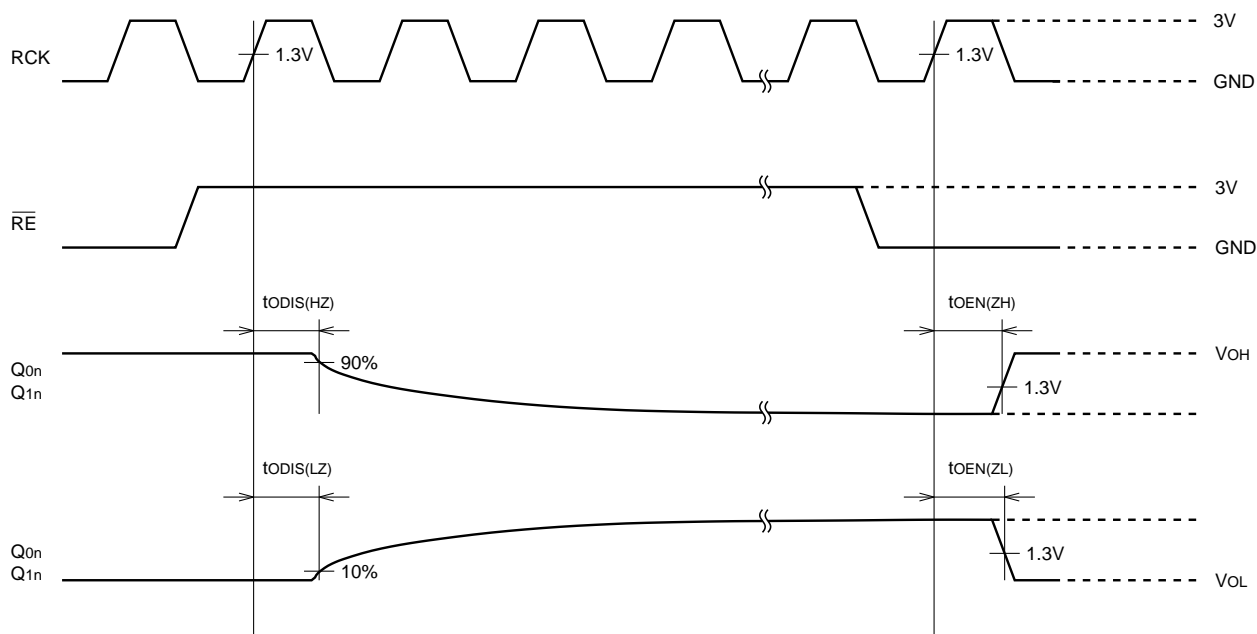
TEST CIRCUIT



Input pulse level : 0 ~ 3V
 Input pulse rise/fall time : 3ns
 Decision voltage input : 1.3V
 Decision voltage output : 1.3V (However, $t_{ODIS(LZ)}$ is 10% of output amplitude and $t_{ODIS(HZ)}$ is 90% of that for decision).
 The load capacitance C_L includes the floating capacitance of connection and the input capacitance of probe.

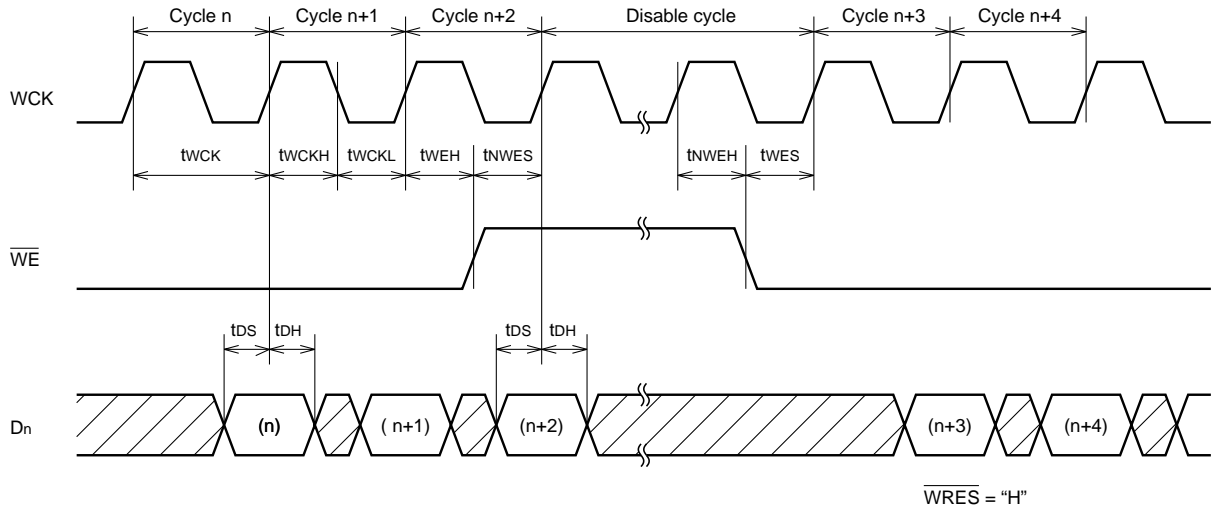
Parameter	SW1	SW2
$t_{ODIS(LZ)}$	Closed	Open
$t_{ODIS(HZ)}$	Open	Closed
$t_{OEN(ZL)}$	Closed	Open
$t_{OEN(ZH)}$	Open	Closed

t_{ODIS}/t_{OEN} TEST CONDITION

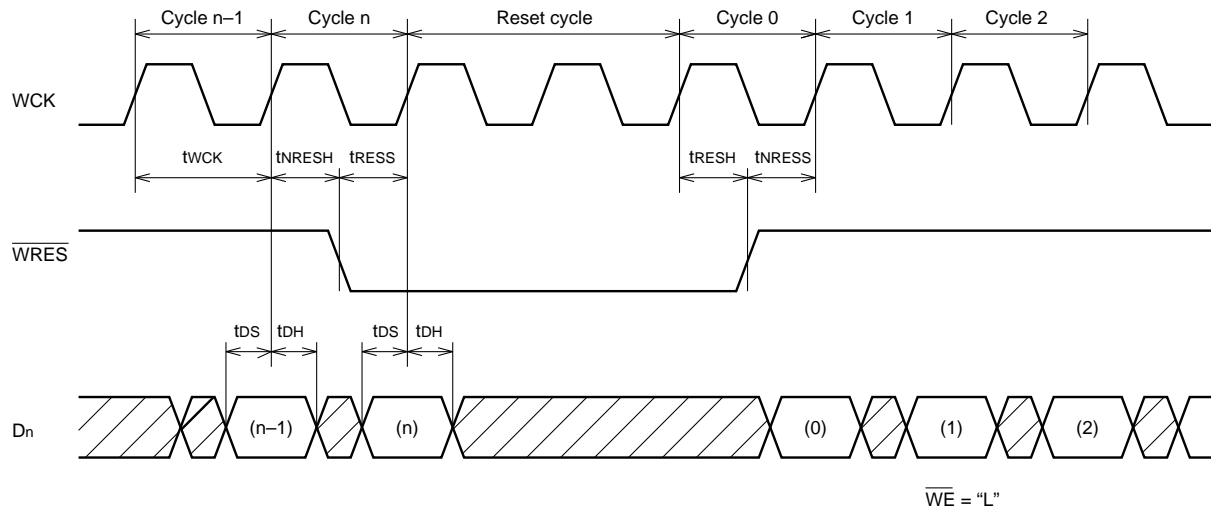


OPERATING TIMING

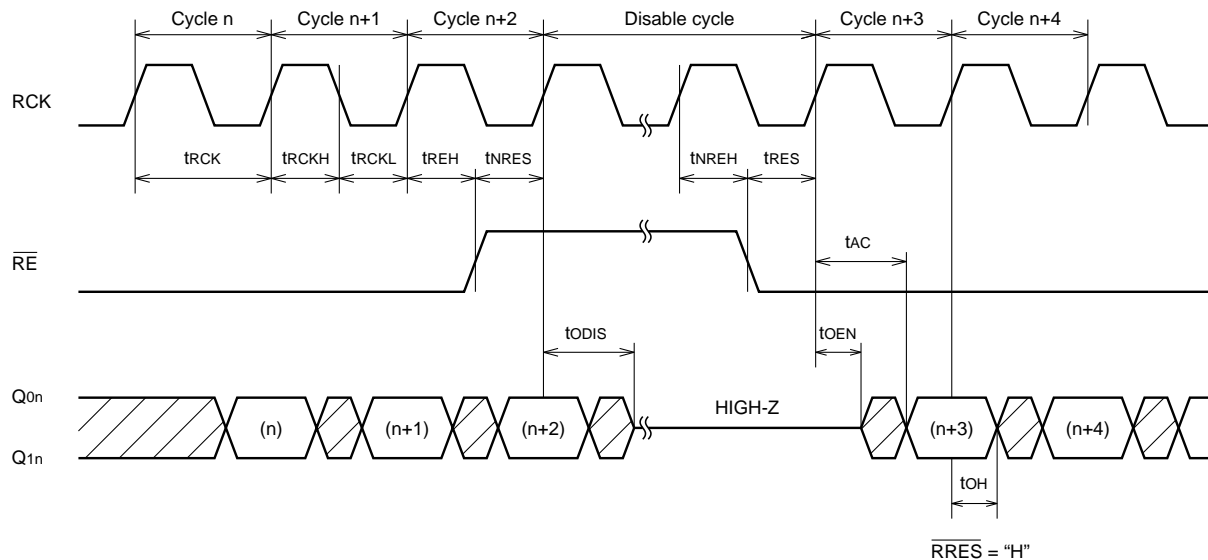
• Write cycle



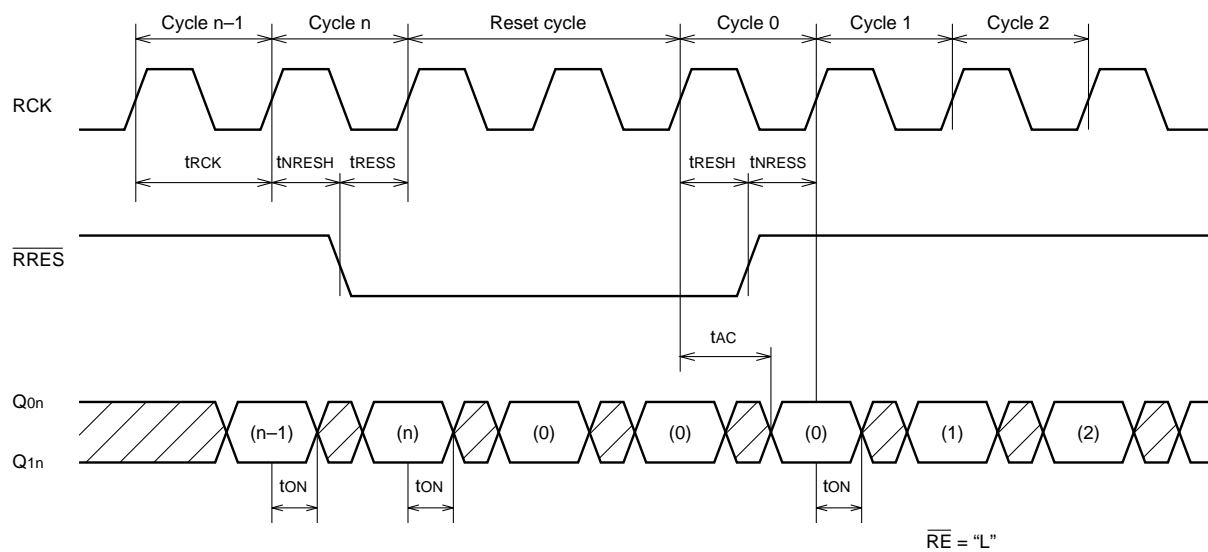
• Write reset cycle



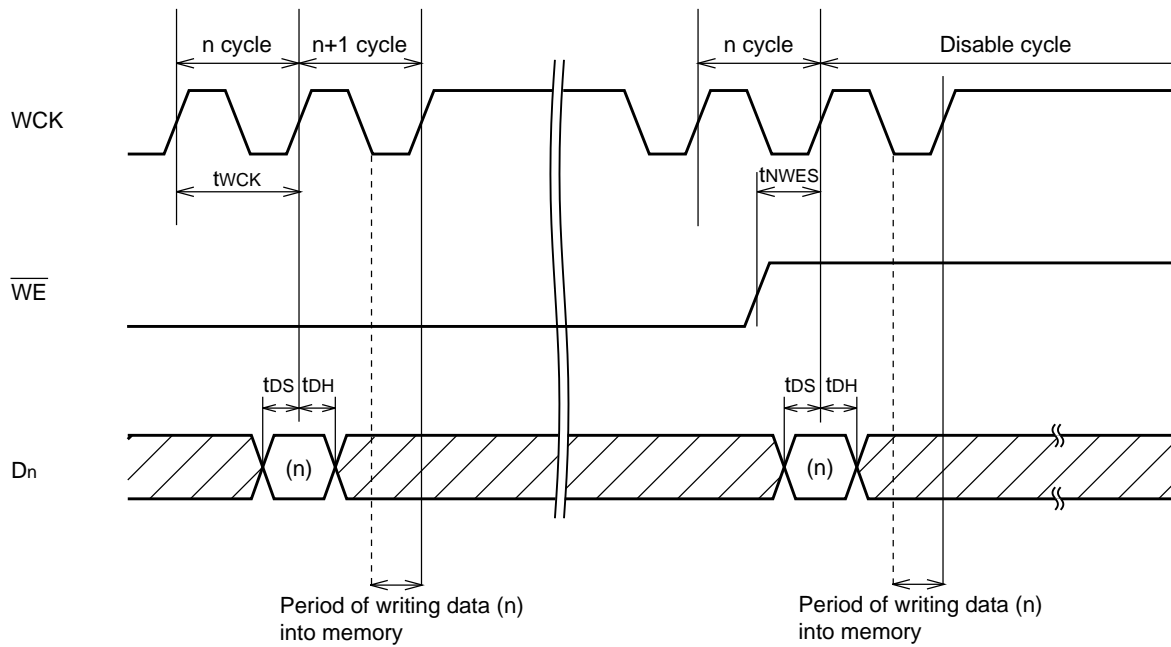
• Read cycle



• Read reset cycle



- Note at WCK stop



$\overline{WRES} = \text{“H”}$

Input data D_n of n cycle is read at the rising edge after WCK of n cycle. Writing operation starts in the “L” period of WCK of $n+1$ cycle and ends at the rising edge after $n+1$ cycle.

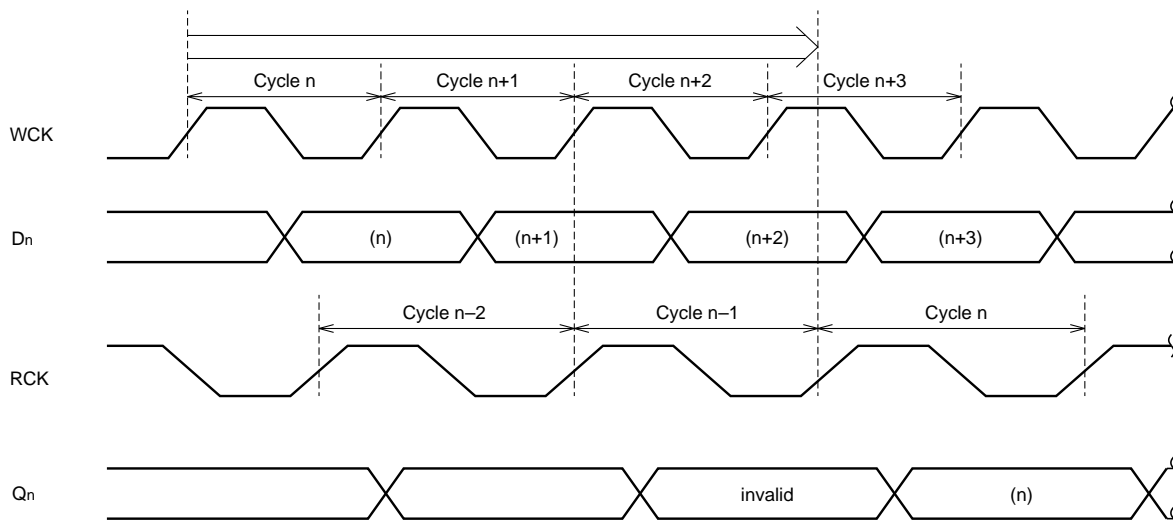
To stop reading write data at n cycle, input WCK for up to the rising edge of $n+1$ cycle.

When the cycle next to n cycle is a disable cycle, input of WCK for a cycle is required after a disable cycle as well.

• Shortest read of data “n” written in cycle n

Cycle n-1 on read side should be started after end of cycle n+1 on write side

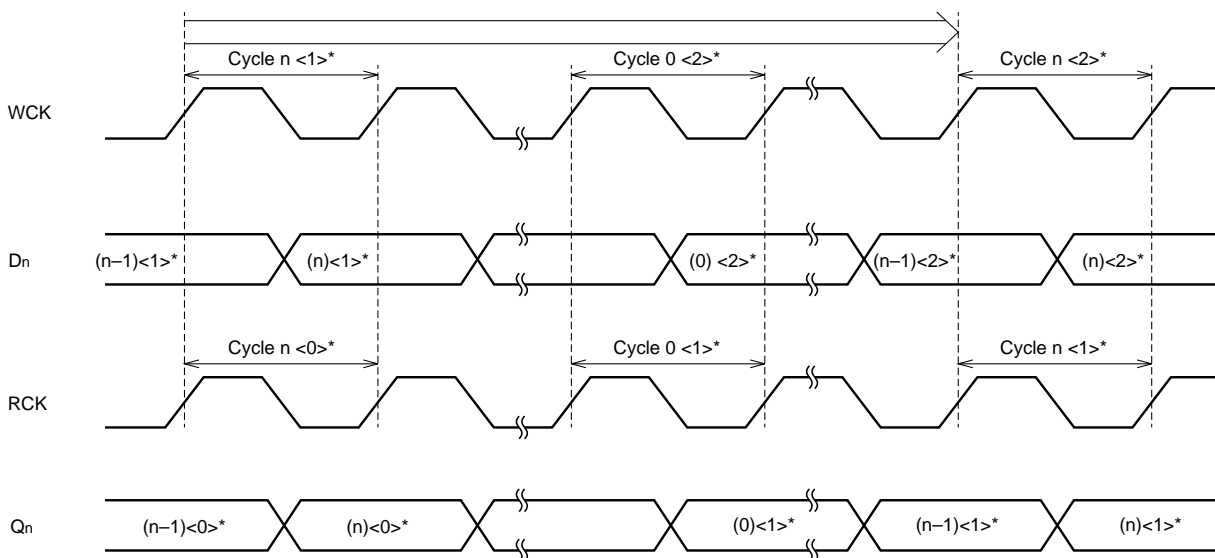
When the start of cycle n-1 on read side is earlier than the end of cycle n+1 on write side, output Q_n of cycle n becomes invalid. In the figure shown below, the read of cycle n-1 is invalid.



• Longest read of data “n” written in cycle n: 1-line delay

Cycle n <1>* on read side should be started when cycle n <2>* on write is started

Output Q_n of n cycle <1>* can be read until the start of reading side n cycle <1> and the start of writing side n cycle <2>* overlap each other.



<0>*, <1>* and <2>* indicates a line value.

APPLICATION EXAMPLE

Laplacian Filter Circuit for Correction of Resolution in the Secondary Scanning Direction.

