Standard e5550-Compatible OTP Identification IC

Description

The T5556 is a contactless OTP (one-time programmable)-**ID**entification **IC** (IDIC®)* for applications in the 125 kHz range. A single coil, connected to the chip, serves as the IC's power supply and bidirectional communication interface.

The on-chip 256-bit OTP memory (8 × 32 bit blocks) can be contactless programmed once through a base station. After configuration and locking, the T5556 operates as R/O tag. One block is reserved for setting the operation modes of the IC.

Reading occurs by damping the coil by an internal load. There are different bitrates and encoding schemes possible. Programming occurs by interrupting the RF field in a special way.

Features

- Low-power, low-voltage operation
- Contactless power supply
- Contactless read/write data transmission
- **R**adio **F**requency (RF): 100 kHz to 150 kHz
- 256 bit OTP memory in 8 blocks of 32 bits
- 224 bits of user data in 7 blocks of 32 bits
- Extensive protection against contactless malprogramming of the OTP memory
- 50 ms to write and verify a block during setup and configuration
- Configuration options:
  Bitrate [bit/s]: RF/8, RF/16, RF/32, RF/40
  RF/50, RF/64, RF/100, RF/128
  Modulation: NRZ, FSK, PSK, Manchester,
  Biphase
  Other: Terminator modes (BT, ST)

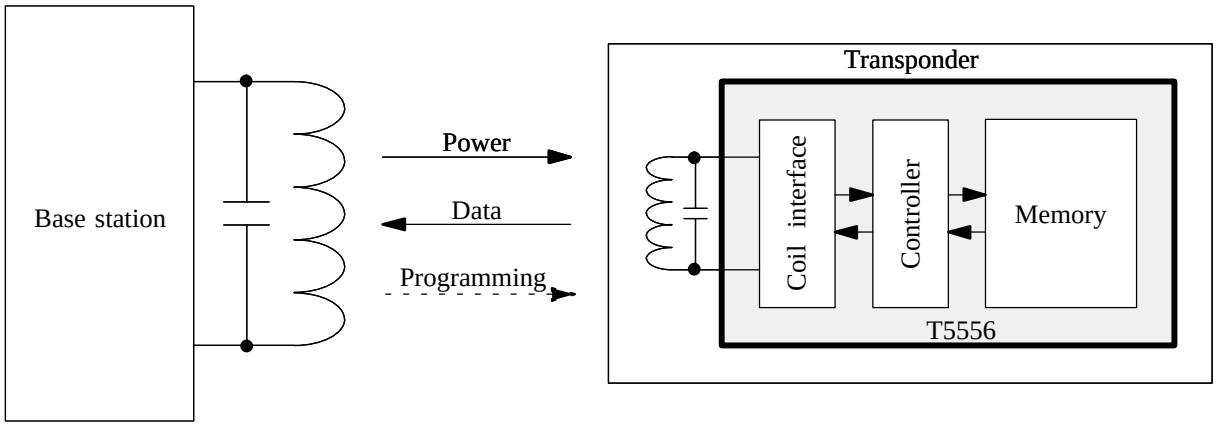


Figure 1. RFID system using T5556 tag

Ordering Information

Extended Type Number	Package	Remarks
T5556A-DOW	DOW	Configuration after production test is an erased memory ('0')

* IDIC® stands for IDentification Integrated Circuit and is a trademark of TEMIC Semiconductors

T5556 Building Blocks

Analog Front End (AFE)

The AFE includes all circuits which are directly connected to the coil. It generates the IC's power supply and handles the bidirectional data communication with the reader unit. It consists of the following blocks:

- Rectifier to generate a dc supply voltage from the ac coil voltage
- Clock extractor
- Switchable load between Coil1/ Coil2 for data transmission from the IC to the reader unit (read)
- Field gap detector for data transmission from the reader unit into the IC (write)

Controller

The main controller has following functions:

- Load mode register with configuration data from block 0 after power-on and also during reading
- Handle write data transmission and the write error modes during programming
- The first two bits of the write data stream are the OP-code ('10').

Bitrate Generator

The bitrate generator can deliver the following bitrates:
RF/8 - RF/16 - RF/32 - RF/40 - RF/50 - RF/64 - RF/100 - RF/128

Write Decoder

Decode the detected gaps during writing. Check if write data stream is valid.

Write decoder is disabled when the OTP bit is set.

Test Logic

Test circuitry allows rapid verification of the IC during test.

HV Generator

On-chip voltage pump for programming of the OTP memory.

Pad Layout

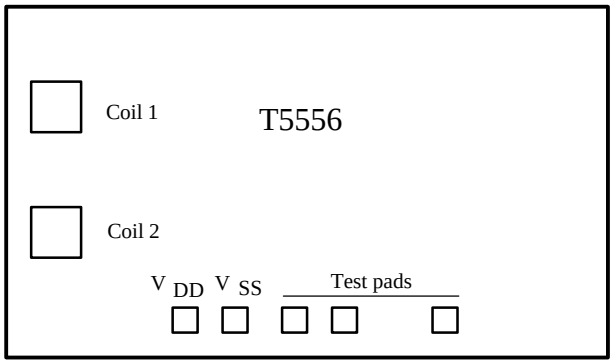


Figure 2. Pad layout

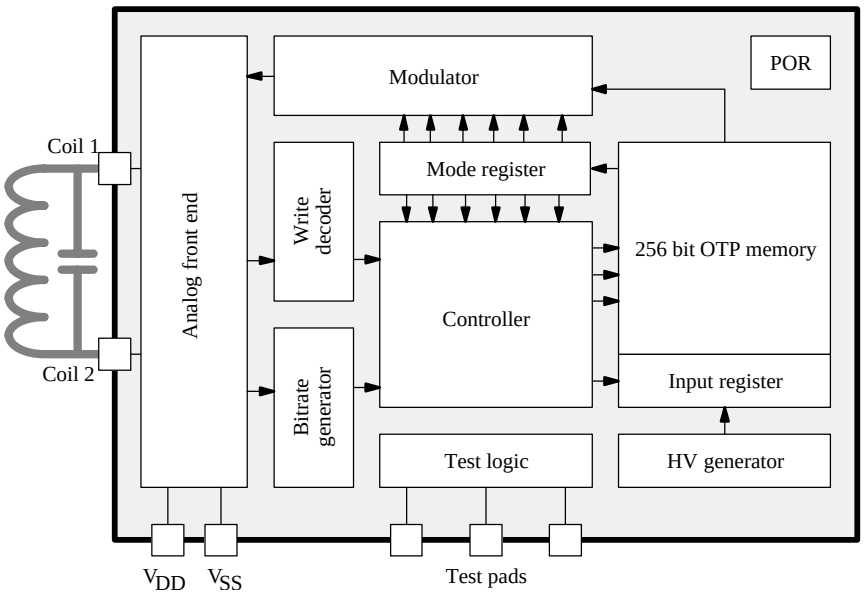


Figure 3. Block diagram T5556

Power-On Reset (POR)

The power-on reset is a delay reset which is triggered when supply voltage is applied.

Mode Register

The mode register stores the mode data from memory block 0. It is continually refreshed at the start of every block. This increases the reliability of the device (if the originally loaded mode information is false, it will be corrected by subsequent refresh cycles).

Modulator

The modulator consists of several data encoders in two stages, which may be freely combined to obtain the desired modulation. The basic types of modulation are:

- PSK: phase shift: 1) every change; 2) every '1'; 3) every rising edge (carrier: fc/2, fc/4 or fc/8)
- FSK: 1) f1 = rf/8 f2 = rf/5; 2) f1 = rf/8, f2 = rf/10
- Manchester: rising edge = H; falling edge = L
- Biphase: every bit creates a change, a data 'H' creates an additional mid-bit change

Note: The following modulation type combinations will not work:

- Stage1 Manchester or Biphase, stage2 PSK2, at any PSK carrier frequency (because the first stage output frequency is higher than the second stage strobe frequency)
- Stage1 Manchester or Biphase and stage2 PSK with bitrate = rf/8 and PSK carrier frequency = rf/8 (for the same reason as above)
- Any stage1 option with any PSK for bitrates rf/50 or rf/100 if the PSK carrier frequency is not an integer multiple of the bitrate (e.g., br = rf/50, PSKcf = rf/4, because 50/4 = 12.5). This is because the PSK carrier frequency must maintain constant phase with respect to the bit clock.

Memory

The memory of the T5556 is a 264 bit OTP memory, which is arranged in 8 blocks of 33 bits each. All 33 bits of a block, including the lock bit, are programmed simultaneously. The programming voltage is generated on-chip.

Block 0 contains the mode data, which are not normally transmitted (see figure 6) after configuration.

Block 1 to 7 are programmable with any ID and CRC data.

Bit 0 of every block is the lock bit for that block. Once locked, the block (including the lockbit itself) cannot be modified again during configuration.

Data from the memory is transmitted serially, starting with block 1, bit 1, up to block 'MAXBLK', bit 32. 'MAXBLK' is a mode parameter set during configuration to a value between 1 and 7.

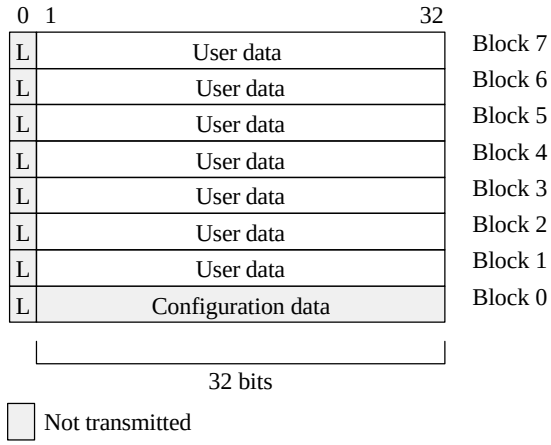


Figure 4. Memory map

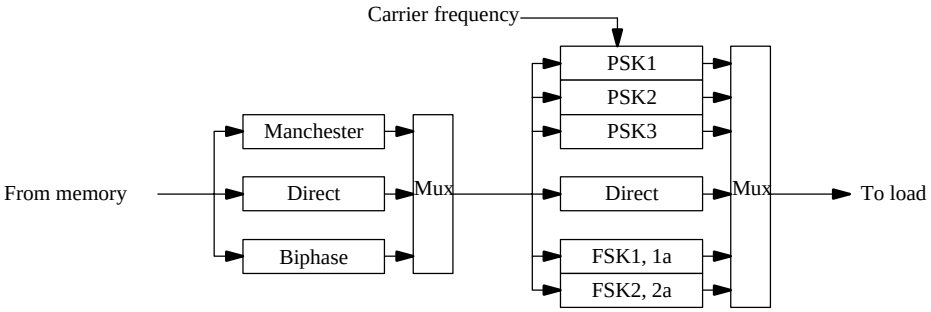
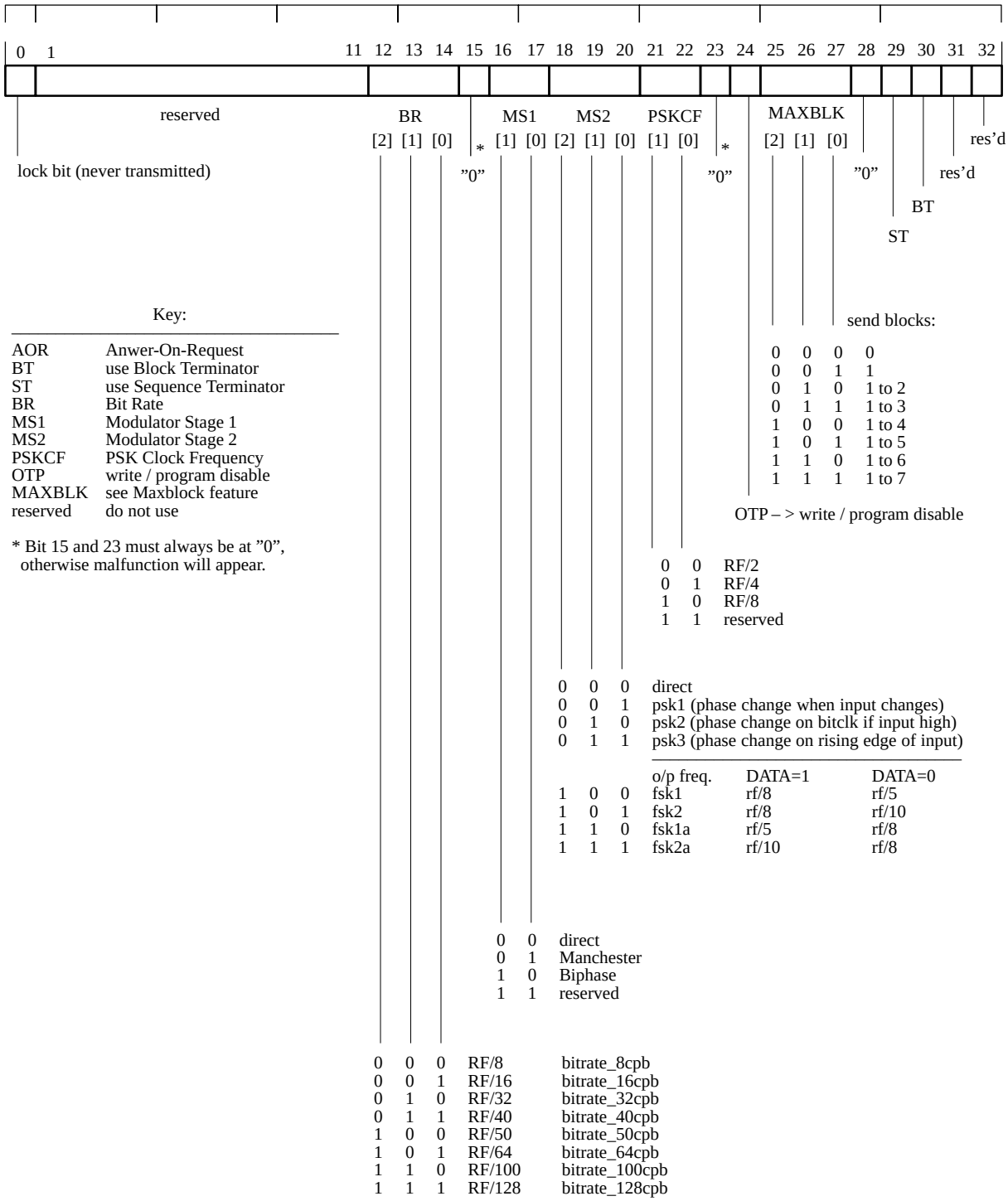


Figure 5. Modulator block diagram



Key:

AOR	Anwer-On-Request
BT	use Block Terminator
ST	use Sequence Terminator
BR	Bit Rate
MS1	Modulator Stage 1
MS2	Modulator Stage 2
PSKCF	PSK Clock Frequency
OTP	write / program disable
MAXBLK	see Maxblock feature
reserved	do not use

* Bit 15 and 23 must always be at "0", otherwise malfunction will appear.

Figure 6. Memory map of block 0

Operating the T5556

General

The basic functions of the T5556 are: **supply** IC from the coil, **read** data from the OTP memory to the reader, contactless programming of data into the IC's. Several **errors** can be detected to protect the memory from being written with the wrong data (see figure 18).

Supply

The T5556 is supplied via a tuned LC circuit which is connected to the Coil 1 and Coil 2 pads. The incoming RF (actually a magnetic field) induces a current into the coil. The on-chip rectifier generates the dc supply voltage (V_{DD}, V_{SS} pads). Overvoltage protection prevents the IC from damage due to high-field strengths. Depending on the coil, the open-circuit voltage across the LC circuit can reach more than 100 V. The first occurrence of RF triggers a power-on reset pulse, ensuring a defined start-up state.

Read

Reading is the mode after power-on reset and OTP memory configuration. It is done by switching a load between the coil pads on and off. This changes the current through the IC coil, which can be detected from the reader unit.

Start-Up

The selected operating mode of the T5556 is activated after the first readout of block 0. The modulation is off while block 0 is read. After this set-up time of 256 field clock periods, modulation with the selected mode starts.

Read Datastream

The first block transmitted is block 1. When the last block is reached, reading restarts with block 1. Block 0 contains the configuration data and is never transmitted. However, the mode register is continuously refreshed with the contents of EEPROM block 0.

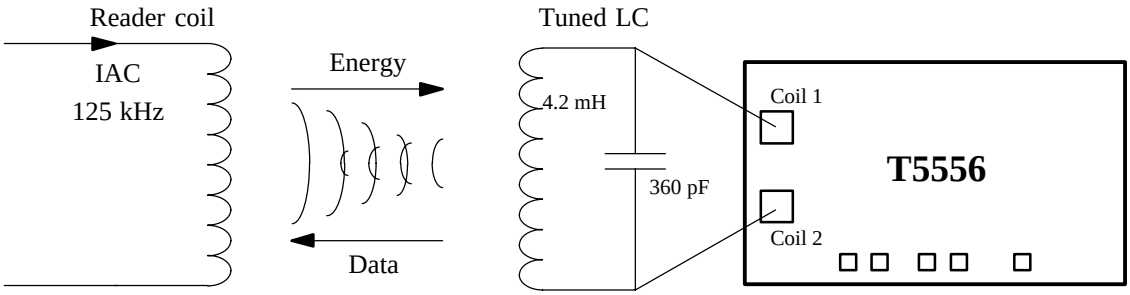


Figure 7. Application circuit

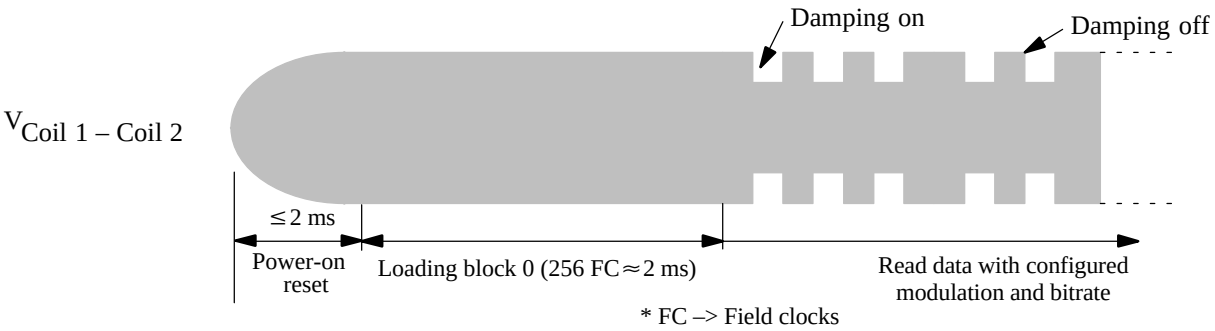


Figure 8. Voltage at Coil1/Coil2 after power-on

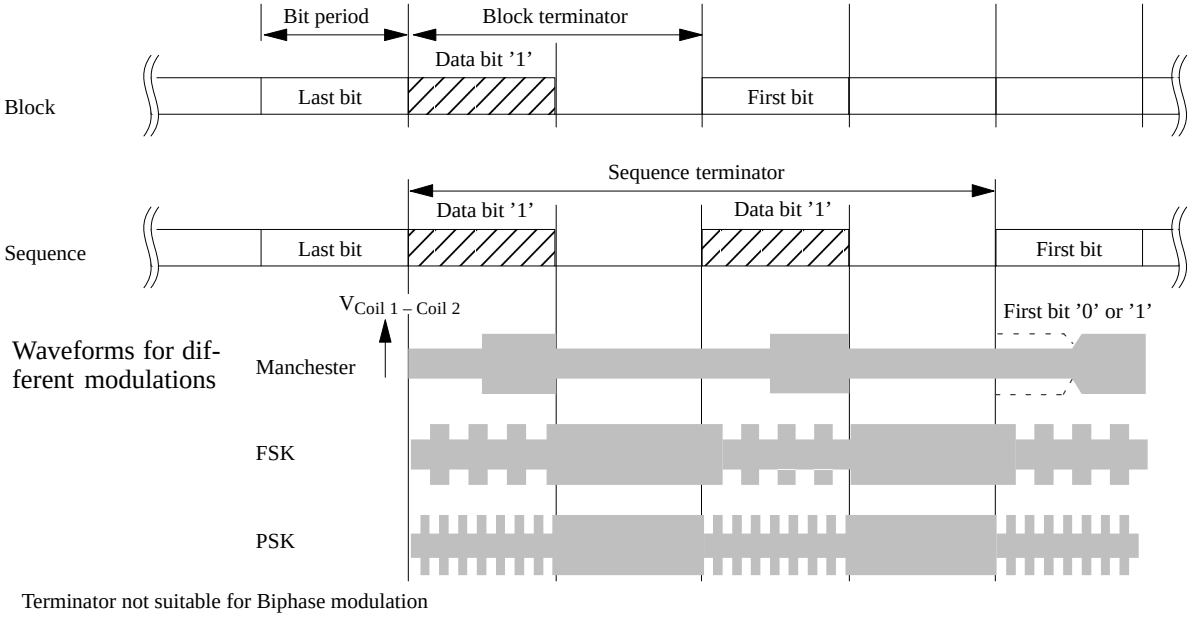


Figure 9. Terminators

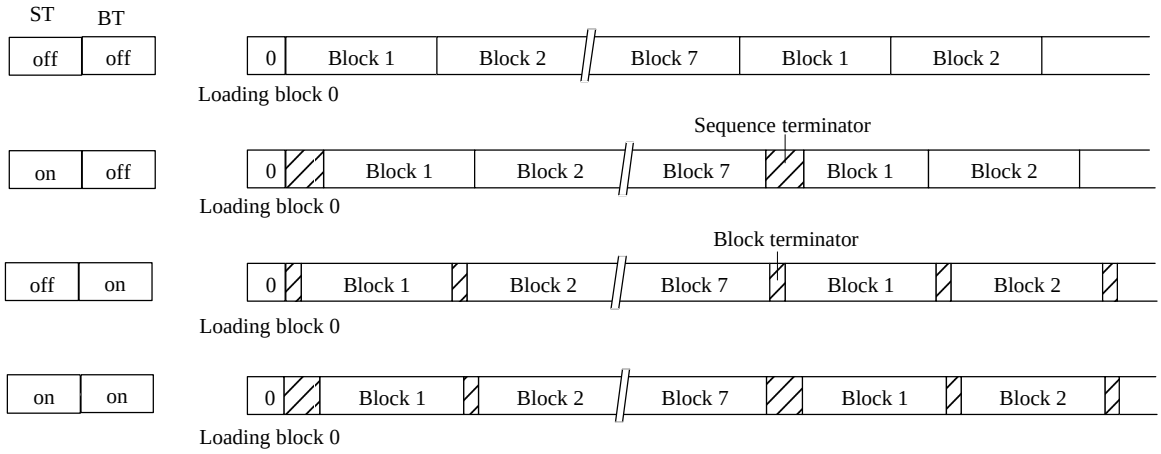


Figure 10. Read data streams and terminators

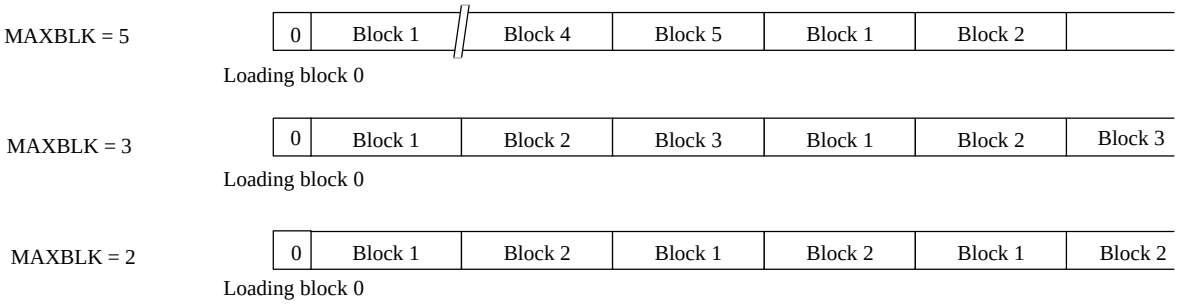


Figure 11. MAXBLK configuration examples

Maxblock Feature

If it is not necessary to read all user data blocks; the MAXBLK field in block 0 is used to limit the number of blocks read. For example, if MAXBLK = 5, the T5556 repeatedly reads and transmits only blocks 1 to 5 (see figure 11).

Terminators

The terminators are (optional selectable) special damping patterns, which may be used to synchronize the reader. There are two types available; a block terminator which precedes every block, and a sequence terminator which always follows the last block.

The sequence terminator consists of two consecutive block terminators. The terminators may be individually enabled with the mode bits ST (sequence terminator enable) or BT (block terminator enable).

Modulation and Bitrate

There are two modulator stages in the T5556 (see figure 4) whose mode can be selected using the appropriate bits in block 0 (MS1[1:0] and MS[2:0]). Also the bitrate can be selected using BR[2:0] in block 0. These options are described in detail in figures 19 through 24.

Configuration

Programming data into the IC occurs via the TEMIC write method. It is based on interrupting the RF field with short gaps. The time between two gaps encodes the '0/1' information to be transmitted.

Start Gap

The first gap is the start gap which triggers write mode. In write mode, the damping is permanently enabled which eases gap detection. The start gap may need to be longer than subsequent gaps in order to be detected reliably.

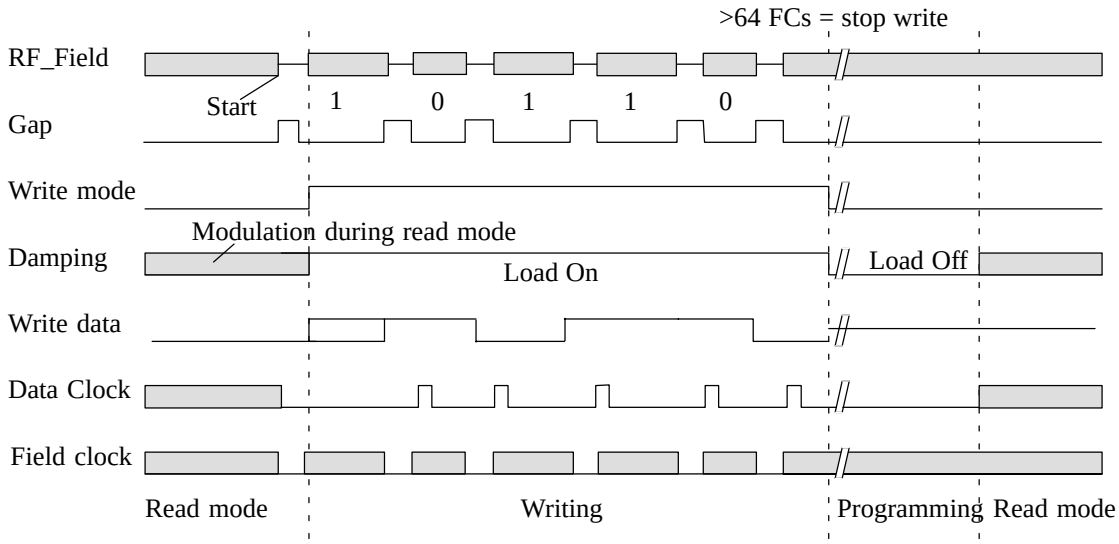


Figure 12. Signals during programming

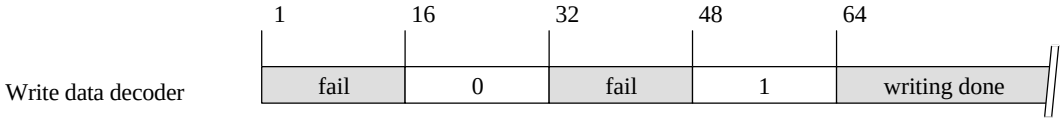


Figure 13. Data coding scheme

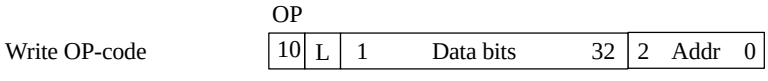


Figure 14. T5556 – OP-code format during configuration

A start gap will be detected at any time after block 0 has been read (field-on plus approximately 2 ms).

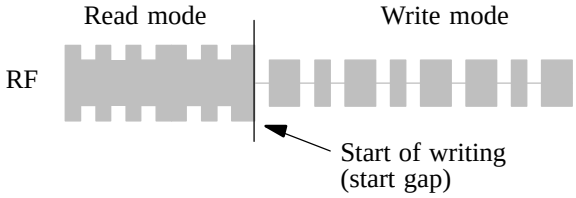


Figure 15. Start of writing

Decoder

The duration of the gaps is usually 50 to 150 µs. The time between two gaps is nominally 24 field clocks for a '0' and 56 field clocks for a '1'. When there is no gap for more than 64 field clocks after previous gap, the T5556 exits write mode; it starts with programming if 38 valid bits were received.

If there is a gap fail – i.e., one or more of the intervals did represent not a valid '0' or '1' – the IC does not program, but enters read mode beginning with block 1, bit 1.

Writing Data into the T5556

The T5556 expects the two bit OP-code first ('10'). If an invalid OP-code is received, the T5556 starts read mode beginning with block 1 after the last gap. The OP-code ('10') is followed by the lock bit, the 32 data bits and the 3-bit block address (see figure 15).

Note: The data bits are read in the same order as written.

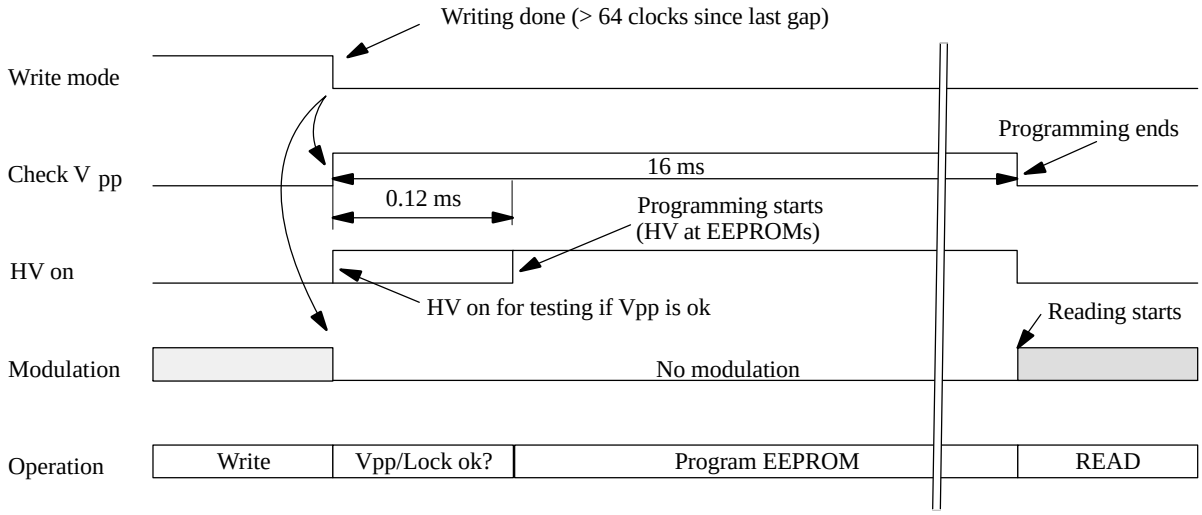


Figure 16. Programming

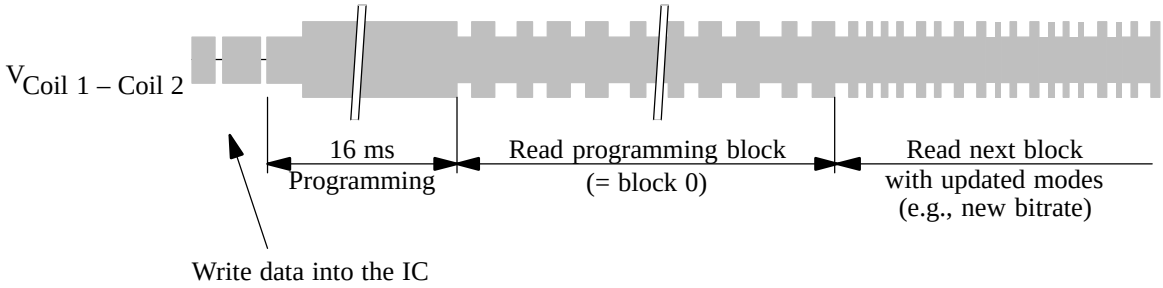


Figure 17. Coil voltage after programming of block 0

OTP Programming

When all necessary information has been written to the T5556, programming may proceed. There is a 32-clock delay between the end of writing and the start of programming. During this time, Vpp – the programming voltage – is measured and the lock bit for the block to be programmed is examined. Further, Vpp is continually monitored throughout the programming cycle. If at any time Vpp is too low, the chip enters read mode immediately. The programming time is 16 ms.

After programming of one block is done, the T5556 enters read mode, starting with the block just programmed. If ei-

ther block or sequence terminators are enabled, the block is preceded by a block terminator. If the mode register (block 0) has been reprogrammed, the new mode will be activated **after** the just-programmed block has been transmitted using the **previous** mode.

In the last programming sequence block 0 has to be written with the OTP bit set.

Error Handling

Several error conditions can be detected to ensure that only valid bits are programmed into the OTP memory. There are two error types which lead to different actions.

Errors During Programming

If writing was successful, the following errors could prevent programming:

- The lock bit of the addressed block is set already
- V_{PP} is too low

In these cases, programming stops immediately. The IC reverts to read mode, starting with the currently addressed block.

Errors During Writing

There are four detectable errors which could occur during writing data into the T5556:

- Wrong number of field clocks between two gaps
- The OP-code is not the write OP-code (’10‘)
- The number of bits received is not equal 38

If any of these conditions is detected, the IC starts read mode immediately after leaving write mode. Reading starts with block 1, bit 1.

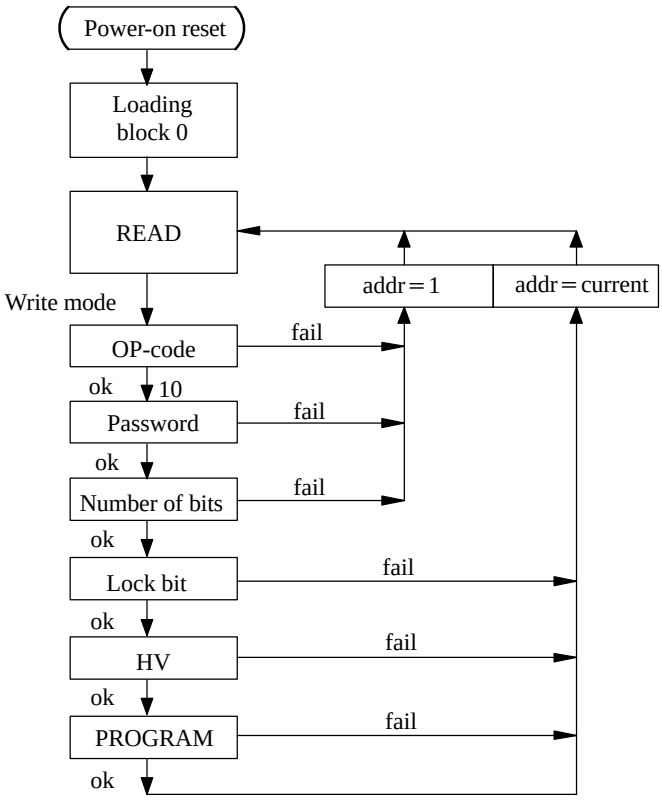


Figure 18. Functional diagram of the T5556

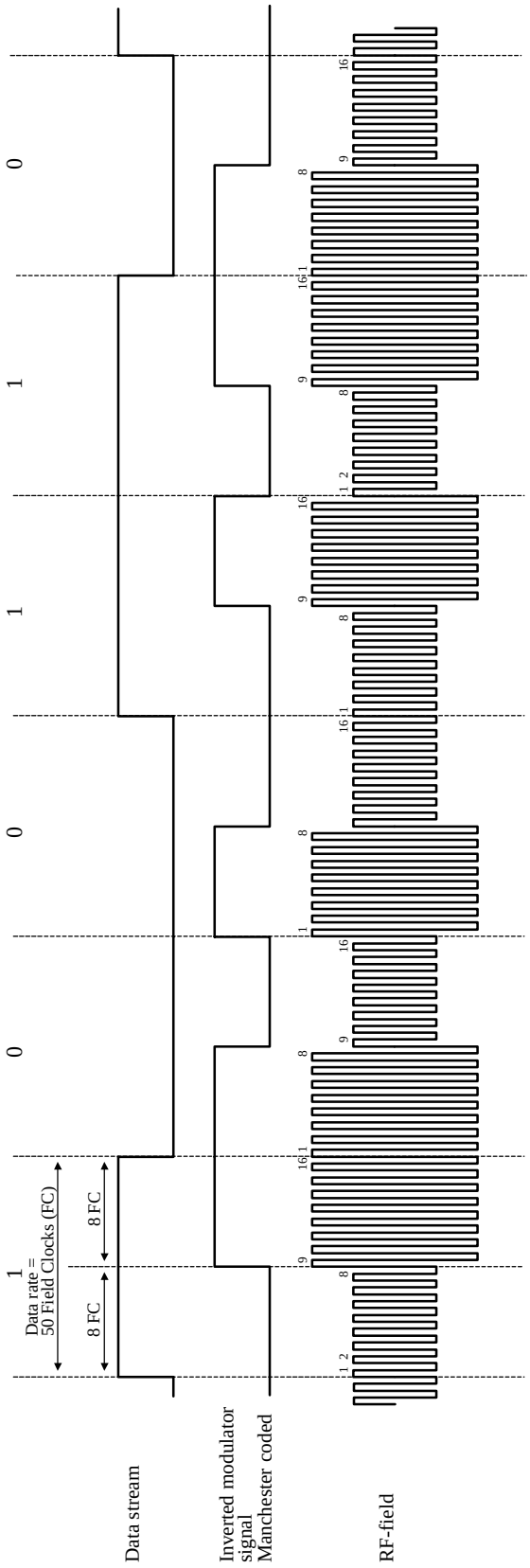


Figure 19. Example of Manchester coding with data rate RF/16

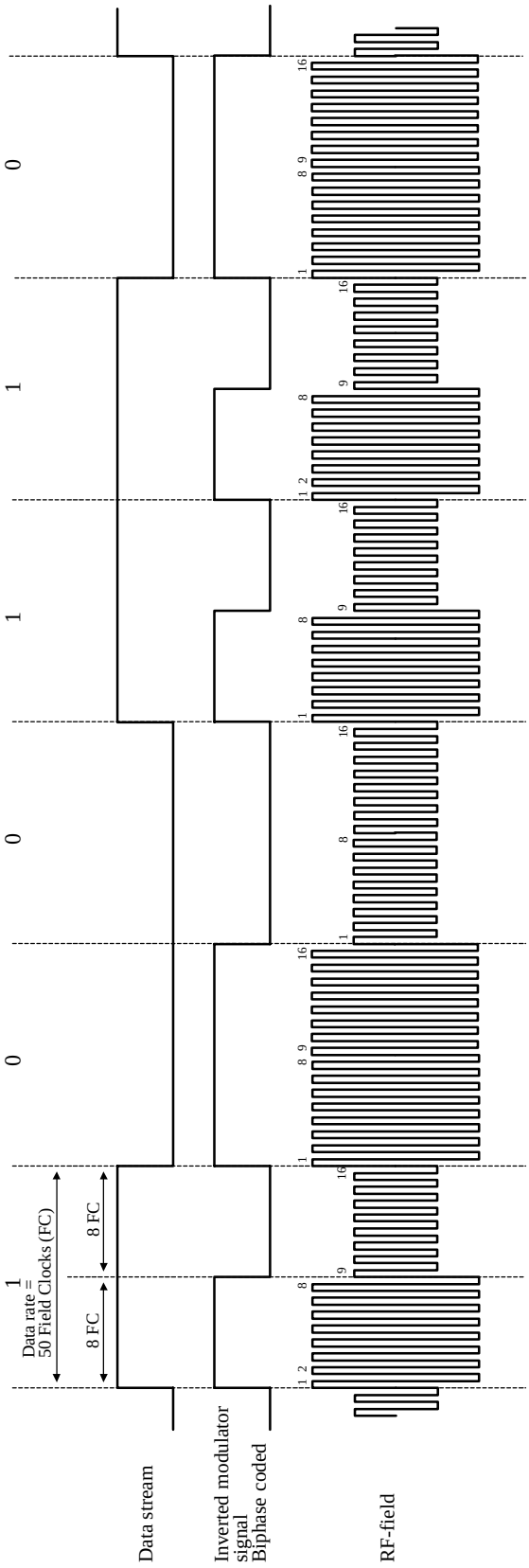


Figure 20. Example of Biphase coding with data rate RF/16

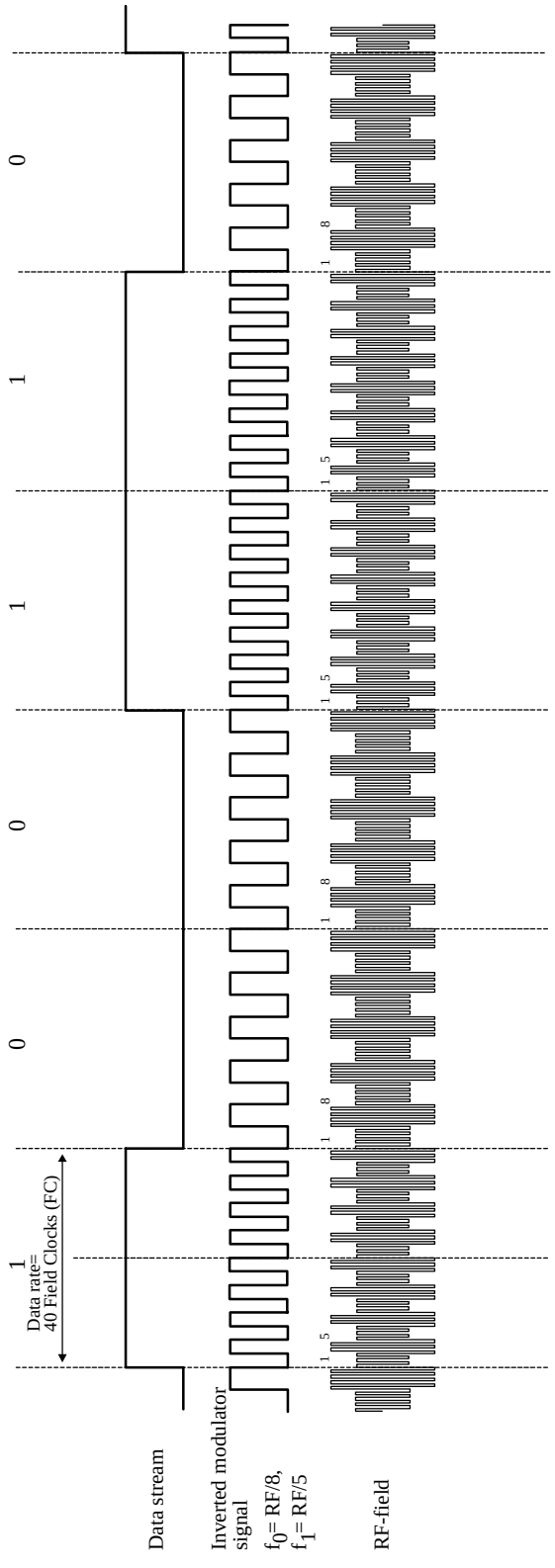


Figure 21. Example of FSK coding with data rate RF/40, sub-carrier f_0 = RF/8, f_1 = RF/5

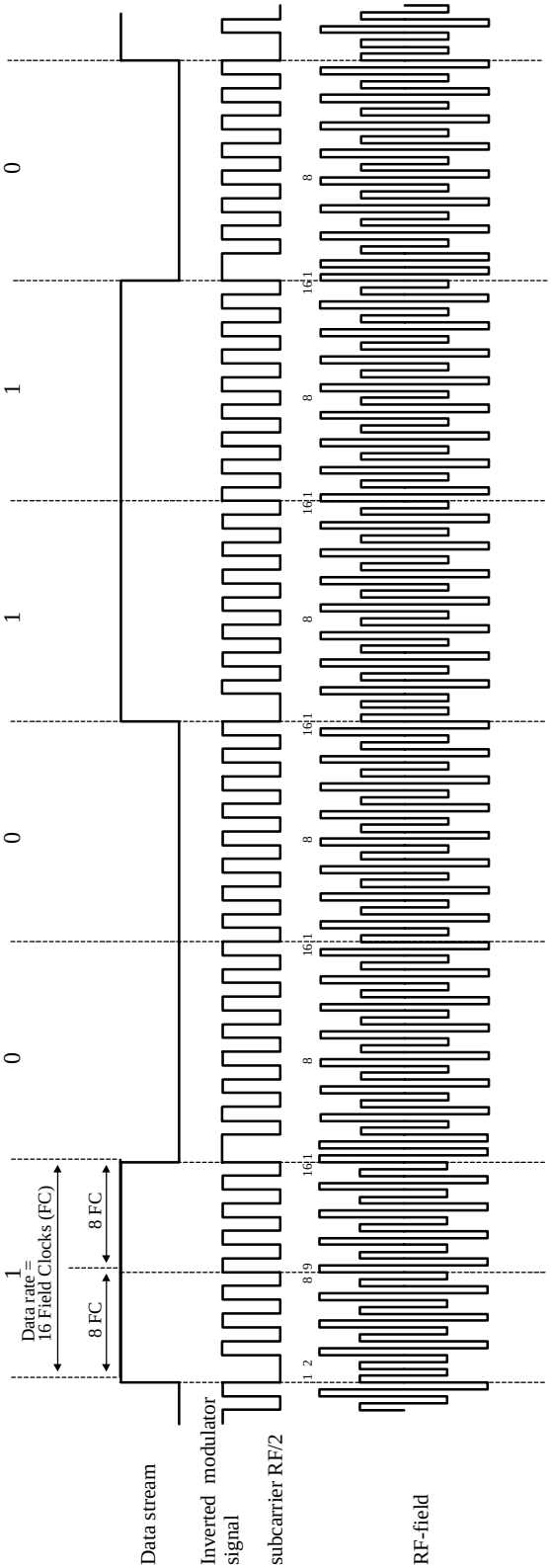


Figure 22. Example of PSK1 coding with data rate RF/16

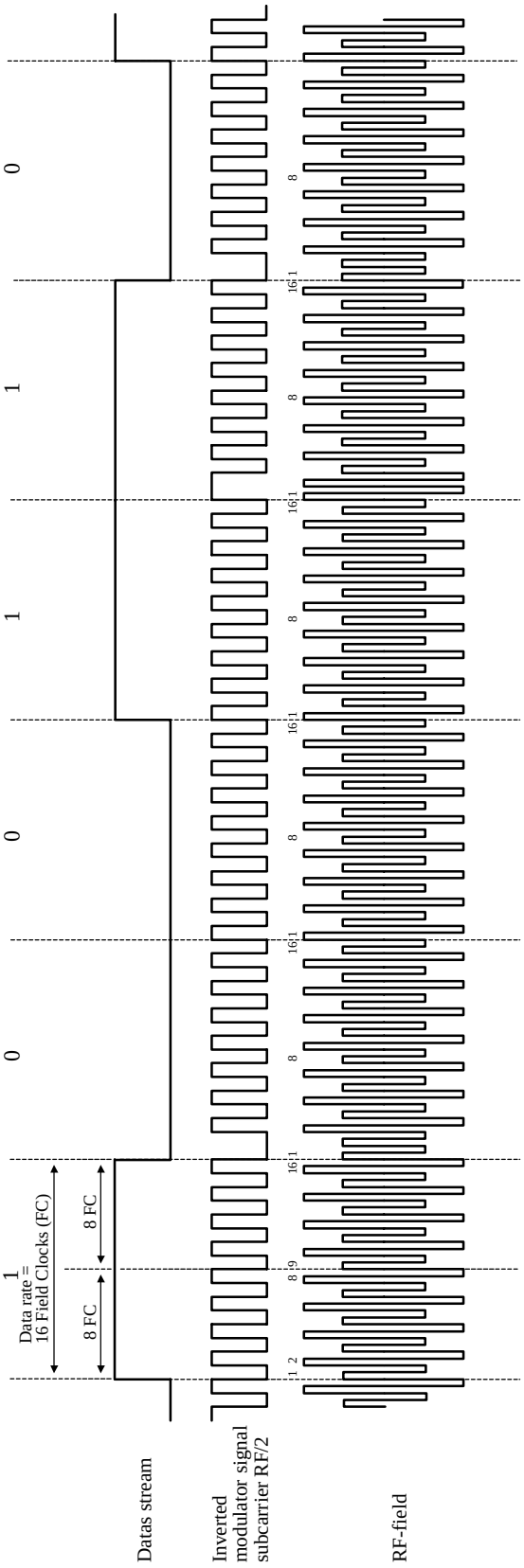


Figure 23. Example of PSK2 coding with data rate RF/16

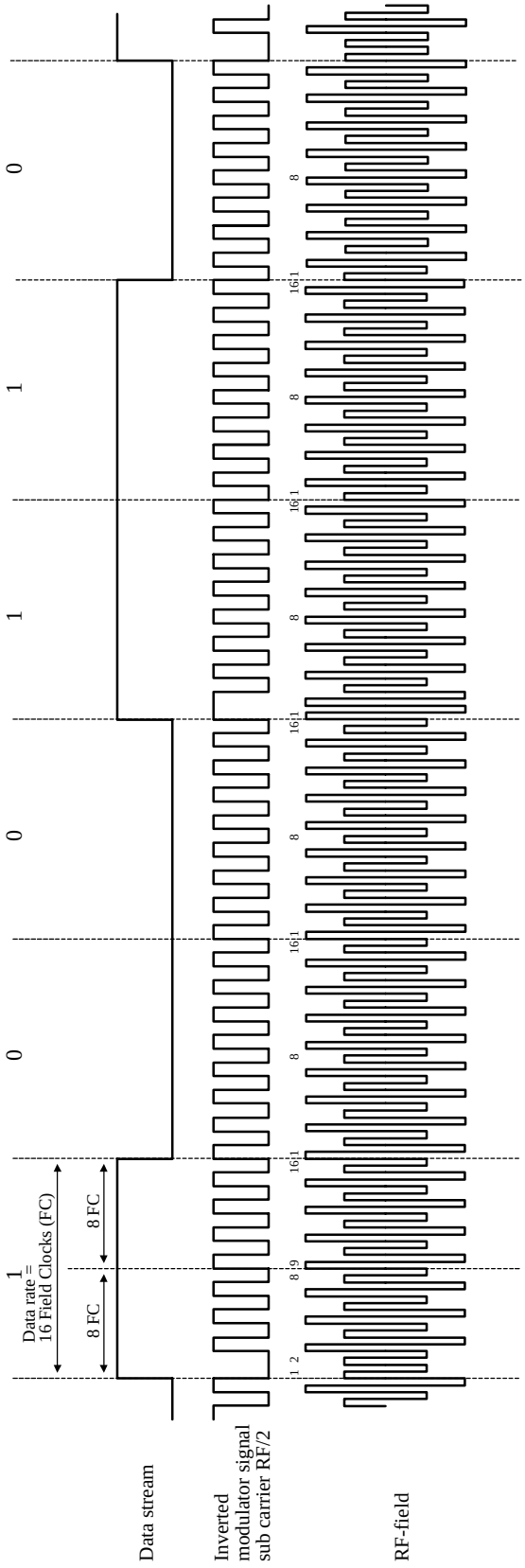


Figure 24. Example of PSK3 coding with data rate RF/16

Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Maximum DC current into Coil 1/ Coil 2	I_{coil}	10	mA
Maximum AC current into Coil 1/ Coil 2, f = 125 kHz	$i_{coil\ pp}$	20	mA
Power dissipation (dice) 1)	P_{tot}	100	mW
Electro-static discharge maximum to MIL-Standard 883 C method 3015	V_{max}	2000	V
Operating ambient temperature range	T_{amb}	–40 to +85	°C
Storage temperature range 2)	T_{stg}	–40 to +125	°C
Maximum assembly temperature for less than 5 min 3)	T_{sld}	+150	°C

Notes: 1) Free-air condition, time of application: 1 s
2) Data retention reduced
3) Assembly temperature of 150°C for less than 5 minutes does not affect the data retention.

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device.

Operating Characteristics

T_{amb} = 25°C; f_{RF} = 125 kHz, reference terminal is V_{SS}

Parameters	Comments	Symbol	Min.	Typ.	Max.	Unit
RF frequency range		f_{RF}	100	125	150	kHz
Supply current (see figure 24)	Read and write over the full temperature range	I_{DD}		5	7.5	µA
	Programming over the full temperature range	I_{DD}		100	200	µA
Clamp voltage	10 mA current into Coil1/2	V_{cl}	9.5		11.5	V
Programming voltage	On-chip HV-Generator	V_{pp}	16		20	V
Programming time		t_P		18		ms
Startup time		$t_{startup}$			4	ms
Data retention		$t_{retention}$	10			Years
Supply voltage	Read and write	V_{DD}			1.6	V
Supply voltage	Read-mode, T = – 30°C	V_{DD}			2.0	V
Coil voltage	Read and write	$V_{coil\ pp}$			6.0	V
Coil voltage	Programming, RF field not damped	$V_{coil\ pp}$			10	V

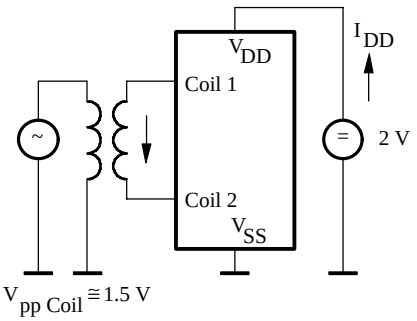
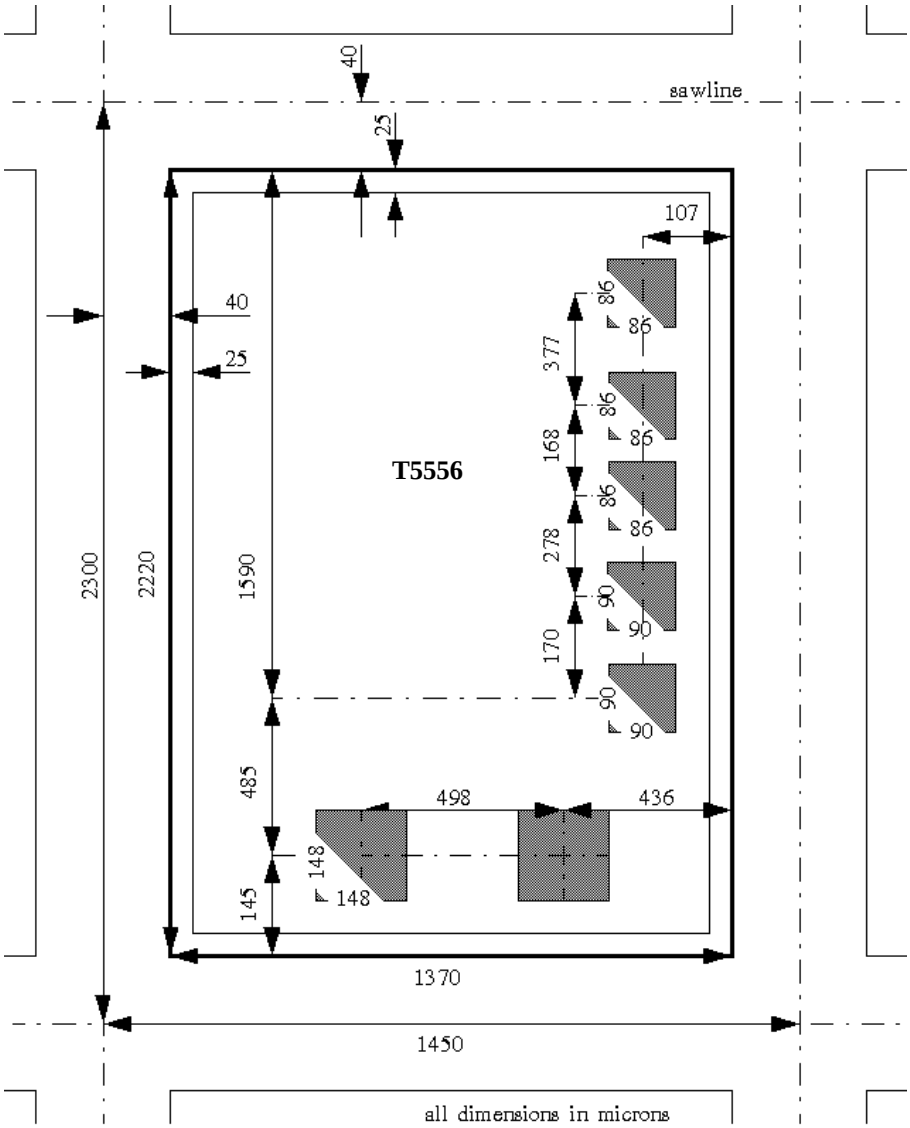


Figure 25. Measurement setup for I_{DD}

Chip Dimensions (μm)



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

Data sheets can also be retrieved from the Internet: http://www.temic–semi.com

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