

**TOSHIBA**

TOSHIBA Original CMOS 16-Bit Microcontroller

**TLCS-900** Series

TMP96C031Z

**TOSHIBA CORPORATION**

# Preface

Thank you very much for making use of Toshiba microcomputer LSIs.  
Before use this LSI, refer the section, "Points of Note and Restrictions".  
Especially, take care below cautions.

## **\*\*CAUTION\*\***

### How to release the HALT mode

Usually, interrupts can release all halts status. However, the interrupts = ( $\overline{NMI}$ , INT0), which can release the HALT mode may not be able to do so if they are input during the period CPU is shifting to the HALT mode (for about 3 clocks of X1) with IDLE or STOP mode. (In this case, an interrupt request is kept on hold internally.)

If another interrupt is generated after it has shifted to HALT mode completely, halt status can be released without difficulty. The priority of this interrupt is compare with that of the interrupt kept on hold internally, and the interrupt with higher priority is handled first followed by the other interrupt.

## CMOS 16-bit Microcontrollers

## TMP96C031ZF

## 1. Outline and Device Characteristics

TMP96C031Z is high-speed advanced 16-bit microcontrollers developed for controlling medium to large-scale equipment. The TMP96C031ZF comes in a 64-pin flat package.

- (1) Original 16-bit CPU
  - TLCS-90 instruction mnemonic upward compatible.
  - 16M-byte linear address space
  - General-purpose registers and register bank system
  - 16-bit multiplication / division and bit transfer/arithmetic instructions
  - High-speed  $\mu$  DMA : 4 channels (1.6  $\mu$ s/2 bytes @20MHz)
- (2) Minimum instruction execution time : 200 ns (@20 MHz)
- (3) External memory expansion
  - Can be expanded up to 16M-byte (for both programs and data).
  - External data bus width selection pin (AM8/ $\overline{16}$ ).
  - Can mix 8- and 16-bit external data buses.
  - … Dynamic data bus sizing
- (4) 8-bit timer : 4 channels
- (5) 16-bit timer : 1 channel
- (6) Pattern generator : 4 bits, 2 channels
- (7) Serial interface : 2 channels
- (8) 6-bit A/D converter : 4 channels
- (9) DRAM controller
- (10) Watchdog timer
- (11) Chip select/wait controller : 4 blocks
- (12) Interrupt functions
  - 3 CPU interrupts … SWI instruction, privileged violation, and Illegal instruction
  - 12 internal interrupts
  - 9 external interrupts ] 7-level priority can be set.
- (13) I/O ports  
37 pins
- (14) Standby function : 3 HALT modes (RUN, IDLE, STOP)

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- For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance / Handling Precautions.
- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.  
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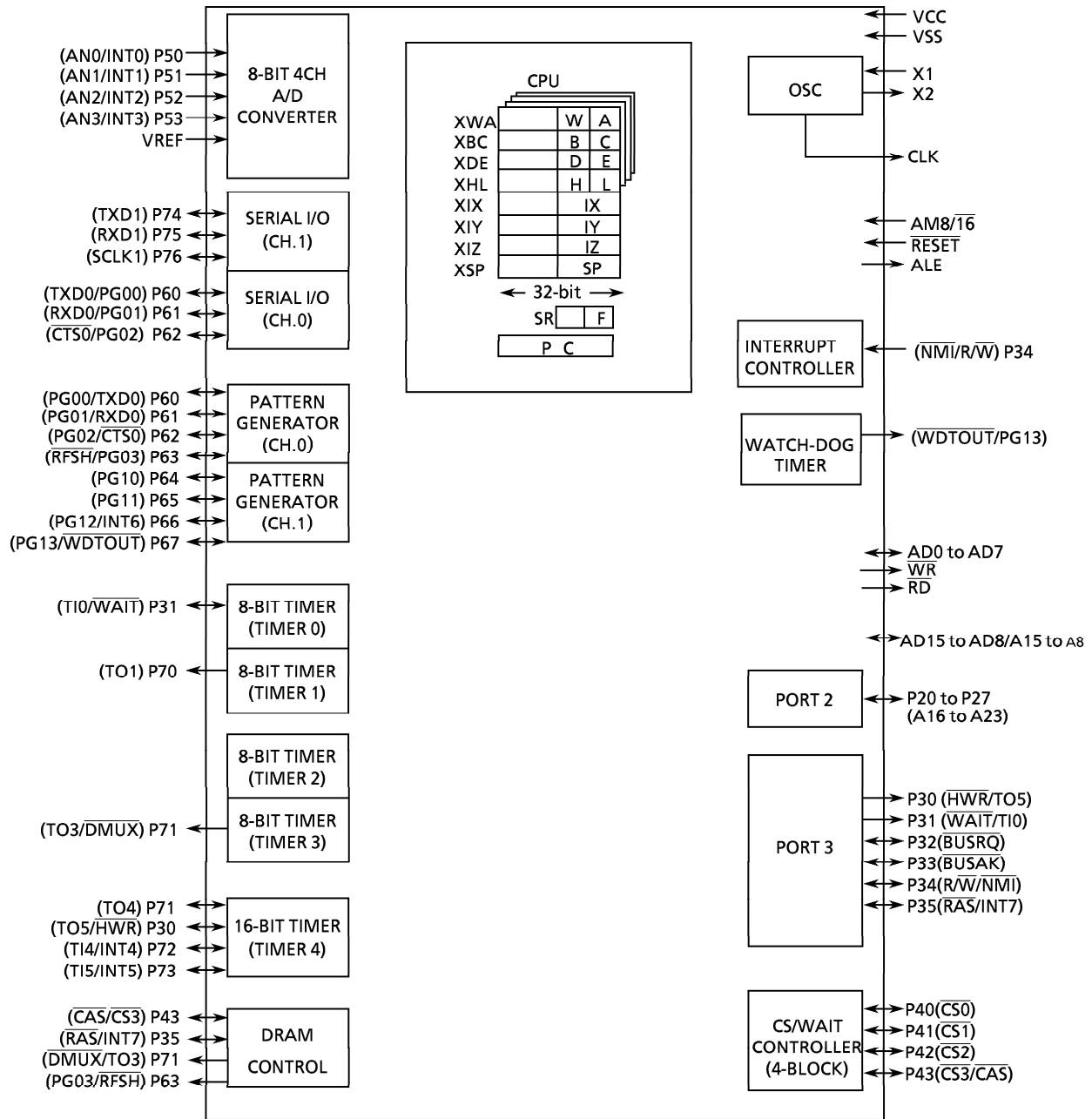


Figure1 TMP96C031Z Block Diagram

## 2. Pin Assignment and Function

### 2.1 Pin Assignment

Figure 2.1 shows pin assignment of TMP96C031ZF.

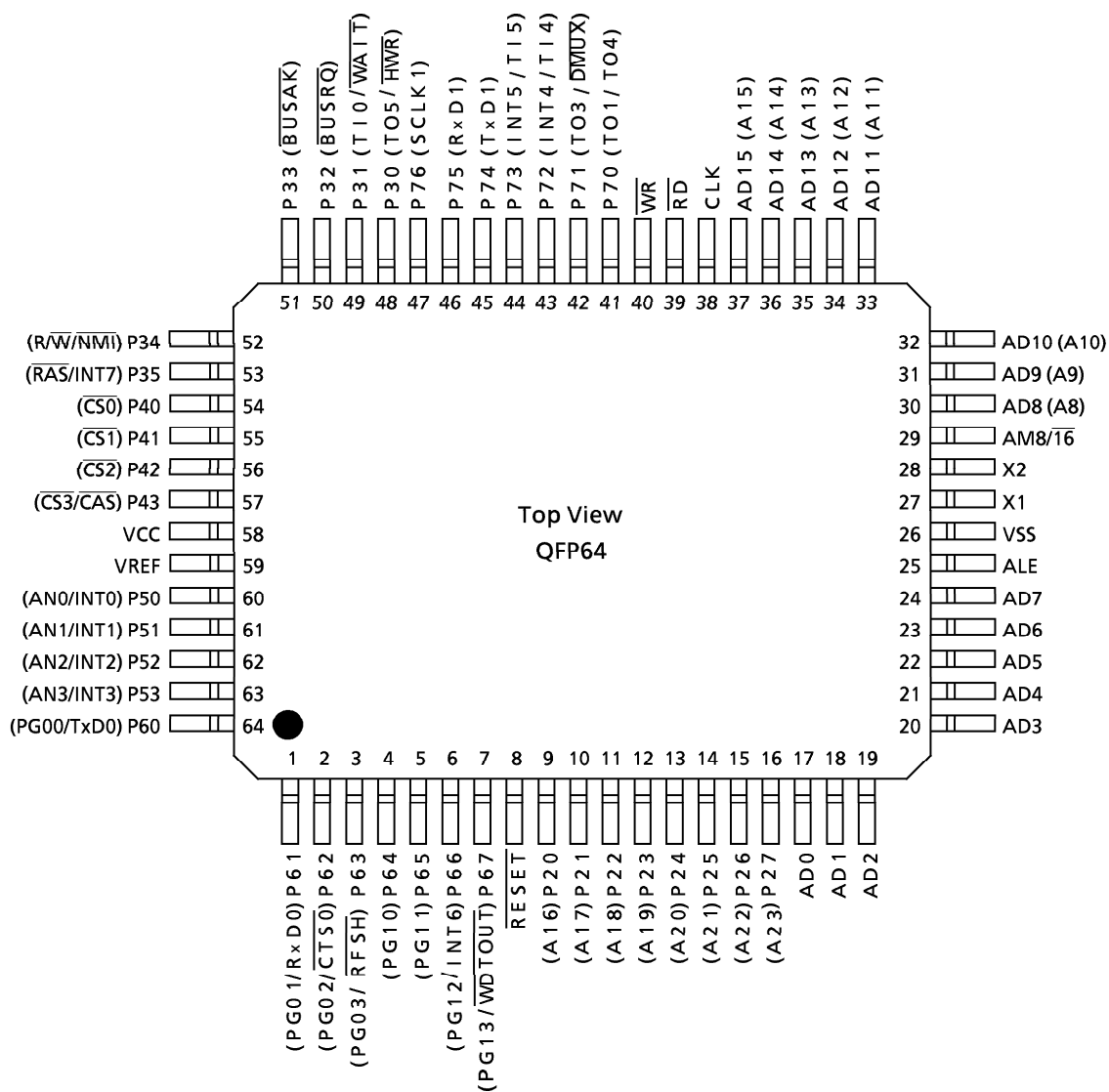


Figure2.1 Pin Assignment (64QFP)

## 2.2 Pin Names and Functions

The names of input/output pins and their functions are described below.

Table 2.2 Pin Names and Functions.

Pin name	Number of pins	I/O	Functions
AD0 to AD7	8	Tri-state	Address/data (lower): 0 to 7 for address/data bus
AD8 to AD15 A8 to A15	8	Tri-state Output	Address data (upper): 8 to 15 for address/data bus Address: 8 to 15 for address bus
P20 to P27 A0 to A7 A16 to A23	8	I/O  Output Output	Port 2: I/O port that allows selection of I/O on a bit basis (with pull-down resistor) Address: 0 to 7 for address bus Address: 16 to 23 for address bus
P30 TO5 HWR	1	I/O Output Output	Port 30: I/O port (with pull-up register) Timer output 5: Timer 4 output pin High write: Strobe signal for writing data on pins AD8 to 15
P31 TIO WAIT	1	I/O Input Input	Port 31: I/O port (with pull-up register) Timer input 0: Timer 0 input Wait: Pin used to request CPU bus wait
P32 BUSRQ	1	I/O Input	Port 32: I/O port (with pull-up register) Bus request: Signal used to request high impedance for AD0 to 15, A0 to 23, $\overline{RD}$ , $\overline{WR}$ , $\overline{HWR}$ , $\overline{R/W}$ , $\overline{RAS}$ , $\overline{CS0}$ , $\overline{CS1}$ , and $\overline{CS2}$ pins. (For external DMAC)
P33 BUSAK	1	I/O Output	Port 33: I/O port (with pull-up register) Bus acknowledge: Signal indicating that AD0 to 15, A0 to 23, $\overline{RD}$ , $\overline{WR}$ , $\overline{HWR}$ , $\overline{R/W}$ , $\overline{RAS}$ , $\overline{CS0}$ , $\overline{CS1}$ , and $\overline{CS2}$ pins are at high impedance after receiving BUSRQ.
P34 $\overline{R/W}$ NMI	1	I/O Output Input	Port 34: I/O port (with pull-up register) Read/write: 1 represents read or dummy cycle; 0, write cycle. Non-maskable interrupt request pin: Interrupt request pin with falling edge. Can also be operated at rising edge by program.
P35 $\overline{RAS}$ INT7	1	I/O Output Input	Port 35: I/O port (with pull-up register) Row address strobe: Outputs RAS strobe for DRAM. Interrupt request pin 7: Interrupt request pin with rising edge.
P40 $\overline{CS0}$	1	Output Output	Port 40: Output port Chip select 0: Outputs 0 when address is within specified address area.
P41 $\overline{CS1}$	1	Output Output	Port 41: Output port Chip select 1: Outputs 0 if address is within specified address area.

Note : The internal I/O of this device cannot be accessed using an external DMA controller.

Pin name	Number of pins	I/O	Functions
P42 CS2	1	Output Output	Port 42: Output port (with pull-up resistor) Chip select 2: Outputs 0 if address is within specified address area.
P43 CS3 CAS	1	Output Output Output	Port 43: Output port (with pull-up resistor) Chip select 3: Outputs 0 if address is within specified address area. Column address strobe : Output CAS strobe for DRAM if address is within specified address area.
VREF	1	Input	A/D convertor reference voltage input
P50 to P53 AN0 to AN3 INT0 to INT3	4	Input Input Input	Port 50 to 53: Input port Analog input: Input to A/D converter Interrupt request pin 0: Interrupt request pin with programmable level/rising edge. Interrupt request pin 1: Interrupt request pin with programmable rising/falling edge. Interrupt request pin 2 to 3: Interrupt request pin with rising edge.
P60 TxD0 PG00	1	I/O Output Output	Port 60: I/O port Serial send data 0 Pattern generator port 00
P61 RxD0 PG01	1	I/O Input Output	Port 61: I/O port Serial receive data 0 Pattern generator port 01
P62 CTS0 PG02	1	I/O Input Output	Port 62: I/O port Serial data send enable 0 (Clear to Send) Pattern generator port 02
P63 RFSH PG03	1	I/O Output Output	Port 63: I/O port Refresh out : This is a state signal output pin which indicates that the DRAM controller is in refresh cycle. Pattern generator port 03
P64 PG10	1	I/O Output	Port 64: I/O port Pattern generator port 10
P65 PG11	1	I/O Output	Port 65: I/O port Pattern generator port 11
P66 INT6 PG12	1	I/O Input Output	Port 66: I/O port Interrupt request pin 6 : Interrupt request pin with rising edge. Pattern generator port 12
P67 WDTOUT PG13	1	I/O Output Output	Port 67: I/O port Watchdog timer output pin Pattern generator port 13
P70 TO1 TO4	1	I/O Output Output	Port 70: I/O port Timer output 1: Timer 0 or 1 output pin Timer output 4: Timer 4 output pin

Pin name	Number of pins	I/O	Functions
P71 TO3 DMUX	1	I/O Output Output	Port 71: I/O Port Timer output 3: Timer 2 or Timer 3 output pin DRAM address multiplexor : This pin outputs row address, column address, and selector select signal.
P72 INT4 TI4	1	I/O Input Input	Port 72: I/O Port Interrupt request pin 4: Interrupt request pin with programmable rising/falling edge. Timer input 4: Timer 4 count/capture trigger signal input
P73 INT5 TI5	1	I/O Input Input	Port 73: I/O Port Interrupt request pin 5: Interrupt request pin with rising edge. Timer input 5: Timer 4 count/capture trigger signal input
P74 TxD1	1	I/O Output	Port 74: I/O Port Serial send data 1
P75 RxD1	1	I/O Input	Port 75: I/O Port Serial receive data 1
P76 SCLK1	1	I/O I/O	Port 76: I/O Port Serial clock I/O 1
CLK	1	Output	Clock output : Outputs 「 X1 ÷ 4 」 clock. Pulled-up during reset.
$\overline{RD}$	1	Output	Read: Strobe signal for reading external memory.
$\overline{WR}$	1	Output	Write: Strobe signal for writing data on pins AD0 to 7.
AM8/ $\overline{16}$	1	Input	Address mode : External data bus width selection pin. Set to "0" for fixed external 16-bit bus or for mixed external 8/16 bit bus and to "1" for fixed external 8-bit bus.
$\overline{RESET}$	1	Input	Reset: Initializes LSI. (With pull-up resistor)
ALE	1	Output	Address latch enable
X1/X2	1	I/O	Oscillator connecting pin
VCC	1		Power supply pin ( + 5 V ) (All Vcc pins should be connected with the power supply pin.)
VSS	1		GND pin (0 V) (All Vss pins should be connected with GND (0 V).)

Note : Pull-up/pull-down resistor can be released from the pin by software.



### 3. Operation

This section describes in blocks the functions and basic operations of TMP96C031Z device.

Check the 「7. Care Points and Resection」 because of the Care Points etc are described.

#### 3.1 CPU

TMP96C031Z device have a built-in high-performance 16-bit CPU (900\_CPU). (For CPU operation, see TLCS-900 CPU in the previous section).

This section describes CPU functions unique to TMP96C031Z that are not described in the previous section.

##### 3.1.1 Reset

To reset the TMP96C031Z, the  $\overline{\text{RESET}}$  input must be kept at 0 for at least 10 system clocks (10 states: 1  $\mu\text{s}$  with a 20 MHz system clock) within an operating voltage range and with a stable oscillation.

When reset is accepted, the CPU sets as follows:

- Program counter (PC) to 8000H.
- Stack pointer (XSP) for system mode to 100H.
- SYSM bit of status register (SR) to 1. (Sets to system mode.)
- IFF2 to 0 bits of status register to 111. (Sets mask register to interrupt level 7.)
- MAX bit of status register to 0. (Sets to minimum mode)
- Bits RFP2 to 0 of status register to 000. (Sets register banks to 0.)

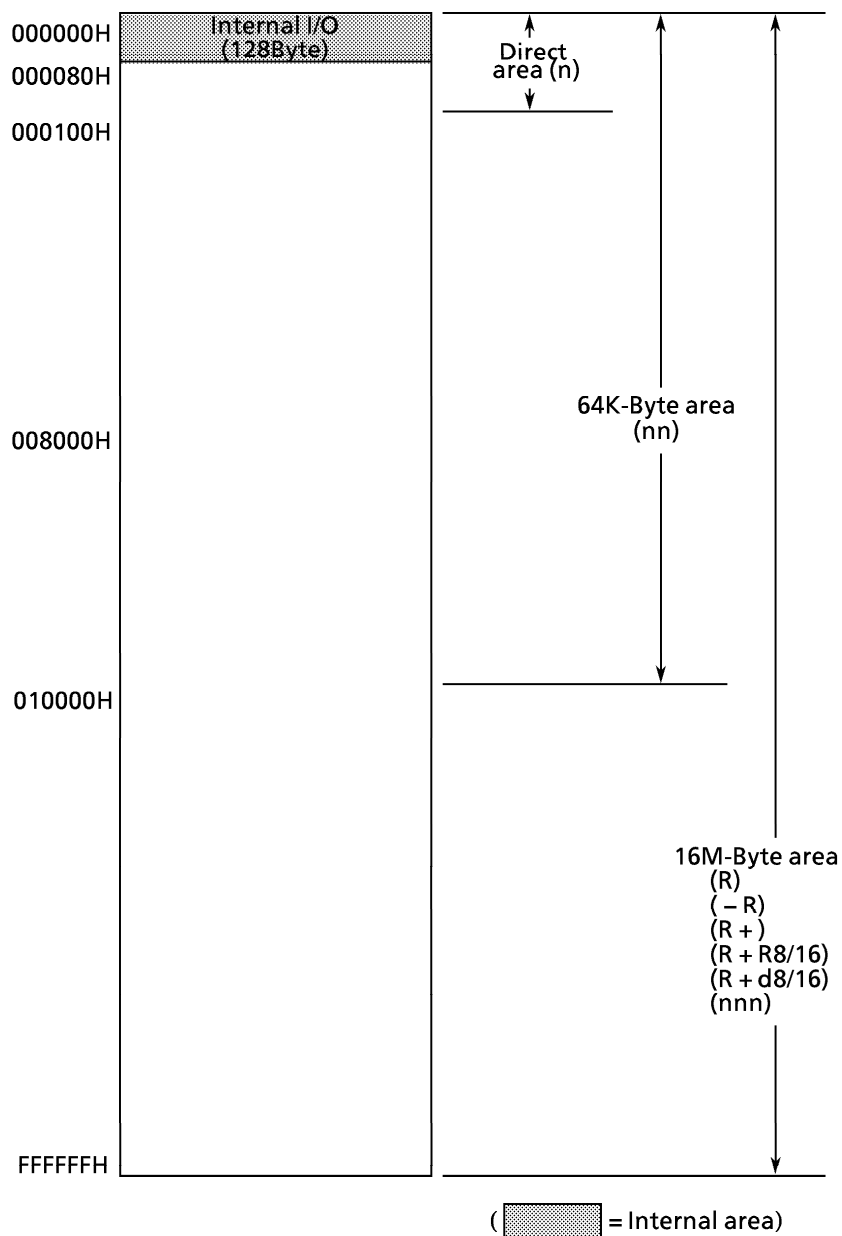
When reset is released, instruction execution starts from address 8000H. CPU internal registers other than the above are not changed.

When reset is accepted, processing for built-in I/Os, ports, and other pins is as follows

- Initializes built-in I/O registers as per specifications.
- Sets port pins (including pins also used as built-in I/Os) to general-purpose input/output port mode (sets I/O ports to input ports).
- Pulls up the CLK pin to 1.
- Sets the ALE pin to 0.

3.2 Memory Map

Figure 3.2 is a memory map of the TMP96C031Z.



Note : The start address after reset is 8000H. Resetting sets the stack pointer (XSP) on the system mode side to 100H.

Figure3.2 Memory map

## 4. Electrical Characteristics

### 4.1 Absolute Maximum Ratings (TMP96C031Z)

Parameter	Symbol	Rating	Unit
Power Supply voltage	V <sub>CC</sub>	- 0.5 to 6.5	V
Input voltage	V <sub>IN</sub>	- 0.5 to V <sub>CC</sub> + 0.5	V
Output Current (total)	∑ I <sub>OL</sub>	100	mA
Output Current (total)	∑ I <sub>OH</sub>	- 100	mA
Power Dissipation (T <sub>a</sub> = 70°C)	P <sub>D</sub>	600	mW
Soldering Temperature (10 s)	T <sub>SOLDER</sub>	260	°C
Storage temperature	T <sub>STG</sub>	- 65 to 150	°C
Operating temperature	T <sub>OPR</sub>	- 20 to 70	°C

Note : The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

## 4.2 DC Characteristics (TMP96C031Z)

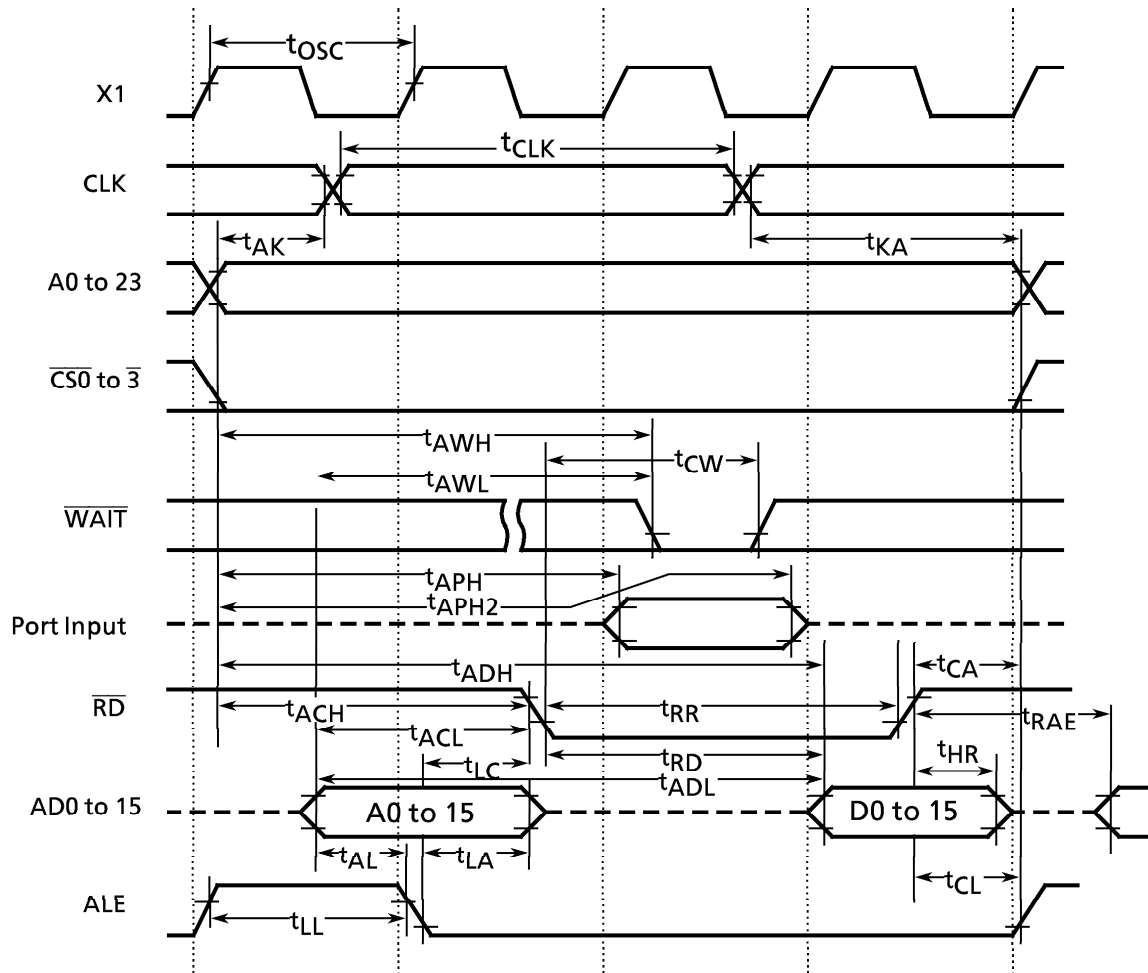
$V_{CC} = 5\text{ V} \pm 10\%$ ,  $T_a = -20\text{ to }70^\circ\text{C}$  (Typical values are for  $T_a = 25^\circ\text{C}$  and  $V_{CC} = 5\text{ V}$ .)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Low Voltage (AD0 to 15)	V IL		-0.3	0.8	V
P2, P3, P4, P5, P6, P7, P8, P9	V IL1		-0.3	0.3 V <sub>CC</sub>	V
RESET, NMI, INT0	V IL2		-0.3	0.25 V <sub>CC</sub>	V
AM8/16	V IL3		-0.3	0.3	V
X1	V IL4		-0.3	0.2 V <sub>CC</sub>	V
Input High Voltage (AD0 to 15)	V IH		2.2	V <sub>CC</sub> + 0.3	V
P2, P3, P4, P5, P6, P7, P8, P9	V IH1		0.7 V <sub>CC</sub>	V <sub>CC</sub> + 0.3	V
RESET, NMI, INT0	V IH2		0.75 V <sub>CC</sub>	V <sub>CC</sub> + 0.3	V
AM8/16	V IH3		V <sub>CC</sub> - 0.3	V <sub>CC</sub> + 0.3	V
X1	V IH4		0.8 V <sub>CC</sub>	V <sub>CC</sub> + 0.3	V
Output Low Voltage	V OL	I <sub>OL</sub> = 1.6 mA		0.45	V
Output High Voltage	V OH	I <sub>OH</sub> = -400 $\mu$ A	2.4		V
	V OH1	I <sub>OH</sub> = -100 $\mu$ A	0.75 V <sub>CC</sub>		V
	V OH2	I <sub>OH</sub> = -20 $\mu$ A	0.9 V <sub>CC</sub>		V
Darlington Drive Current (8 Output Pins max.)	I DAR	V <sub>EXT</sub> = 1.5 V R <sub>EXT</sub> = 1.1 k $\Omega$	-1.0	-3.5	mA
Input Leakage Current	I LI	0.0 $\leq$ V <sub>in</sub> $\leq$ V <sub>CC</sub>	0.02 (Typ)	$\pm$ 5	$\mu$ A
Output Leakage Current	I LO	0.2 $\leq$ V <sub>in</sub> $\leq$ V <sub>CC</sub> - 0.2	0.05 (Typ)	$\pm$ 10	$\mu$ A
Operating Current (RUN)	I <sub>CC</sub>	t <sub>osc</sub> = 20 MHz	30 (Typ)	60	mA
IDLE			2.0 (Typ)	10	mA
STOP (T <sub>a</sub> = -20 to 70°C)		0.2 $\leq$ V <sub>in</sub> $\leq$ V <sub>CC</sub> - 0.2	0.2 (Typ)	50	$\mu$ A
STOP (T <sub>a</sub> = 0 to 50°C)		0.2 $\leq$ V <sub>in</sub> $\leq$ V <sub>CC</sub> - 0.2		10	$\mu$ A
Power Down Voltage (@STOP, RAM Back up)	V STOP	V IL2 = 0.2 V <sub>CC</sub> , V IH2 = 0.8 V <sub>CC</sub>	2.0	6.0	V
RESET Pull Up Resistor	R RST		50	150	k $\Omega$
Pin Capacitance	C IO	t <sub>osc</sub> = 1 MHz		10	pF
Schmitt Width RESET, NMI, INT0 (P50)	V TH		0.4	1.0 (Typ)	V
Programmable Pull Down Resistor	R KL		10	80	k $\Omega$
Programmable Pull Up Resistor	R KH		50	150	k $\Omega$

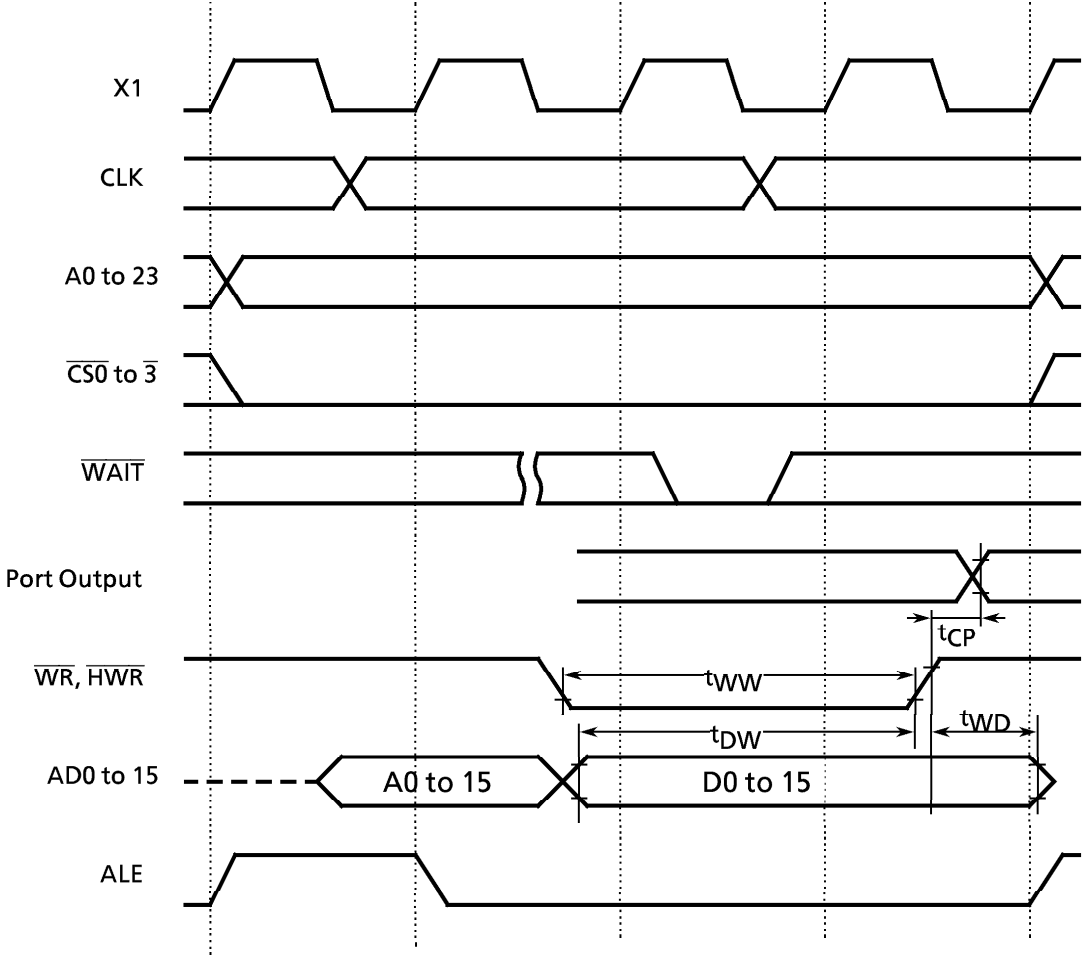
Note : I-DAR is guaranteed for a total of up to 8 ports.



(1) Read Cycle



(2) Write Cycle



## 4.4 DRAM Control AC Characteristics (TMP96C031Z)

$V_{CC} = 5\text{ V} \pm 10\%$  ,  $T_A = -20\text{ to }70^\circ\text{C}$   
(4 MHz to 20 MHz)

No.	Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	RAS cycle time	$t_{RC}$	4X-10		240		190		ns
2	RAS fall → data input	$t_{RAC}$		2X-50		75		50	ns
3	CAS fall → data input	$t_{CAC}$		1X-42		20.5		8	ns
4	RAS high pulse width	$t_{RP}$	2X-40		85		60		ns
5	RAS low pulse width	$t_{RAS}$	2X-20		105		80		ns
6	$\overline{\text{CAS}}$ fall → $\overline{\text{RAS}}$ rise	$t_{RSH}$	1X-25		38		25		ns
7	RAS fall → $\overline{\text{CAS}}$ rise	$t_{CSH}$	2X-20		105		80		ns
8	$\overline{\text{CAS}}$ low pulse width	$t_{CAS}$	1.5X-30		64		45		ns
9	$\overline{\text{RAS}}$ fall → $\overline{\text{CAS}}$ fall	$t_{RCD}$	1X-10	1X + 10	53	73	40	60	ns
10	$\overline{\text{CAS}}$ rise → RAS fall	$t_{CRP}$	1.5X-50		44		25		ns
11	RAS fall → A0-15 hold	$t_{RAH}$	-30		-30		-30		ns
12	A0 to 15 valid → RAS fall	$t_{ASRL}$	1X-10		53		40		ns
13	A0 to 23 valid → RAS fall	$t_{ASRH}$	1.5X-10		84		65		ns
14	$\overline{\text{WR}}$ fall → RAS rise	$t_{RWL}$	2X-50		75		50		ns
15	$\overline{\text{WR}}$ fall → CAS rise	$t_{CWL}$	2X-50		75		50		ns
16	Data output → CAS fall setup	$t_{DS}$	1X-30		33		20		ns
17	CAS fall → data output hold	$t_{DH}$	1.5X-50		44		25		ns
18	RAS fall → data output hold	$t_{DHR}$	2.5X-50		106		75		ns
19	$\overline{\text{WR}}$ fall → CAS fall setup	$t_{WCS}$	1X-30		33		20		ns
20	CAS fall → $\overline{\text{WR}}$ hold	$t_{WCH}$	1X-30		33		20		ns
21	$\overline{\text{RAS}}$ fall → DMUX fall	$t_{RDM}$	0.5X-10	0.5X	21	31	15	25	ns
22	DMUX fall → $\overline{\text{CAS}}$ fall	$t_{CDM}$	0.5X	0.5X + 10	31	41	25	35	ns
23	RAS fall → $\overline{\text{CAS}}$ rise	$t_{CHR}^*1$	2X-50		75		50		ns
24	RAS rise → $\overline{\text{CAS}}$ fall	$t_{RPC}^*$	1.5X-30		64		45		ns
25	CAS high pulse width	$t_{CP}^*$	1.5X-60		34		15		ns
26	CAS fall → RAS fall	$t_{CSR}^*$	0.5X-10		21		15		ns
27	RAS low pulse width	$t_{RASS}^*2$	2000X		125		100		$\mu\text{s}$
28	RAS precharge time	$t_{RPS}^*2$	4X-50		200		150		ns
29	CAS hold time	$t_{CHS}^*2$	-10		-10		-10		ns
30	RFSH fall → $\overline{\text{CAS}}$ fall	$t_{CFL}^*$	1X-10		53		40		ns
31	$\overline{\text{CAS}}$ rise → RFSH rise	$t_{CFH}^*$	0.5X-10		21		15		ns

\*1  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  interval refresh mode

\*2  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  self-refresh mode

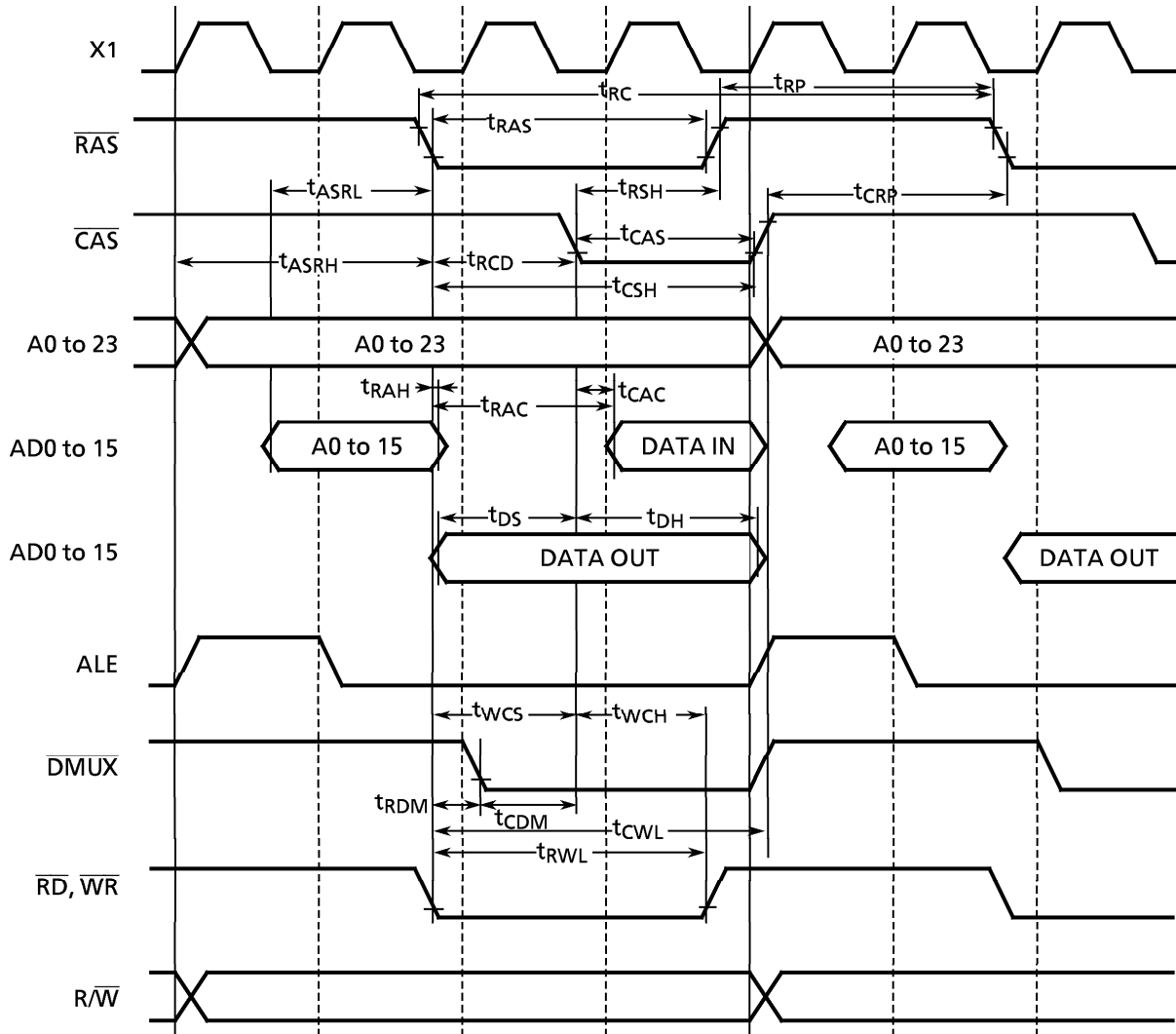
\* Both refresh modes

## AC Measuring Conditions

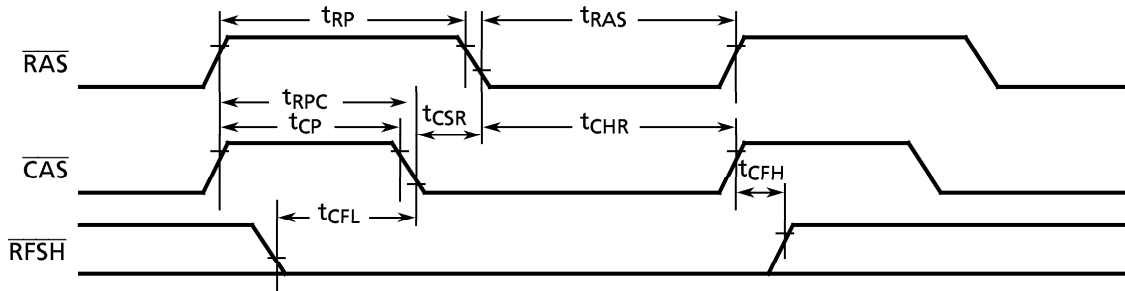
- Output Level : High 2.2 V / Low 0.8 V ,  $C_L = 50\text{ pF}$   
(However  $C_L = 100\text{ pF}$  for AD0 to AD15, A0 to A23,  $\overline{\text{RD}}$ ,  $\overline{\text{WR}}$ ,  $\overline{\text{HWR}}$ ,  $\overline{\text{R/W}}$ ,  $\overline{\text{RAS}}$ )
- Input Level : High 2.4 V / Low 0.45 V (AD0 to AD15)  
High 0.8  $V_{CC}$  / Low 0.2  $V_{CC}$  (Except for AD0 to AD15)



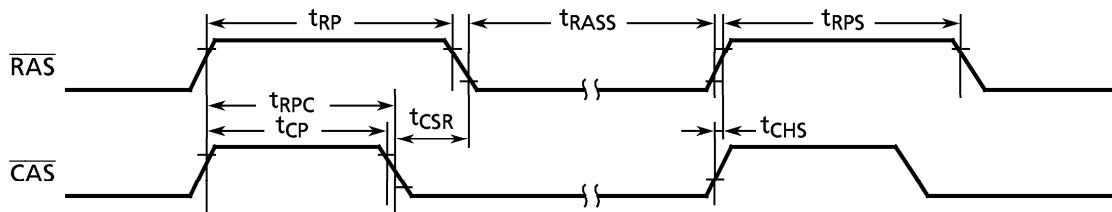
(1) Read/Write Access Cycle



(2)  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  interval refresh cycle



(3)  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  self-refresh cycle



## 4.5 A/D Conversion Characteristics

V<sub>CC</sub> = 5 V ± 10% TA = -20 to 70°C

Parameter	Symbol	Min	Typ.	Max	Unit
Analog reference voltage	V <sub>REF</sub>	V <sub>CC</sub> - 1.5		V <sub>CC</sub>	V
Analog reference voltage	A <sub>GN</sub> D	V <sub>SS</sub>		V <sub>SS</sub>	
Analog input voltage range	V <sub>A</sub> IN	V <sub>SS</sub>		V <sub>CC</sub>	
Analog current for analog reference voltage	I <sub>REF</sub>		0.5	1.5	mA
Total error	Error(Quantize error of ± 0.5 LSB not included)			2.0	LSB

## 4.6 Serial Channel Timing – I/O Interface Mode

## (1) SCLK Input Mode

V<sub>CC</sub> = 5 V ± 10% TA = -20 to 70°C

Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK cycle	t <sub>SCY</sub>	16X		1		0.8		μs
Output Data → Rising edge of SCLK	t <sub>OSS</sub>	t <sub>SCY</sub> /2 - 5X - 50		137		100		ns
SCLK rising edge → Output Data hold	t <sub>OHS</sub>	5X - 100		212		150		ns
SCLK rising edge → Input Data hold	t <sub>HSR</sub>	0		0		0		ns
SCLK rising edge → effective data input	t <sub>SRD</sub>			t <sub>SCY</sub> - 5X - 100		587		450 ns

## (2) SCLK Output Mode

Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK cycle (programmable)	t <sub>SCY</sub>	16X	8192X	1	512	0.8	409.6	μs
Output Data → SCLK rising edge	t <sub>OSS</sub>	t <sub>SCY</sub> - 2X - 150		725		550		ns
SCLK rising edge → Output Data hold	t <sub>OHS</sub>	2X - 80		45		20		ns
SCLK rising edge → Input Data hold	t <sub>HSR</sub>	0		0		0		ns
SCLK rising edge → effective data input	t <sub>SRD</sub>			t <sub>SCY</sub> - 2X - 150		725		550 ns

## 4.7 Timer/Counter Input Clock (TI0, TI4, TI5)

V<sub>CC</sub> = 5 V ± 10% TA = -20 to 70°C

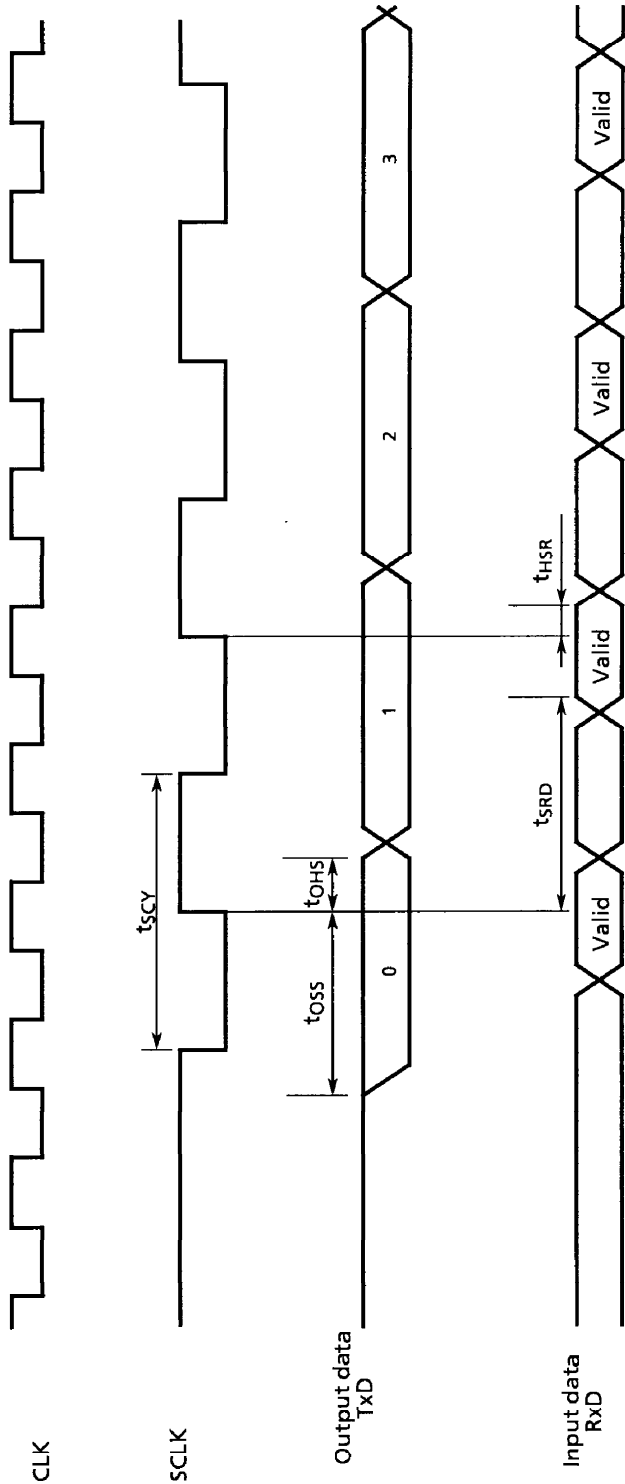
Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Clock Cycle	t <sub>VCK</sub>	8X + 100		600		500		ns
Low level clock Pulse width	t <sub>VCKL</sub>	4X + 40		290		240		ns
High level clock Pulse width	t <sub>VCKH</sub>	4X + 40		290		240		ns

## 4.8 Interrupt Operation

V<sub>CC</sub> = 5 V ± 10% TA = -20 to 70°C

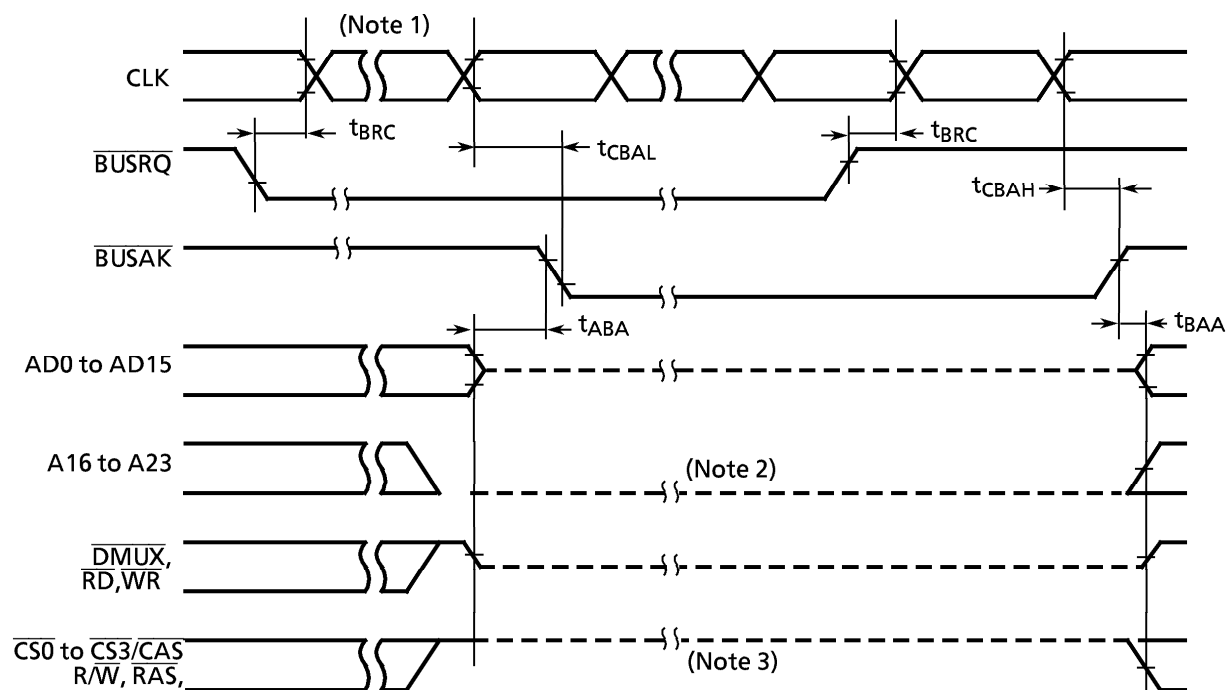
Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
NMI, INT0 Low level Pulse width	t <sub>INTAL</sub>	4X		250		200		ns
NMI, INT0 High level Pulse width	t <sub>INTAH</sub>	4X		250		200		ns
INT1 to INT7 Low level Pulse width	t <sub>INTBL</sub>	8X + 100		600		500		ns
INT1 to INT7 High level Pulse width	t <sub>INTBH</sub>	8X + 100		600		500		ns

4.9 Timing Chart for I/O Interface Mode



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4.10 Timing Chart for Bus Request/BUS Acknowledge



Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
BUSRQ set-up time for CLK	t <sub>BRC</sub>	120		120		120		ns
CLK → BUSAK falling edge	t <sub>CBAL</sub>		2.0x + 120		214		220	ns
CLK → BUSAK rising edge	t <sub>CBAH</sub>		0.5x + 40		71		65	ns
Output Buffer is off to BUSAK ↓	t <sub>ABA</sub>	0	80	0	80	0	80	ns
BUSAK ↑ to Output Buffer is on.	t <sub>BAA</sub>	0	80	0	80	0	80	ns

Note 1 : The Bus will be released after the  $\overline{\text{WAIT}}$  request is inactive, when the  $\overline{\text{BUSRQ}}$  is set to "0" during "Wait" cycle.

Note 2 : An internal programmable pull-down resistor must be connected.

Note 3 : An internal programmable pull-up resistor must be connected.

4.11 Typical characteristics

$V_{CC}=5\text{ V}$ ,  $T_a=25^\circ\text{C}$ , unless otherwise noted.

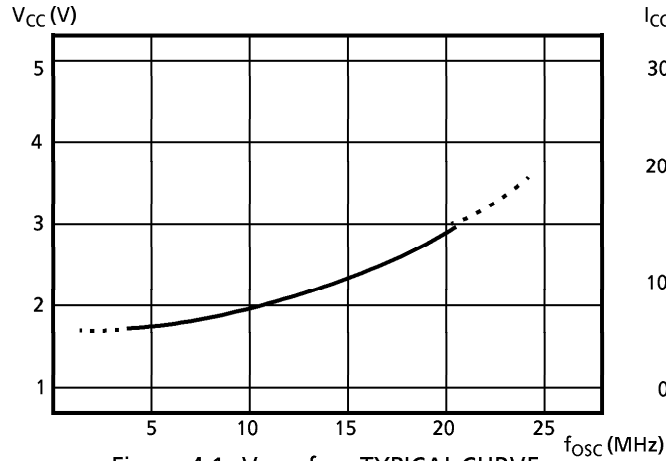


Figure 4.1  $V_{CC} - f_{OSC}$  TYPICAL CURVE

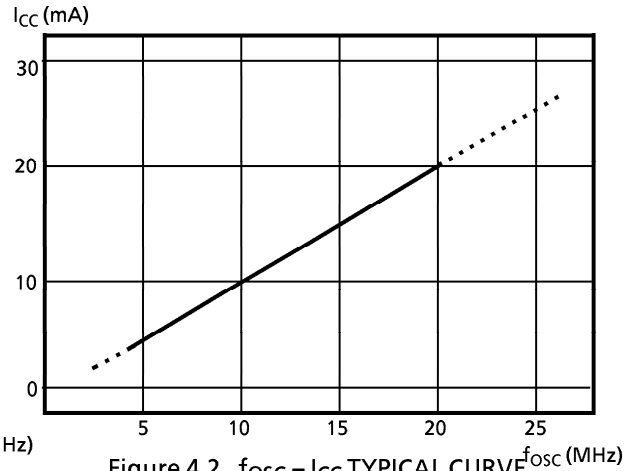


Figure 4.2  $f_{OSC} - I_{CC}$  TYPICAL CURVE

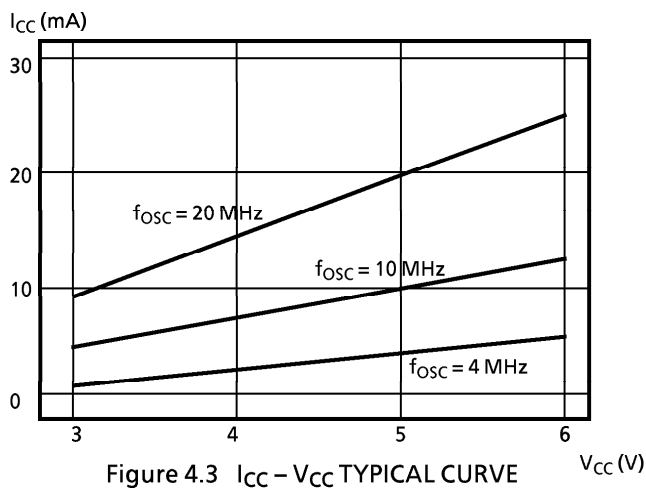


Figure 4.3  $I_{CC} - V_{CC}$  TYPICAL CURVE

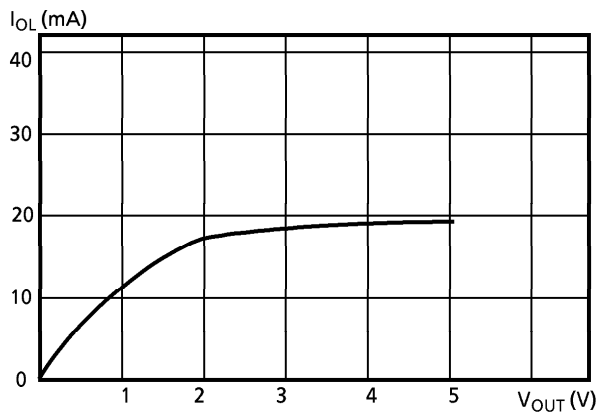


Figure 4.4  $V_{OUT} - I_{OL}$  TYPICAL CURVE

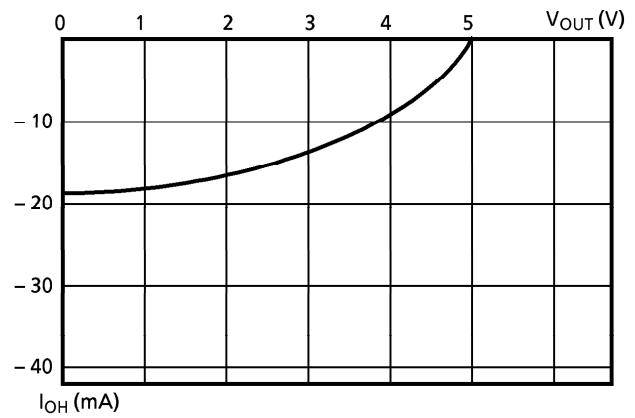


Figure 4.5  $V_{OUT} - I_{OH}$  TYPICAL CURVE