A Cirrus Logic Company

CS4328

18-Bit, Stereo D/A Converter for Digital Audio

Features

- Complete Stereo DAC System
  - 8× Interpolation Filter
  - 64× Delta-Sigma DAC
  - Analog Post Filter
- Adjustable System Sampling Rates including 32kHz, 44.1kHz & 48kHz
- 120 dB Signal-to-Noise Ratio
- Low Clock Jitter Sensitivity
- Completely Filtered Line-Level Outputs
  - Linear Phase Filtering
  - Zero Phase Error Between Channels
  - No External Components Needed
- Flexible Serial Interface for Either 16 or 18 bit Input Data

General Description

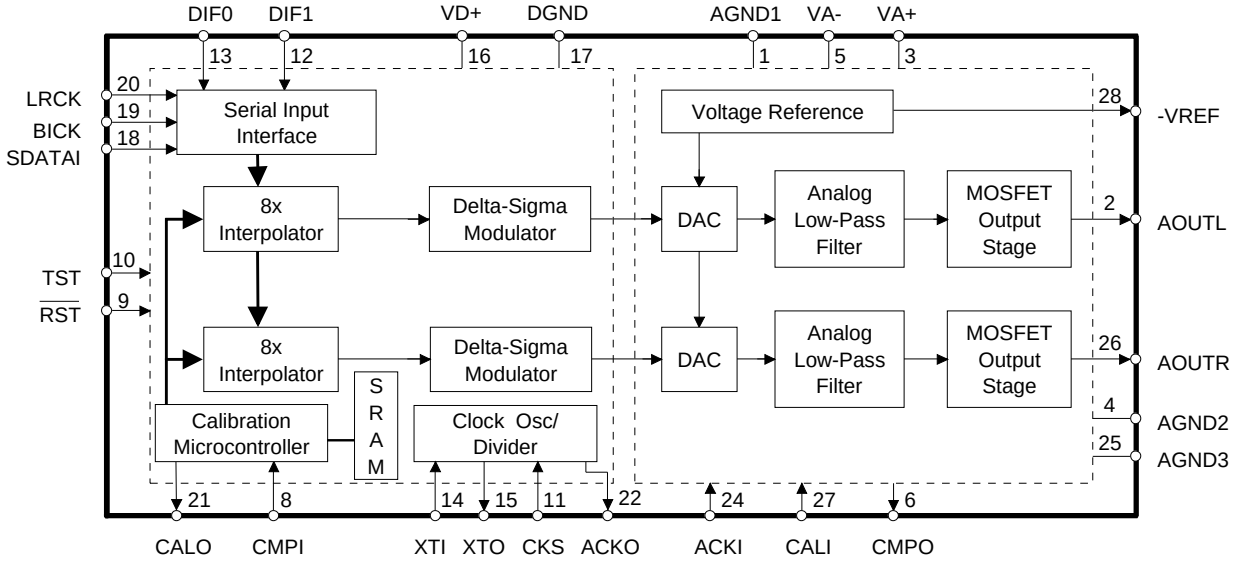
The CS4328 is a complete stereo digital-to-analog output system. In addition to the traditional D/A function, the CS4328 includes an 8× digital interpolation filter followed by a 64× oversampled delta-sigma modulator. The modulator output controls the reference voltage input to an ultra-linear analog low-pass filter. This architecture allows for infinite adjustment of sample rate between 1 kHz and 50 kHz while maintaining linear phase response simply by changing the master clock frequency.

The CS4328 also includes an extremely flexible serial port utilizing two select pins to support four different interface modes.

The master clock can be either 256 or 384 times the input word rate, supporting various audio environments.

ORDERING INFORMATION:

CS4328-KP	0 to 70 °C	28-pin Plastic DIP
CS4328-KS	0 to 70 °C	28-pin Plastic SOIC
CS4328-BP	-40 to +85 °C	28-pin Plastic DIP
CS4328-BS	-40 to +85 °C	28-pin Plastic SOIC
CDB4328	CS4328 Evaluation Board	



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ANALOG CHARACTERISTICS (T_A = 25°C for K grade, T_A = -40 to +85 °C for B grade; VA+,VD+ = 5V; VA- = -5V; Logic "1" = VD+; Logic "0" = DGND; Full-Scale Output Sinewave, 991 Hz; Input Word Rate = 48 kHz; Input Data = 18 Bits; BICK = 3.072 MHz; R_L = 10kΩ; Measurement Bandwidth is 10 Hz to 20 kHz, unweighted; unless otherwise specified.)

Parameter*	Symbol	CS4328-K Min	CS4328-K Typ	CS4328-K Max	CS4328-B Min	CS4328-B Typ	CS4328-B Max	Units
Specified Temperature Range	T_A	0		+70	-40		+85	°C
Resolution		16	-	-	16	-	-	Bits
Dynamic Performance								
Signal-to-Noise Ratio (A-weighted) (Note 1)	SNR	120	-	-	120	-	-	dB
Total Harmonic Distortion + Noise (A-Weighted)	THD+N							
0 dB Output,		-	-93	-90	-	-88	-85	dB
-20 dB Output,		-	-77	-73	-	-75	-70	dB
-60 dB Output,		-	-37	-33	-	-35	-30	dB
Deviation From Linear Phase (Note 2)	-	-	± 0.5	-	-	± 0.5	-	deg
Passband: to -3 dB corner (Notes 3, 4)	-	0	to	23.5	0	to	23.5	kHz
to 0.00025 dB corner (Notes 3, 4)		0	to	21.6	0	to	21.6	kHz
Frequency Response 10 Hz to 20 kHz (Note 2)	-	-0.05	+0.1	+0.2	-0.05	+0.1	+0.2	dB
Passband Ripple (Note 4)	-	-	-	0.00025	-	-	0.00025	dB
StopBand (Note 3)	-	26.4	-	-	26.4	-	-	kHz
StopBand Attenuation (Note 2)	-	90	-	-	90	-	-	dB
Group Delay (IWR = Input Word Rate)	tgd	-	33/IWR	-	-	33/IWR	-	s
Interchannel Isolation (1 kHz)	-	-100	-110	-	-95	-105	-	dB
dc Accuracy								
Interchannel Gain Mismatch	-	-	0.1	-	-	0.1	-	dB
Gain Error	-	-	-	± 5	-	-	± 5	%
Gain Drift	-	-	150	-	-	150	-	ppm/°C
Offset Error (after calibration)	-	-	-	± 1	-	-	± 1	mV
Analog Output								
Full Scale Output Voltage	VOUT	3.8	4.0	4.2	3.8	4.0	4.2	Vpp
Power Supplies								
Power Supply Current: VA+	IA+	-	40	55	-	40	55	mA
VA-	IA-	-	-40	-55	-	-40	-55	mA
VD+	ID+	-	50	60	-	50	60	mA
Power Dissipation	-	-	650	850	-	650	850	mW
Power Supply Rejection Ratio (1 kHz)	PSRR	-	50	-	-	50	-	dB

Notes:
1. Idle channel, digital input all zeros.
2. Combined digital and analog filter characteristics.
3. The passband and stopband edges scale with frequency. For input word rates, IWR, other than 48 kHz, the 0.00025 dB passband edge is 0.45×IWR and the stopband edge is 0.55×IWR.
4. Digital filter characteristics.

* Definitions are at the end of this data sheet. Specifications are subject to change without notice.

DIGITAL CHARACTERISTICS

(TA = 25 °C; VA+ ,VD+ = 5V ± 5%; VA- = -5V ± 5%)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	70%VD+	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	30%VD+	V
High-Level Output Voltage at Io = -20µA	V_{OH}	4.4	-	-	V
Low-Level Output Voltage at Io = 20µA	V_{OL}	-	-	0.1	V
Input Leakage Current (Note 5)	I_{in}	-	-	1.0	µA

Note: 5. TST, DIF0 & DIF1 have internal pull-down devices, nominally 90kΩ.

ABSOLUTE MAXIMUM RATINGS (AGND1-3, DGND = 0V, all voltages with respect to ground.)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Digital	VD+	-0.3	6.0	V
	Positive Analog	VA+	-0.3	6.0	V
	Negative Analog	VA-	0.3	-6.0	V
	|VA+ - VD+|		-	0.4	V
Input Current, Any Pin Except Supplies		I_{in}	-	±10	mA
Digital Input Voltage		V_{IND}	-0.3	(VD+)+0.4	V
Ambient Operating Temperature (power applied)		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AGND1, AGND2, AGND3, DGND = 0V; all voltages with respect to ground)

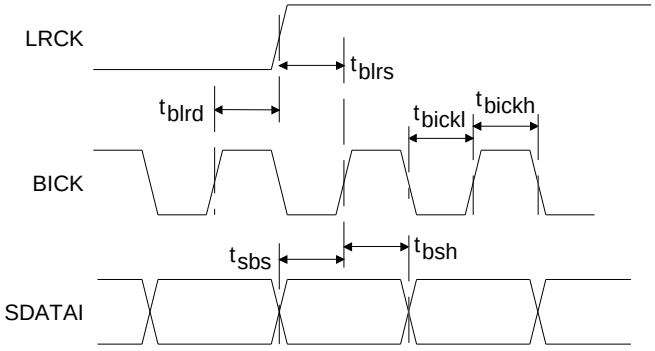
Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.75	5.0	5.25	V
	Positive Analog	VA+	4.75	5.0	5.25	V
	Negative Analog	VA-	-4.75	-5.0	-5.25	V
	|VA+ - VD+|		-	-	0.4	V

SWITCHING CHARACTERISTICS

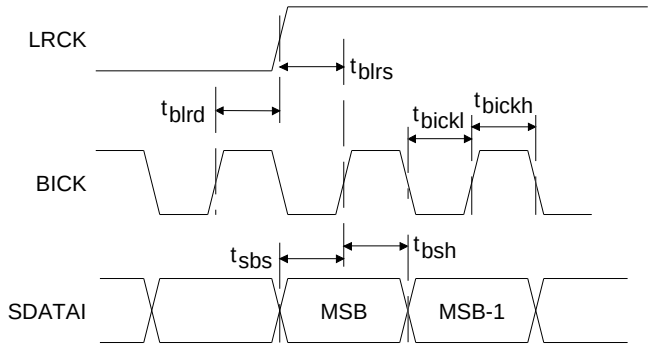
(T_A = 25 °C; VA+, VD+ = 5V ± 5%; VA- = -5V ± 5%; Inputs: Logic 0 = 0V, Logic 1 = VD+, C_L = 20 pF)

Parameter		Symbol	Min	Typ	Max	Units
Master Clock Frequency using Internal Oscillator:						
CKS=H		XTI/XTO	10.7	-	19.2	MHz
CKS=L		-	7.1	-	13.9	MHz
Master Clock Frequency using External Clock:						
CKS=H		XTI/XTO	0.384	-	19.2	MHz
CKS=L		-	0.256	-	13.9	MHz
XTI/XTO Pulse Width Low		-	21	-	-	ns
XTI/XTO Pulse Width High		-	21	-	-	ns
BICK Pulse Width Low		t_{bickl}	30	-	-	ns
BICK Pulse Width High		t_{bickh}	30	-	-	ns
BICK Period		t_{bickw}	80	-	-	ns
BICK rising to LRCK edge delay	(Note 6)	t_{blrd}	35	-	-	ns
BICK rising to LRCK edge setup time	(Note 6)	t_{blrs}	35	-	-	ns
SDATAI valid to BICK rising setup time	(Note 6)	t_{sbs}	35	-	-	ns
BICK rising to SDATAI hold time	(Note 6)	t_{bsh}	35	-	-	ns
$\overline{RST}$ Minimum Pulse Width Low		2 periods of XTI/XTO				

Note: 6. "BICK rising" refers to modes 0, 1, and 3. For mode 2, replace "BICK rising" with "BICK falling."



Serial Input Timing (Modes 0, 1, &3)



Serial Input Timing (Mode 2)

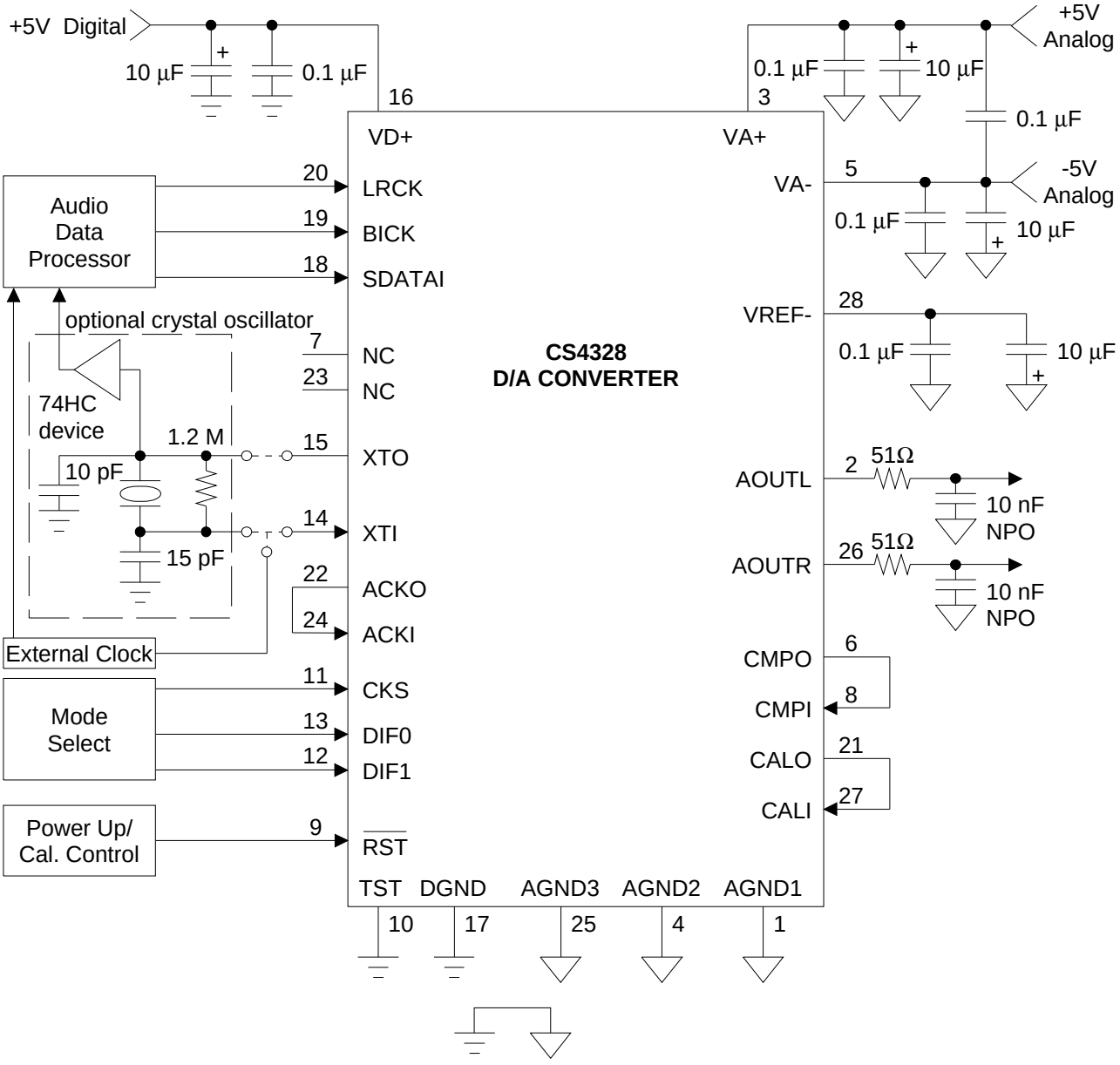


Figure 1. Typical Connection Diagram

GENERAL DESCRIPTION

The CS4328 is a complete stereo digital-to-analog system designed for digital audio. The system accepts data at standard audio frequencies, such as 48 kHz, 44.1 kHz, and 32 kHz; and produces line-level outputs.

The architecture includes an 8× oversampling filter followed by a 64× oversampled one-bit delta-sigma modulator. The output from the one bit modulator controls the polarity of a reference voltage which is then passed through an ultra-linear analog low-pass filter. The result is line-level outputs with no need for further filtering.

SYSTEM DESIGN

Very few external components are required to support the DAC. Normal power supply decoupling components and voltage reference bypass capacitors are all that's required.

System Clock Input

The master clock (XTI/XTO) input to the DAC is used to operate the digital interpolation filter and the delta-sigma modulator. The master clock can be either a crystal placed across the XTI and XTO pins, or an external clock input to the XTI pin with the XTO pin left floating.

The frequency of XTI/XTO is determined by the desired Input Word Rate, IWR, and the setting of the Clock Select pin, CKS. IWR is the frequency at which words for each channel are input to the DAC and is equal to LRCK frequency. Setting CKS low selects an XTI/XTO frequency of 256× IWR while setting CKS high selects 384× IWR. The ACKO pin will always be 128× IWR and is used by the analog low-pass smoothing filter. Table 1 illustrates various audio word rates and corresponding frequencies used in the DAC.

LRCK (kHz)	CKS	XTI/XTO (MHz)	ACKO (MHz)
32	low	8.192	4.096
32	high	12.288	4.096
44.1	low	11.2896	5.6448
44.1	high	16.9344	5.6448
48	low	12.288	6.144
48	high	18.432	6.144

Table 1. Common Clock Frequencies

The remaining system clocks, LRCK and BICK, must be synchronously derived from XTI/XTO. If the CS4328 internal oscillator is used, the circuit must be configured and XTO buffered as shown in Figure 1. XTI/XTO can be divided to produce LRCK and BICK using a synchronous counter such as 74HC590. Notice that the value of the capacitor on XTO is 10 pF and the XTI capacitor is 15 pF, which allows for 5 pF of gate and stray capacitance.

It is also possible to divide ACKO, 128× IWR, to derive BICK and LRCK. However, external circuitry must be used to apply a "kick-start" pulse to LRCK in order to activate ACKO. The sequence for the cancellation of RESET, beginning of calibration and activation of ACKO is shown in Figure 2 with the required transitions indicated by arrows. A momentary loss of XTI/XTO or power will require a "kick-start" pulse to resume operation.

Serial Data Interface

Data is input to the CS4328 via three serial input pins; SDATAI is the serial data input, BICK is the serial data clock and LRCK defines the channel and delineation of data. The DAC supports four serial data formats which are selected via the digital input format pins DIF0 and DIF1. The different formats control the relationship of LRCK to SDATAI and the edge of BICK used to

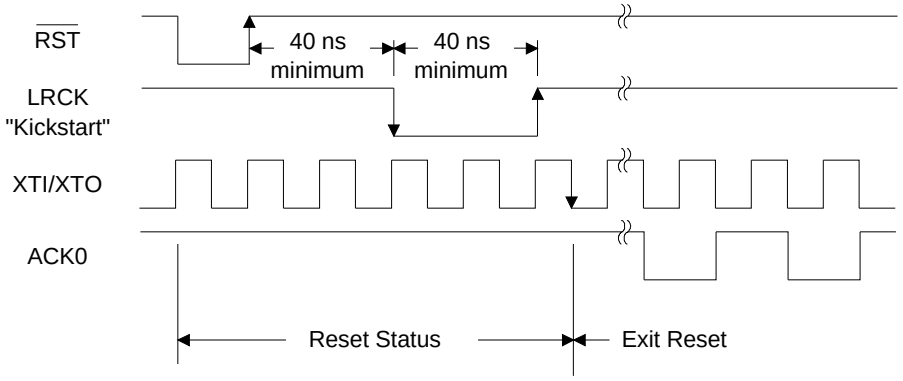


Figure 2. RESET Cancellation Timing

latch data. Table 2 lists the four formats, along with the associated figure number. Format 0 is compatible with existing 16-bit D/A converters and digital filters. Format 1 is an 18-bit version of format 0. Format 2 is similar to Crystal ADCs and many DSP serial ports. Format 3 is compatible with the I^2S serial data protocol. Formats 2 and 3 support 18-bit input or 16-bit followed by two zeros. In all four serial input modes, the serial data is MSB-first and 2's-complement format.

Formats 0, 2 and 3 will operate with 16-bit data and 16 BICK pulses as well. See Figure 6 for 16-bit timing. However, the use of BICK = 64× IWR is recommended to minimize the possibility of performance degradation resulting from BICK coupling into VREF-.

DIF1	DIF0	Mode	Figure
0	0	0	3
0	1	1	3
1	0	2	4
1	1	3	5

Table 2. Digital Input Formats

Reset and Offset Calibration

$\overline{\text{RST}}$ is an active low signal that resets the digital filter and the delta-sigma modulator, synchronizes LRCK with internal control signals and starts an offset calibration cycle upon exiting reset. When $\overline{\text{RST}}$ goes low, CALO goes high and stays high until the end of an offset calibration cycle. An offset calibration cycle takes 1024 IWR cycles to complete. CALO must be connected to CALI and CMPO must be connected to CMPI for offset calibration. During an offset calibration the analog output is forced to zero.

Power-Up Considerations

Upon initial application of power to the DAC, offset calibration and digital filter registers will be indeterminate. $\overline{\text{RST}}$ should be low during power-up to activate an internal mute and prevent this erroneous information from being output from the DAC. Bringing $\overline{\text{RST}}$ high will begin a calibration cycle and initialize these registers.

Muting

There are two types of mutes that can be implemented with the CS4328. The first is a -50 dB

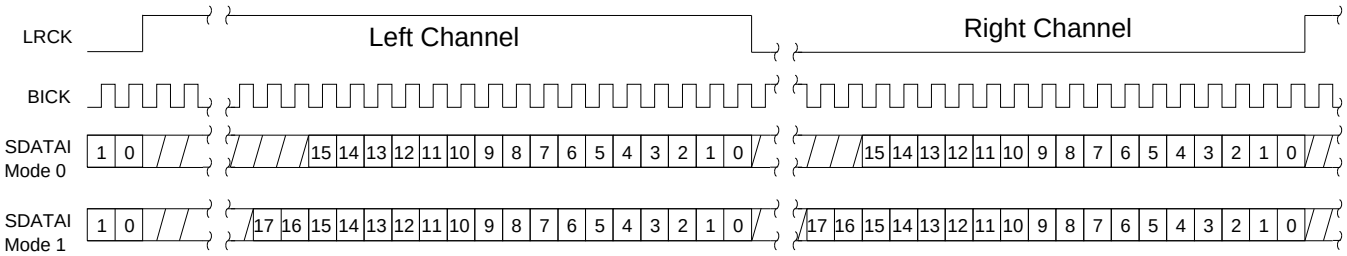


Figure 3. Digital Input Formats 0 & 1

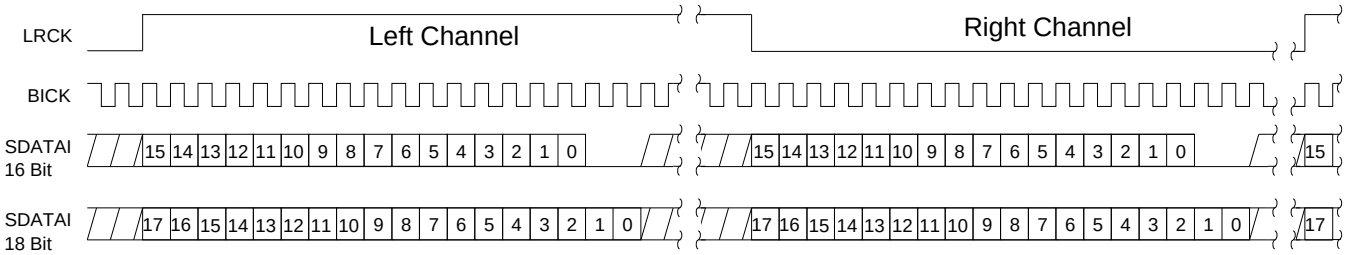


Figure 4. Digital Input Format 2

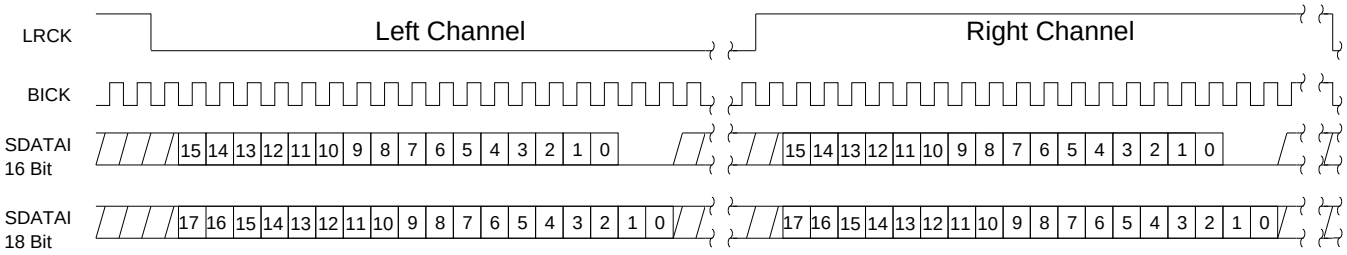
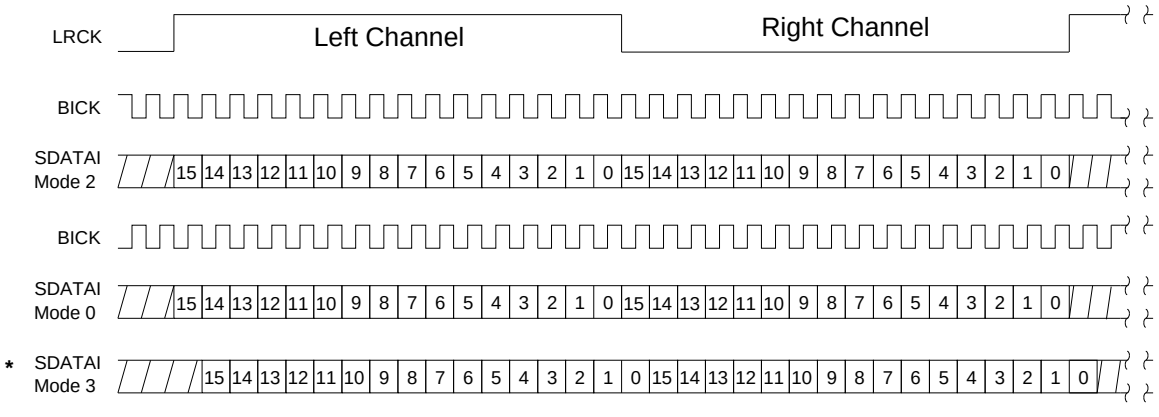


Figure 5. Digital Input Format 3



***** LRCK must be inverted.

Figure 6. Digital Input Formats 0, 2 and 3 with 16 BICK Periods

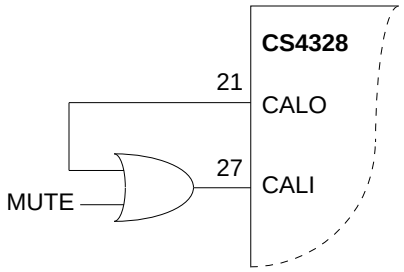


Figure 7. -50dB Muting

mute which can be activated by forcing the CALI pin high. Figure 7 shows how to implement a -50 dB mute using an OR gate. The propagation of the gate will be the only delay in moving the CS4328 to a muted state.

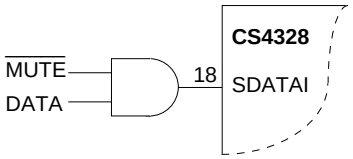


Figure 8. -120 dB Muting

The second mute option is a two stage operation which involves forcing SDATAI to 0 using an AND gate as shown in Figure 8. The first mute occurs following 33 LRCK cycles when the 0 input data propagates to the output of the DAC. The rms noise present at the output will typically be 93 dB below fullscale. Following a total of 4096 LRCK cycles with 0 input data the output of the CS4328 will mute and lower the output rms noise to a minimum of 120 dB below fullscale. Upon release of the MUTE command and non-zero input data the CS4328 output mute will immediately release. However, 33 LRCK cycles are required for input data to propagate to the output of the CS4328.

Grounding and Power Supply Decoupling

As with any high resolution converter, the CS4328 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 1 shows the recommended power arrangements with VA+ connected to a clean +5 volt supply and VA- connected to a clean -5 volt supply. VD+, which powers the digital interpolation filter and delta-sigma modulator, may be powered from the system +5 volt logic supply. Decoupling capacitors should be located as near to the CS4328 as possible.

The printed circuit board layout should have separate analog and digital regions with individual ground planes. The CS4328 should straddle the ground plane break as shown on the CDB4328 Evaluation board. Optional jumpers for connecting these planes should be included near the DAC, where power is brought on to the board and near the regulators. All signals, especially clocks, should be kept away from the VREF- pin to avoid unwanted coupling into the CS4328. The VREF- decoupling capacitors, particularly the 0.1 µF, must be positioned to minimize the electrical path from VREF- to Pin 1 AGND and to minimize the path between VREF- and the capacitors. Extensive use of ground plane fill on both the analog and digital sections of the circuit board will yield large reductions in radiated noise effects. An application note "*Layout and Design Rules for Data Converters*" is printed in the Application Note section of this book.

Analog Output and Filtering

Full scale analog output for each channel is typically 4V peak-to-peak. The analog outputs can drive load impedances as low as 600Ω and are short-circuit protected to 20mA.

The CS4328 analog filter is a 5th order switched-capacitor filter followed by a second-order continuous-time filter. The switched-capacitor filter is clock dependent and will scale with the IWR frequency. The continuous-time filter is fixed and not related to IWR. A low-pass filter consisting of a 51Ω resistor and a .01 µF NPO capacitor is recommended on the analog outputs.

Performance Plots

The following collection of CS4328 measurement plots (IWR = 48 kHz) were taken with an Audio Precision Dual Domain System One. All FFT plots are 16,384 point.

Figure 9 shows the **frequency response** with a 48 kHz input word rate. The response is very flat out to half the input word rate.

Figure 10 shows the **muted noise** with all zeros data into the CS4328. This plot is dominated by the noise floor of the System One.

Figure 11 shows the **unmuted noise**. This data was taken by feeding the CS4328 continuous zeros, but pulling CALI low. This unmutes the output stage of the CS4328. This plot shows the noise shaping characteristics of the delta-sigma modulator combined with the analog filter.

Figure 12 shows the A-weighted **THD+N vs signal amplitude** for a dithered 1kHz input signal. Notice that there is no increase in distortion as the signal level decreases. This indicates very good low-level linearity, one of the key benefits of the delta-sigma technique.

Figure 13 shows the **fade-to-noise linearity** test result using track 20 of the CBS CD-1. The input test signal is a dithered 500 Hz sine wave which gradually fades from -60 dB level to -120 dB. During the fading, the output level from the CS4328 is measured and compared to the ideal level. Notice the very close tracking of the output level to the ideal, even at low level inputs of -90 dB. The gradual shift of the plot away from zero at signal levels < -100 dB is caused by the background noise starting to dominate the measurement.

Figure 14 shows the **impulse response**, taken from the single positive full scale value on track 17 of the CD-1 test disk. Notice the high degree of symmetry, indicating good phase linearity.

Figure 15 shows a 16K **FFT plot result, with a 1 kHz -90 dB dithered input**. Notice the complete lack of distortion components and tones.

Figure 16 shows a bandlimited, 10 Hz to 22 kHz, **time domain plot** of the CS4328 output with a **1 kHz, -90 dB dithered** input. Notice the clear residual sine wave shape, in the presence of noise.

Figure 17 shows the **monotonicity test** result plot. The input data to the CS4328 is +1 LSB, -1 LSB four times, then +2 LSB, -2 LSB four times and so on, until +10 LSB, -10 LSB. This data pattern is taken from track 21 of the CD-1 test disk. Notice the increasing staircase envelope, with no decreasing elements. Notice also the clear resolution of the LSB. For this test, one LSB is a 16-bit LSB.

The following tests were done by filtering the analog output of the CS4328 with the System One analyzer 1 kHz notch filter to reduce the peak signal level. The resulting signal was then amplified and applied to the DSP module, avoiding distortion in the System One A/D converter.

Figure 18 shows a **16K FFT Plot with a 1 kHz, 0 dB** input. Notice the low order harmonic distortion at < -100 dB.

Figure 19 shows a **16K FFT Plot with a 1 kHz, -10 dB** input. Notice the almost complete absence of distortion, with a small residual 2nd harmonic at -110 dB.

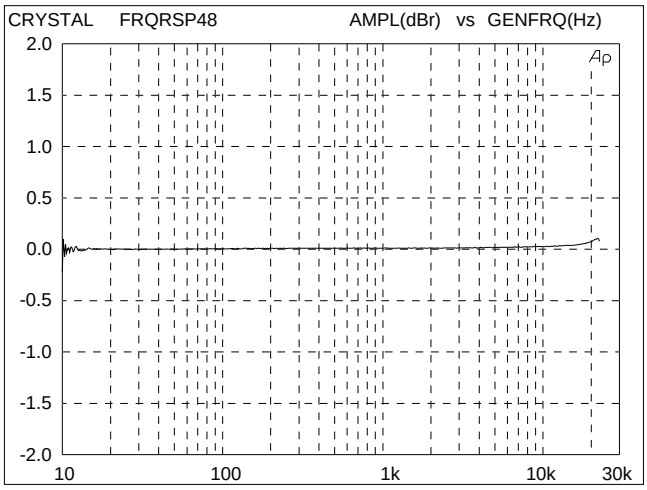


Figure 9. Frequency Response (48 kHz word rate)

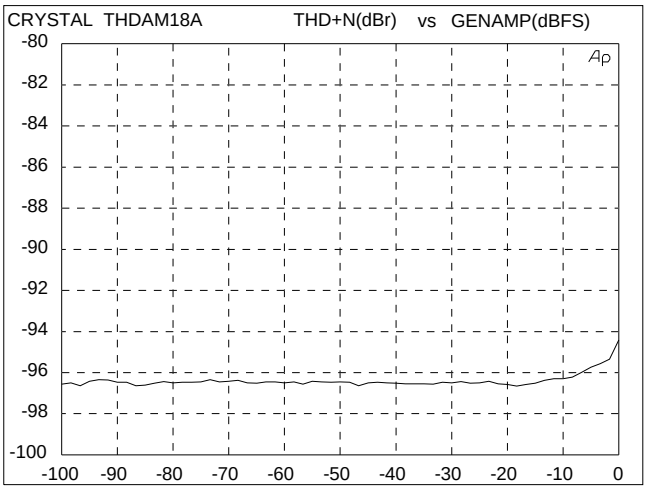


Figure 12. THD+N vs 18-bit Input Signal Level

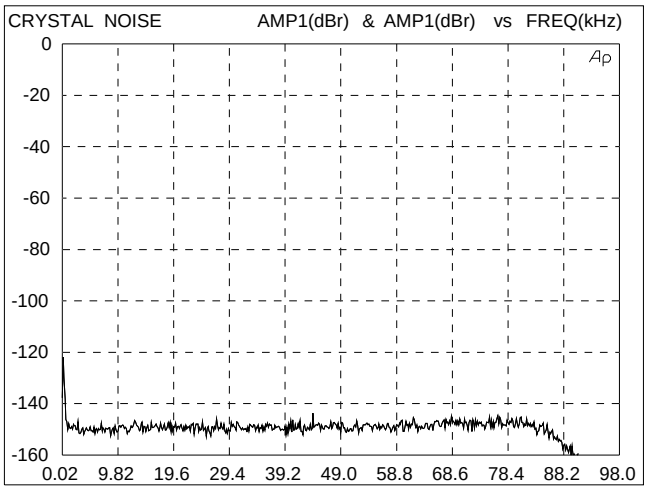


Figure 10. Muted Idle Channel Noise

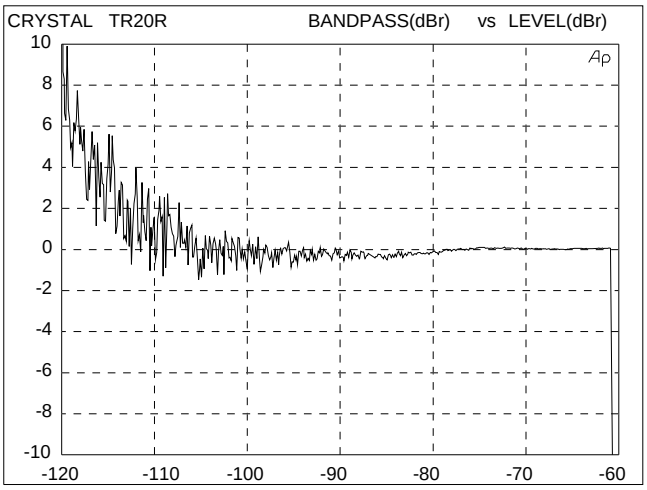


Figure 13. Fade-to-Noise Linearity

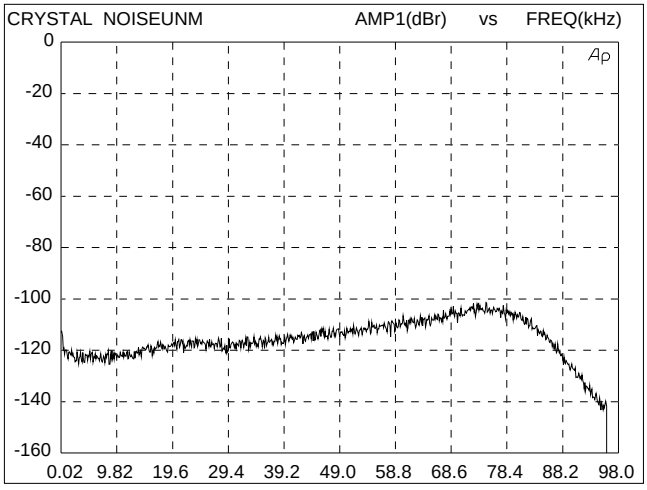


Figure 11. Unmuted Idle Noise

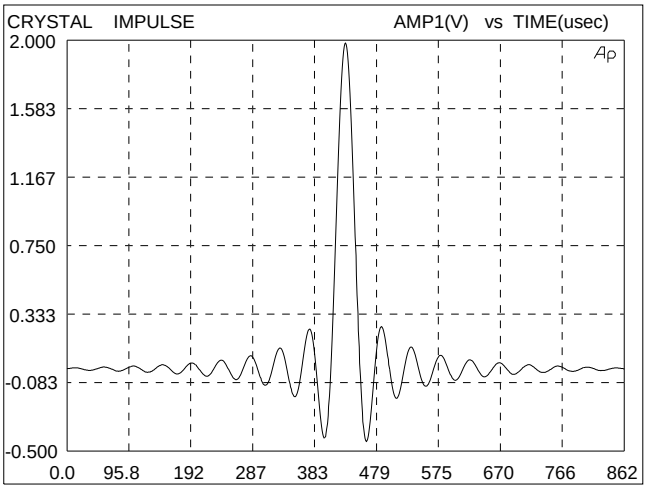


Figure 14. Impulse Response

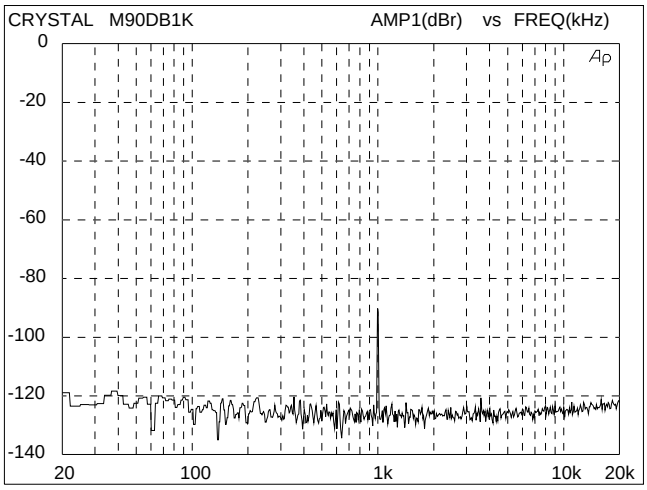


Figure 15. 1 kHz, -90 dB Input FFT Plot

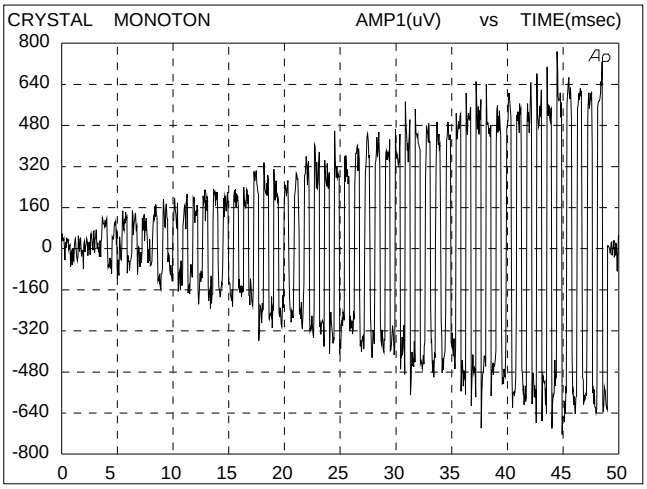


Figure 17. Monotonicity Test (16-bit data)

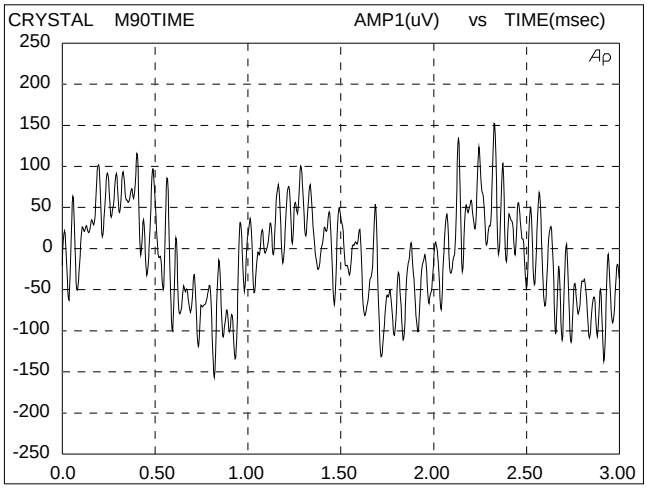


Figure 16. 1 kHz, -90 dB Input Time Domain Plot

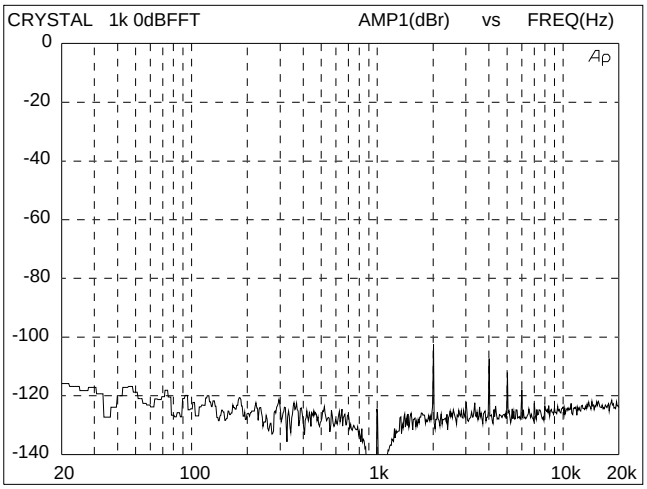


Figure 18. 1 kHz, 0 dB Input FFT Plot

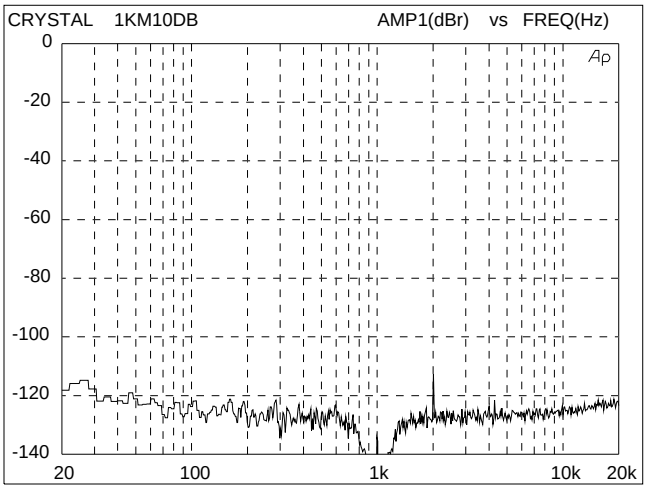


Figure 19. 1 kHz, -10 dB Input FFT Plot

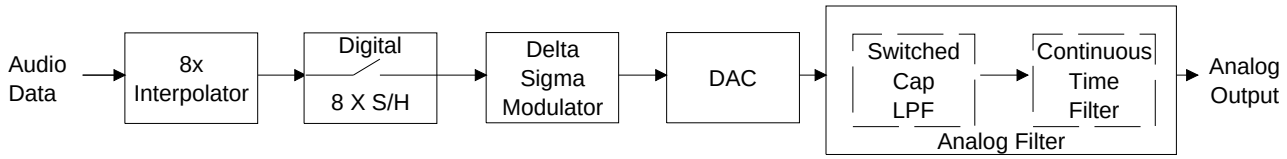


Figure 20. CS4328 Architecture

THEORY OF OPERATION

The CS4328 architecture can be considered in five blocks: Interpolation, sample/hold, delta-sigma modulation, D/A conversion, and analog filtering.

Audio data is input to the CS4328 digital interpolation filter which removes images of the input signal that are present at multiples of the input sample frequency, Fs (Figure 21). Following the interpolation stage, the resulting frequency spectrum has images of the input signal at multiples of eight times the input sample frequency, 8× Fs (Figure 22). Eliminating the images between Fs and 8× Fs greatly relaxes the requirements of the analog filtering, allowing the suppression of images while leaving the audio band of interest unaltered.

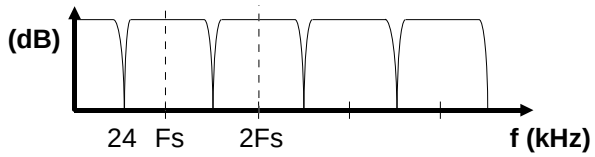


Figure 21. Input Data Spectrum

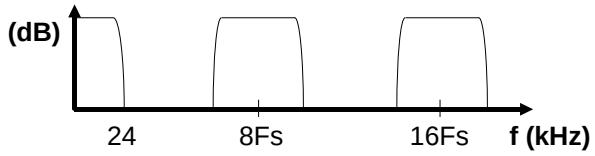


Figure 22. 8X Interpolated Data Spectrum

The CS4328 interpolation stage is followed by a sample-and-hold function where the data points from the interpolator are held for eight (64× Fs) clock cycles. The resulting frequency response is a sinx/x characteristic with zeros at 8× Fs multiples. The sinx/x zeros completely attenuate signals at 8× Fs and largely suppress the remaining energy of the images (Figure 23). The 8× interpolation followed by the 8× sample-and-hold results in data at a rate of 64× Fs.

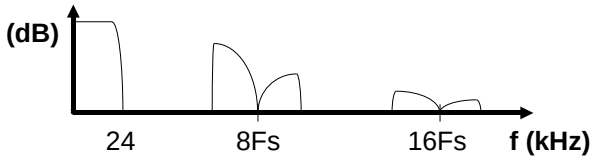


Figure 23. Spectrum After S/H

The delta-sigma modulator takes in the 64× Fs data (3.072 MHz for 48kHz sampled systems) and performs fifth-order noise shaping. In the digital modulator of the CS4328, 18-bit audio data is modulated to a 1-bit, 64× Fs signal. The 5th-order noise shaper allows 1-bit quantization to support 18-bit audio processing by suppressing quantization noise in the bandwidth of interest. Figure 24 shows the frequency spectrum of the modulator output.

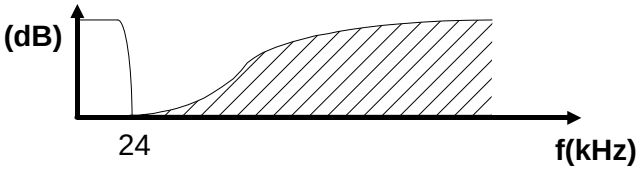


Figure 24. Modulator Output Spectrum

The CS4328's digital modulator is followed by a D-to-A converter that translates the 1-bit signal into a series of charge packets. The magnitude of the charge in each packet is determined by sampling of a voltage reference onto a switched

capacitor, where the polarity of each packet is controlled by the 1-bit signal. The result is a 1-bit D/A conversion process that is very insensitive to clock jitter. This is a major improvement over previous generations of 1-Bit D/A converters where the magnitude of charge in the D/A process is determined by switching a current reference for a period of time defined by periods of the master clock.

The final stage of the CS4328 is made up of a 5th order switched-capacitor low pass filter and a 2nd order continuous time filter. The switched-capacitor filter eliminates out-of-band energy resulting from the noise shaping process (Figure 25). The switched-capacitor stage scales with the master clock signal being applied to the CS4328. The final stage is a 2nd order continuous time filter that eliminates high frequency energy that appears at multiples of the 64× Fs sample rate (Figure 26).

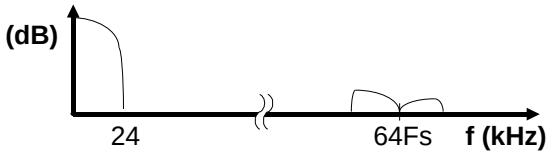


Figure 25. Spectrum After Switched-Capacitor Filter

Figure 26. Spectrum After Continuous Time Filter

Figures 27-30 are computer simulations of the combined response of the CS4328 digital and analog filters with an input word rate of 48 kHz.

Figure 27 shows the individual and combined phase response of the CS4328 filters. Notice the digital filter equalization of the analog filter to produce a linear phase response.

Figures 28-30 are plots of the CS4328 magnitude response.

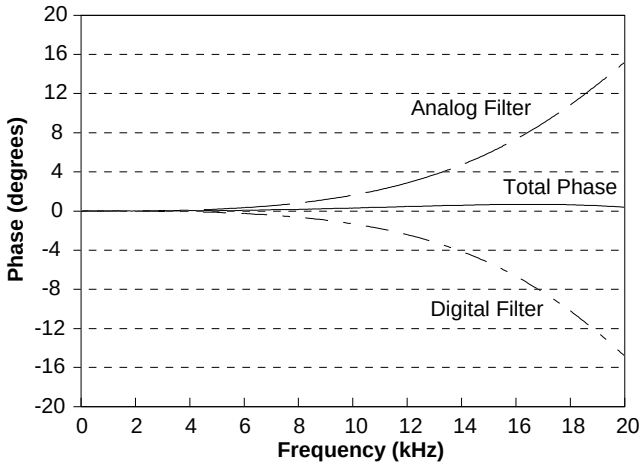


Figure 27. Deviation From Linear Phase

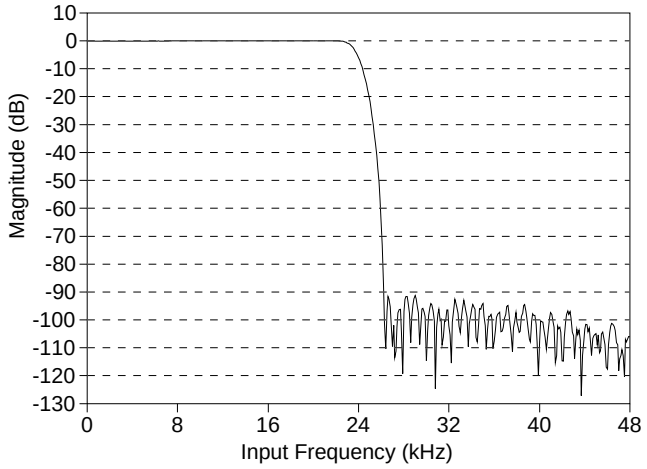


Figure 28. Combined Digital and Analog Filter Frequency Response

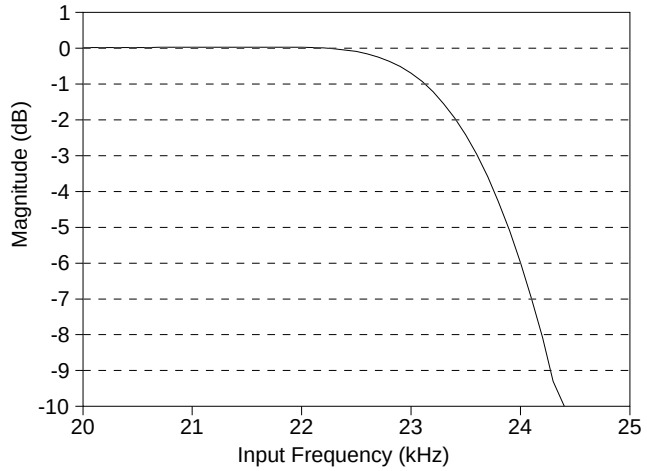


Figure 29. Combined Digital and Analog Filter Frequency Response

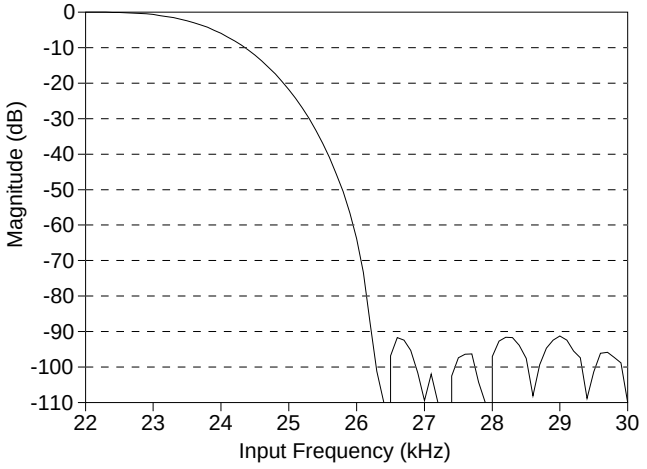
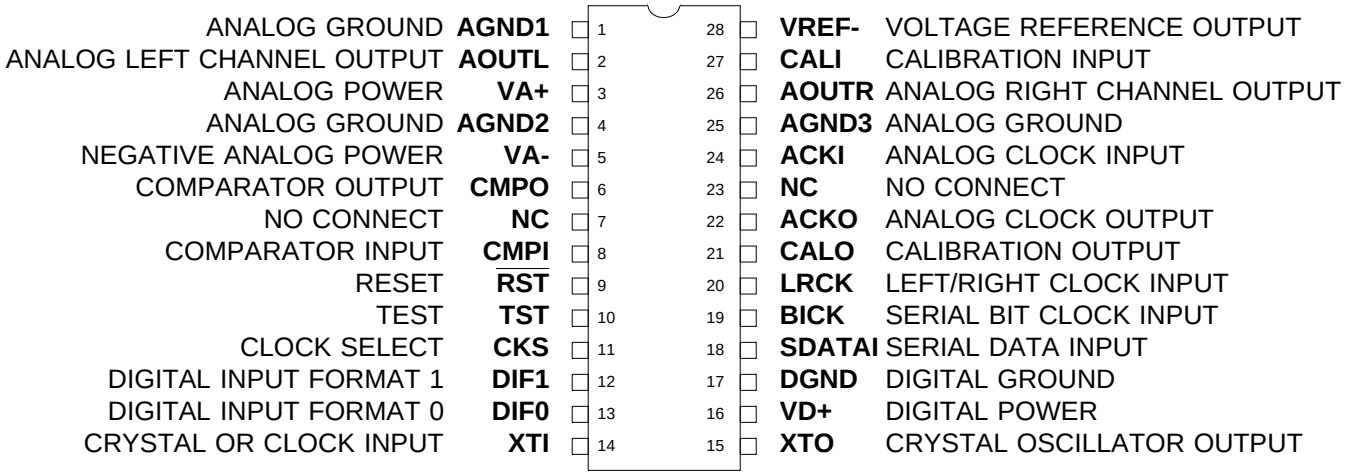


Figure 30. Combined Digital and Analog Filter Transition Band

PIN DESCRIPTIONS



Power Supply Connections

VA+ - Positive Analog Power, PIN 3.
Positive analog supply. Nominally +5 volts.

VA- - Negative Analog Power, PIN 5.
Negative analog supply. Nominally -5 volts.

AGND1, AGND2, AGND3 - Analog Grounds, PINS 1, 4, 25.
Analog ground reference.

VD+ - Positive Digital Power, PIN 16.
Positive supply for the digital section. Nominally +5 volts.

DGND - Digital Ground, PIN 17.
Digital ground for the digital section.

Analog Outputs

VREF- - Voltage Reference Output, PIN 28.
Nominally -3.68 volts. Normally connected to a 0.1µF ceramic capacitor in parallel with a 10µF or larger electrolytic capacitor. Note the negative output polarity.

AOUTL - Analog Left Channel Output, PIN 2.
Analog output for the left channel. Typically 4V peak-to-peak for a full-scale input signal.

AOUTR - Analog Right Channel Output, PIN 26.
Analog output for the right channel. Typically 4V peak-to-peak for a full-scale input signal.

Digital Inputs

XTI - Crystal or Clock Input, PIN 14.

A crystal oscillator can be connected between this pin and XTO, or an external CMOS clock can be input on XTI. The frequency must be either 256× or 384× the input word rate based on the clock select pin, CKS.

ACKI - Analog Clock Input, PIN 24.

This is the master clock input for the analog section of the chip and must be 128× the input word rate. ACKI is typically connected to the Analog Clock Ouput pin, ACKO.

CALI - Calibration Input, PIN 27.

Input to the analog section that is used during offset calibration. Normally connected to the Calibration Output pin, CALO.

CMPI - Comparator Input, PIN 8

Input to the digital section that is used during offset calibration. Normally connected to the Comparator Output pin, CMPO.

LRCK - Left/Right Clock, PIN 20.

This input determines which channel is currently being input on the Serial Data Input pin, SDATAI. The format of LRCK is controlled by DIF0 and DIF1.

BICK - Serial Bit Input Clock, PIN19.

Clocks the individual bits of the serial data in from the SDATAI pin. The edge used to latch SDATAI is controlled by DIF0 and DIF1.

SDATAI - Serial Data Input, PIN 18.

Two's complement MSB-first serial data of either 16 or 18 bits is input on this pin. The data is clocked into the CS4328 via the BICK clock and the channel is determined by the LRCK clock. The format for the previous two clocks is determined by the Digital Input Format pins, DIF0 and DIF1

DIF0,DIF1 - Digital Input Format, PINS 13, 12

These two pins select one of four formats for the incoming serial data stream. These pins set the format of the BICK and LRCK clocks with respect to SDATAI. The formats are listed in Table 2.

CKS - Clock Speed Select, PIN 11.

Selects the clock frequency input on the XTI pin. CKS low selects 256× the input word rate (LRCK frequency) while CKS high selects 384×.

$\overline{\text{RST}}$ - Reset and Calibrate, PIN 9.

When reset is low the filters and modulators are held in reset. When reset goes high, an offset calibration is initiated.

Digital Outputs

XTO - Crystal Oscillator Output, PIN 15.

When a crystal oscillator is used, it is tied between this pin and XTI. When an external clock is input, this pin should be left floating.

ACKO - Analog Clock Output, PIN 22.

This output is 128× the input word rate (LRCK frequency). Normally connected to the Analog Clock Input pin, ACKI.

CALO - Calibration Output, PIN 21.

Used during offset calibration. Must be connected to the Calibration Input pin, CALI.

CMPO - Comparator Output, PIN 6.

Used during offset calibration. Must be connected to the Comparator Input pin, CMPI.

Miscellaneous

NC - No Connection, PINS 7, 23.

These two pins are bonded out to test outputs. They must not be connected to any external component or any length of PC trace.

TST -Test Input, PIN 10.

Allows access to the CS4328 test modes, which are reserved for factory use. Must be tied to DGND.

PARAMETER DEFINITIONS

Total Harmonic Distortion + Noise - The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels.

Signal-to-Noise Ratio - The ratio of the full scale rms value of the signal to the rms sum of all other spectral components over the specified bandwidth with an input of all zeros.

Frequency Response - A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

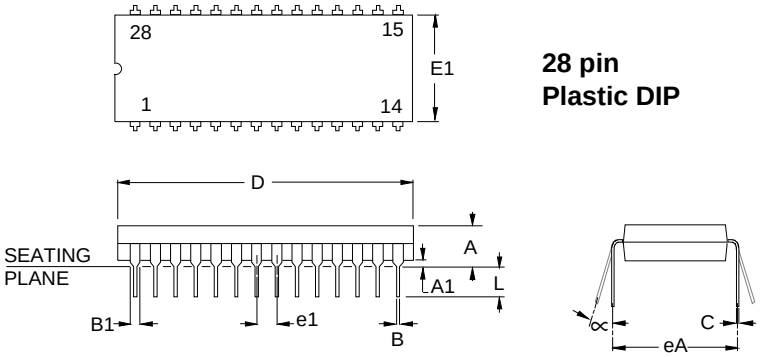
Interchannel Isolation - A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with all zeros to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch - The gain difference between left and right channels. Units in decibels.

Gain Error - The deviation from the nominal full scale analog output for a full scale digital input.

Gain Drift - The change in gain value with temperature. Units in ppm/°C.

Offset Error - The deviation of the mid-scale transition (111...111 to 000...000) from the ideal (AGND). Units in mV.

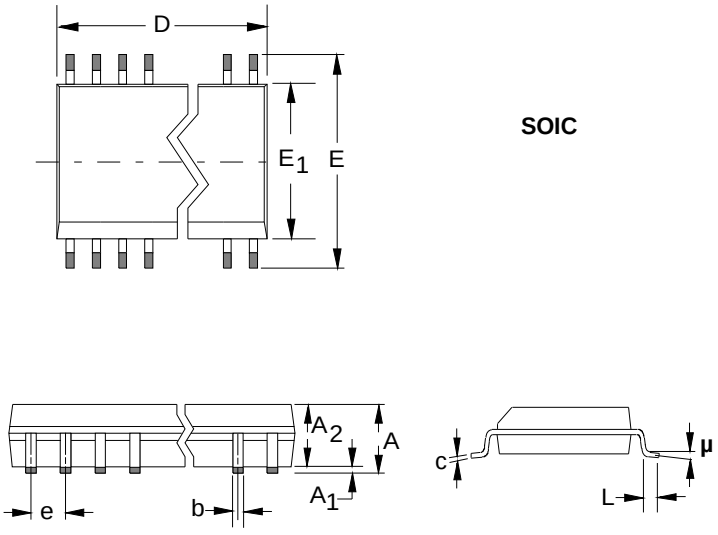


28 pin
Plastic DIP

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	3.94	4.32	5.08	0.155	0.170	0.200
A1	0.51	0.76	1.02	0.020	0.030	0.040
B	0.36	0.46	0.56	0.014	0.018	0.022
B1	1.02	1.27	1.65	0.040	0.050	0.065
C	0.20	0.25	0.38	0.008	0.010	0.015
D	36.45	36.83	37.21	1.435	1.450	1.465
E1	13.72	13.97	14.22	0.540	0.550	0.560
e1	2.41	2.54	2.67	0.095	0.100	0.105
eA	15.24	-	15.87	0.600	-	0.625
L	3.18	-	3.81	0.125	-	0.150
∝	0°	-	15°	0°	-	15°

NOTES:

1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25mm (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION eA TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION E1 DOES NOT INCLUDE MOLD FLASH.



SOIC

pins	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
16	9.91	10.16	10.41	0.390	0.400	0.410
20	12.45	12.70	12.95	0.490	0.500	0.510
24	14.99	15.24	15.50	0.590	0.600	0.610
28	17.53	17.78	18.03	0.690	0.700	0.710

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.41	2.54	2.67	0.095	0.100	0.105
A_1	0.127	-	0.300	0.005	-	0.012
A_2	2.29	2.41	2.54	0.090	0.095	0.100
b	0.33	0.46	0.51	0.013	0.018	0.020
c	0.203	0.280	0.381	0.008	0.011	0.015
D	see table above					
E	10.11	10.41	10.67	0.398	0.410	0.420
E_1	7.42	7.49	7.57	0.292	0.295	0.298
e	1.14	1.27	1.40	0.040	0.050	0.055
L	0.41	-	0.89	0.016	-	0.035
μ	0°	-	8°	0°	-	8°

A Cirrus Logic Company

CDB4328

CS4328 Evaluation Board

Features

- Demonstrates recommended layout and grounding arrangements
- CS4328 Supports multiple input formats
- CS8412 Receives AES/EBU, S/PDIF, & EIAJ-340 Compatible Digital Audio
- Digital and Analog Patch Areas
- Operation with on-board CS8412 or externally supplied system timing

General Description

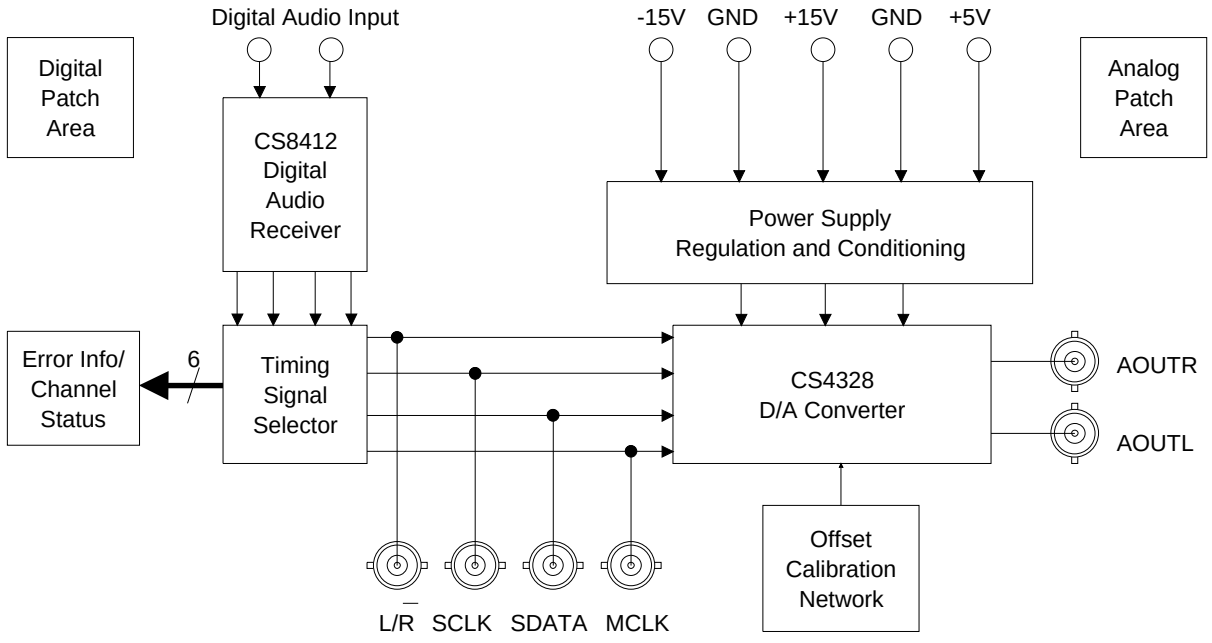
The CDB4328 evaluation board allows fast evaluation of the CS4328 18-bit, stereo D/A converter. The board provides an analog output interface via BNC connectors for both channels. Evaluation requires an analog signal analyzer, a digital signal source, and a power supply.

Also included is a CS8412 digital audio receiver I.C., which will accept AES/EBU, S/PDIF, and EIAJ-340 compatible audio data. The CS8412 can provide the system timing necessary to operate the CS4328.

The evaluation board may also be configured to accept external timing signals for operation in a user application during system development.

ORDERING INFORMATION: CDB4328

Block Diagram



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581
http://www.crystal.com

Power Supply Circuitry

Figure 1 shows the evaluation board power supply circuitry. Power is supplied to the evaluation board by five binding posts. The ±5 V analog power supply inputs of the converter are derived from ± 15 V using the voltage regulators U5 and U6. The +5 V digital supply for the converter and the discrete logic on the board is provided by the +5 V and DGND binding posts. D1, D2, and D3 are transient suppressors which also provide protection from incorrectly connected power supply leads. C1-C8 provide general power supply filtering for the analog supplies. As shown in Figure 2, C20-C24 provide localized decoupling for the converter VA+ and VA- pins. Note that C22 is connected between VA- and VA+ and not VA- and AGND. The evaluation board uses both an analog and a digital ground plane which are connected at J1. This ground plane arrangement isolates the board's digital logic from the analog circuitry.

Offset Calibration & Reset Circuitry

Figure 1, shows the offset calibration circuit provided on the evaluation board. Upon power-up, this circuit provides a pulse on the Digital to Analog Converter's $\overline{RST}$ pin initiating an offset calibration cycle. Pressing and releasing S2 also initiates an offset calibration cycle.

Serial Data Interface

Figure 1 shows that there are two options for inputing serial data into the CS4328. Serial data can be provided via the SDATA BNC connector on the evaluation board. BNC connectors for SCLK, the serial data input clock, and L/$\overline{R}$, the clock that defines the channel and delineates the data, are also provided on the evaluation board. This information can also be provided by the on-board CS8412. JP3 selects the source of SDATA, SCLK, and L/$\overline{R}$ that will be provided to the converter. JP3 selections are shown in Table 1.

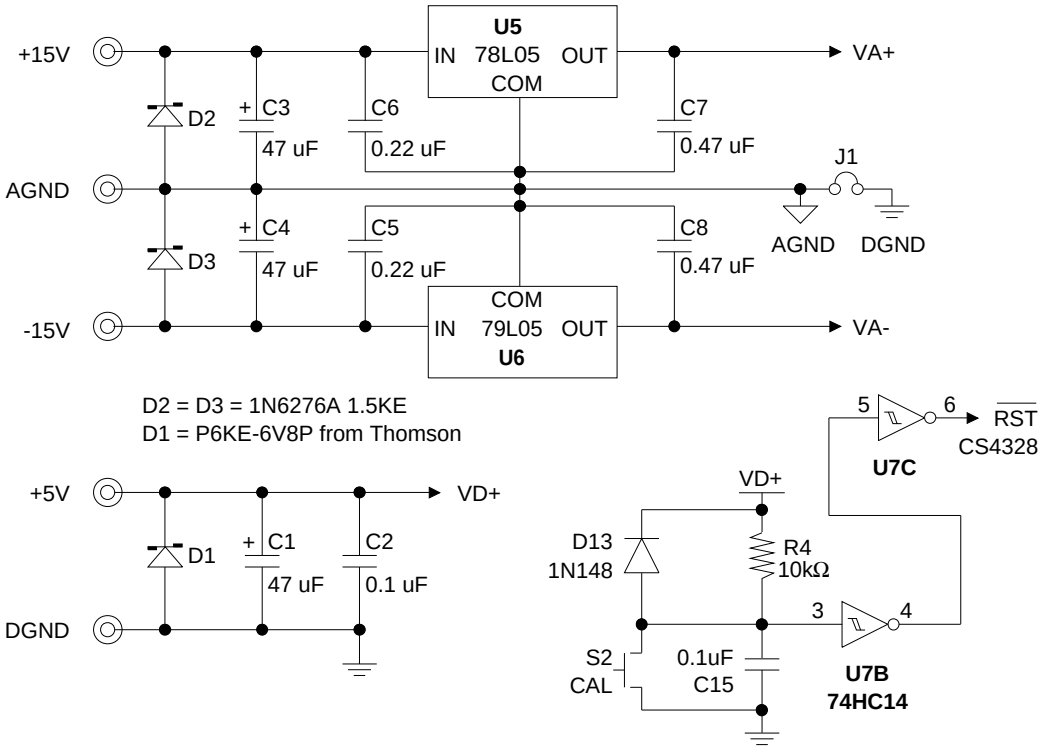


Figure 1. Power Supply and Reset Circuitry

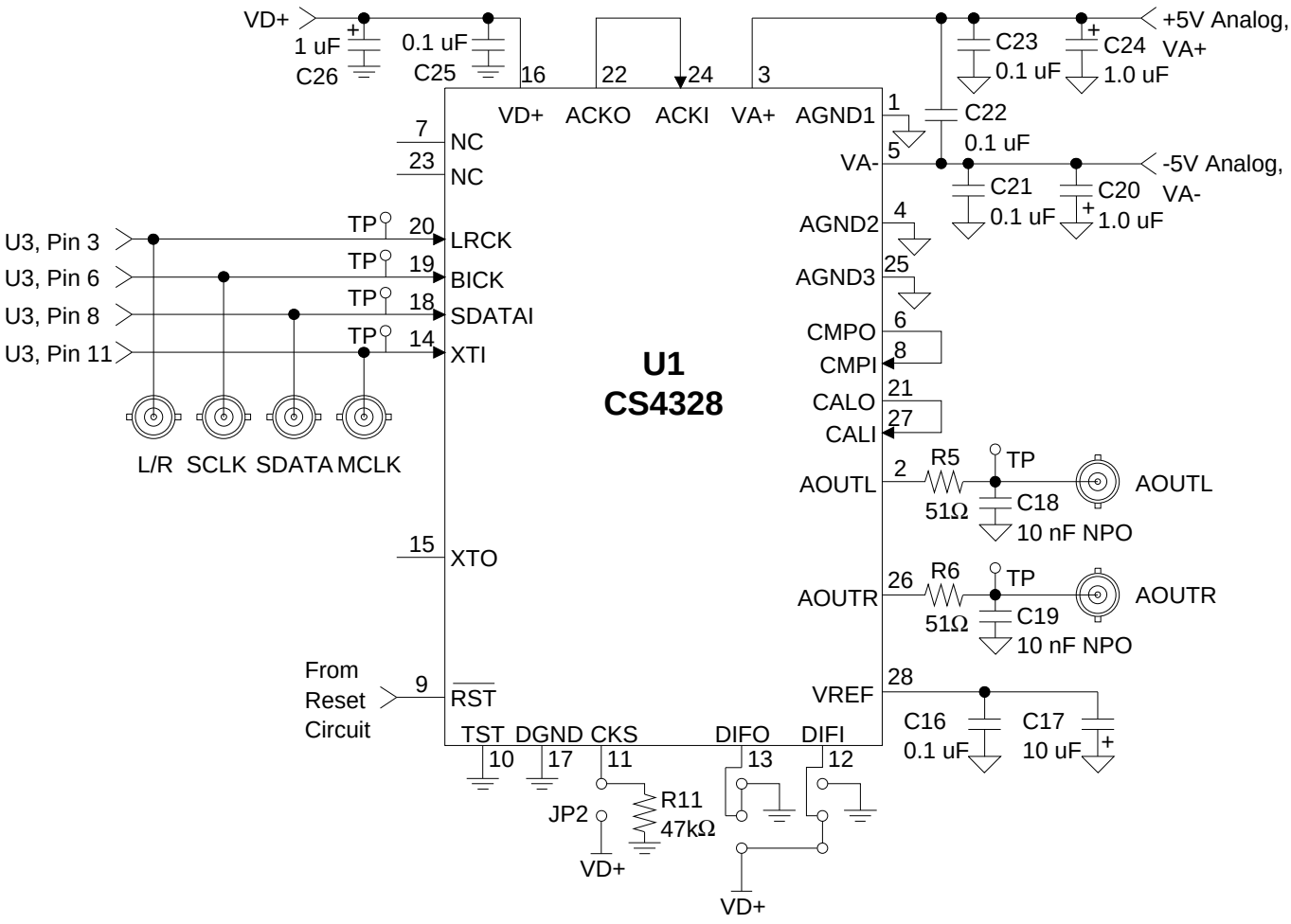


Figure 2. CS4328 DAC Connections

The CS4328 supports four serial data input formats. The selection of which is made via the digital input format pins DIF0 and DIF1. The different formats control the relationship of L/$\overline{R}$ to SDATA and the edge of SCLK used to latch the data. Consult the CS4328 data sheet for an explanation of the different formats.

Position	Input Option Selected
EXT CLK	SDATA,SCLK, L/$\overline{R}$ provided by an external source.
8412	SDATA,SCLK, L/$\overline{R}$ provided by the CS8412

Table 1. JP3 Selectable Options

System Timing

The master clock input to the CS4328 can be provided by several sources. JP3 selects the source of the master clock that is to be supplied to the XTI pin of the converter. When EXT CLK is selected, the master clock is provided by one of two sources. The 12.288 MHz clock signal provided by U8 can be used as the master clock for both the CS4328 and the external system that provides the serial data to the board. The other option is for a master clock that is synchronized to the external serial data coming into the board, be used as the master clock for the CS4328 as well. However, if an external

master clock is to be used, U8 must be removed from it's socket to prevent the two clock signals from interfering with one another. When 8412 is selected by JP3, the master clock for the CS4328 is provided by the MCK output of the CS8412. The CKS pin of the CS4328 can be pulled either high or low via JP2. This determines whether the master clock frequency has to be 384X or 256X the input word rate. Consult the CS4328 data sheet for the common master clock frequencies table.

Analog Outputs

The analog outputs are available at 2 BNC connectors labeled AOUTL and AOUTR. R5 and C18 remove the remaining very high frequency components from the left channel output signal while R6 and C19 do so for the right channel output signal.

Digital Audio Standard Interface

Included on the evaluation board is a CS8412 Digital Audio Interface Receiver. This device can receive and decode data according to the AES/EBU, S/PDIF, and EIAJ-340 interface standard. Figure 3 shows the schematic for the CS8412. The input is coupled to the device through a transformer that is included on the board. The input to the device can be configured to accept either professional or consumer input modes. Consult the CS8412 data sheet for an explanation of the two input modes.

The LEDs, D4-D8, perform two functions. When S1 is in the Channel Status position, the LEDs display the channel status information for the channel selected by JP1. When S1 is in the Error Information position, the LEDs D4-D6, display encoded error information that can be decoded by consulting the CS8412 data sheet. Encoded sample frequency information is displayed on LEDs D7-D9 provided a proper clock is being applied to the FCK pin of JP1. When an LED is lit, this indicates a "1" on the corresponding pin located on the CS8412. When an LED is off, this indicates a "0" on the corresponding pin. Neither the L or R option should be selected if the FCK pin of JP1 is being driven by a clock signal.

Serial Output Interface

The SDATA, SCLK, L/$\overline{R}$, and MCLK BNC connectors can also be used to provide a serial output interface for the CS8412. With JP3 in the 8412 position, the outputs from the CS8412 can be brought off the board to an external evalution system. This data can be configured in one of seven selectable formats. These formats are outlined in the CS8412 data sheet.

CDB5336/7/8/9 Interface to CDB4328

Many users find it informative to evaluate a combined ADC and DAC system connected together yielding analog input and analog output. This can be accomplished by interconnecting a CDB5326/7/8/9 or CDB5336/7/8/9 to a CDB4328 evaluation board. The following information contains several techniques to accomplish this goal. There are two general points which need to be mentioned. An analog input of ± 3.68 V will produce a full scale digital output from the CS5336/7/8/9 and the CS5326/7/8/9. A full scale digital input to the CS4328 will produce a full scale output of ± 2 V resulting in an overall loss of approximately 5.2 dB from input to output. Also it is recommended that the power connections for each board are brought directly from the power supply and not in a "daisy-chain" manner from board to board.

Connecting the CDB4328 to the CDB5336/7/8/9 can be accomplished using one of two methods:

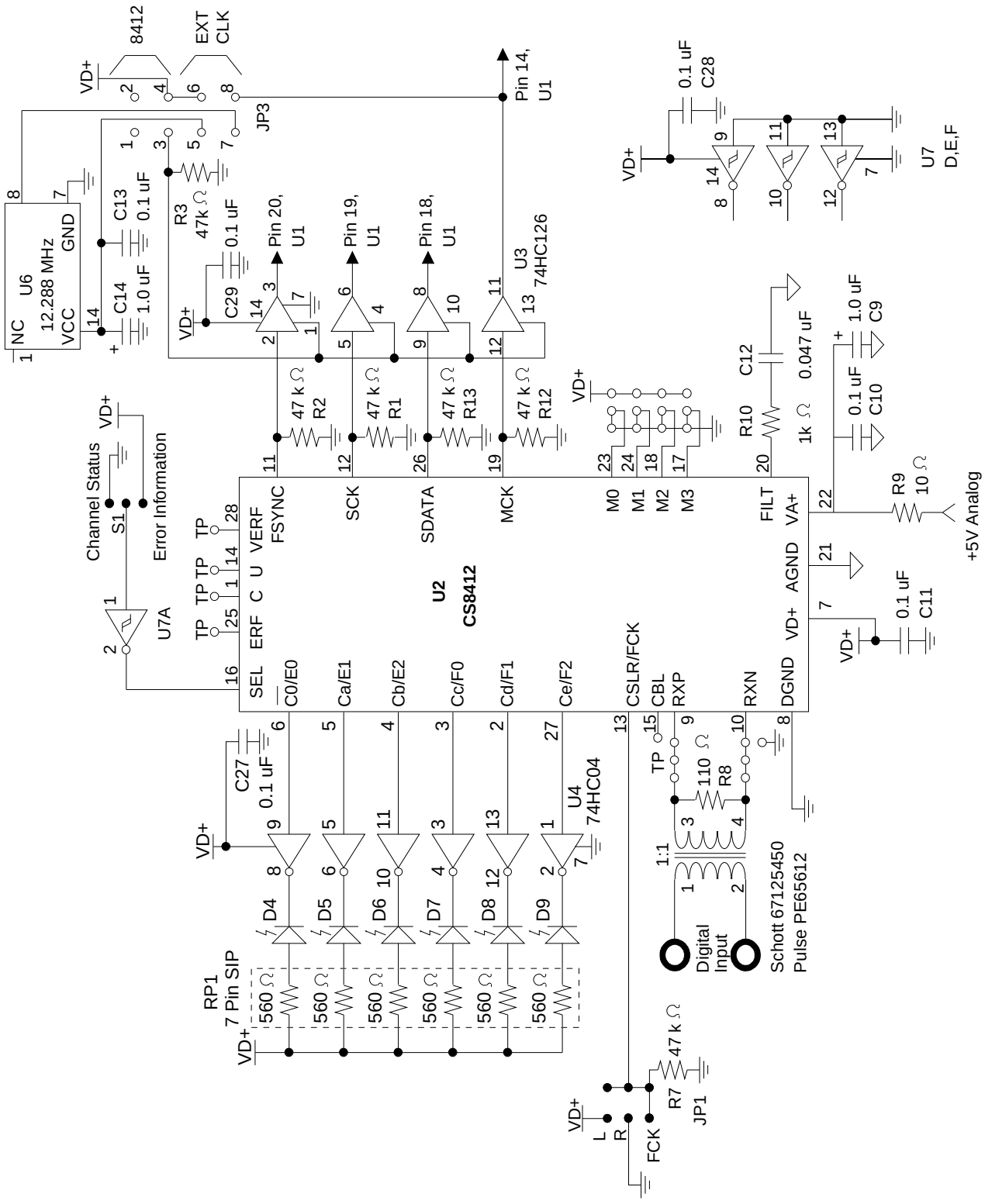


Figure 3. CS8412 Digital Audio Receiver Connections

the trace at the SDATA BNC connector and place a jumper between the SDATA BNC and U8 pin 11. CMODE is set LOW for a master clock of 256 times the sample rate. P7 must have both the internal and external jumpers installed. This will route the master clock to the EXTCLKIN BNC for connection to the CDB4328 MCLK.

If a CS5336/8 is installed an additional modification is required to invert the SCLK prior to transmission to the CDB4328. This can be implemented as follows: cut the trace at the SCLK BNC and install a jumper between U7 pin 4 and the SCLK BNC.

CDB5336/7/8/9 and CDB4328 Interconnection for Method 2

Shielded coaxial cables with BNC connectors should be used to make the following connections: L/R to L/$\overline{R}$, SCLK to SCLK, SDATA to SDATA, EXTCKIN to MCLK.

CDB4328 Interfacing to the CDB5326/7/8/9

A method of interfacing the CDB5326/7/8/9 and the CDB4328 requires a direct interface through the EXTCLKIN, SCLK, SDATA, and L/R BNC connectors. This technique requires modifications to the CDB5326/7/8/9 to derive the proper clock frequencies. This is done by utilizing a 12.288 MHz clock and supplying a clock to the CDB5326/7/8/9 at 6.144 MHz.

CDB4328 Configuration

The CS4328 must be set to receive data in format 2 (DIF1 high and DIF0 low). Modify the jumpers located near pins 12 and 13 of the CS4328. JP2 sets the clock to sample frequency ratio (CKS) on the CS4328 and is set low for a 256 ratio.

JP3 selects the source of SDATA, SCLK and L/R that will be provided to the converter and should be removed to access the multiple clocks from the CDB5326/7/8/9. Remove the 12.288 MHz oscillator (U8).

CDB5326/7/8/9 Configuration

Remove the clock source jumper (P2). Remove the 6.144 MHz oscillator (U2) and replace with the 12.288 MHz oscillator from the CDB4328.

Install a divide by 2 function on the CDB5326/7/8/9 digital patch area. Use a 74HC74 with the D input connected to the $\overline{Q}$ output. Connect the oscillator output to the 74HC74 clock input. Connect the $\overline{Q}$ output to U1 pin 23.

Position P2 to connect the oscillator output to the EXTCLKIN.

CDB5326/7/8/9 and CDB4328 Interconnection

Shielded coaxial cables with BNC connectors should be used to make the following connections: L/$\overline{R}$ to L/$\overline{R}$, SCLK to SCLK, SDATA to SDATA, EXTCLKIN to MCLK.

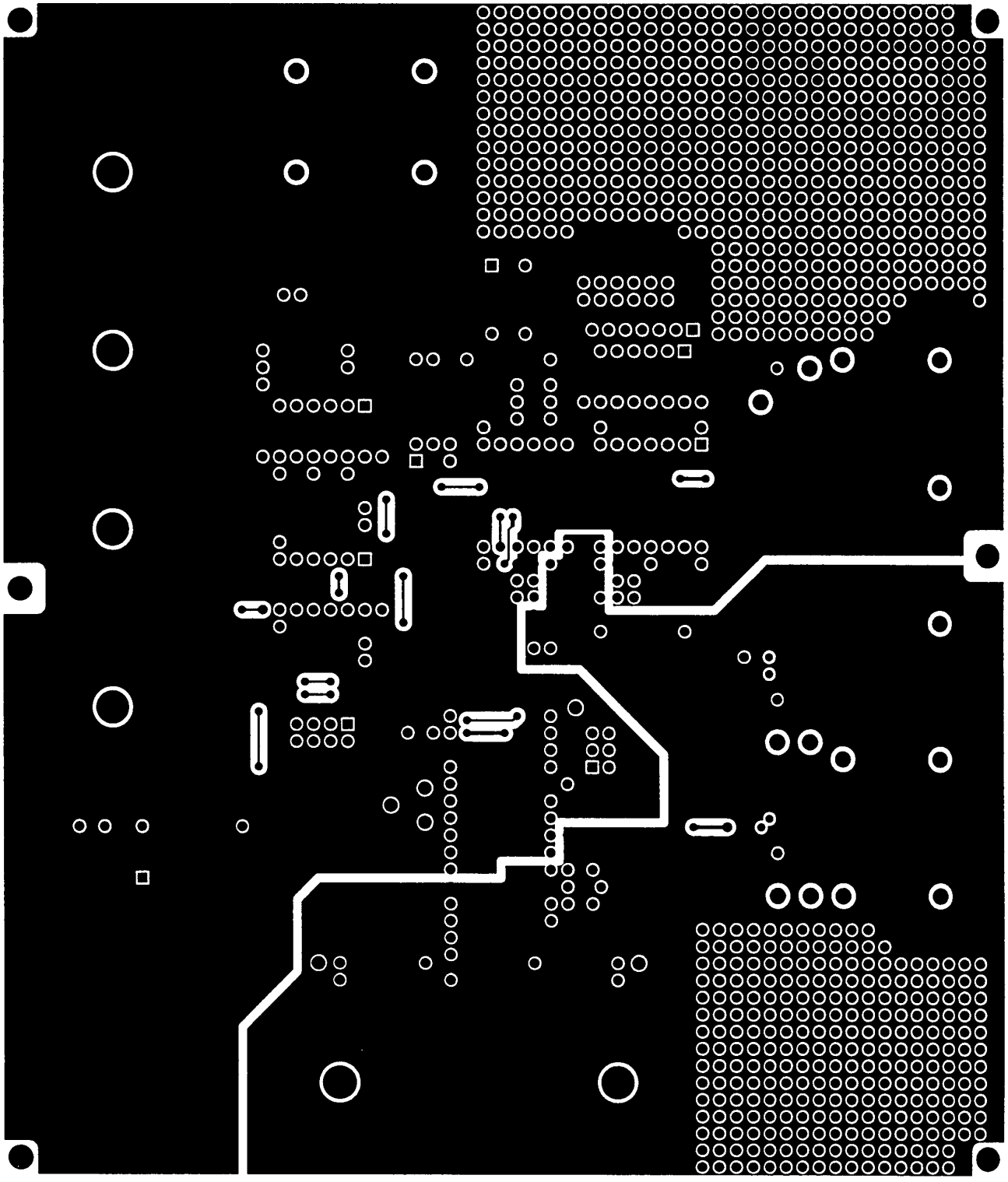


Figure 4. Top Ground Plane Layer (NOT TO SCALE)

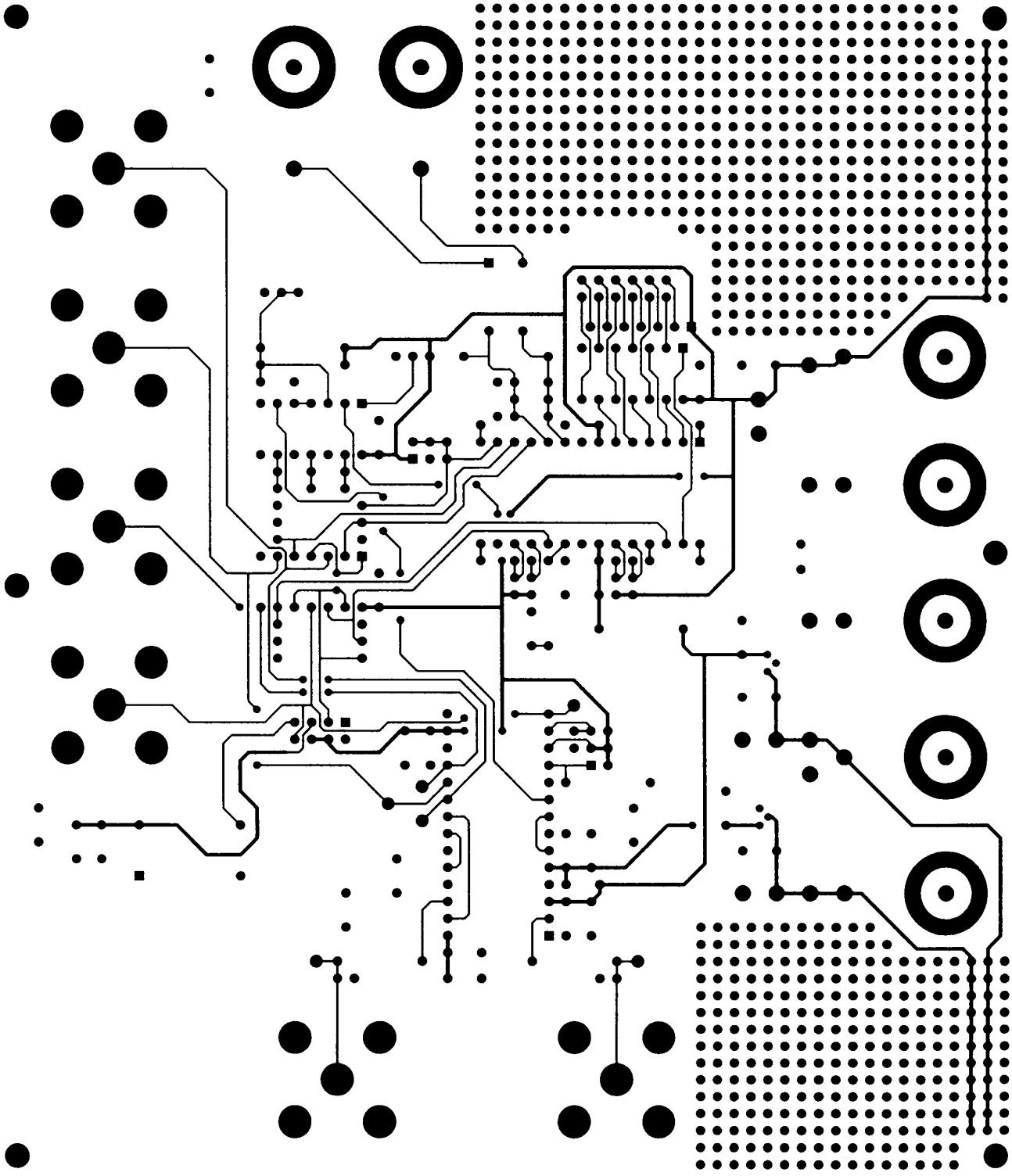


Figure 5. Bottom Trace Layer (NOT TO SCALE)

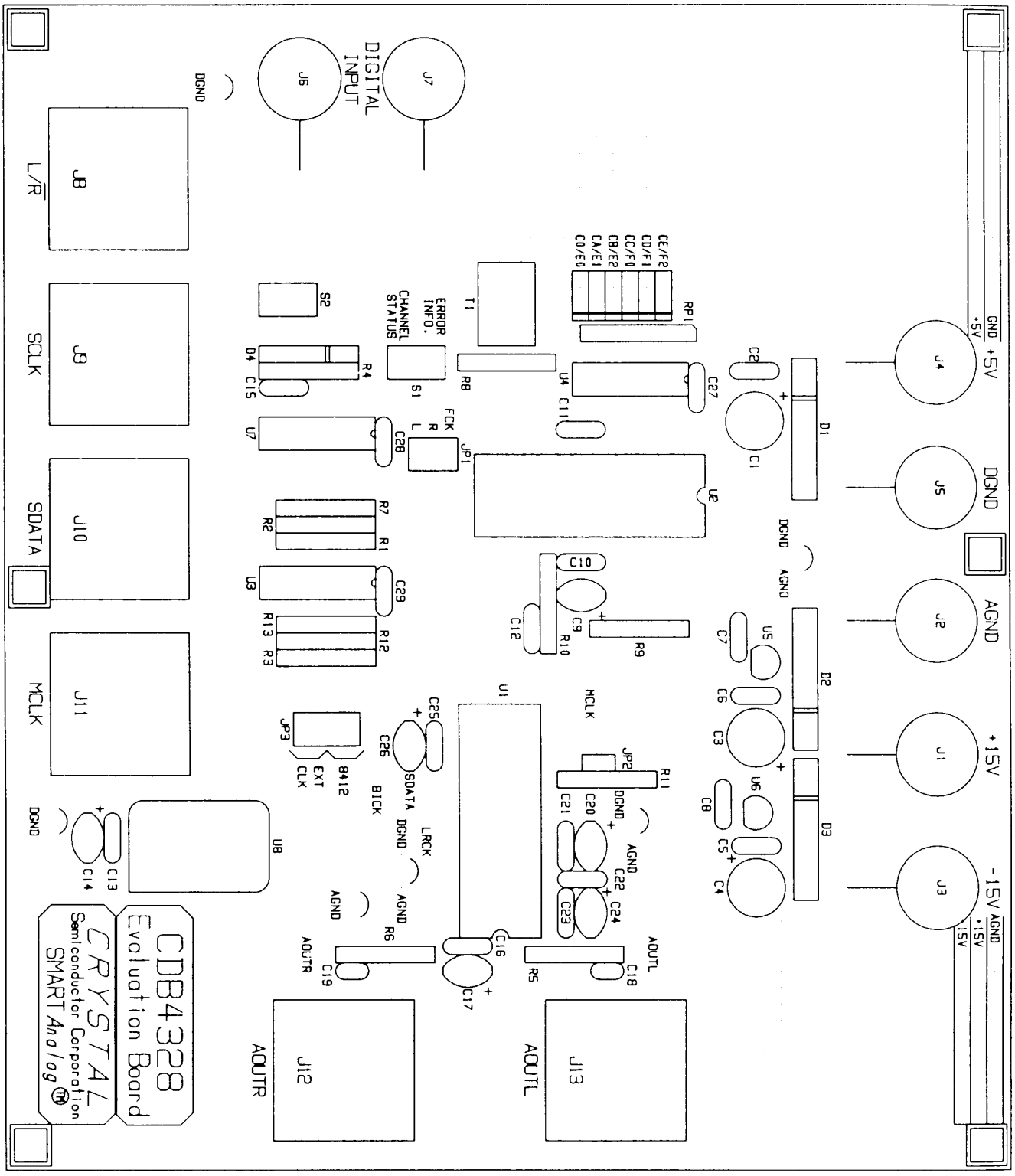


Figure 5. Silk Screen Layer (NOT TO SCALE)

• Notes •