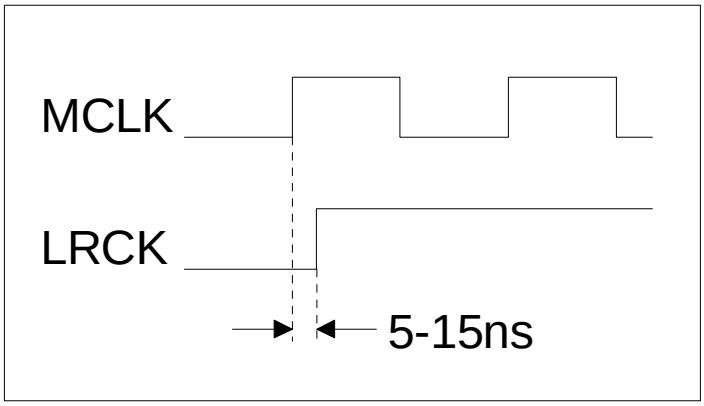
A Cirrus Logic Company

4/25/97

Errata: CS5335 Revision C

CS5335 20-Bit, Stereo A/D Converter for Digital Audio (DS237PP2, NOV '96)

1. Minimum sample rate is 8 kHz.
2. SDATA will go to zero and remain inactive if the LRCK rising edge lags the MCLK rising edge by 5-15 ns when operating in slave mode. This condition can be corrected by synchronizing the LRCK with the falling edge of MCLK or by inverting the MCLK.



For more information contact:
Steve Green - Applications Engineer 512-912-3321
Tom Stein - Product Marketing Engineer 512-912-3113

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, Texas 78760
(512) 445 7222 FAX: (512) 445 7581
http://www.crystal.com