Integrated Circuit Systems, Inc.

ICS8402I

350MHz, Crystal-to-LVCMOS / LVTTL Frequency Synthesizer

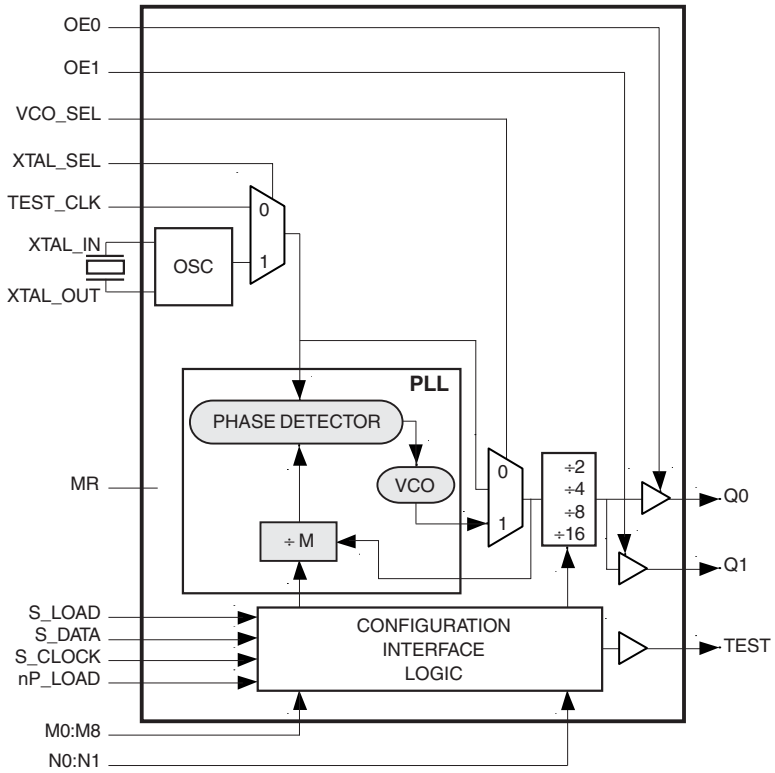
General Description

The ICS8402I is a general purpose, Crystal-to-LVCMOS/LVTTL High Frequency Synthesizer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8402I has a selectable TEST_CLK or crystal inputs. The VCO operates at a frequency range of 250MHz to 700MHz. The VCO frequency is programmed in steps equal to the value of the input reference or crystal frequency. The VCO and output frequency can be programmed using the serial or parallel interfaces to the configuration logic. The low phase noise characteristics of the ICS8402I make it an ideal clock source for Gigabit Ethernet and SONET applications.

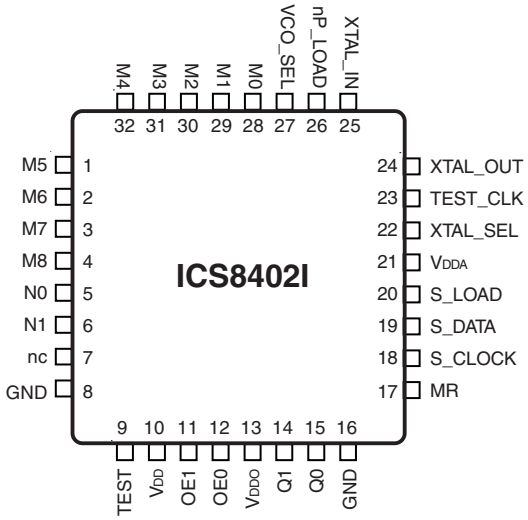
Features

- (2) LVCMOS/LVTTL outputs
- Selectable crystal oscillator interface or LVCMOS/LVTTL TEST_CLK
- Output frequency range: 15.625MHz - 350MHz
- Crystal input frequency range: 12MHz to 40MHz
- VCO range: 250MHz to 700MHz
- Parallel or serial interface for programming counter and output dividers
- RMS period jitter: 30ps (maximum)
- Cycle-to-cycle jitter: 100ps (maximum)
- Full 3.3V or mixed 3.3V core/2.5V output supply voltage
- -40°C to 85°C ambient operating temperature
- Lead-Free fully RoHS compliant

Block Diagram



Pin Assignment



32-Lead LQFP
7mm x 7mm x 1.4mm package body
Y Package
Top View

Functional Description

NOTE: The functional description that follows describes operation using a 25MHz crystal. Valid PLL loop divider values for different crystal or input frequencies are defined in the Input Frequency Characteristics, Table 5, NOTE 1.

The ICS8402I features a fully integrated PLL and therefore requires no external components for setting the loop bandwidth. A fundamental crystal is used as the input to the on-chip oscillator. The output of the oscillator is fed into the phase detector. A 25MHz crystal provides a 25MHz phase detector reference frequency. The VCO of the PLL operates over a range of 250MHz to 700MHz. The output of the M divider is also applied to the phase detector.

The phase detector and the M divider force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low), the PLL will not achieve lock. The output of the VCO is scaled by a divider prior to being sent to each of the LVCMOS output buffers. The divider provides a 50% output duty cycle.

The programmable features of the ICS8402I support two input modes to program the M divider and N output divider. The two input operational modes are parallel and serial. *Figure 1* shows the timing diagram for each mode. In parallel mode, the nP_LOAD input is initially LOW. The data on inputs M0 through M8 and N0 and N1 is passed directly to the M divider and N output divider. On the LOW-to-HIGH transition of the nP_LOAD input, the data is latched and the M divider remains loaded until the next LOW transition on nP_LOAD or until a serial event occurs. As a result, the M and N bits can be hardwired to set the M divider and N output divider to a specific default state that will automatically occur during power-up. The TEST output is LOW when operating in the parallel input mode. The relationship between the VCO frequency, the crystal frequency and the M divider is defined as follows: fVCO = fxtal x M

The M value and the required values of M0 through M8 are shown in Table 3B, Programmable VCO Frequency Function Table. Valid M values for which the PLL will achieve lock for a 25MHz reference are defined as $10 \leq M \leq 28$. The frequency out is defined as follows: $FOUT = \frac{fVCO}{N} = fxtal \times \frac{M}{N}$

Serial operation occurs when nP_LOAD is HIGH and S_LOAD is LOW. The shift register is loaded by sampling the S_DATA bits with the rising edge of S_CLOCK. The contents of the shift register are loaded into the M divider and N output divider when S_LOAD transitions from LOW-to-HIGH. The M divide and N output divide values are latched on the HIGH-to-LOW transition of S_LOAD. If S_LOAD is held HIGH, data at the S_DATA input is passed directly to the M divider and N output divider on each rising edge of S_CLOCK. The serial mode can be used to program the M and N bits and test bits T1 and T0. The internal registers T0 and T1 determine the state of the TEST output as follows:

T1	T0	TEST Output
0	0	LOW
0	1	Shift Register Output
1	0	Output of M divider
1	1	CMOS Fout

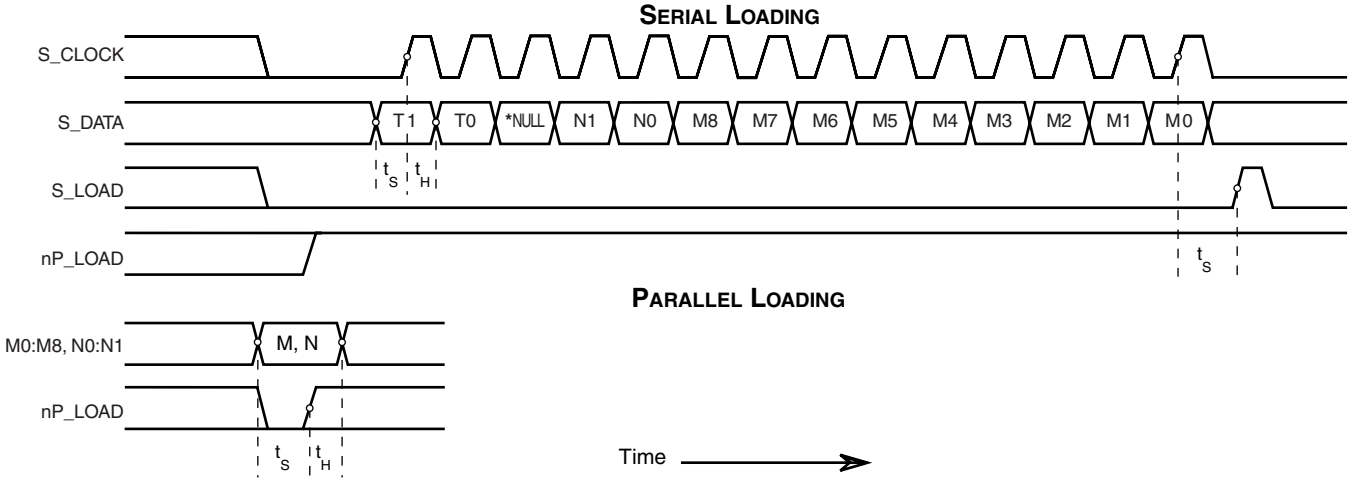


Figure 1. Parallel & Serial Load Operations

***NOTE:** The NULL timing slot must be observed.

Table 1. Pin Descriptions

Number	Name	Type		Description
1	M5	Input	Pullup	M divider inputs. Data latched on LOW-to-HIGH transition of nP_LOAD input. LVCMOS / LVTTL interface levels.
2, 3, 4, 28, 29, 30, 31, 32	M6, M7, M8, M0, M1, M2, M3, M4	Input	Pulldown	
5, 6	N0, N1	Input	Pulldown	Determines output divider value as defined in Table 3C, Function Table. LVCMOS / LVTTL interface levels.
7	nc	Unused		No connect.
8, 16	GND	Power		Power supply ground.
9	TEST	Output		Test output which is ACTIVE in the serial mode of operation. Output driven LOW in parallel mode. LVCMOS / LVTTL interface levels.
10	V_{DD}	Power		Core supply pin.
11, 12	OE1, OE0	Input	Pullup	Output enable. When logic HIGH, the outputs are enabled (default). When logic LOW, the outputs are in Tri-State. See Table 3D, OE Function Table. LVCMOS / LVTTL interface levels.
13	V_{DDO}	Power		Output supply pin.
14, 15	Q1, Q0	Output		Clock outputs. LVCMOS / LVTTL interface levels.
17	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, the internal dividers are reset causing the outputs to go low. When logic LOW, the internal dividers and the outputs are enabled. Assertion of MR does not effect loaded M, N, and T values. LVCMOS / LVTTL interface levels.
18	S_CLOCK	Input	Pulldown	Clocks in serial data present at S_DATA input into the shift register on the rising edge of S_CLOCK. LVCMOS / LVTTL interface levels.
19	S_DATA	Input	Pulldown	Shift register serial input. Data sampled on the rising edge of S_CLOCK. LVCMOS / LVTTL interface levels.
20	S_LOAD	Input	Pulldown	Controls transition of data from shift register into the dividers. LVCMOS / LVTTL interface levels.
21	V_{DDA}	Power		Analog supply pin.
22	XTAL_SEL	Input	Pullup	Selects between crystal or test inputs as the PLL reference source. Selects XTAL inputs when HIGH. Selects TEST_CLK when LOW. LVCMOS / LVTTL interface levels
23	TEST_CLK	Input	Pulldown	Test clock input. LVCMOS / LVTTL interface levels.
24, 25	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
26	nP_LOAD	Input	Pulldown	Parallel load input. Determines when data present at M8:M0 is loaded into M divider, and when data present at N1:N0 sets the N output divider value. LVCMOS / LVTTL interface levels.
27	VCO_SEL	Input	Pullup	Determines whether synthesizer is in PLL or bypass mode. LVCMOS / LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD}, V_{DDA}, V_{DDO} = 3.465V		13		pF
		V_{DD}, V_{DDA} = 3.465V, V_{DDO} = 2.625V		11		pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ
R_{OUT}	Output Impedance	V_{DDO} = 3.465V	5	7	12	Ω
		V_{DDO} = 2.625V		7		Ω

Table 3A. Parallel and Serial Mode Function Table

Inputs							Conditions
MR	nP_LOAD	M	N	S_LOAD	S_CLOCK	S_DATA	
H	X	X	X	X	X	X	Reset. Forces outputs LOW.
L	L	Data	Data	X	X	X	Data on M and N inputs passed directly to the M divider and N output divider. TEST output forced LOW.
L	↑	Data	Data	L	X	X	Data is latched into input registers and remains loaded until next LOW transition or until a serial event occurs.
L	H	X	X	L	↑	Data	Serial input mode. Shift register is loaded with data on S_DATA on each rising edge of S_CLOCK.
L	H	X	X	↑	L	Data	Contents of the shift register are passed to the M divider and N output divider.
L	H	X	X	↓	L	Data	M divider and N output divider values are latched.
L	H	X	X	L	X	X	Parallel or serial input do not affect shift registers.
L	H	X	X	H	↑	Data	S_DATA passed directly to M divider as it is clocked.

NOTE: L = LOW
H = HIGH
X = Don't care
↑ = Rising edge transition
↓ = Falling edge transition

Table 3B. Programmable VCO Frequency Function Table

VCO Frequency (MHz)	M Divide	256	128	64	32	16	8	4	2	1
		M8	M7	M6	M5	M4	M3	M2	M1	M0
250	10	0	0	0	0	0	1	0	1	0
275	11	0	0	0	0	0	1	0	1	1
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
650	26	0	0	0	0	1	1	0	1	0
675	27	0	0	0	0	1	1	0	1	1
700	28	0	0	0	0	1	1	1	0	0

NOTE 1: These M divide values and the resulting frequencies correspond to crystal or TEST_CLK input frequency of 25MHz.

Table 3C. Programmable Output Divider Function Table

Inputs		N Divider Value	Output Frequency (MHz)	
N1	N0		Minimum	Maximum
0	0	2	125	350
0	1	4	62.5	175
1	0	8	31.25	87.5
1	1	16	15.625	43.75

Table 3D. Output Enable & Clock Enable Function Table

Control Inputs		Output	
OE0	OE1	Q0	Q1
0	0	Hi-Z	Hi-Z
0	1	Hi-Z	Enabled
1	0	Enabled	Hi-Z
1	1	Enabled	Enabled

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDA} = 3.3V±5\%$, $V_{DDO} = 3.3V±5\%$ or $2.5V±5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
I_{DD}	Power Supply Current				125	mA
I_{DDA}	Analog Supply Current				18	mA
I_{DDO}	Output Supply Current				10	mA

Table 4B. LVCMOS / LVTTL DC Characteristics, $V_{DD} = V_{DDA} = 3.3V±5\%$, $V_{DDO} = 3.3V±5\%$ or $2.5V±5\%$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	VCO_SEL, XTAL_SEL, MR, S_LOAD, nP_LOAD, S_DATA, S_CLOCK, OE0, OE1, N0:N1, M0:M8		2		V_{DD} + 0.3	V
		TEST_CLK		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	VCO_SEL, XTAL_SEL, MR, S_LOAD, nP_LOAD, S_DATA, S_CLOCK, OE0, OE1, N0:N1, M0:M8		-0.3		0.8	V
		TEST_CLK		-0.3		1.3	V
I_{IH}	Input High Current	M0-M4, M6-M8, N0, N1, MR, S_CLOCK, TEST_CLK, S_DATA, S_LOAD, nP_LOAD	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		M5, OE0, OE1, XTAL_SEL, VCO_SEL	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	M0-M4, M6-M8, N0, N1, MR, S_CLOCK, TEST_CLK, S_DATA, S_LOAD, nP_LOAD	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		M5, OE0, OE1, XTAL_SEL, VCO_SEL	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage; NOTE 1		V_{DDO} = 3.465V	2.6			V
			V_{DDO} = 2.625V	1.8			V
V_{OL}	Output Low Voltage; NOTE 1					0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}/2$.

TABLE 5. INPUT FREQUENCY CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency	TEST_CLK; NOTE 1		12		40	MHz
		XTAL_IN XTAL_OUT NOTE 1		12		40	MHz
		S_CLOCK				50	MHz

NOTE 1: For the input crystal and TEST_CLK frequency range, the M value must be set for the VCO to operate within the 250MHz to 700MHz range. Using the minimum input frequency of 12MHz, valid values of M are $21 \leq M \leq 58$. Using the maximum frequency of 40MHz, valid values of M are $7 \leq M \leq 17$.

TABLE 6. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		12		40	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance (C_O)				7	pF

TABLE 7A. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
F_{OUT}	Output Frequency			15.625		350	MHz
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 1, 3				40	100	ps
*t*jit(per)	Period Jitter, RMS; NOTE 1				8	30	ps
*t*sk(o)	Output Skew; NOTE 2, 3					80	ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	0.25		1.1	ns
t_S	Setup Time	M, N to nP_LOAD		5			ns
		S_DATA to S_CLOCK		5			ns
		S_CLOCK to S_LOAD		5			ns
t_H	Hold Time	M, N to nP_LOAD		5			ns
		S_DATA to S_CLOCK		5			ns
		S_CLOCK to S_LOAD		5			ns
odc	Output Duty Cycle		*f* ≤ 300MHz	40		60	%
t_{LOCK}	PLL Lock Time					1	ms

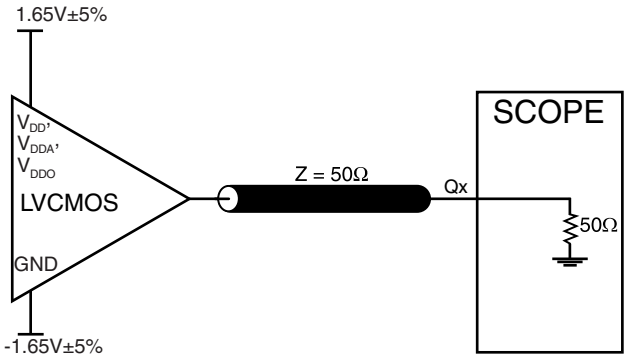
See Parameter Measurement Information section.
NOTE 1: Jitter performance using XTAL inputs.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

Table 7B. AC Characteristics, $V_{DD} = V_{DDA} = 3.3V±5\%$, $V_{DDO} = 2.5V±5\%$, T_A = -40°C to 85°C

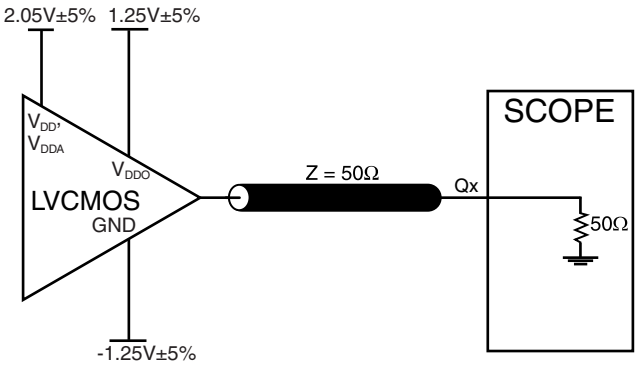
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
F_{OUT}	Output Frequency			15.625		350	MHz
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 1, 3				40	100	ps
*t*jit(per)	Period Jitter, RMS; NOTE 1					30	ps
*t*sk(o)	Output Skew; NOTE 2, 3					60	ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	0.25		1.0	ns
t_S	Setup Time	M, N to nP_LOAD		5			ns
		S_DATA to S_CLOCK		5			ns
		S_CLOCK to S_LOAD		5			ns
t_H	Hold Time	M, N to nP_LOAD		5			ns
		S_DATA to S_CLOCK		5			ns
		S_CLOCK to S_LOAD		5			ns
odc	Output Duty Cycle		$f \leq$ 300MHz	40		60	%
t_{LOCK}	PLL Lock Time					1	ms

See Parameter Measurement Information section.
NOTE 1: Jitter performance using XTAL inputs.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

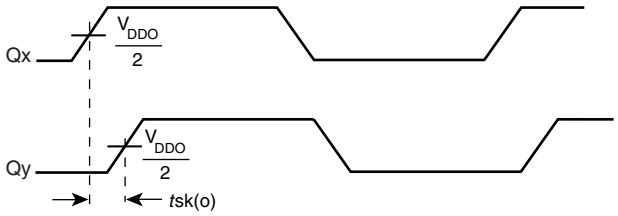
Parameter Measurement Information



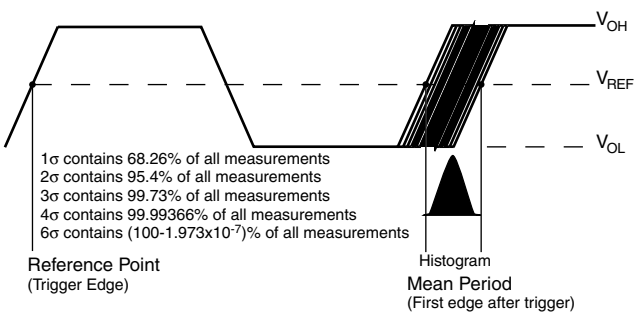
3.3V Core/3.3V Output Load AC Test Circuit



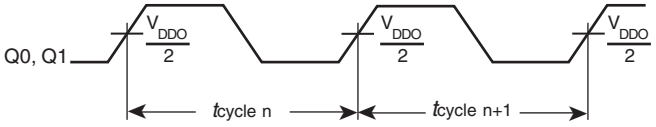
3.3V Core/2.5V Output Load AC Test Circuit



Output Skew



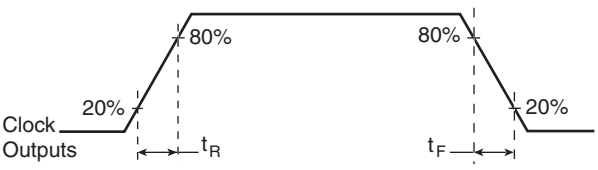
Period Jitter



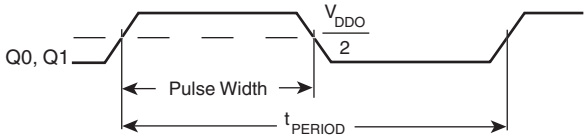
$t_{jit(cc)} = t_{cycle\ n} - t_{cycle\ n+1}$

1000 Cycles

Cycle-to-Cycle Jitter



Output Rise/Fall Time



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

Output Duty Cycle/Pulse Width/Period

Application Information

Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS8402I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 2* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA} pin.

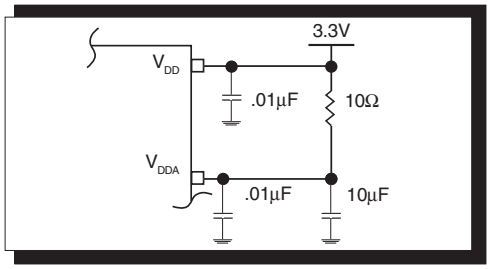


Figure 2. Power Supply Filtering

Crystal Input Interface

The ICS8402I has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 3* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

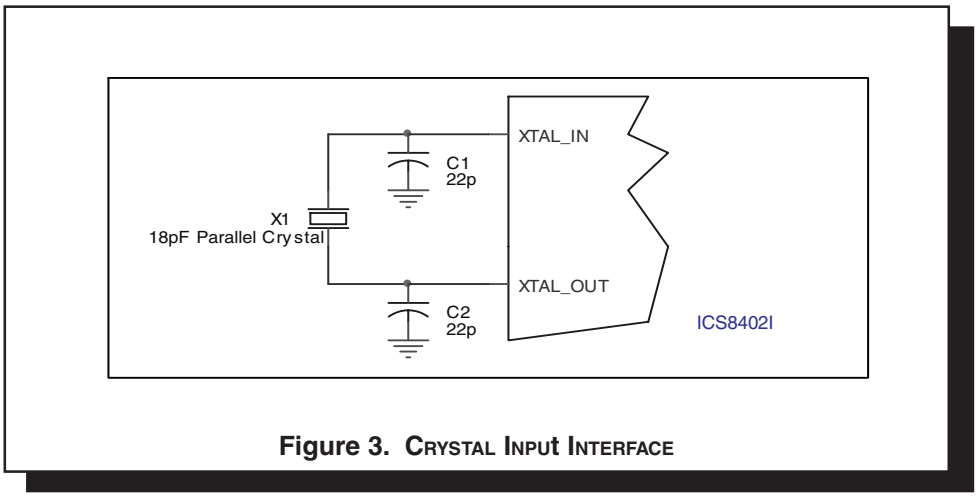


Figure 3. Crystal Input Interface

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for 32 Lead LQFP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Transistor Count

The transistor count for ICS8402I is: 3784

Package Outline - Y Suffix for 32 Lead LQFP

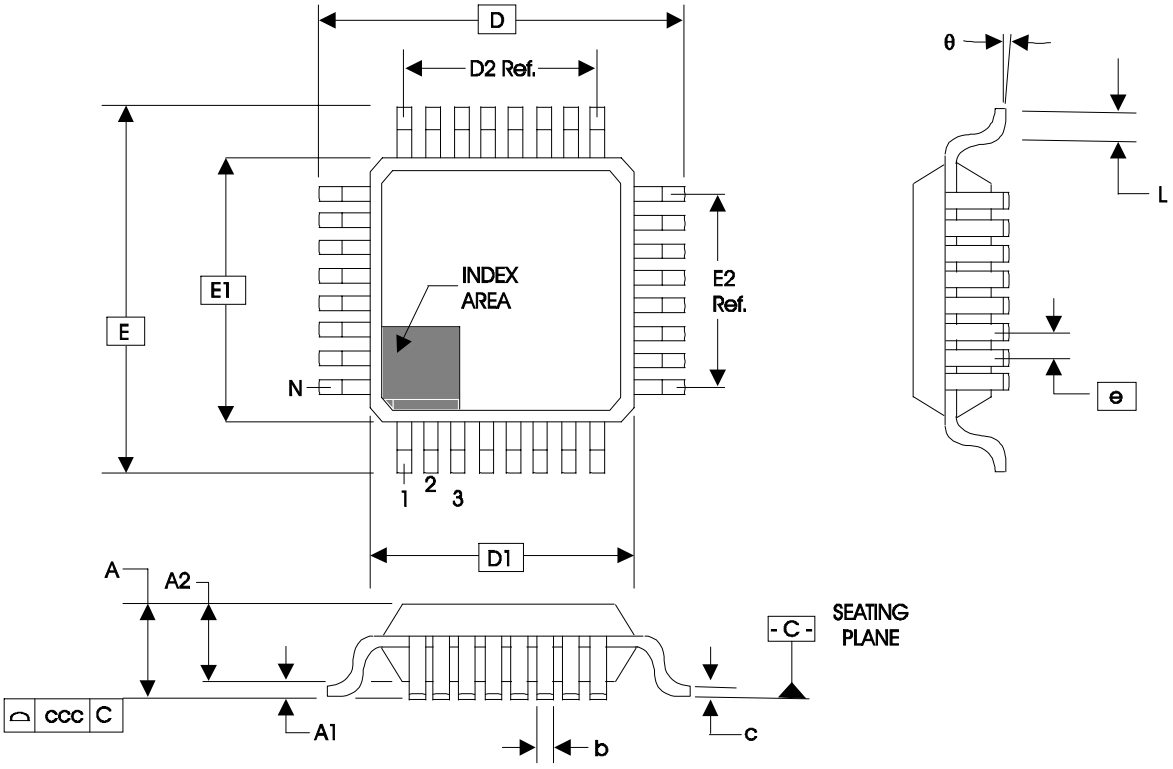


Table 9. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60 Ref.	
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026

Table 10. Ordering Information

Part/Order Number	Marking	Package	Count	Temperature
ICS8402AYI	ICS8402AYI	32 Lead LQFP	250 per tray	-40°C to 85°C
ICS8402AYIT	ICS8402AYI	32 Lead LQFP on Tape and Reel	1000	-40°C to 85°C
ICS8402AYILF	TBD	32 Lead "Lead-Free" LQFP	250 per tray	-40°C to 85°C
ICS8402AYILFT	TBD	32 Lead "Lead-Free" LQPF on Tape and Reel	1000	-40°C to 85°C