

NB7L32M

2.5V/3.3V, 14GHz ÷2 Clock Divider w/CML Output and Internal Termination

Descriptions

The NB7L32M is an integrated ÷2 divider with differential clock inputs and asynchronous reset.

Differential clock inputs incorporate internal 50 Ω termination resistors and accept LVPECL (Positive ECL), CML, or LVDS. The high frequency reset pin is asserted on the rising edge. Upon power-up, the internal flip-flops will attain a random state; the reset allows for the synchronization of multiple NB7L32M's in a system.

The differential 16 mA CML output provides matching internal 50 Ω termination which guarantees 400 mV output swing when externally receiver terminated 50 Ω to V_{CC} (See Figure 16).

The device is housed in a small 3x3 mm 16 pin QFN package.

Features

- Maximum Input Clock Frequency 14 GHz Typical
- 200 ps Max Propagation Delay
- 30 ps Typical Rise and Fall Times
- < 0.5 ps Maximum (RMS) Random Clock Jitter
- Operating Range: V_{CC} = 2.375 V to 3.465 V with V_{EE} = 0 V
- CML Output Level (400 mV Peak-to-Peak Output), Differential Output Only
- 50 Ω Internal Input and Output Termination Resistors
- Functionally Compatible with Existing 2.5 V / 3.3 V LVEL, LVEP, EP, and SG Devices
- These are Pb-Free Devices



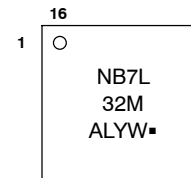
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QFN-16
MN SUFFIX
CASE 485G

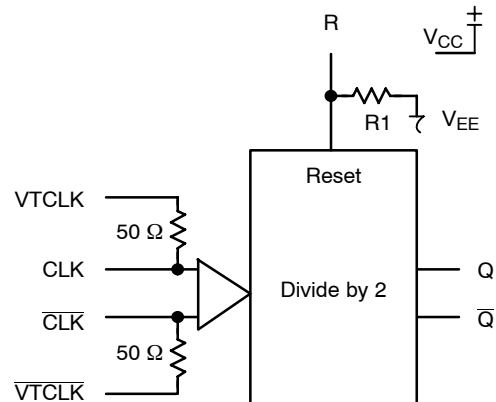
MARKING DIAGRAM*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

*For additional marking information, refer to Application Note AND8002/D.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

CLK	CLK	R	Q	Q̄
x	x	H	L	H
Z	W	L	÷2	÷2

Z = LOW to HIGH Transition
W = HIGH to LOW Transition
x = Don't Care

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

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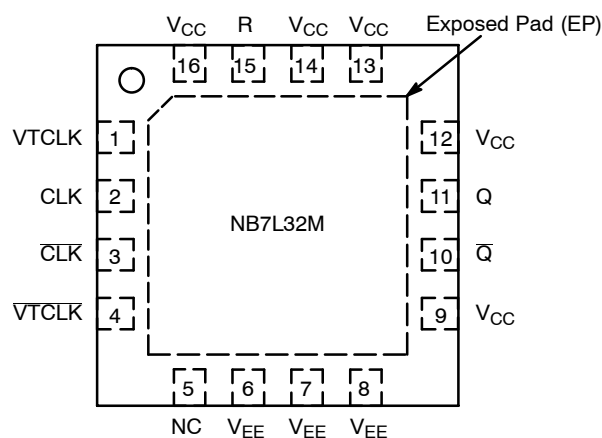


Figure 1. Pin Configuration (Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Description
1	VTCLK	-	Internal 50 Ω termination pin. In the differential configuration when the input termination pin (VTCLK, VTCLK) are connected to a common termination voltage or left open, and if no signal is applied on CLK/CLK input then the device will be susceptible to self-oscillation.
2	CLK	ECL, CML, LVDS Input	Noninverted differential input. In the differential configuration when the input termination pin (VTCLK, VTCLK) are connected to a common termination voltage or left open and if no signal is applied on CLK/CLK input, then the device will be susceptible to self-oscillation.
3	CLK	ECL, CML, LVDS Input	Inverted differential input. In the differential configuration when the input termination pin (VTCLK, VTCLK) are connected to a common termination voltage or left open and if no signal is applied on CLK/CLK input, then the device will be susceptible to self-oscillation.
4	VTCLK	-	Internal 50 Ω termination pin. In the differential configuration when the input termination pin (VTCLK, VTCLK) are connected to a common termination voltage or left open and if no signal is applied on CLK/CLK input, then the device will be susceptible to self-oscillation.
5	NC	-	No connect. NC pin must be left open.
6, 7, 8	VEE	-	Negative supply voltage.
9, 12, 13, 14, 16	VCC	-	Positive supply voltage.
10	Q	CML Output	Inverted differential output. Typically terminated with 50 Ω resistor to VCC.
11	Q	CML Output	Noninverted differential output. Typically terminated with 50 Ω resistor to VCC.
15	R	LVTTL/LVCMOS	Reset Input. Internal pulldown to 75 k Ω to VEE.
-	EP	-	Exposed Pad. The thermally exposed pad (EP) on package bottom (see case drawing) must be attached to a heat-sinking conduit. EP is electrically isolated from VCC and VEE.

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Table 2. ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor	R1	75 k Ω
ESD Protection	Human Body Model Machine Model	> 500 V > 30 V
Moisture Sensitivity (Note 1)	QFN-16	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count		349
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{CC}	Positive Power Supply	V _{EE} = 0 V		3.6	V
V _{EE}	Negative Power Supply	V _{CC} = 0 V		-3.6	V
V _I	Positive Input Negative Input	V _{EE} = 0 V V _{CC} = 0 V	V _I ≤ V _{CC} V _I ≥ V _{EE}	3.6 -3.6	V V
V _{INPP}	Differential Input Voltage			2.8	V
I _{IN}	Input Current Through R _T (50 Ω Resistor)	Static Surge		45 80	mA mA
I _{out}	Output Current	Continuous Surge		25 50	mA mA
T _A	Operating Temperature Range	QFN-16		-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient) (Note 2)	0 lfpm 500 lfpm	QFN-16 QFN-16	41.6 35.2	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	1S2P	QFN-16	4.0	°C/W
T _{sol}	Wave Solder	Pb-Free	<3 sec @ 260°C	265	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

2. JEDEC standard multilayer board – 1S2P (1 signal, 2 power) with 8 filled thermal vias under exposed pad.

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Table 4. DC CHARACTERISTICS, CLOCK INPUTS, CML OUTPUTS $V_{CC} = 2.375\text{ V to }3.465\text{ V}$, $V_{EE} = 0\text{ V}$,
 $T_A = -40^\circ\text{C to }+85^\circ\text{C}$

Symbol	Characteristic	Min	Typ	Max	Unit
I_{CC}	Power Supply Current (Note 3)	50	65	80	mA
V_{OH}	Output HIGH Voltage (Note 4)	$V_{CC} - 40$	$V_{CC} - 10$	V_{CC}	mV
V_{OL}	Output LOW Voltage (Note 4)	$V_{CC} - 500$	$V_{CC} - 400$	$V_{CC} - 330$	mV
R_{TOUT}	Internal Output Termination Resistor	45	50	55	Ω
R_{Temp} Coef	Internal I/O Termination Resistor Temperature Coefficient		6.38		$\text{m}\Omega/^\circ\text{C}$

DIFFERENTIAL CLK/CLK INPUT DRIVEN SINGLE-ENDED (see Figure 10 and 12)

V_{th}	Input Threshold Reference Voltage Range (Note 6)	1050		V_{CC}	mV
V_{IH}	Single-ended Input HIGH Voltage	$V_{th} + 150$		$V_{CC} + 300$	mV
V_{IL}	Single-ended Input LOW Voltage	V_{EE}		$V_{th} - 150$	mV

DIFFERENTIAL CLK/CLK INPUTS DRIVEN DIFFERENTIALLY (see Figure 11 and 13)

V_{IHD}	Differential Input HIGH Voltage	1200		$V_{CC} + 300$	mV
V_{ILD}	Differential Input LOW Voltage	V_{EE}		$V_{CC} - 75$	mV
V_{CMR}	Input Common Mode Range (Differential Configuration, Note 7)	1125		V_{CC}	mV
V_{ID}	Differential Input Voltage ($V_{IHD} - V_{ILD}$)	150		2500	mV

I_{IH}	Input HIGH Current	CLK/CLK ($V_{TCLK}/R/V_{TCLK}/\bar{R}$ Open)	0	30	100	μA
I_{IL}	Input LOW Current	CLK/CLK ($V_{TCLK}/R/V_{TCLK}/\bar{R}$ Open)	-50	0	50	μA
R_{TIN}	Internal Input Termination Resistor		45	50	55	Ω

LVTTL/LVC MOS RESET INPUT

V_{IH}	Single-ended Input HIGH Voltage		2000		V_{CC}	mV
V_{IL}	Single-ended Input LOW Voltage		V_{EE}		800	mV
I_{IH}	Input HIGH Current	R	0	30	100	μA
I_{IL}	Input LOW Current	R	0	10	100	μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. Input termination pins open and all outputs loaded with external $R_L = 50\ \Omega$ receiver termination resistor.
4. CML outputs require $R_L = 50\ \Omega$ receiver termination resistors to V_{CC} for proper operation. (See Figure 9)
5. Input and output parameters vary 1:1 with V_{CC} .
6. V_{th} is applied to the complementary input when operating in single-ended mode.
7. $V_{CMR(MIN)}$ varies 1:1 with V_{EE} , V_{CMR} max varies 1:1 with V_{CC} . The V_{CMR} range is referenced to the most positive side of the differential input signal.

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Table 6. AC CHARACTERISTICS $V_{CC} = 2.375\text{ V to }3.465\text{ V}$, $V_{EE} = 0\text{ V}$ (Note 8)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OUTPP}	Output Voltage Amplitude (@ $V_{INPP(MIN)}$) $f_{in} \leq 7\text{ GHz}$ (See Figures 2, 3, 4, 5, 6, and 7) $f_{in} \leq 12\text{ GHz}$	190 160	330 320		190 160	330 320		190 160	330 320		mV
f_{IN}	Maximum Input Clock Frequency (See Figures 2 and 3)	12	14		12	14		12	14		GHz
t_{PLH} , t_{PHL}	Propagation Delay to Output Differential (See Figure 8) CLK to Q R to Q	130 200	155 240	200 300	130 200	155 240	200 300	130 200	155 260	200 300	ps
t_{skew}	Duty Cycle Skew (Note 9) Device-to-Device Skew (Note 12)		2 6	20 50		2 6	20 50		2 6	20 50	
t_{RR}	Reset Recovery (See Figure 8)	300	135		300	135		300	135		ps
t_{PW}	Minimum Pulse Width R	500	210		500	210		500	210		ps
t_{JITTER}	Random Clock Jitter (RMS) (Note 11) $f_{in} \leq 7\text{ GHz}$ $f_{in} = 12\text{ GHz}$		0.13 0.14	0.5 0.5		0.13 0.14	0.5 0.5		0.13 0.14	0.5 0.5	ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 10)	150		2500	150		2500	150		2500	mV
t_r t_f	Output Rise/Fall Times @ 1 GHz (20% – 80%)		30	45		30	45		30	45	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

8. Measured by forcing $V_{INPP(MIN)}$ from a 50% duty cycle clock source. All loading with an external $R_L = 50\ \Omega$ to V_{CC} . Input edge rates 40 ps (20% – 80%).

9. Duty cycle skew is measured between differential outputs using the deviations of the sum of T_{pw-} and T_{pw+} 1 GHz.

10. $V_{INPP(MAX)}$ cannot exceed $V_{CC} - V_{EE}$. Input voltage swing is a single-ended measurement operating in differential mode.

11. Additive RMS jitter with 50% duty cycle input clock signal.

12. Device-to-device skew is measured between outputs under identical transition @ 1 GHz.

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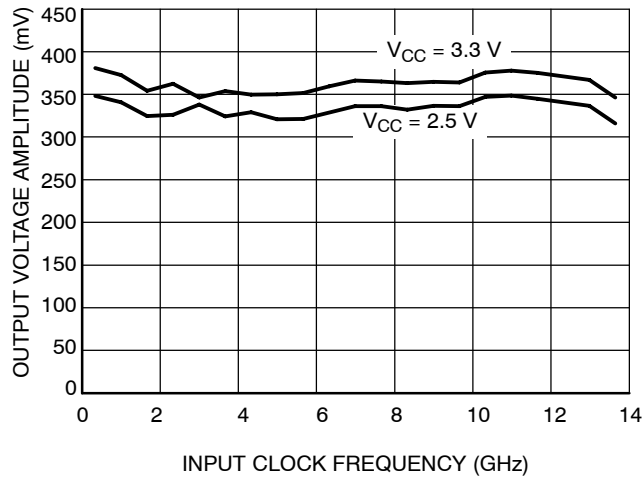


Figure 2. Output Voltage Amplitude (V_{OUTPP}) versus Input Clock Frequency (f_{OUT}) at Ambient Temperature ($V_{INPP} = 150$ mV)

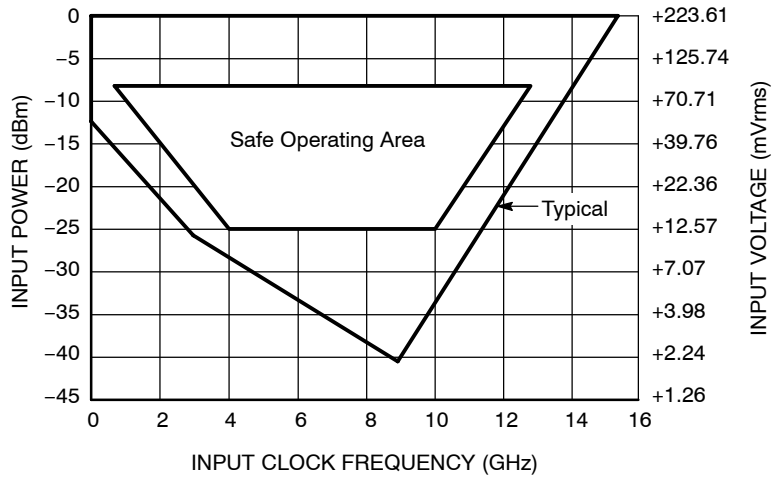


Figure 3. Input Signal Amplitude vs Input Clock Frequency (All Temperatures and Power Supplies; Guaranteed Output Amplitude of at Least $V_{OUTPP} = 160$ mV)

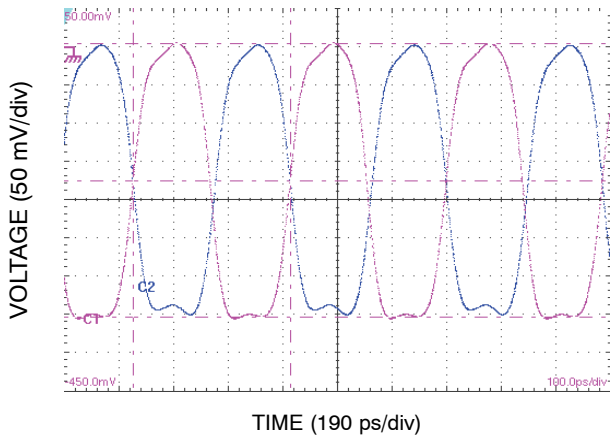


Figure 4. Typical Output Waveform with $f_{IN} = 7$ GHz ($V_{CC} = 2.5$ V, $V_{INPP} = 400$ mV, Room Temperature, $V_{OUTPP} = 357$ mV, $t_r = 33$ ps, $t_f = 30$ ps, $f_{OUT} = 3.499$ GHz)

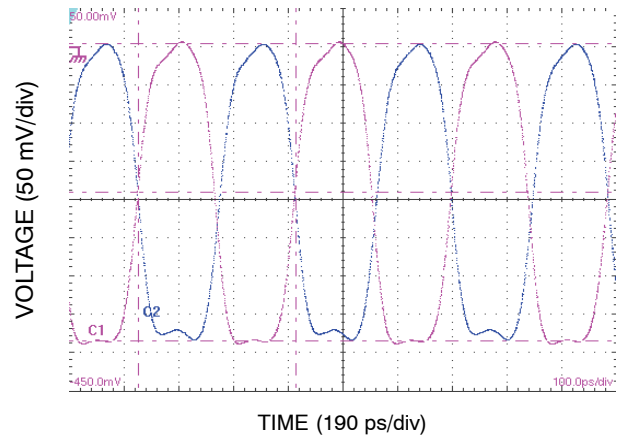


Figure 5. Typical Output Waveform with $f_{IN} = 7$ GHz ($V_{CC} = 3.3$ V, $V_{INPP} = 400$ mV, Room Temperature, $V_{OUTPP} = 387$ mV, $t_r = 32$ ps, $t_f = 29.8$ ps, $f_{OUT} = 3.499$ GHz)

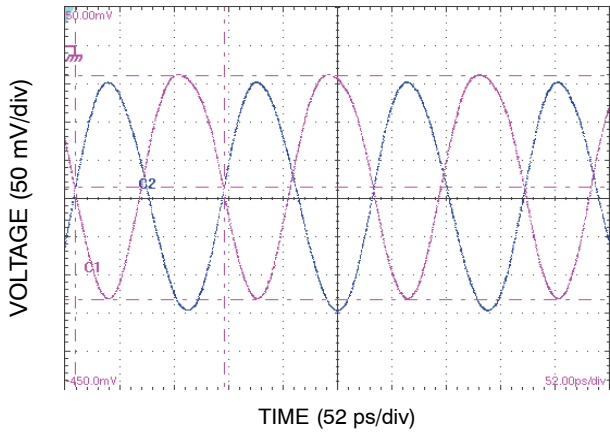


Figure 6. Typical Output Waveform with $f_{IN} = 14$ GHz ($V_{CC} = 2.5$ V, $V_{INPP} = 400$ mV, Room Temperature, $V_{OUTPP} = 292$ mV, $t_r = 25$ ps, $t_f = 27$ ps, $f_{OUT} = 7.01$ GHz)

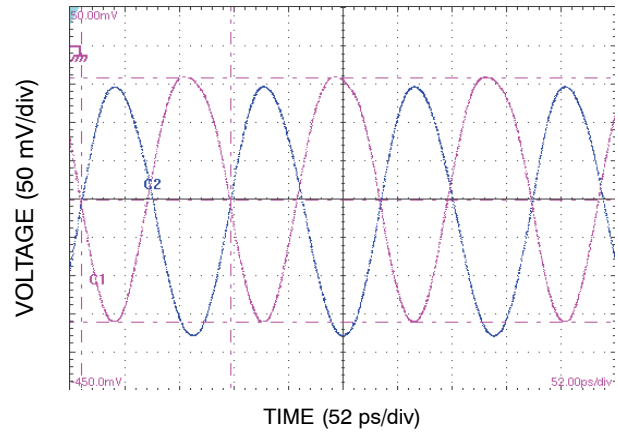


Figure 7. Typical Output Waveform with $f_{IN} = 14$ GHz ($V_{CC} = 3.3$ V, $V_{INPP} = 400$ mV, Room Temperature, $V_{OUTPP} = 319$ mV, $t_r = 25$ ps, $t_f = 26$ ps, $f_{OUT} = 7.01$ GHz)

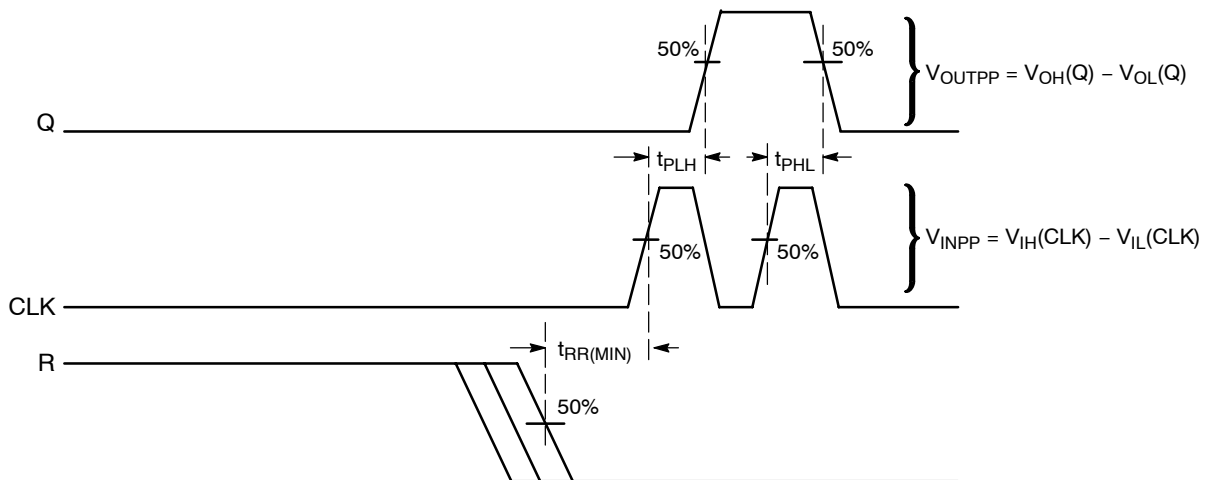


Figure 8. AC Reference Measurement (Timing Diagram)

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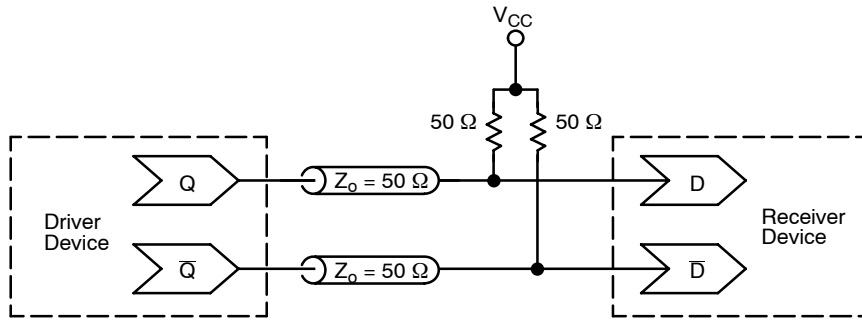


Figure 9. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8073/D – Termination of CML Logic Devices.)

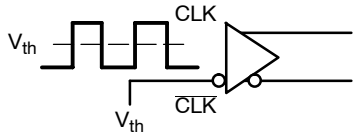


Figure 10. Differential Input Driven Single-Ended

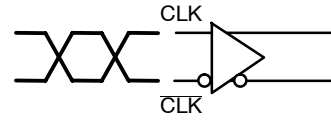


Figure 11. Differential Inputs Driven Differentially

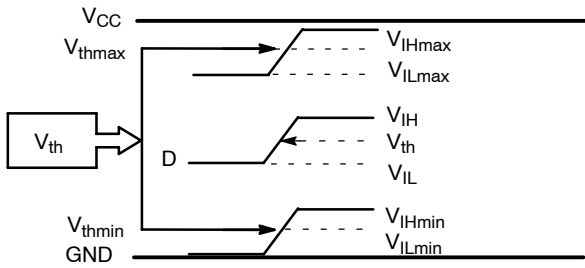


Figure 12. V_{th} Diagram

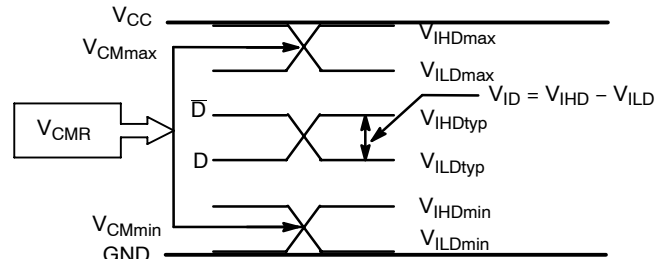


Figure 13. V_{CM} Diagram

NOTE: $V_{EE} \leq V_{IN} \leq V_{CC} + 300 \text{ mV}$; $V_{IH} > V_{IL}$

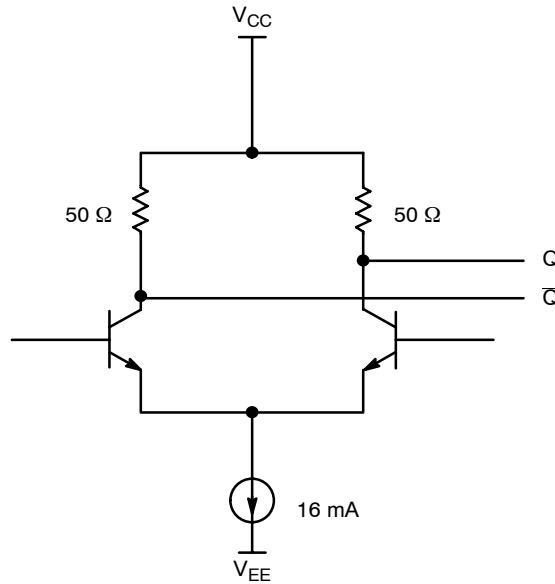


Figure 14. CML Output Structure

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APPLICATION INFORMATION

All NB7L32M inputs can accept PECL, CML, and LVDS signal levels. The limitations for differential input signal (LVDS, PECL, or CML) are minimum input swing of 150 mV and the maximum input swing of 2500 mV. Within these conditions, the input voltage can range from V_{CC} to 1.2 V. Examples interfaces are illustrated below in a 50 Ω environment ($Z = 50 \Omega$). For output termination and interface, refer to application note AND8020/D.

Table 5. INTERFACING OPTIONS

Interfacing Options	Connections
CML	Connect VTD and \overline{VTD} to V_{CC} (See Figure 15)
LVDS	Connect VTD and \overline{VTD} Together (See Figure 17)
AC-COUPLED	Bias VTD and \overline{VTD} Inputs within Common Mode Range (V_{CMR}) (See Figure 16)
RSECL, PECL, NECL	Standard ECL Termination Techniques (See Figure 9)

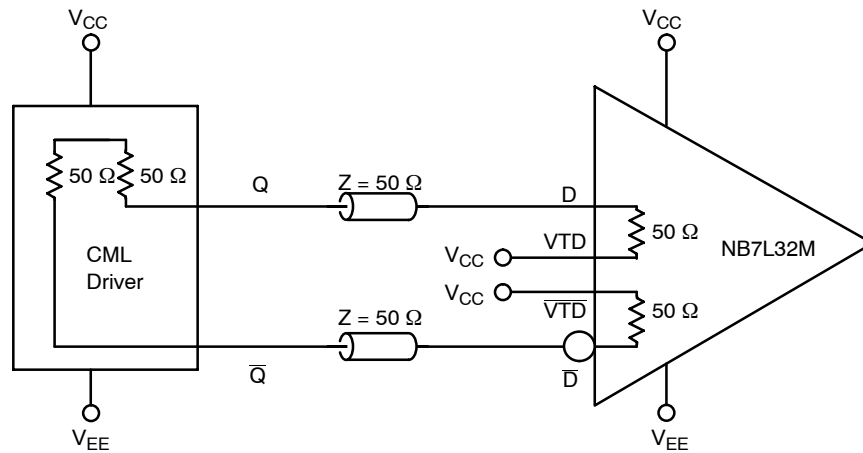
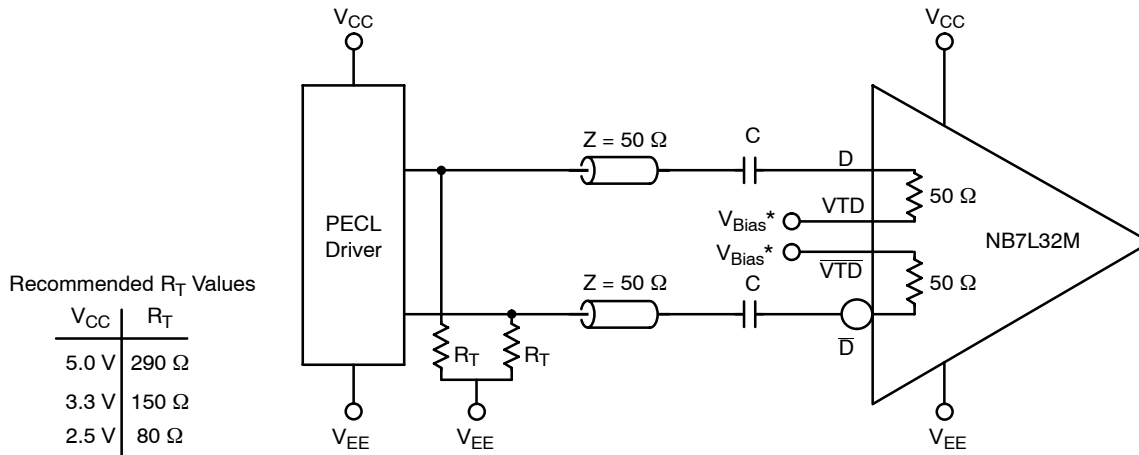


Figure 15. CML to NB7L32M Interface



Recommended R_T Values

V_{CC}	R_T
5.0 V	290 Ω
3.3 V	150 Ω
2.5 V	80 Ω

* V_{Bias} must be within common mode range limits (V_{CMR})

Figure 16. PECL to NB7L32M Interface

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APPLICATION INFORMATION

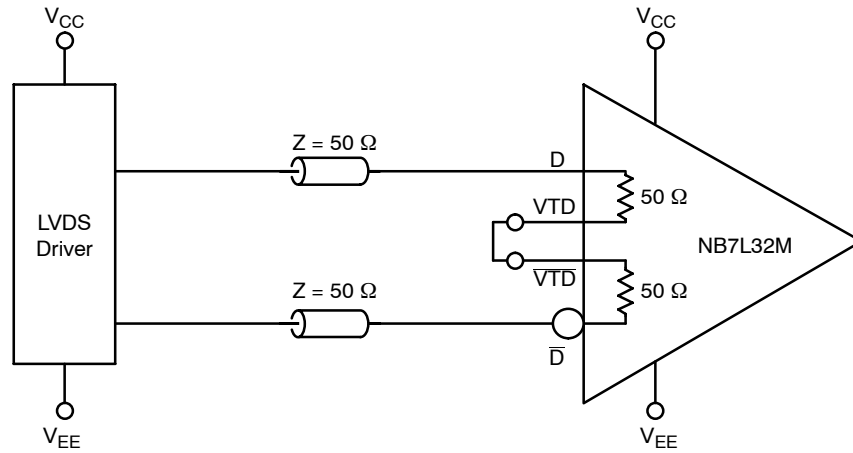


Figure 17. LVDS to NB7L32M Interface

ORDERING INFORMATION

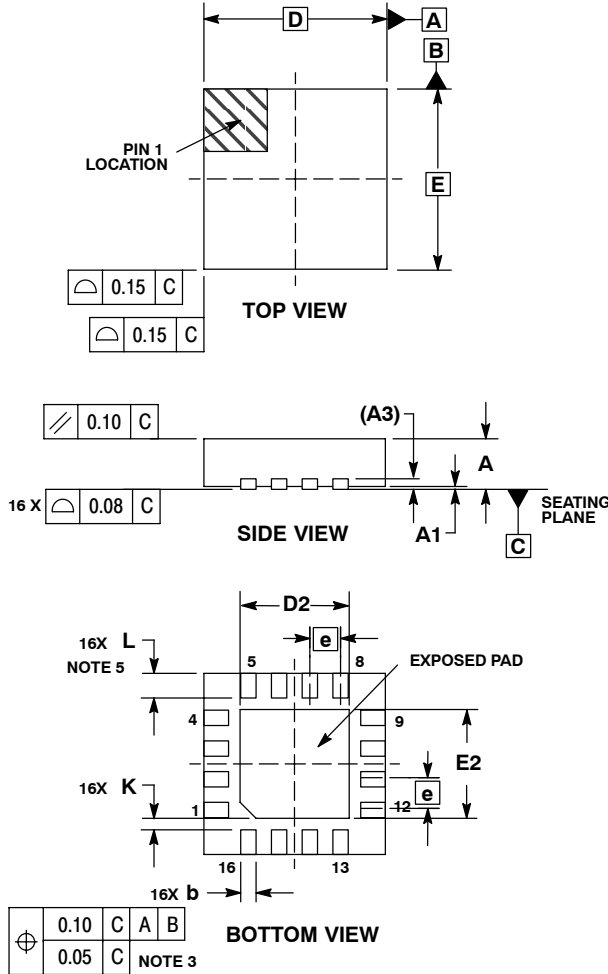
Device	Package	Shipping†
NB7L32MMNG	QFN-16 (Pb-Free)	123 Units / Rail
NB7L32MMNR2G	QFN-16 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NB7L32M

PACKAGE DIMENSIONS

16 PIN QFN
MN SUFFIX
CASE 485G-01
ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. L_{max} CONDITION CAN NOT VIOLATE 0.2 MM MINIMUM SPACING BETWEEN LEAD TIP AND FLAG

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20	REF
b	0.18	0.30
D	3.00	BSC
D2	1.65	1.85
E	3.00	BSC
E2	1.65	1.85
e	0.50	BSC
K	0.20	---
L	0.30	0.50

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