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DS3277-1.2

NJ8820

FREQUENCY SYNTHESISER (PROM INTERFACE)

The NJ8820 is a synthesiser circuit fabricated on the GPS CMOS process and is capable of achieving high sideband attenuation and low noise performance. It contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented as eight 4-bit words read from an external memory, with the necessary timing signals generated internally.

It is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 series to produce a universal binary coded synthesiser.

The NJ8820 is available in Plastic DIL (DP) and Miniature Plastic DIL (MP) packages, both with operating temperature range of −30°C to +70°C. The NJ8820MA is available only in Ceramic DIL package with operating temperature range of −40°C to +85°C.

FEATURES

- Low Power Consumption
- Direct Interface to ROM or PROM
- High Performance Sample and Hold Phase Detector
- >10MHz Input Frequency

ORDERING INFORMATION

NJ8820 BA DP Plastic DIL Package
NJ8820 BA MP Miniature Plastic DIL Package
NJ8820 MA DG Ceramic DIL Package

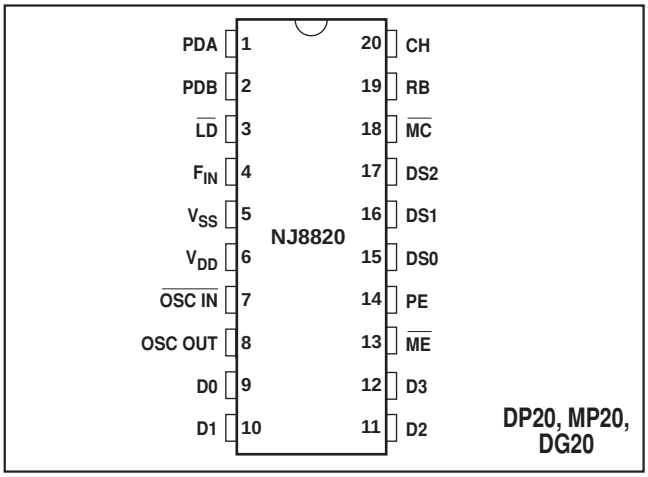

Fig.1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_{DD}-V_{SS}$	−0·5V to 7V
Input voltage	
Open drain outputs, pins 3 and 13	7V
All other pins	$V_{SS}-0{\cdot}3V$ to $V_{DD}+0{\cdot}3V$
Storage temperature	−65°C to +150°C (DG package, NJ8820MA)
Storage temperature	−55°C to +125°C (DP and MP packages, NJ8820)

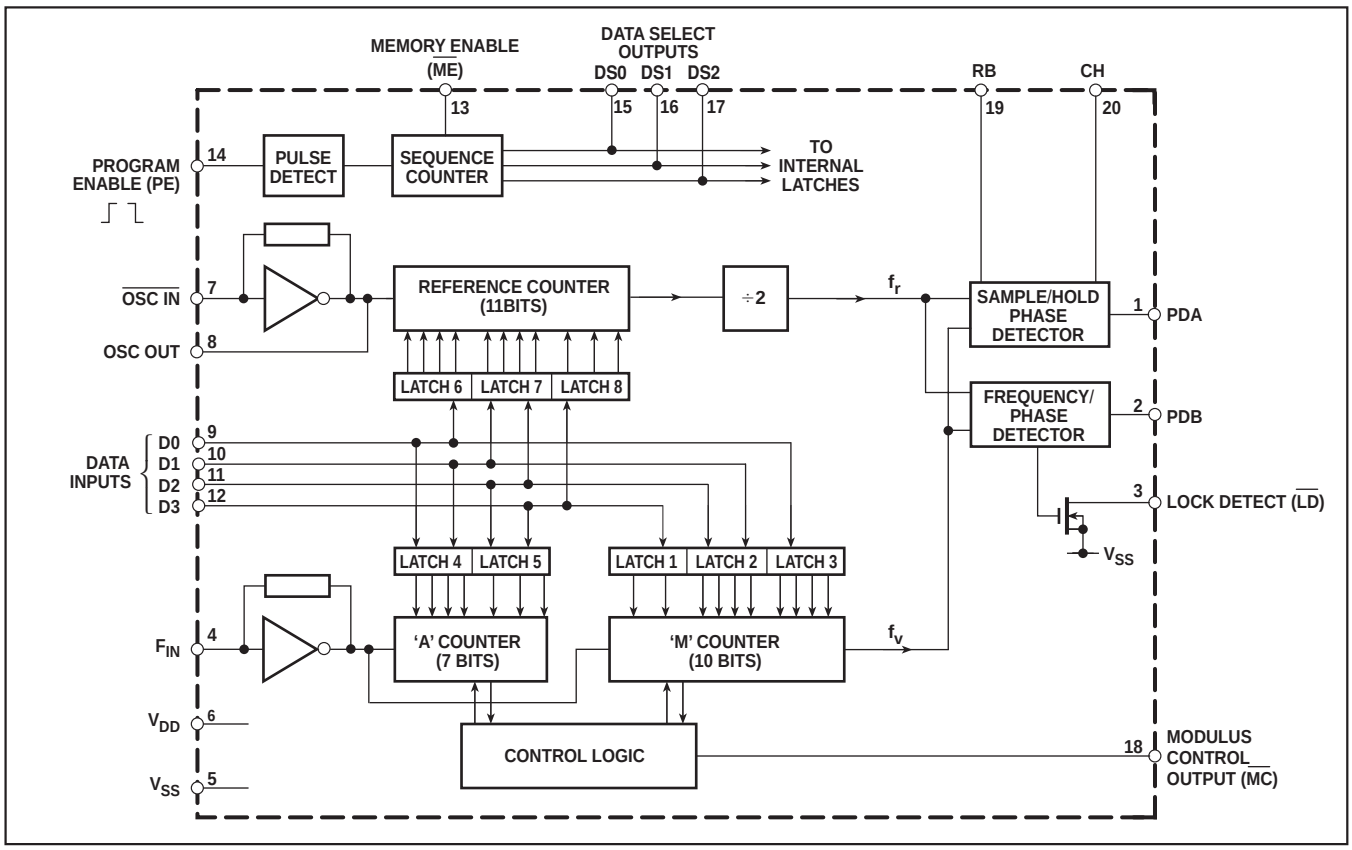

Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS AT V_{DD} = 5V

Test conditions unless otherwise stated:

V_{DD}–V_{SS}=5V ±0·5V. Temperature range NJ8820 BA: –30°C to +70°C; NJ8820 MA: –40°C to +85°C

DC Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		3·5	5·5	mA	f_{osc}, f_{FIN} = 10MHz } 0 to 5V square wave
		0·7	1·5	mA	f_{osc}, f_{FIN} = 1·0MHz }
OUTPUT LEVELS					
Memory Enable Output ($\overline{ME}$)					
Low level			0·4	V	I_{SINK} = 4mA
Open drain pull-up voltage			7	V	
Data Select Outputs (DS0-DS2)					
High level	4·6			V	I_{SOURCE} = 1mA
Low level			0·4	V	I_{SINK} = 2mA
Modulus Control Output ($\overline{MC}$)					
High level	4·6			V	I_{SOURCE} = 1mA
Low level			0·4	V	I_{SINK} = 1mA
Lock Detect Output ($\overline{LD}$)					
Low level			0·4	V	I_{SINK} = 4mA
Open drain pull-up voltage			7	V	
PDB Output					
High level	4·6			V	I_{SOURCE} = 5mA
Low level			0·4	V	I_{SINK} = 5mA
3-state leakage current			±0·1	µA	
INPUT LEVELS					
Data Inputs (D0-D3)					
High level	4·25			V	TTL compatible
Low level			0·75	V	See note 1
Program Enable Input (PE)					
Trigger level	V_{BIAS} ±100mV			V	V_{BIAS} = self-bias point of PE (nominally V_{DD}/2)

AC Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
F_{IN} and $\overline{OSC\ IN}$ input level	200			mVRMS	10MHz AC-coupled sinewave
Max. operating frequency, f_{FIN} and f_{osc}	10·6			MHz	Input squarewave V_{DD} to V_{SS}, See note 5.
Propagation delay, clock to $\overline{MC}$		30	50	ns	See note 2.
PE pulse length, t_W	5			µs	Pulse to V_{SS} or V_{DD}.
Data set-up time, t_{DS}	1			µs	
Data hold time, t_{DH}	10			ns	
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	
Hold capacitor, CH			1	nF	See note 3.
Output resistance, PDA			5	kΩ	
Digital phase detector gain		0·4		V/Rad	
Power supply rise time	100			µs	10% to 90%, see note 4.

NOTES

1. Data inputs have internal pull-up resistors to enable them to be driven from TTL outputs.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. The finite output resistance of the internal voltage follower and 'on' resistance of the sample switch driving this pin will add a finite time constant to the loop. An external 1nF hold capacitor will give a maximum time constant of 5µs, typically.
4. To ensure correct operation of power-on programming.
5. Operation at up to 15MHz is possible with a full logic swing but is not guaranteed.

PIN DESCRIPTIONS

Pin no.	Name	Description
1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. Output at $(V_{DD}-V_{SS})/2$ when the system is in lock. Voltage increases as f_v phase lead increases; voltage decreases as f_r phase lead increases. Output is linear over only a narrow phase window, determined by gain (programmed by RB).
2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. $f_v > f_r$ or f_v leading: positive pulses with respect to the bias point V_{BIAS} $f_v < f_r$ or f_r leading: negative pulses with respect to the bias point V_{BIAS} $f_v = f_r$ and phase error within PDA window: high impedance.
3	$\overline{LD}$	An open-drain lock detect output at low level when phase error is within PDA window (in lock); high impedance at all other times.
4	F_{IN}	The input to the main counters, normally driven from a prescaler, which may be AC-coupled or, when a full logic swing is available, may be DC-coupled.
5	V_{SS}	Negative supply (ground).
6	V_{DD}	Positive supply.
7, 8	$\overline{OSC\ IN}$/ OSC OUT	These pins form an on-chip reference oscillator when a series resonant crystal is connected across them. Capacitors of appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. An external reference signal may, alternatively, be applied to $\overline{OSC\ IN}$. This may be a low-level signal, AC-coupled, or if a full logic swing is available it may be DC-coupled. The program range of the reference counter is 3 to 2047, with the division ratio being twice the programmed number.
9,10, 11, 12	D0-D3	Information on these inputs is transferred to the internal data latches during the appropriate data read time slot. D3 is MSB, D0 is LSB.
13	$\overline{ME}$	An open drain output for use in controlling the power supply to an external ROM or PROM. $\overline{ME}$ is low during the data read period and high impedance at other times.
14	PE	A positive or negative pulse or edge AC-coupled into this pin initiates the single-shot data read procedure. Grounding this pin repeats the data read procedure in a cyclic manner.
15, 16, 17	DS0-DS2	Internally generated three-state data select outputs, which may be used to address external memory.
18	$\overline{MC}$	Modulus control output for controlling an external dual-modulus prescaler. $\overline{MC}$ will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. $\overline{MC}$ then goes high and remains high until the 'M' counter completes its cycle, at which point both 'A' and 'M' counters are reset. This gives a total division ratio of $MP+A$, where P and $P+1$ represent the dual-modulus prescaler values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including ÷128/129. The programming range of the 'M' counter is 8-1023 and, for correct operation, $M \geqslant A$. Where every possible channel is required, the minimum total division ratio should be P^2-P.
19	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V_{SS}.
20	CH	An external hold capacitor should be connected between this pin and V_{SS}.

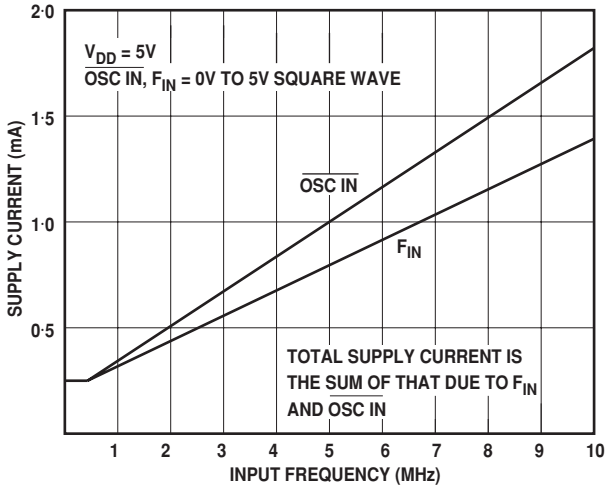

Fig. 3 Typical supply current v. input frequency

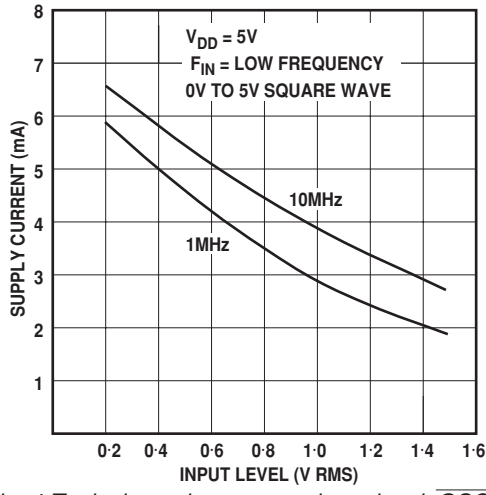

Fig. 4 Typical supply current v. input level, $\overline{OSC\ IN}$

PROGRAMMING

Program information can be obtained from an external ROM or PROM under the control of the NJ8820. Twenty-eight data bits are required per channel arranged as eight 4-bit words leaving four redundant bits, two of which are available on the data bus driving the data transfer time slot and may be used for external control purposes. A suitable PROM would be the 74S287, giving up to 32 channel capability as shown in Fig. 5. Note that the choice of PNP transistor and supply bypass capacitor on the ROM should be such that the ROM will power up in time: for example, at 10MHz oscillator frequency, the ROM must be powered up in less than 25μs.

Reading this data is normally done in single shot mode, with the data read cycle started by either a positive or negative pulse on the program enable (PE) pin. The data read cycle is generated from a program clock at 1/64 of the reference oscillator frequency. A memory enable signal ($\overline{ME}$) is supplied to allow power-down of the ROM when it is not in use. Data select outputs (DS0-DS2) remain in a high impedance state when the program cycle is completed to allow the address bus to be used for other functions if desired. The data map, data read cycle and timing diagram are shown in Figs. 6 to 8. Data is latched internally during the portions of the program cycle shown shaded in Fig. 7 and all data is transferred to the counters and latched during the data transfer time slot.

Alternatively, the PE pin may be grounded, causing the data read cycle to repeat cyclically to allow continuous up-dating of the program information. In this mode, external memory will be enabled continuously ($\overline{ME}$ low) and the data read cycle will repeat every sixteen cycles of the internal program clock, i.e. every $1024/f_{osc}$ seconds. This programming method is not recommended because the higher power consumption and the possibilities of noise into the loop from the digital data lines.

Power-on Programming

On power-up, the data read cycle is automatically initiated, making it unnecessary to provide a PE pulse. The circuit detects the power supply rising above a threshold point (nominally 1·5V) and, after an internally generated delay to allow the supply to rise fully, the circuit is programmed in the normal way. This delay is generated by counting reference oscillator pulses and is therefore dependent on the crystal used. The delay consists of 53248 reference oscillator cycles, giving a delay of about 5ms at 10MHz.

To ensure correct operation of this function, the power supply rise time should be less than 5ms (at 10MHz), rising smoothly through the threshold point.

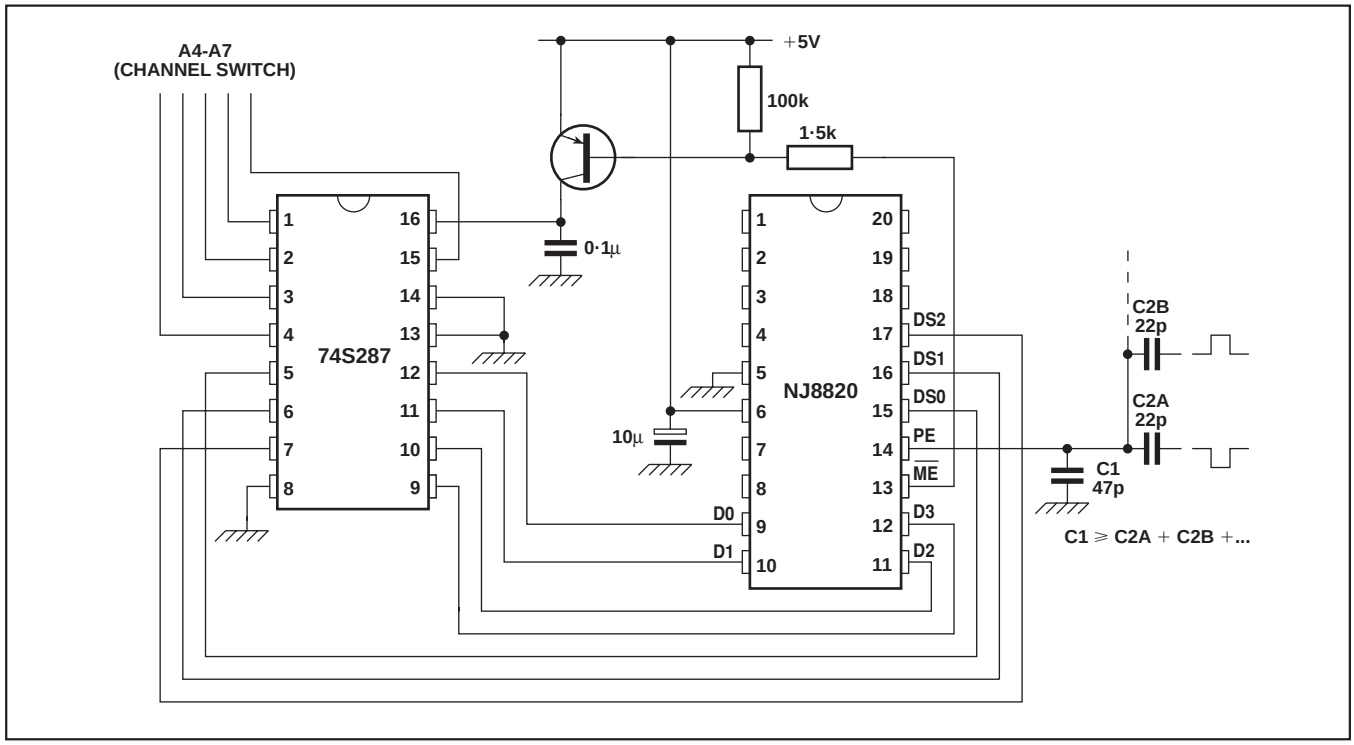

Fig. 5 Programming via PROM

WORD	DS2	DS1	DS0	D3	D2	D1	D0
1	0	0	0	M1	M0	-	-
2	0	0	1	M5	M4	M3	M2
3	0	1	0	M9	M8	M7	M6
4	0	1	1	A3	A2	A1	A0
5	1	0	0	-	A6	A5	A4
6	1	0	1	R3	R2	R1	R0
7	1	1	0	R7	R6	R5	R4
8	1	1	1	-	R10	R9	R8

Fig. 6 Data map

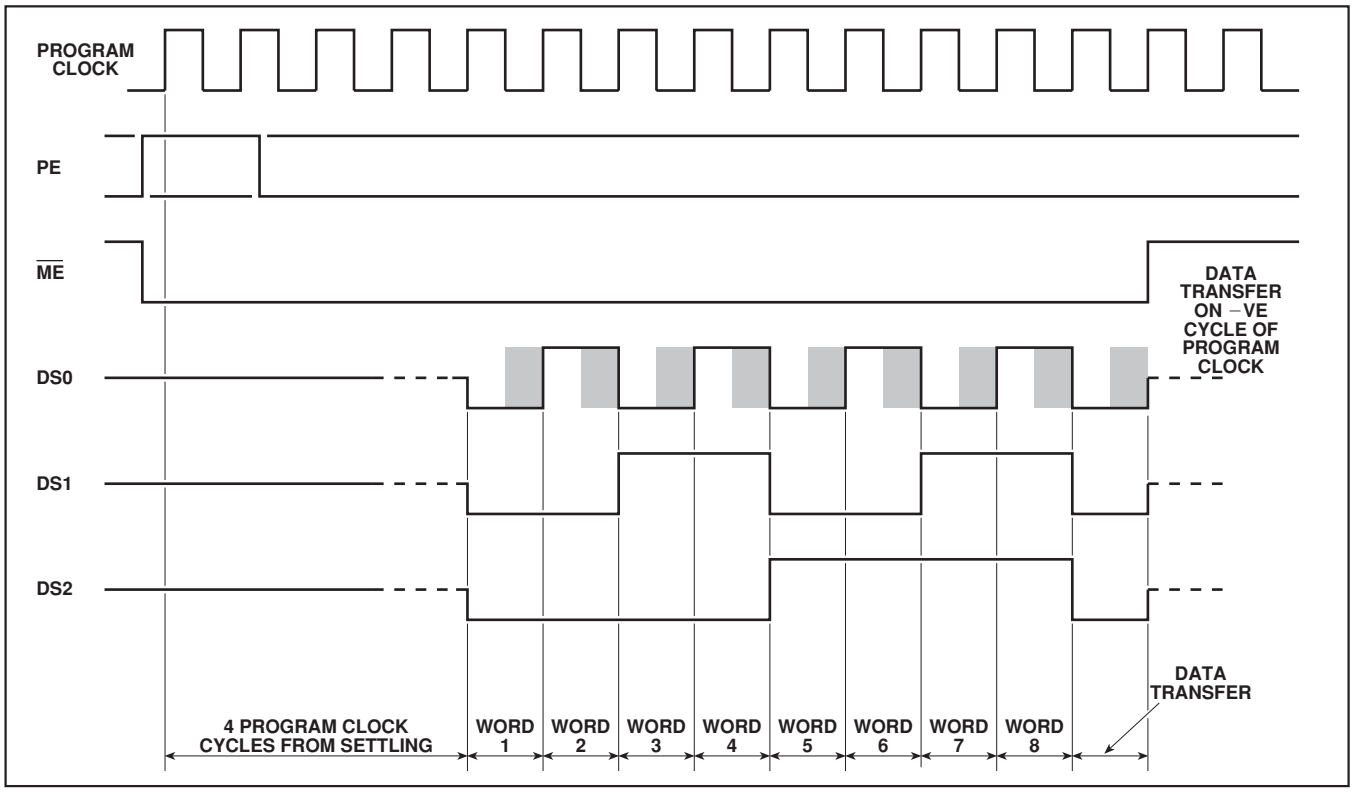

Fig.7 Data selection

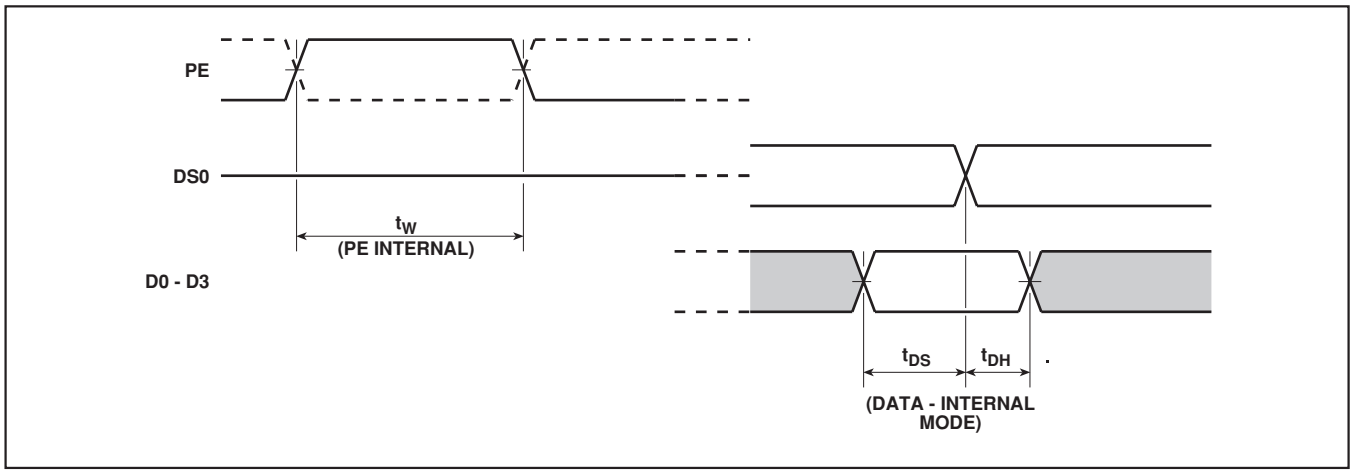

Fig.8 Timing diagram

PHASE COMPARATORS

The digital phase/frequency detector drives a three-state output, PDB, which provides a 'coarse' error signal to enable fast switching between channels. The PDB output is active until the phase error is within the sample and hold phase detector, PDA, window, when PDB becomes high impedance. Phase-lock is indicated at this point by a low level on $\overline{LD}$. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

An internally generated ramp, controlled by the digital output from both the reference and main divider chains, is sampled at the reference frequency to give the 'fine' error signal, PDA. When in phase lock, this output would be typically at $(V_{DD}-V_{SS})/2$ and any offset from this would be proportional to phase error. The relationship between this offset and the phase error is the phase comparator gain, which is programmable with an external resistor, RB. An internal 50pF capacitor is used in the sample and hold comparator.

CRYSTAL OSCILLATOR

When using the internal oscillator, the stability may be enhanced at high frequencies by the inclusion of a resistor between pin 8 (OSC OUT) and the other components. A value of 2·2kΩ is advised.

PROGRAMMING/POWER UP

Data and signal input pins should not have input applied to them prior to the application of V_{DD}, as otherwise latch-up may occur.

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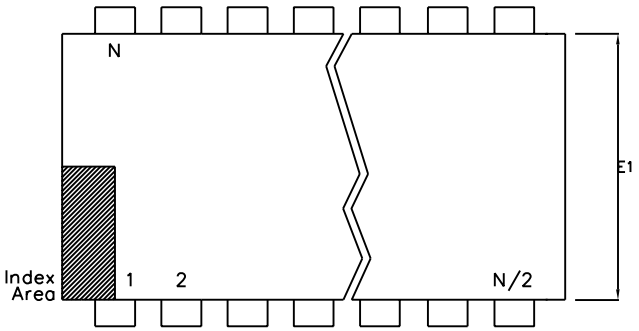
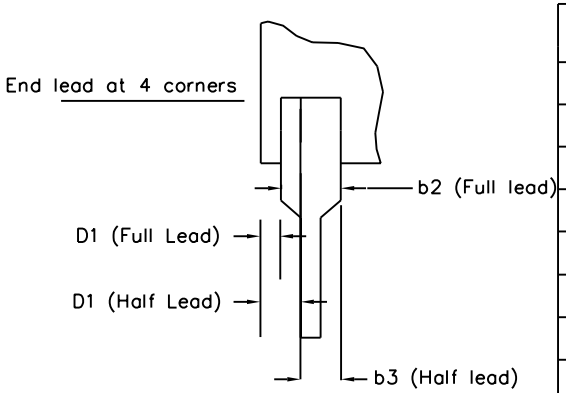
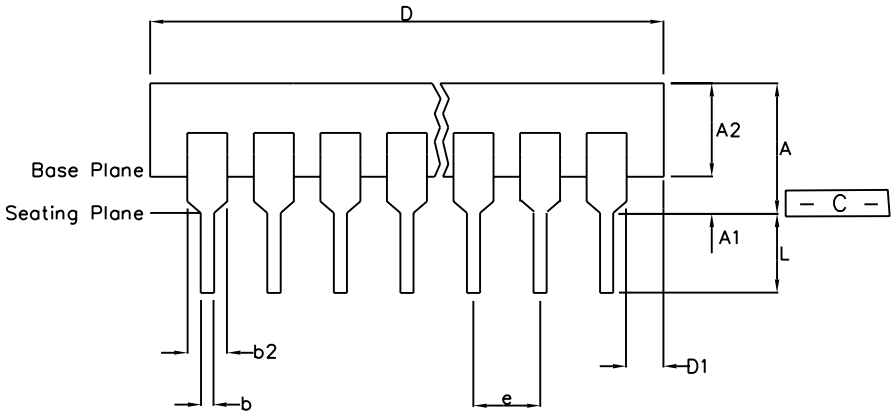
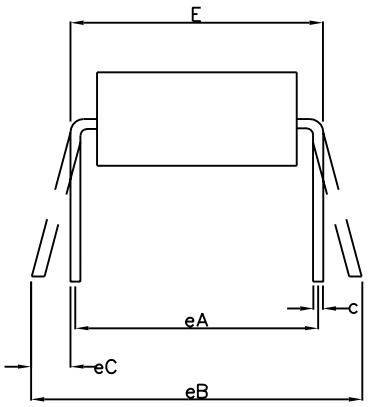








	Min mm	Max mm	Min Inches	Max Inches
A		5.33		0.210
A1	0.38		0.015	
A2	2.92	4.95	0.115	0.195
b	0.36	0.56	0.014	0.022
b2	1.14	1.78	0.045	0.070
b3	n/a	n/a	n/a	n/a
c	0.20	0.36	0.008	0.014
D	24.89	26.92	0.980	1.060
D1	0.13		0.005	
E	7.62	8.26	0.300	0.325
E1	6.10	7.11	0.240	0.280
e	2.54 BSC		0.100 BSC	
eA	7.62 BSC		0.300 BSC	
eB		10.92		0.430
eC	0.00	1.52	0.000	0.060
L	2.92	3.81	0.115	0.150
N	20		20	
Conforms to Jedec MS-001AD Issue D				

Notes:
1. Dimensions D, D1 & E1 do not include mould flash or protrusions.
2. Dimensions E & eA are measured with leads constrained to be perpendicular to datum – C –
3. Dimensions eB & eC are measured with the leads unconstrained
4. Controlling dimensions are Inches. Millimeter conversions are not necessarily exact.
5. N is the maximum of terminal positions.

This drawing supersedes: –
UK drawing # 418/ED/39502/005

ISSUE	1	2		
ACN	202562	213107		
DATE	9Jun97	15Jul02		
APPRD.				

ZARLINK SEMICONDUCTOR

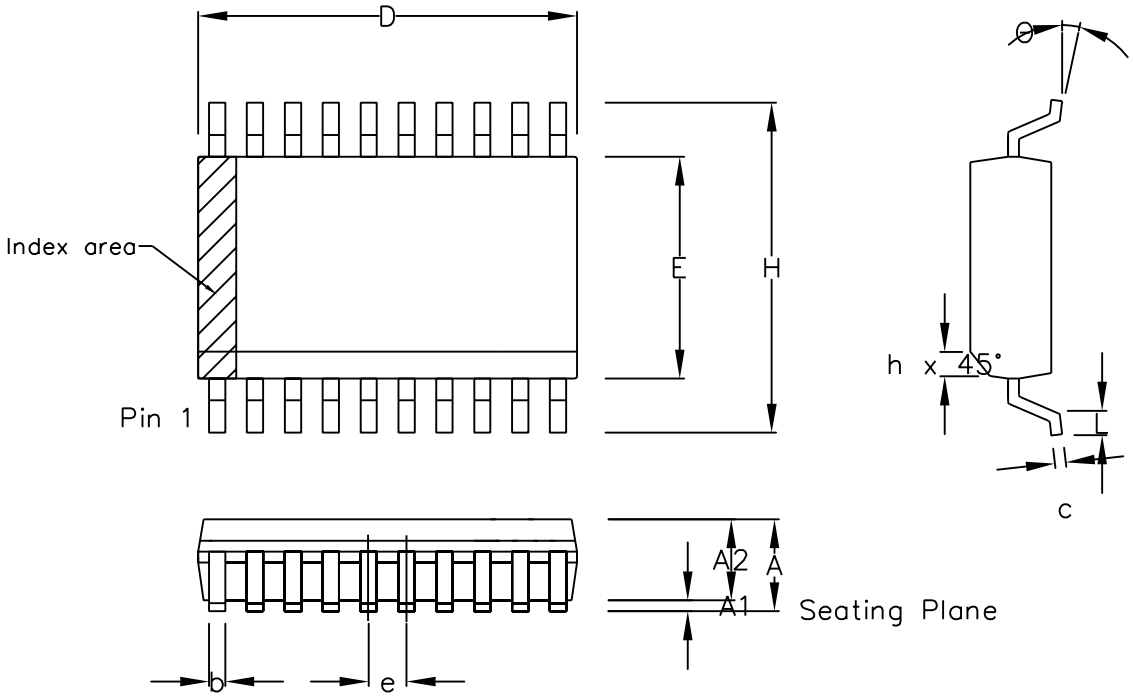
Previous package codes

DP / E

Package Code DA

Package Outline for 20 lead PDIP

GPD00347



Symbol	Control Dimensions in millimetres				Altern. Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A	2.35		2.65		0.093		0.104
A1	0.10		0.30		0.004		0.012
A2	2.25		2.35		0.089		0.092
D	12.60		13.00		0.496		0.512
H	10.00		10.65		0.394		0.419
E	7.40		7.60		0.291		0.299
L	0.40		1.27		0.016		0.050
e	1.27 BSC.				0.050 BSC.		
b	0.33		0.51		0.013		0.020
c	0.23		0.32		0.009		0.013
θ	0°		8°		0°		8°
h	0.25		0.75		0.010		0.029
	Pin features						
N	20						
Conforms to JEDEC MS-013AC Iss. C							

Notes:
1. The chamfer on the body is optional. If it not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimension are in millimeters.
3. Dimension D do not include mould flash, protrusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protrusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.004" total in excess of b dimension.

ISSUE	1	2	3	
ACN	6746	201941	213098	
DATE	7Apr95	27Feb97	15Jul02	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

MP / S

Package Code DC

Package Outline for 20 lead SOIC (0.300" Body Width)

GPD00015

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www.zarlink.com