TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74ACT245P, TC74ACT245F, TC74ACT245FW, TC74ACT245FT
TC74ACT640P, TC74ACT640F, TC74ACT640FW, TC74ACT640FT

OCTAL BUS TRANSCEIVER

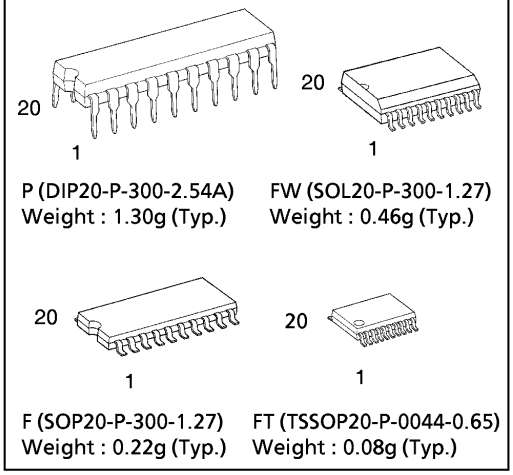
TC74ACT245P/F/FW/FT 3 – STATE, NON – INVERTING
TC74ACT640P/F/FW/FT 3 – STATE, INVERTING

(Note) The JEDEC SOP (FW) is not available in Japan.

The TC74ACT245 and 640 are advanced high speed CMOS OCTAL BUS TRANSCEIVERs fabricated with silicon gate and double - layer metal wiring C^2MOS technology.
They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.
These devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL,NMOS and CMOS output voltage levels.
They are intended for two - way asynchronous communication between data busses. The direction of data transmission is determined by the level of the DIR input.
The enable input ($\overline{G}$) can be used to disable the device so that the busses are effectively isolated.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES :

- High Speed ····· t_{pd} = 4.7ns(typ.) at V_{CC} = 5V
- Low Power Dissipation ····· I_{CC} = 8μA(Max.) at Ta = 25°C
- Compatible with TTL outputs ···· V_{IL} = 0.8V(Max.)
  V_{IH} = 2.0V(Min.)
- Symmetrical Output Impedance ··· $|I_{OH}| = I_{OL}$ = 24mA(Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Pin and Function Compatible with 74F245/640



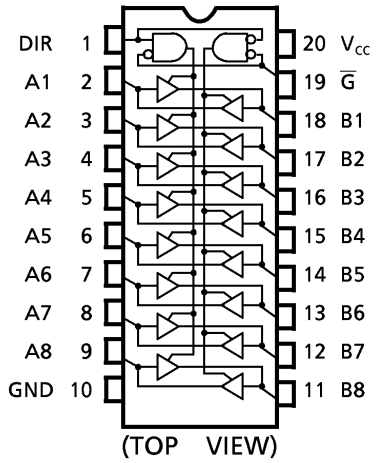
P (DIP20-P-300-2.54A) Weight : 1.30g (Typ.)
FW (SOL20-P-300-1.27) Weight : 0.46g (Typ.)
F (SOP20-P-300-1.27) Weight : 0.22g (Typ.)
FT (TSSOP20-P-0044-0.65) Weight : 0.08g (Typ.)

APPLICATION NOTES

1) Do not apply a signal to any bus terminal when it is in the out put mode. Damage may result.
2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.

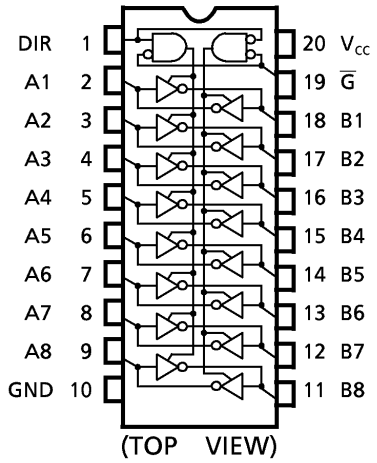
PIN ASSIGNMENT

TC74ACT245



(TOP VIEW)

TC74ACT640

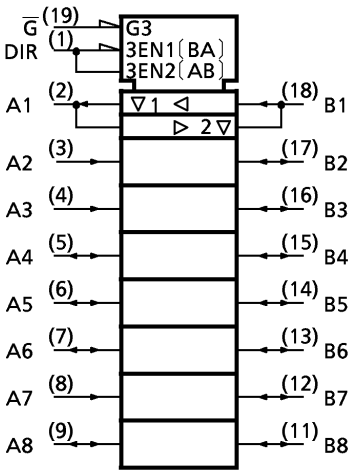


(TOP VIEW)

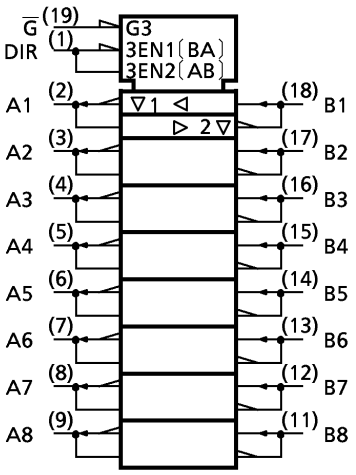
961001EBA2

IEC LOGIC SYMBOL

TC74ACT245



TC74ACT640



TRUTH TABLE

INPUTS		FUNCTION		OUTPUTS	
$\overline{G}$	DIR	A BUS	B BUS	ACT245	ACT640
L	L	OUTPUT	INPUT	A = B	A = $\overline{B}$
L	H	INPUT	OUTPUT	B = A	B = $\overline{A}$
H	X	High Impedance		Z	Z

X : Don't Care
Z : High Impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP/TSSOP)	mW
Storage Temperature	T_{stg}	−65~150	°C

*500mW in the range of Ta = −40°C~65°C. From Ta = 65°C to 85°C a derating factor of −10mW/°C should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt / dV	0~10	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
High - Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V_{IL}			4.5 ~ 5.5	—	—	0.8	—	0.8	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA I_{OH} = −24mA I_{OH} = −75mA*	4.5 4.5 5.5	4.4 3.94 —	4.5 — —	— — —	4.4 3.80 3.85	— — —	V
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA I_{OL} = 24mA I_{OL} = 75mA*	4.5 4.5 5.5	— — —	0.0 — —	0.1 0.36 —	— — —	0.1 0.44 1.65	V
3 - State Output Off - State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	—	—	±0.5	—	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	—	—	±0.1	—	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	8.0	—	80.0	
	I_C	PER INPUT : V_{IN} = 3.4V OTHER INPUT : V_{CC} or GND		5.5	—	—	1.35	—	1.5	mA

* : This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, R_L = 500Ω, Input $t_r = t_f$ = 3ns)

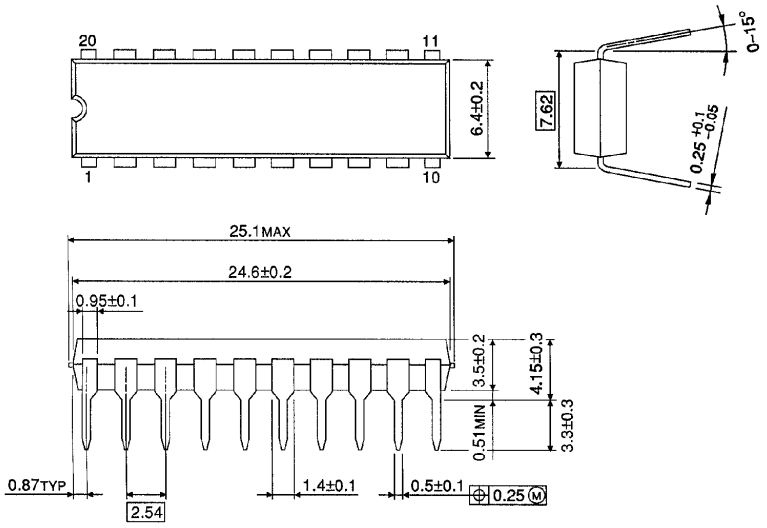
PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time*	t_{pLH} t_{pHL}		5.0 ± 0.5	−	5.0	8.0	1.0	9.0	ns
Propagation Delay Time**	t_{pLH} t_{pHL}		5.0 ± 0.5	−	5.7	8.5	1.0	9.5	
Output Enable Time	t_{pZL} t_{pZH}		5.0 ± 0.5	−	7.3	12.3	1.0	14.0	
Output Disable Time	t_{pLZ} t_{pHZ}		5.0 ± 0.5	−	6.3	9.7	1.0	11.0	
Input Capacitance	C_{IN}	DIR, $\overline{G}$		−	5	10	−	10	pF
Bus Input Capacitance	$C_{I/O}$	An, Bn		−	13	−	−	−	
Power Dissipation Capacitance	C_{PD} (1)	TC74ACT245		−	38	−	−	−	
		TC74ACT640		−	43	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8 \text{ (per bit)}$$

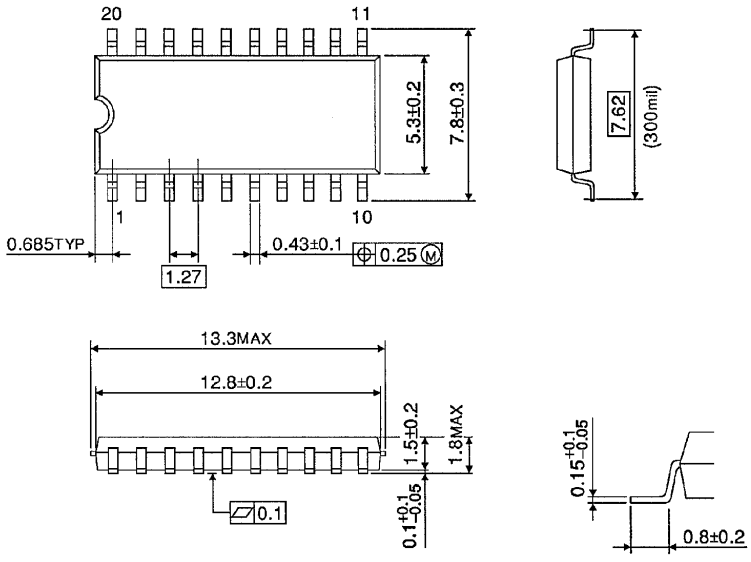
(2) * for TC74ACT245 only
** for TC74ACT640 only

DIP 20PIN OUTLINE DRAWING (DIP20-P-300-2.54A) Unit in mm



Weight : 1.30g (Typ.)

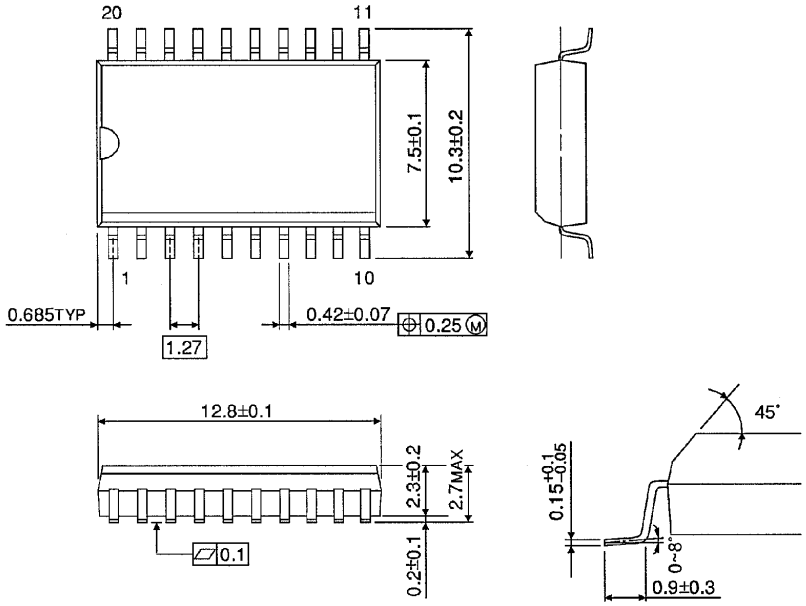
SOP 20PIN (200mil BODY) OUTLINE DRAWING (SOP20-P-300-1.27) Unit in mm



Weight : 0.22g (Typ.)

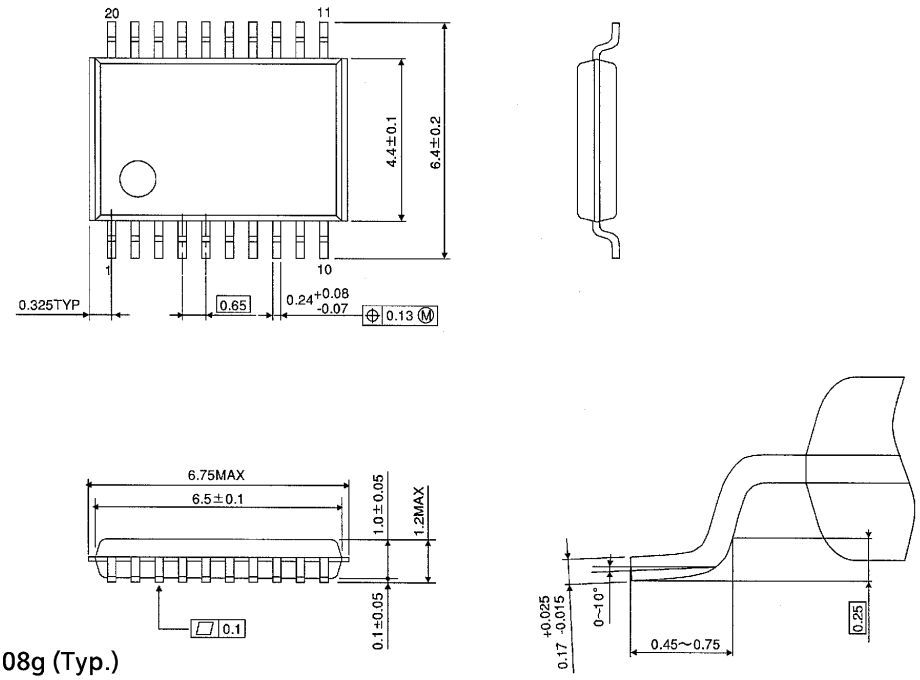
SOP 20PIN (300mil BODY) OUTLINE DRAWING (SOL20-P-300-1.27) Unit in mm

(Note) This package is not available in Japan.



Weight : 0.46g (Typ.)

TSSOP 20PIN OUTLINE DRAWING (TSSOP20-P-0044-0.65) Unit in mm



Weight : 0.08g (Typ.)