Juno™ UR8HC007-001

Input Device and Power Management Companion IC for Jupiter Devices

HID & SYSTEM MANAGEMENT PRODUCTS, H/PC IC FAMILY

DESCRIPTION

Juno™ 01 is a member of a series of multi-functional companion ICs for Jupiter and other devices running Microsoft® Windows® CE and utilizing RISC-based processors. The IC interfaces the system via either asynchronous serial or the Serial Peripheral Interface (SPI) and provides keyboard scanning, special general purpose I/O (GPIO) and unique system power management capabilities.

The Zero-Power™ Juno™ will power down even between key presses. Semtech's proprietary circuitry (patent pending) allows the IC to power down even when PS/2 devices are connected and active. Typical power consumption is less than 1 µA, a first for embedded ICs.

The Juno™ provides continuous operation between 3 and 5V and scans a fully programmable 8 X 16 keyboard matrix. The IC is equipped with three Zero-Power™ PS/2 ports for the hot-plug connection of an external PS/2 keyboard and mouse as well as an internal PS/2 mouse, including those with MouseWheels.

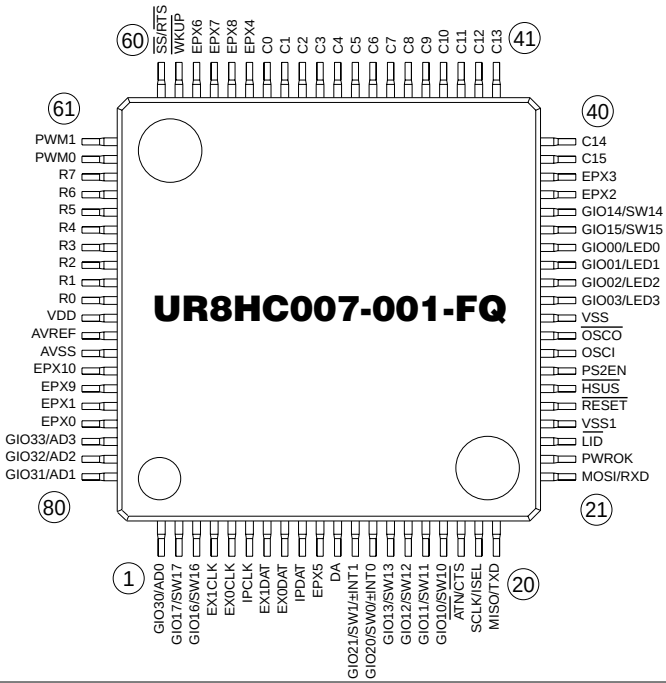
In addition, the Juno™ offers special general purpose I/O (GPIO), ideal for use for lid functions, power switches, ring indicators, docking signals, battery measurement, LEDs, etc.

The integration of features, many of them programmable, on one IC increases flexibility and reduces component count and cost.

FEATURES

- Typically consumes less than 1 µA
- Scans a fully programmable 8 X 16 matrix that supports Japanese, English and European keyboards
- Operates continuously between 3 and 5 Volts
- Offers unique power management capabilities that work in harmony with Windows® CE's power modes
- Always runs in "Stop" mode without data or event loss
- Provides three Zero-Power™ PS/2 ports for the hot-plug connection of external keyboards/mice & internal mouse, including MouseWheels
- Uses proprietary circuitry, so "Stop" mode is entered even when PS/2 devices are connected and active
- Available in 1.7mm high package to accommodate slim designs
- GPIO pins provide interrupt at both falling and rising edge of signals, ideal for lid functions, power, ring indicators, docking signals, battery measurement, etc.
- Has additional GPIO available for LEDs, switches, etc.
- Offers internal control of LCD brightness/contrast, audio, etc. as well as four 10-bit A/D channels for power management monitoring
- Cost-effective, reducing overall system costs by integrating features that would typically require multiple additional components
- Provides programmable features that allow for maximum design differentiation without customization
- Other Juno™ versions offer control of internal pointing device

PIN ASSIGNMENTS



APPLICATIONS

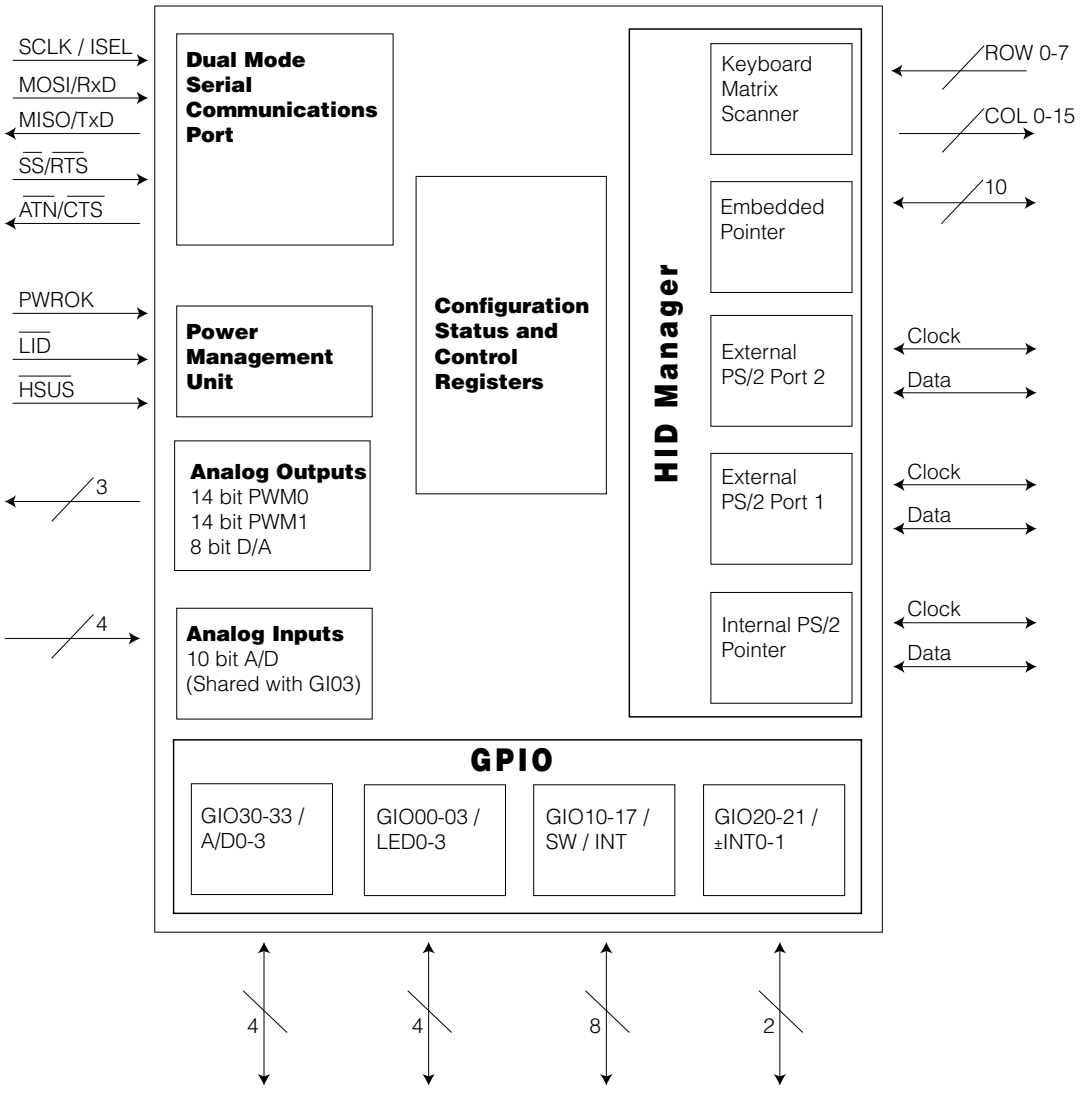
- Jupiter devices/Professional PCs
- H/PCs, Web Phones, & G3 Terminals

ORDERING CODE

Package options	**Pitch in mm's**	**TA = 0°C to +75°C**
80-pin, Plastic LQFP	0.5	UR8HC007-001-XX-FQ
Other materials	**Type**	**Part number**
Technical Reference Manual	Document	DOC8-007-001-TR-XXX
Juno™ Evaluation Kit	Evaluation Kit	EVK8-007-001-XXX

XX = Optional for customization
XXX = Denotes revision number

FUNCTIONAL DIAGRAM



PIN DEFINITIONS

Pin Numbers

Mnemonic	QFP	Type	Name and Function
Power Supply			
VDD	71	PWR	**Positive Supply Voltage**
AVREF	72	AI	Positive analog reference voltage
AVSS	73	PWR	**Ground**: analog signal
VSS	30	PWR	**Ground**: negative supply voltage
VSS1	24	PWR	Auxiliary Ground; must be tied to pin 30
Reset			
_RESET	25	I	**Controller hardware reset pin**: when at Low-level, this pin holds the UR8HC007in a reset state. This pin must be held at a logic-low until Power Supply voltage (VDD) reaches the minimum operating level (2.7V).
Oscillator pins			
OSCI	28	I	**Oscillator input**: connect ceramic resonator with built-in load capacitors or CMOS clock from external oscillator 4 MHz operating frequency
_OSCO	29	O	**Oscillator Output**: connect ceramic resonator with built-in load capacitors or keep open if external oscillator is used
Keyboard / Event Wake-up			
_WKUP	59	I/pD	**Wake-up**: wakes up the chip if there is a key press in the scanned keyboard matrix (Active-Low) or drives the pin High when running
Scanned matrix pins			
ROW0-ROW7	62-55	I	**Row matrix outputs**
COL0-COL7 COL8-COL11 COL12-COL13 COL14-COL15	54-47 38-35 27-26 79-78	O	**Column matrix outputs**
PS/2 ports			
PS2EN	27	O	**Control output**: when Low, disables PS/2 communications by holding the PS/2 Clock lines low
IPDAT	9	I5V/nD5V	**PS/2 Data** line for Internal Pointing Device
IPCLK	6	I5V/nD5V	**PS/2 Clock** line for Internal Pointing Device
EX0DAT	8	I5V/nD5V	**PS/2 Data** line for External Device 0
EX0CLK	5	I5V/nD5V	**PS/2 Clock** line for External Device 0
EX1DAT	7	I5V/nD5V	**PS/2 Data** line for External Device 1
EX1CLK	4	I5V/nD5V	**PS/2 Clock** line for External Device 1

PIN DEFINITIONS (CON'T)

Pin Numbers Mnemonic	QFP	Type	Name and Function
General Purpose Input/Ouput			
GIO0			
GIO00/LED0-GIO3/LED3	34-31	I/O	General purpose input/output pin, LED driver
GIO1			
GIO10/SW10-GIO15/SW15	17-14 36-35	I/O	General purpose input/output pin, Switch input
GIO16/SW16-GIO17/SW17	3-2	I5V/nD5V	General purpose input/output pin, Switch input
Note: In order to have a Negative Edge Interrupt capability for SW10 - SW17, the corresponding Switch Inputs should also be connected to the extended resistive network acting on the _WKUP pin. Switch closure must be tied to Ground; the IC will remain in high power consumption mode until all the switches are released.			
GIO2			
GIO20/SW0/±INT0 GIO20/SW0/±INT0	13-12	I/O, I±Int	General purpose input/output pin, Switch Input. Capable of Interrupt on both Positive and Negative edges
GIO3 - analog input			
GIO30/AD0	1	I/O/Ai	General purpose input/output pin, A/D input 0
GIO31/AD1	80	I/O/Ai	General purpose input/output pin, A/D input 1
GIO32/AD2	79	I/O/Ai	General purpose input/output pin, A/D input 2
GIO33/AD3	78	I/O/Ai	General purpose input/output pin, A/D input 3
Analog output			
PWM0	62	O	Channel 0 of Pulse Width Modulator
PWM1	61	O	Channel 1 of Pulse Width Modulator
DA	11	Ao	D/A output (Range: AVSS to AVREF)
Reserved for embedded pointing device			
EPX0	77	I/O/Ai	Driver, A/D
EPX1	76	I/O/Ai	Driver, A/D
EPX2	37	I/O	Control, Driver
EPX3	38	I/O	Control, Driver
EPX4	55	I/O	Control, Driver
EPX5	10	I/O/Ao	Control, Driver, Analog Adjustment
EPX6	58	I/Ipup/O	Left Button
EPX7	57	I/Ipup/O	Middle Button
EPX8	56	I/Ipup/O	Right Button
EPX9	75	I/O/Ai	Driver, A/D
EPX10	74	I/O/Ai	Driver, A/D
System status monitoring			
_LID	23	I±Int	Lid closed signal from the lid switch (Active-Low). Capable of Interrupt on both Positive and Negative edges
PWROK	22	I±Int	Power OK signal. Capable of Interrupt on both Positive and Negative edges

PIN DEFINITIONS (CON'T)

Mnemonic	Pin Numbers QFP	Type	Name and Function
_HSUS	26	I	Host_Suspended signal (Active-Low). When Low, indicates that Host Computer System is in Power-reduced or Stop mode.
Communication interface			
_SS/_RTS	60	I_Int	Slave_Select (SPI Mode) or Ready_To_Send (Asynchronous Serial Mode). Active-Low signal Input. Low-level indicates that the Host System has data for the UR8HC007-001 peripheral device or the Host System is ready to accept data from the UR8HC007-001 peripheral device. Capable of Interrupt on Negative edge. Pin 60 and pin 18 should both be "Low" for data exchange to occur.
_ATN/_CTS	18	O	Attention (SPI Mode) or Clear_To_Send (Asynchronous Serial Mode). Active-Low signal Output. Low-level indicates that the UR8HC007-001 peripheral device has data for the Host System or the UR8HC007 peripheral device is ready to accept data from the Host System. Pin 18 and pin 60 should both be "Low" for data exchange to occur.
MISO/TXD	20	I/O / O	Master-In-Slave-Out (SPI Mode) or Transmit Data (Asynchronous Serial Mode, Idle = "High" = 1)
MOSI/RXD	21	I	Master-Out-Slave-In (SPI Mode) or Receive Data (Asynchronous Serial Mode)
SCLK/ISEL	19	I	Serial Clock (SPI Mode) or Interface Select (Asynchronous Serial Mode). Tie "Low" to select Asynchronous Serial Mode. In SPI Mode, use the following Clock sequence: Idle-High / Negative-Edge (Shift Data) \ Positive-Edge (Latch Data), Idle-High.

Note 1: An underscore in front of the pin mnemonic denotes an active low signal.

JUNO™ FAMILY COMMUNICATIONS INTERFACE

The Juno™ family of controllers implements two modes of serial communications: The "Synchronous Peripheral Interface" (SPI) mode and the "Asynchronous Serial Interface" (ASI).

The SPI is a synchronous bi-directional, multi-slave interface that supports bit rates up to 500 Kb/s. Several Hosts and companion chips implement the SPI protocol in order to communicate with a wide range of peripherals such as EEPROMs, A/D converters, MCUs and other system components. Alternatively, the SPI may be implemented through software on the Host side.

The Juno™ family implements the _ATN as an additional hand-shake signal in order to support low power operation of the bus.

The ASI is an asynchronous interface (UART type) that operates at a fixed baud rate of 62.5 Kb/s.

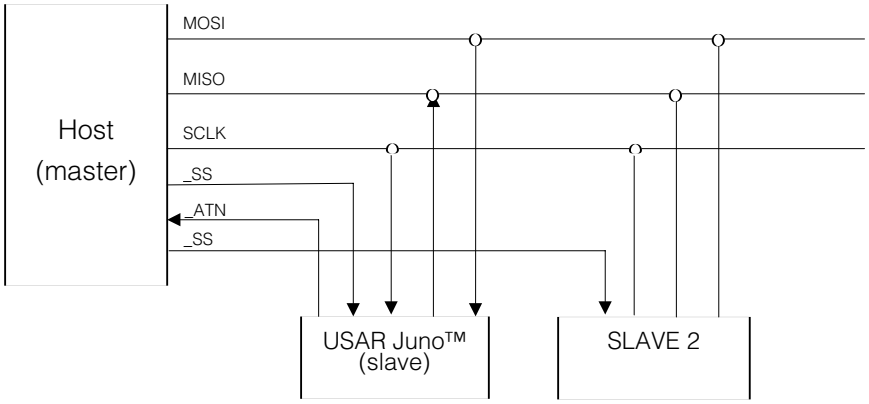
Both interfaces are implemented through the same set of four pins.

The IC determines the mode of communication with the Host during power-up by reading the value of the SCLK/ISEL pin. If the pin is tied low, the ASI mode is enabled. If it is high, the SPI interface is enabled.

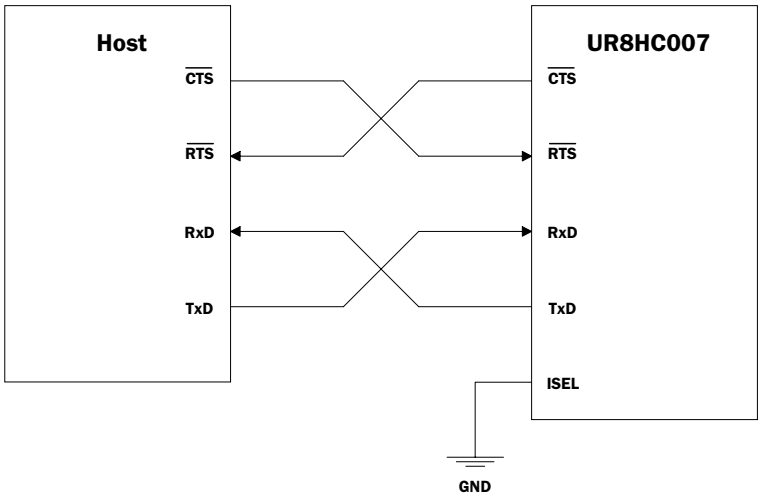
Please refer to the Juno™ Technical Reference Manual for a description of handshake and critical timing parameters for each interface.

The diagrams below describe the SPI and ASI communications interfaces, respectively.

SPI Communications Interface



ASI Communications Interface



Overview

The Juno™ UR8HC007 implements and supports four types of transaction messages.

1. Commands from the UR8HC007 to the Host system

2. Commands from the Host system to the UR8HC007

3. Human Input Device (HID) reports to the system

4. Event Alert messages to the system

The protocol is fundamentally implemented through a set of general packet commands that allow handling and reporting of each individual controller register and each bit within each register. In this manner, the system achieves maximum flexibility in manipulating the operation of the UR8HC007 controller.

General Message Structure

Communications between the Juno™ UR8HC007 and the Host processor are implemented using a set of packet protocols and commands. The general structure of a message is shown in the following diagram:

Protocol Header
Command/Report Identifier
Message Body (if applicable)
LRC

General Message Format

The Protocol Header identifies the type of transaction. The following table lists the available protocols.

Protocol Headers

Protocols used in commands issued by the Host	
Protocol	**Header**
Simple Commands	80H
Write Register bit	81H
Read Register bit	82H
Write Register	83H
Read Register	84H
Write Block	85H
Read Block	86H
Protocols used in responses, reports and alerts issued by the controller	
Protocol	**Header**
Simple Commands	80H
Report Register bit & Event Alerts	81H
Report Register	83H
Report Block	85H
Pointing Device Data Report	87H
Keyboard Device Data Report	88H

HID Data Report

The Pointing Device Data Reports format covers both absolute (where applicable) and relative positioning devices. In addition, it provides support for MouseWheel-type of input devices.

Keyboard Data Report

The Keyboard Data Reports return changes on the keyboard matrix or the External PS/2 keyboard device. Keys are uniquely identified according to the Key Number table listed in Appendix A of the Juno™ Technical Reference Manual. The Key Up or Key Release numbers comprise the logic OR of the Key Number and 80H.

LRC (Longitudinal Redundancy Check)

The LRC is calculated for the whole packet, including the Protocol Header. The LRC is calculated by first taking the bitwise exclusive OR of all bytes from the message. If the most significant bit (MSB) of the LRC is set, the LRC is modified by clearing the MSB and changing the state of the next most significant bit. Thus, the Packet Check Byte will never consist of a valid LRC with the most significant bit set.

General Commands Format

For protocols used by either the host or the UR8HC007, a set of simple commands is implemented. These support the basic communication protocol and handle reset and errors in transmission.

A simple command would have the following structure:

Header (80H)
Command Code
LRC

Simple Command Structure

Following is a summary of the simple commands used by both the Host and the UR8HC007:

Simple Commands Summary

Command	Protocol	Cmd Code	Description
Initialize	Simple	20H	Forces the recipient to enter the known default power-on state
Initialization Complete	Simple	21H	Issued as a hand-shake response only to the "Initialize" command.
Resend Request	Simple	25H	Issued upon error in the reception of a package. The recipient will resend the last transmitted packet

REGISTERS

The Juno™ implements a set of internal registers that can be used to control and monitor the operation of the various functional units of the controller IC. These registers can be accessed through the Read/Write Register commands described in the Commands chapter of the *Juno™ Technical Reference Manual*. The register architecture of the Juno™ allows for maximum flexibility and expandability of the controller operation. At the same time, by using the default values for each register, a system can utilize all the basic functionality of the IC controller with minimum Host driver intervention.

Registers' Page Organization

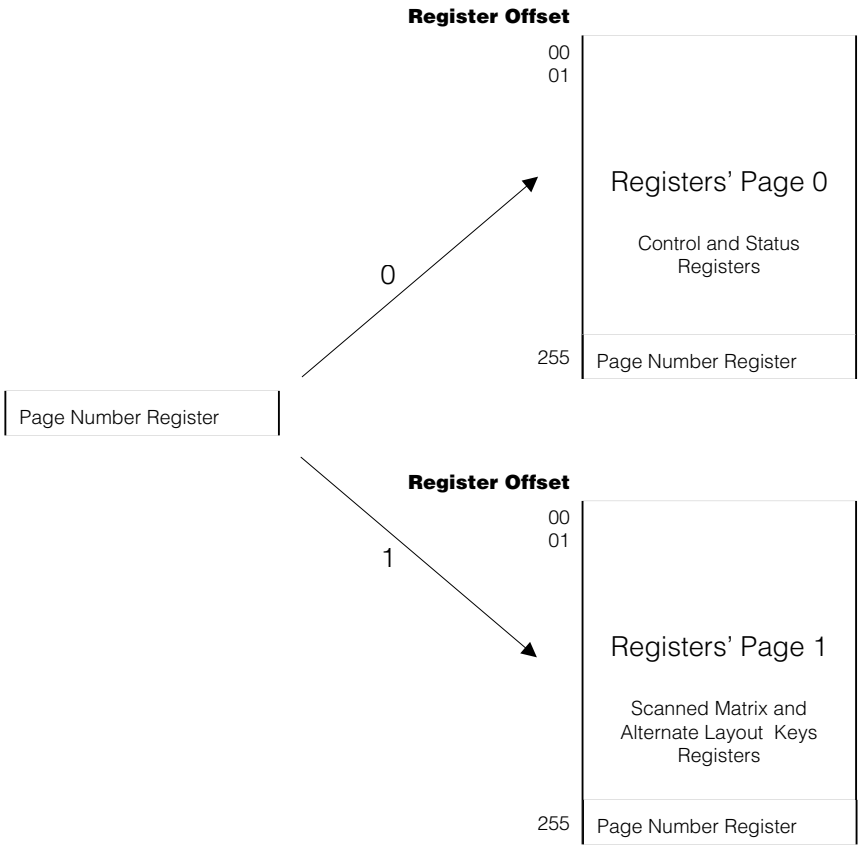


Figure 1: Registers' Page Organization

POWER MANAGEMENT MODES OF OPERATION

The UR8HC007 has three modes of operation relating to its power consumption.

The "Stop" mode is the lowest power consumption mode. In this mode, the crystal is stopped and the IC consumes only 1 µA of leakage current. This is the default mode to which the IC will revert any time an event or a signal condition does not force it to exit this mode.

The "Wait" mode is entered each time it is necessary for a timer to be running in order to perform a system function. Such functions include the LED blinking mode and the use of one of the PWM channels. Typical power consumption in this mode is several hundred µAs.

The "Run" mode is entered briefly, only to process an event or while an interrupt-generating signal condition persists. The controller IC will remain in this mode only for as long a signal prohibits it from reentering a lower power consumption mode or for as long as it is necessary to process a Host-related transaction (a few milliseconds).

POWER MANAGEMENT

The Juno™ UR8HC007 family of controllers implements two power management methods: system-coordinated power management and Self Power Management™ (SPM).

System-coordinated power management primarily determines the tasks performed and the type of reports communicated to the Host. The Juno™ monitors the system states through the PWROK (Power OK), _LID (Lid closed) and _HSUS (Host suspended) lines. In addition to these signal inputs, the UR8HC007 family provides a set of registers, described in the "Registers" chapter of the *Juno™ Technical Reference Manual*, that can be used by the host to control the PM-related performance of the controller through software. According to the status of these lines (or register settings), the Juno™ will enable or disable specific tasks and reports suited to the current power and system management state of the Host.

Self Power Management™ describes a method implemented by the Juno™ controller that, independently of any system intervention, results in the lowest power consumption possible within the given parameters of its operation. Through Self Power Management™, the Juno™ controllers are capable of typically operating at only 1 µA, independent of the state of the system. Self Power Management™ primarily determines the actual power consumption of the controller IC.

The Juno™ implements the Semtech-patented Self Power Management™ method to achieve the minimum power consumption possible, independent of the Host power management state.

Even when the Host is in the active state, the IC can still operate most of the time at only 1 µA, even with external PS/2 devices attached to it.

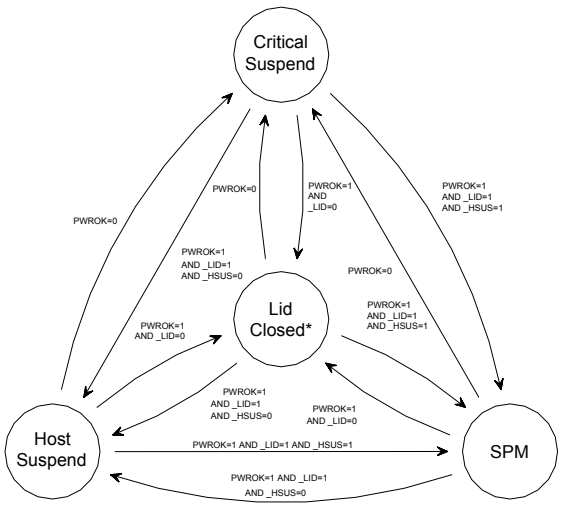


Figure 2: USAR Juno™ State Diagram

ZERO-POWER™ OPERATION OF PS/2 PORTS

The Juno™ implements the Semtech-patented "Message loss-less wake-up™" method to operate all three PS/2 ports. This method enables the controller to interface with devices attached to its PS/2 ports while still operating in the "Stop" mode. Typical power consumption of the PS/2 ports is therefore 1 µA.

If a PS/2 device reports a data packet, the controller will exit the "Stop" mode for as long as it takes to process the device message and relay the information, if necessary, to the Host system. This operation is done transparently to the Host, without any message loss or any response delays from the input devices.

This unique technology allows computers to operate at their minimum power consumption state even with PS/2 devices attached. Systems that employ an internal pointing device, such as a touch pad or a force stick, can benefit the most from this feature, since the pointing device will force the controller to exit its "Stop" mode only when there is data to be reported.

PS/2 PORTS

The UR8HC007-001 provides three PS/2 ports for the hot-plug connection of an external keyboard, an external mouse and an internal mouse.

All of the internal and external devices are active at all times. Data from both the external and internal keyboards and mice are merged and seamlessly presented to the system.

5-Volt Tolerant PS/2 ports

The UR8HC007 controller can be powered by a power supply between 3 and 5 Volts (+/- 10%). Even when the USAR controller is powered by a 3-Volt supply, the three PS/2 ports can directly interface with 5-Volt powered devices — without the need of any external level-shifting circuitry. The Host can enable or disable all the external PS/2 ports simultaneously, in sync with the 5-Volt power plane that powers them. Alternatively, it can select any PS/2 port selectively, through the "HID enable/disable control" register.

PS/2 Mouse Handling

The Juno™ provides a port for the connection of an internal PS/2 mouse. This port supports MouseWheel functionality.

An internal mouse connected to a system's PS/2 port consumes a significant amount of power as it must always be "on." A mouse connected to one of Juno's™ PS/2 ports consumes minimal power because the Juno™ will power down even when the internal mouse is connected and active.

HID MANAGER

The UR8HC007 Human Input Device (HID) Manager is responsible for the configuration and handling of HID devices that are embedded or attached to the controller. The HID Manager has the following responsibilities:
1. Enabling and disabling embedded and attached input devices through the "HID enable/disable control" register
2. Formatting and relaying input device reports to the Host
3. Controlling the configuration and operation of both embedded and attached input devices

The HID Manager consists of the four functional blocks: the PS/2 Port Manager; the Keyboard Manager; the Pointing Device Manager; and the Direct Port Manager.

The function of each Manager is explained in full in the *Juno™ Technical Reference Manual*.

OTHER JUNO™ SERIES MEMBERS

Other members of the Juno™ series of companion ICs offers advanced, ergonomic control of an internal pointing device. Enabled pointing devices include touch pads, touch screens or force sticks. If the application requires an internal pointing device, using a pointing-enabled Juno™ will eliminate the need for a dedicated mouse encoder IC.

KEYBOARD ENCODING

The UR8HC007-001 will encode an 8-row by 16-column keyboard matrix. OEMs may reprogram the matrix by sending commands to the IC from the system. The Juno™ supports English, Japanese and European keyboards. In addition, the IC supports both sticky keys and notebook-style keyboards.

The keyboard below, the Fujitsu FKB7654, is the default keyboard for the UR8HC007-001.

Fujitsu FKB7654

GENERAL PURPOSE INPUT OUTPUT

The Juno™ provides many GPIO pins which enable OEMs to easily differentiate their products.

Four GPIO ports provide interrupt at both falling and rising edge of signals. Two of these pins are dedicated for use as a Lid indicator and Digital power monitor. The other two may be used for a ring indicator, docking signal, soft power button, etc.

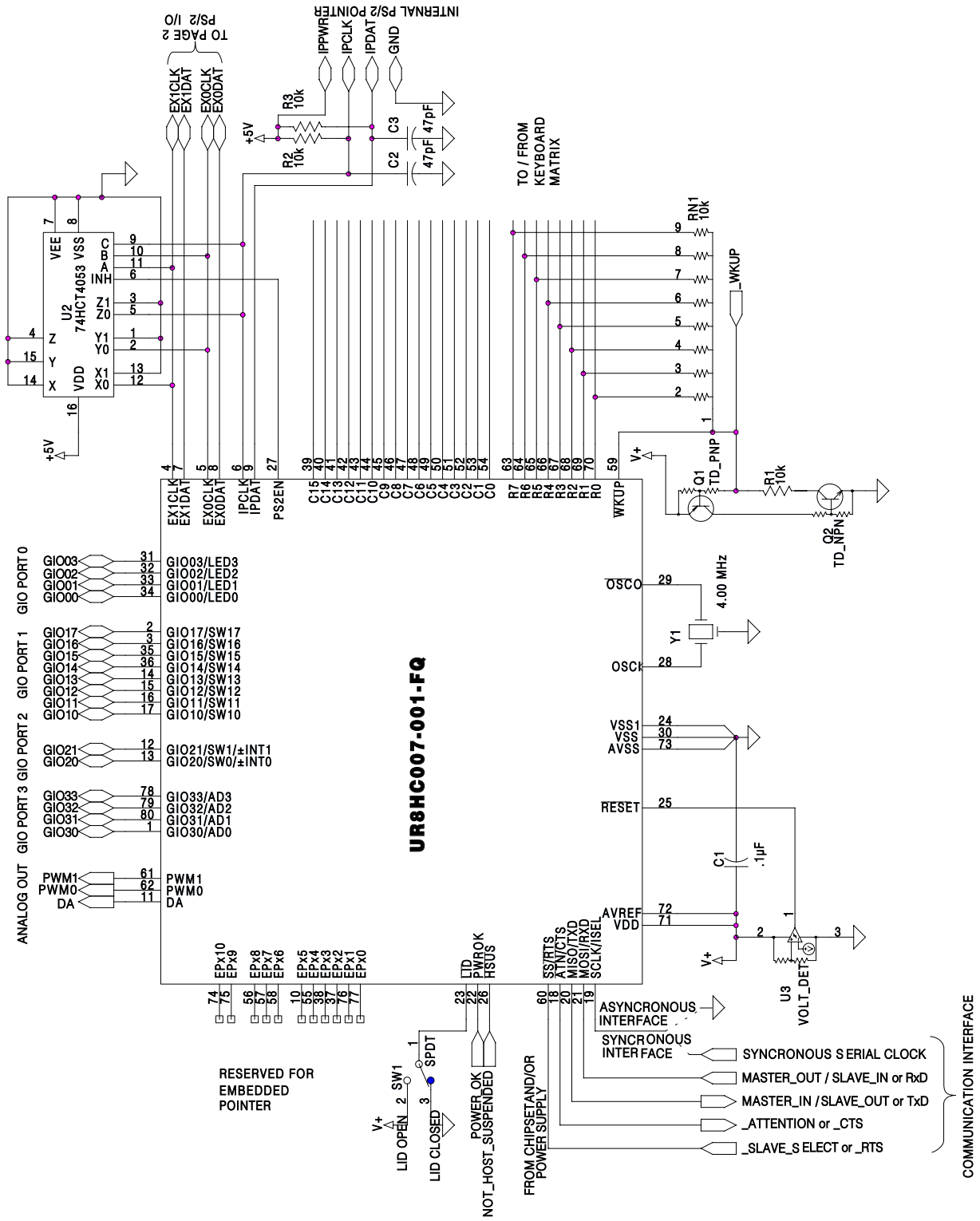
Three GPIO pins provide A/D input and are ideal for battery measurement.

Three GPIO pins provide two Pulse Width Modulation (PWM) channels and one D/A channel and may be used for analog control functions such as LCD brightness/contrast or audio volume control.

Four GPIO pins with high drive ability are set aside as LED drivers or I/O.

Eight GPIO pins can be used as system control outputs or inputs, for example, for switches.

SAMPLE SCHEMATIC FOR THE UR8HC007-001-FQ



JUNO™ ELECTRICAL CHARACTERISTICS

Absolute maximum ratings

(VSS = 0V, Ambient Temperature T_A is in the range T_{LOW} to T_{HIGH})

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 to +7.0	V
Input voltage			
All pins except 2-9	V_{IN}	-0.3 to VDD+0.3	V
Pins 2-9 (PS/2 ports XXXDAT, XXXCLK, GIO16/SW16, GIO17/SW17)	V_{IN}	-0.3 to +5.8	V
Output current			
Total peak for all pins	ΣI_{OH} (Peak)	-80	
	ΣI_{OL} (Peak)	80	mA
Total average for all pins	ΣI_{OH} (Avg)	-40	
	ΣI_{OL} (Avg)	40	mA
All pins except 31-34			
Peak for each pin	I_{OH} (Peak)	-10	
	I_{OL} (Peak)	10	mA
Average for each pin	I_{OH} (Avg)	-5	
	I_{OL} (Avg)	5	mA
Pins 31-34 (GIO00/LED0 - GIO03/LED3)			
Peak for each pin	I_{OH} (Peak)	-10	
	I_{OL} (Peak)	20	mA
Average for each pin	I_{OH} (Avg)	-5	
	I_{OL} (Avg)	15	mA
Temperature range			
Operating Temperature	T_{LOW} to T_{HIGH}	-20 to 85	ºC
Storage Temperature	T_{STG}	-40 to 125	ºC

POWER CONSUMPTION WHILE OPERATING THE PWM CHANNELS

Users should consider the built-in PWM channels for generating slowly changing DC control voltages. Since continuous clocking is necessary for the PWM operations, the only penalty for using the built-in PWM channels is the requirement for the chip to operate at least in the Reduced Power Mode, with typical Current Consumption of 750 µA.

NOTES FOR ELECTRICALS

Note1:

Current Consumption values do not include any loading on the Output pins or Analog Reference Current for the built-in A/D or D/A modules.

Note 2:

Since the built-in A/D module consumes current only during short periods of time (when A/D conversion is actually requested), the Analog Reference Current for the built-in A/D module is not a significant contributor to the overall power consumption.

Note 3:

The Analog Reference Current for the built-in D/A module correlates linearly to the Output Voltage. For D/A output of 0V, the Analog Reference Current is null. For D/A outputs approaching Full Scale (AVREF), the maximum Analog Reference Current is indicated in this Table. This current is a significant contributor to the overall power consumption.

JUNO™ ELECTRICAL CHARACTERISTICS, (CON'T)

Recommended Operating Conditions, Digital Section

(VSS = 0V, Ambient Temperature TA is in the range TLOW to THIGH)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	VDD	2.7	3.0	5.5	V
Input logic high voltage					
All pins except 2-9	VIH	0.8VDD		VDD	V
Pins 2-9 (PS/2 ports xxxDAT, xxxCLK, GIO16/SW16, GIO17/SW17)	VIH	0.8VDD		5.5	V
Input logic low voltage					
All pins except 28	VIL	0		0.2VDD	V
Pin 28 (OSCI)	VIL	0		0.16VDD	V
Input current					
VI = VSS, VDD)	IIL / IIL	-5.0	0	5.0	µA
Input Pull-up Current (pins 56-58 / IP6-IP8, VI = VSS)	IPUP	-120		-10	µA
Output voltage					
IOH = -1.0 mA	VOH	VDD-1.0			V
IOL = 1.6 mA	VOL			0.4	V
Current Consumption (see note 1 below)					
Full Speed Mode (Fosc=4MHz)	IDD		3.5	7.0	mA
Reduced Power Mode (Fosc=4MHz)	IDD		750		µA
Stop Mode (Interrupts active, Fosc=0)	IDD		.1	1.0 (TA = 25ºC) 10(TA = 85ºC)	µA

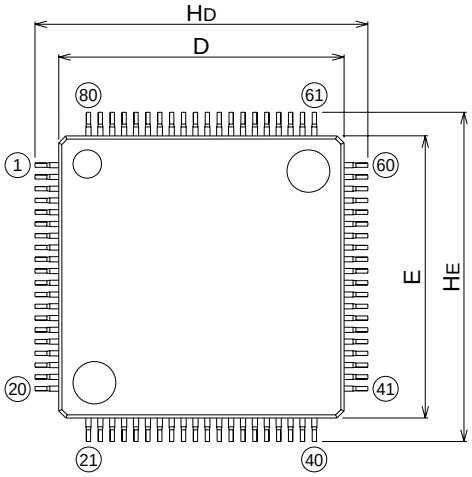
Recommended operating conditions, analog section

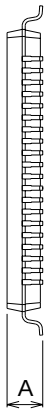
(VSS = 0V, Ambient Temperature TA is in the range TLOW to THIGH)

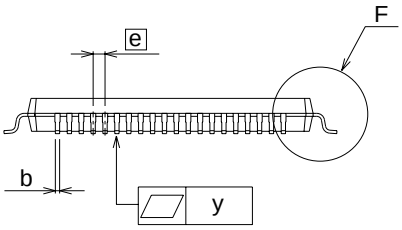
Parameter	Symbol	Min	Typ	Max	Unit
Analog Signal Ground	AVSS		0		V
Analog Reference Voltage	AVREF	2.7	VDD	VDD	V
A/D Resolution -				10	Bits
A/D Absolute Accuracy				± 4	LSb
A/D Analog Input Voltage Range	VIA	AVSS		AVREF	V
A/D Analog Input Current	IIA			5.0	µA
Analog Reference Current (see note 2) (A/D is active)	IAVREF			200	µA
D/A Resolution -				8	Bits
D/A Absolute Accuracy -				2.5	%
D/A Output Impedance	RO	1	2.5	4.0	KOhms
Analog Reference Current (see note 3) (D/A is active, Output = Full Scale)	IAVREF			3.2	mA

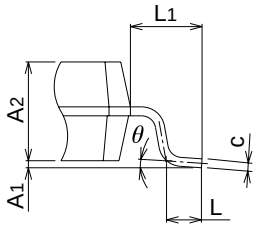
Note 1: please see left
Note 2: please see left
Note 3: please see left

MECHANICALS FOR THE UR8HC007 LQFP PACKAGE

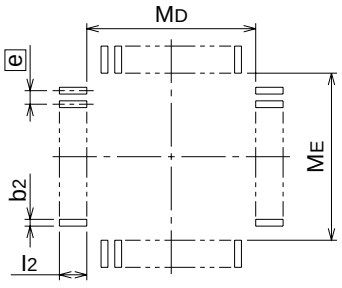








Detail F



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A_1	0	0.1	0.2
A_2	–	1.4	–
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	11.9	12.0	12.1
E	11.9	12.0	12.1
e	–	0.5	–
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
L	0.3	0.5	0.7
L_1	–	1.0	–
y	–	–	0.1
θ	0°	–	10°
b_2	–	0.225	–
l_2	1.0	–	–
M_D	–	12.4	–
M_E	–	12.4	–

BILL OF MATERIALS FOR THE UR8HC007-001-FQ

Quantity	Manufacturer	Part#	Description
1	Generic	C1296-104-X50	.1uF Ceramic Chip Cap, Z5U, SMT, 1206
2	Generic	C1206-470-N50	47 pF Ceramic Chip Cap, NPO orX7R, SMT, Size:1206
1	Harris	CD74HCT4053M	SMT Triple 2-ch Ana Mult/Dem
3	Generic	R1206-103-TF-5	10K Resistor, 5% Thick Film, SMT, 1206
1	CTS	745-101-R103CT-ND	10K, 8 resistors, bussed, 10 pins, SMT
1	AVX	PBRC-4.00BR	4.00MHz Ceramic Resonator w/Caps, SMT
2	ALCO	ADE-03	Switch, 3 Position Dip, THD

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