TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74HC279AP, TC74HC279AF

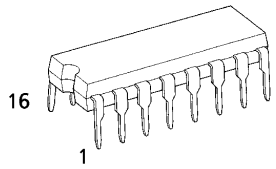
QUAD $\overline{S}-\overline{R}$ LATCH

The TC74HC279A is a high speed CMOS QUAD S - R LATCH fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
Each latch has an independent Q output and Set and Reset inputs. $\overline{S}$ and $\overline{R}$ are active low. When $\overline{S}$ input is low, the Q output goes high and when $\overline{R}$ input is low, the Q output goes low. When both $\overline{S}$ and $\overline{R}$ are low, $\overline{S}$ takes precedence resulting Q=low. When both of $\overline{S}$ and $\overline{R}$ are held high, Q output doesn't change.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

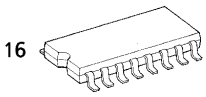
FEATURES :

- High Speed····· t_{pd} = 12ns(typ.) at V_{CC} = 5V
- Low Power Dissipation····· I_{CC} = 2μA(Max.) at Ta = 25°C
- High Noise Immunity····· $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)

- Symmetrical Output Impedance··· $|I_{OH}| = I_{OL}$ = 4mA(Min.)
- Balanced Propagation Delays····· $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range···· V_{CC} (opr.) = 2V~6V
- Pin and Function Compatible with 74LS279

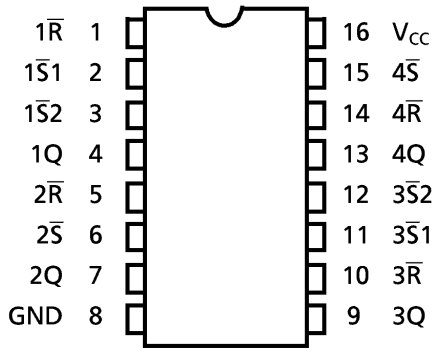


P (DIP16-P-300-2.54A)
Weight : 1.00g (Typ.)



F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)

PIN ASSIGNMENT



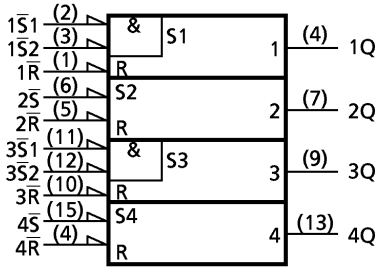
(TOP VIEW)

TRUTH TABLE

INPUTS		OUTPUTS
S #	$\overline{R}$	Q
H	H	Qn
L	H	H
H	L	L
L	L	H

NOTE :
Qn −− The level of Q before the indicated input condition were established.
# −− For latches with doubles $\overline{S}$ input.
H = Both $\overline{S}$ input high
L = One of both inputs low

IEC LOGIC SYMBOL



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ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7	V
DC Input Voltage	V_{IN}	−0.5~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	−65~150	°C

*500mW in the range of Ta= −40°C~65°C. From Ta=65°C to 85 °C a derating factor of −10mW/ °C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2~6	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	t_r, t_f	0~ 1000 (V_{CC} = 2.0V) 0~ 500 (V_{CC} = 4.5V) 0~ 400 (V_{CC} = 6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
High - Level Input Voltage	V_{IH}			2.0 4.5 6.0	1.50 3.15 4.20	− − −	− − −	1.50 3.15 4.20	− − −	V
Low - Level Input Voltage	V_{IL}			2.0 4.5 6.0	− − −	− − −	0.50 1.35 1.80	− − −	0.50 1.35 1.80	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	− − −	1.9 4.4 5.9	− − −	V
			I_{OH} = −4 mA I_{OH} = −5.2mA	4.5 6.0	4.18 5.68	4.31 5.80	− −	4.13 5.63	− −	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20μA	2.0 4.5 6.0	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL} = 4 mA I_{OL} = 5.2mA	4.5 6.0	− −	0.17 0.18	0.26 0.26	− −	0.33 0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	2.0	−	20.0	

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AC ELECTRICAL CHARACTERISTICS (C_L = 15pF, V_{CC} = 5V, Ta = 25°C, Input $t_r = t_f$ = 6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		—	4	8	ns
Propagation Delay Time ($\overline{S}1$, $\overline{S}2-Q$)	t_{pLH} t_{pHL}		—	12	22	
Propagation Delay Time ($\overline{S}-Q$)	t_{pLH} t_{pHL}		—	9	17	
Propagation Delay Time ($\overline{R}-Q$)	t_{pLH} t_{pHL}		—	11	20	

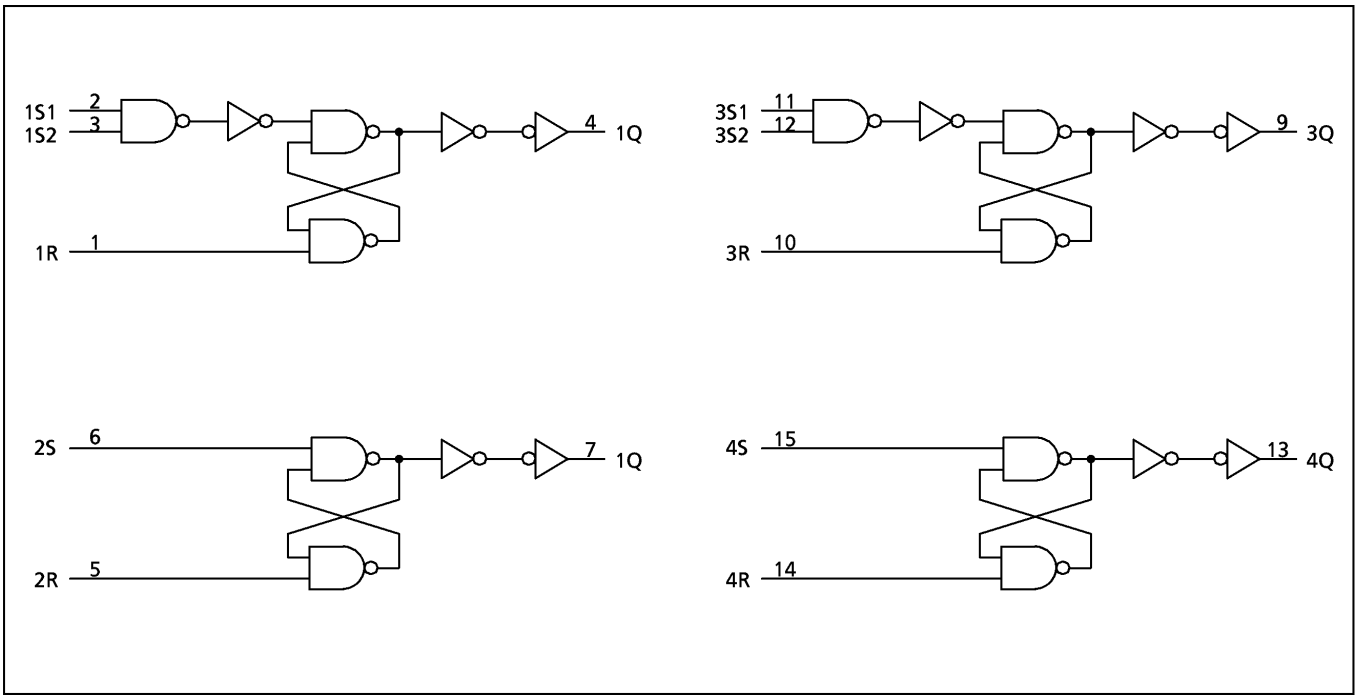
AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0 4.5 6.0	— — —	30 8 7	75 15 13	— — —	95 19 16	ns
Propagation Delay Time ($\overline{S}1$, $\overline{S}2-Q$)	t_{pLH} t_{pHL}		2.0 4.5 6.0	— — —	45 15 13	130 26 22	— — —	165 33 28	
Propagation Delay Time ($\overline{S}-Q$)	t_{pLH} t_{pHL}		2.0 4.5 6.0	— — —	38 12 10	100 20 17	— — —	125 25 21	
Propagation Delay Time ($\overline{R}-Q$)	t_{pLH} t_{pHL}		2.0 4.5 6.0	— — —	42 14 12	120 24 20	— — —	150 30 26	
Input Capacitance	C_{IN}			—	5	10	—	10	pF
Power Dissipation Capacitance	C_{PD} (1)			—	18	—	—	—	

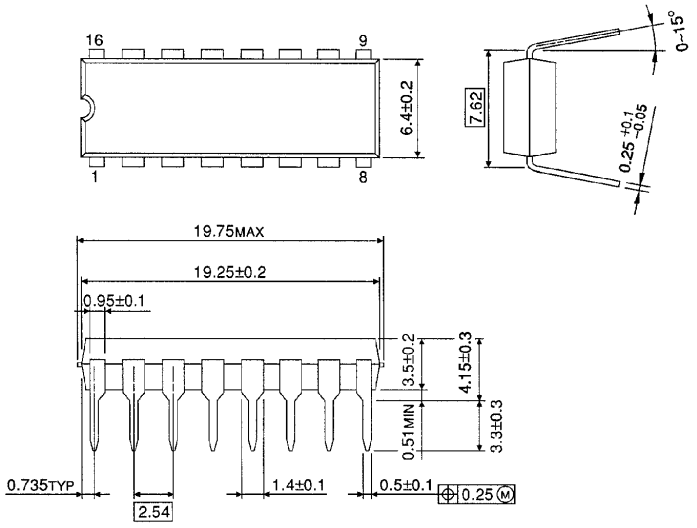
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 4 \text{ (per circuit)}$$

SYSTEM DIAGRAM

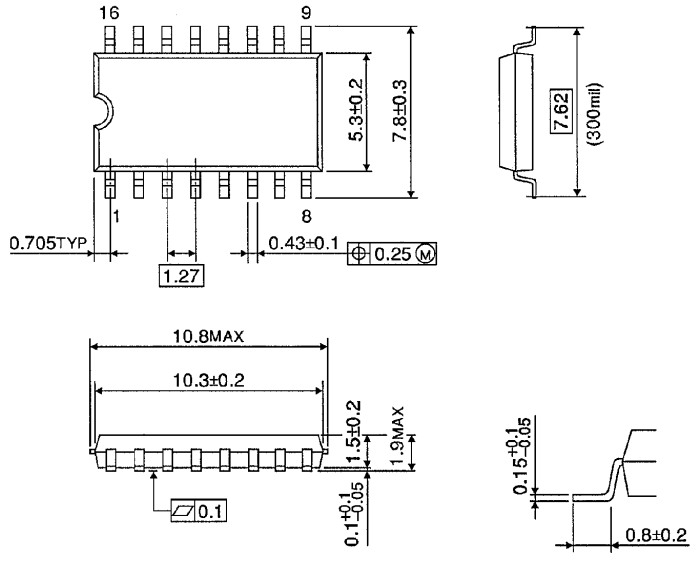


DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A) Unit in mm



Weight : 1.00g (Typ.)

SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27) Unit in mm



Weight : 0.18g (Typ.)