DATA SHEET

TDA8754
Triple 8-bit video ADC up to 270 Msps

Preliminary specification
Supersedes data of 2003 Jul 16

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Philips
Semiconductors

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CONTENTS

1 FEATURES

- 3.3 V power supply
- Triple 8-bit ADC
- Analog sampling rate from 12 up to 270 Msps
- Maximum data rate:
  - Single port mode: 140 MHz
  - Dual port mode: 270 MHz
  - 3.3 V LV-TTL outputs.
- PLL control via I^{2}C-bus:
  - Low PLL drift with temperature (2 phase steps maximum)
  - PLL generates the ADC sampling clock which can be locked on the line frequency from 15 to 150 kHz
  - Integrated PLL divider
  - Programmable phase clock adjustment cells.
- Three clamp circuits for programming a clamp code from −24 to +136 by steps of 1 LSB (mid-scale clamping for YUV signal)
- Internal generation of clamp signal
- Three independent blanking functions
- Input:
  - 410 MHz analog bandwidth
  - Two independent analog inputs selectable via I^{2}C-bus
  - Analog input from 0.5 to 1 V (p-p) to produce a full-scale ADC input of 1 V (p-p)
  - Three controllable amplifiers: gain control via I^{2}C-bus to produce full-scale peak-to-peak output with a half LSB resolution.
- Synchronisation:
  - Frame and field detection for interlaced video signal
  - Parasite synchronization pulse detection and suppression
  - Sync processing for composite sync, 3-level sync and sync-on-green signals
  - Polarity and activity detection.
- IC control via I^{2}C-bus serial interface
- Power-down mode.

2 APPLICATIONS

- RGB/YUV high-speed digitizing
- LCD panels drive
- LCD projection system
- New TV concept.

3 GENERAL DESCRIPTION

The TDA8754 is a complete triple 8-bit ADC with an integrated PLL running up to 270 Msps and analog preprocessing functions (clamp and PGA) optimized for capturing RGB/YUV graphic signals.

The PLL generates a pixel clock from inputs HSYNC and COAST.

The TDA8754 offers full sync processing for sync-on-green applications. A clamp signal may be generated internally or provided externally.

The clamp levels, gains and other settings are controlled via the I^{2}C-bus interface.

This IC supports display resolutions up to QXGA (2048 × 1536) at 85 Hz.

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		3.0	3.3	3.6	V
V_{CCD}	digital supply voltage		3.0	3.3	3.6	V
V_{CCO}	output supply voltage		3.0	3.3	3.6	V
f_{PLL}	analog PLL frequency		12	–	270	MHz
ENOB	effective number of bits	f_{clk} = 270 MHz; f_i = 10 MHz	–	7.6	–	bits
INL	integral non-linearity	f_{clk} = 270 MHz; f_i = 10 MHz	–	±0.6	±1.3	LSB
DNL	differential non-linearity	f_{clk} = 270 MHz; f_i = 10 MHz	–	±0.25	±0.6	LSB
P_{tot}	power dissipation		–	1	1.3	W

5 ORDERING INFORMATION

TYPE NUMBER	PACKAGE			SAMPLING FREQUENCY
	NAME	DESCRIPTION	VERSION	
TDA8754HL/11	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1	110 MHz
TDA8754HL/14				140 MHz
TDA8754HL/17				170 MHz
TDA8754HL/21				210 MHz
TDA8754HL/25				250 MHz
TDA8754HL/27				270 MHz
TDA8754EL/11	LBGA208[1]	plastic low profile ball grid array package; 208 balls; body 17 × 17 × 1.05 mm	SOT774-1	110 MHz
TDA8754EL/14				140 MHz
TDA8754EL/17				170 MHz
TDA8754EL/21				210 MHz
TDA8754EL/25				250 MHz
TDA8754EL/27				270 MHz

Note

1. Values are not yet guarantee.

6 BLOCK DIAGRAM

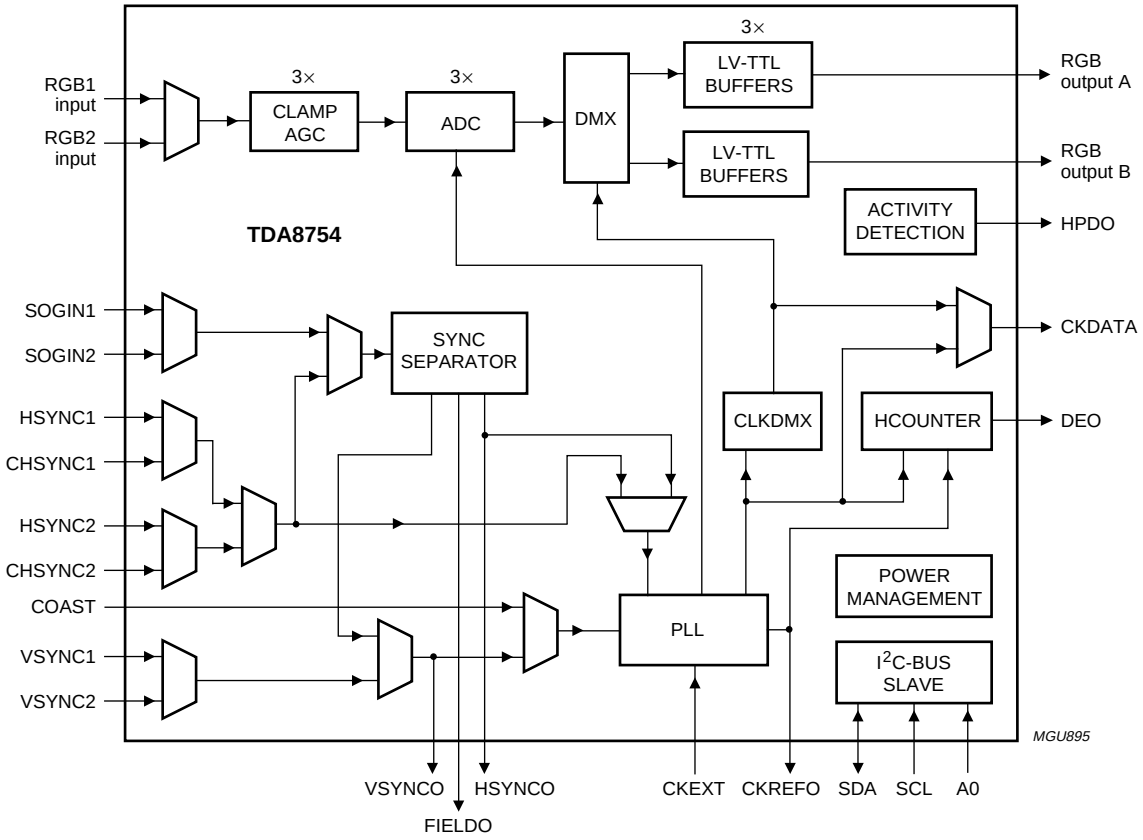


Fig.1 Block diagram.

7 PINNING

7.1 LQFP144 package

SYMBOL	PIN	DESCRIPTION
GNDD(TTL)	1	TTL input digital ground
$V_{CCD(TTL)}$	2	TTL input digital supply voltage
HSYNC2	3	horizontal synchronization pulse input 2
CHSYNC2	4	composite horizontal synchronization pulse input 2
$V_{CCA(PLL)}$	5	PLL analog supply voltage
HSYNC1	6	horizontal synchronization pulse input 1
CHSYNC1	7	composite horizontal synchronization pulse input 1
GNDA(PLL)	8	PLL analog ground
CZ	9	PLL filter input
GNDA(CPO)	10	CPO analog ground
CP	11	PLL filter input
PMO	12	phase measurement output (test)
GNDA(SUB)	13	SUB analog ground
CAPSOGIN1	14	decoupling SOG input 1
CAPSOGO	15	decoupling SOG output
CAPSOGIN2	16	decoupling SOG input 2
GNDA(SOG)	17	SOG analog ground
SOGIN1	18	sync-on-green input 1
$V_{CCA(SOG)}$	19	SOG analog supply voltage
SOGIN2	20	sync-on-green input 2
$V_{CCA(R)}$	21	red channel analog supply voltage
RIN1	22	red channel analog input 1
GNDA(R1)	23	red channel 1 analog ground
RIN2	24	red channel analog input 2
GNDA(R2)	25	red channel 2 analog ground
DEC	26	main regulator decoupling input
RBOT	27	red channel ladder decoupling input
RCLPC	28	red channel clamp capacitor input
$V_{CCA(G)}$	29	green channel analog supply voltage
GIN1	30	green channel analog input 1
GNDA(G1)	31	green channel 1 analog ground
GIN2	32	green channel analog input 2
GNDA(G2)	33	green channel 2 analog ground
GBOT	34	green channel ladder decoupling input
GCLPC	35	green channel clamp capacitor input
$V_{CCA(B)}$	36	blue channel analog supply voltage
BIN1	37	blue channel analog input 1
GNDA(B1)	38	blue channel 1 analog ground

SYMBOL	PIN	DESCRIPTION
BIN2	39	blue channel analog input 2
GNDA(B2)	40	blue channel 2 analog ground
BBOT	41	blue channel ladder decoupling input
BCLPC	42	blue channel clamp capacitor input
AGCO	43	AGC output
GNDD(ADC)	44	ADC digital ground
$V_{CCD(ADC)}$	45	ADC digital supply voltage
GNDD(SUB)	46	SUB digital ground
PWD	47	power-down control input
TEST	48	test input; must be connected to ground
BB0	49	blue channel ADC output B bit 0
BB1	50	blue channel ADC output B bit 1
BB2	51	blue channel ADC output B bit 2
BB3	52	blue channel ADC output B bit 3
BB4	53	blue channel ADC output B bit 4
BB5	54	blue channel ADC output B bit 5
BB6	55	blue channel ADC output B bit 6
BB7	56	blue channel ADC output B bit 7
$V_{CCO(BB)}$	57	blue channel B output supply voltage
GNDO(BB)	58	blue channel B output ground
BOR	59	blue channel ADC output bit out of range
BA0	60	blue channel ADC output A bit 0
BA1	61	blue channel ADC output A bit 1
BA2	62	blue channel ADC output A bit 2
BA3	63	blue channel ADC output A bit 3
BA4	64	blue channel ADC output A bit 4
BA5	65	blue channel ADC output A bit 5
BA6	66	blue channel ADC output A bit 6
BA7	67	blue channel ADC output A bit 7
$V_{CCO(BA)}$	68	blue channel A output supply voltage
GNDO(BA)	69	blue channel A output ground
GB0	70	green channel ADC output B bit 0
GB1	71	green channel ADC output B bit 1
GB2	72	green channel ADC output B bit 2
GB3	73	green channel ADC output B bit 3
GB4	74	green channel ADC output B bit 4
GB5	75	green channel ADC output B bit 5
GB6	76	green channel ADC output B bit 6
GB7	77	green channel ADC output B bit 7
$V_{CCO(GB)}$	78	green channel B output supply voltage
GNDO(GB)	79	green channel B output ground

SYMBOL	PIN	DESCRIPTION
GOR	80	green channel ADC output bit out of range
GA0	81	green channel ADC output A bit 0
GA1	82	green channel ADC output A bit 1
GA2	83	green channel ADC output A bit 2
GA3	84	green channel ADC output A bit 3
GA4	85	green channel ADC output A bit 4
GA5	86	green channel ADC output A bit 5
GA6	87	green channel ADC output A bit 6
GA7	88	green channel ADC output A bit 7
$V_{CCO(GA)}$	89	green channel A output supply voltage
GNDO(GA)	90	green channel A output ground
RB0	91	red channel ADC output B bit 0
RB1	92	red channel ADC output B bit 1
RB2	93	red channel ADC output B bit 2
RB3	94	red channel ADC output B bit 3
RB4	95	red channel ADC output B bit 4
RB5	96	red channel ADC output B bit 5
RB6	97	red channel ADC output B bit 6
RB7	98	red channel ADC output B bit 7
$V_{CCO(RB)}$	99	red channel B output supply voltage
GNDO(RB)	100	red channel B output ground
ROR	101	red channel ADC output bit out of range
RA0	102	red channel ADC output A bit 0
RA1	103	red channel ADC output A bit 1
RA2	104	red channel ADC output A bit 2
RA3	105	red channel ADC output A bit 3
RA4	106	red channel ADC output A bit 4
RA5	107	red channel ADC output A bit 5
RA6	108	red channel ADC output A bit 6
RA7	109	red channel ADC output A bit 7
$V_{CCO(RA)}$	110	red channel A output supply voltage
GNDO(RA)	111	red channel A output ground
$V_{CCO(CLK)}$	112	clock output digital supply voltage
CKDATA	113	data clock output
GNDO(CLK)	114	clock output digital ground
GNDD(I2C)	115	I^2C-bus lines digital ground
$V_{CCD(I2C)}$	116	I^2C-bus lines digital supply voltage
A0	117	I^2C-bus address control input
SDA	118	I^2C-bus serial data input and output
SCL	119	I^2C-bus serial clock input
DIS	120	I^2C-bus disable control input

SYMBOL	PIN	DESCRIPTION
TDO	121	scan test output
TCK	122	scan test mode input; must be connected to ground
CLP	123	clamp pulse input
STBYDIV	124	DVI standby output
GNDD(MCF)	125	MCF digital ground
$V_{CCD(MCF)}$	126	MCF digital supply voltage
HSYNCO	127	horizontal synchronization pulse output
DEO	128	data enable output
HPDO	129	hot plug detector output
GNDO(TTL)	130	TTL output digital ground
$V_{CCO(TTL)}$	131	TTL output digital supply voltage
VSYNCO	132	vertical synchronization pulse output
FIELDO	133	field information output
CLPO	134	clamp output
CKREFO	135	reference output clock; re-synchronized horizontal negative pulse
CSYNCO	136	composite synchronization output
ACRX2	137	test pin; should be connected to ground
ACRX1	138	test pin; should be connected to ground
GNDD(SLC)	139	SLC digital ground
$V_{CCD(SLC)}$	140	SLC output digital supply voltage
CKEXT	141	external clock input
COAST	142	PLL coast control input
VSYNC2	143	vertical synchronization pulse input 2
VSYNC1	144	vertical synchronization pulse input 1

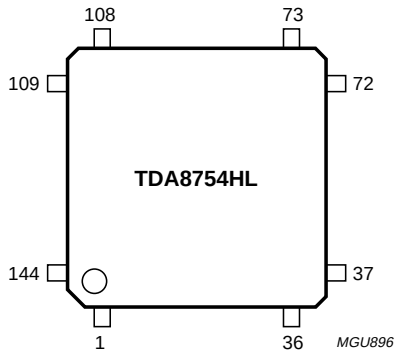


Fig.2 Pin configuration LQFP144 package.

7.2 LBGA208 package

SYMBOL	BALL	DESCRIPTION
SOGIN1	A1	sync-on-green input 1
GNDA(PLL)	A2	PLL analog ground
SOGIN2	A3	sync-on-green input 2
GNDA(PLL)	A4	PLL analog ground
HSYNC2	A5	horizontal synchronization pulse input 2
CHSYNC2	A6	composite horizontal synchronization pulse input 2
COAST	A7	PLL coast control input
CSYNCO	A8	composite synchronization output
FIELDO	A9	field information output
HSYNCO	A10	horizontal synchronization pulse output
SCL	A11	I^2C-bus serial clock input
n.c.	A12	not connected
n.c.	A13	not connected
DIS	A14	I^2C-bus disable control input
A0	A15	I^2C-bus address control input
CKDATA	A16	data clock output
GNDA(PLL)	B1	PLL analog ground
PMO	B2	phase measurement output (test)
GNDA(PLL)	B3	PLL analog ground
GNDA(PLL)	B4	PLL analog ground
$V_{CCA(PLL)}$	B5	PLL analog supply voltage
CLP	B6	clamp pulse input
CKEXT	B7	external clock input
CKREFO	B8	reference output clock; re-synchronized horizontal negative pulse
VSYNCO	B9	vertical synchronization pulse output
DEO	B10	data enable output
SDA	B11	I^2C-bus serial data input and output
n.c.	B12	not connected
n.c.	B13	not connected
n.c.	B14	not connected
GNDO(CLK)	B15	clock output digital ground
$V_{CCO(CLK)}$	B16	clock output digital supply voltage
RIN1	C1	red channel analog input 1
GNDA	C2	analog ground
CAPSOGIN1	C3	decoupling SOG input 1
CAPSOGIN2	C4	decoupling SOG input 2
CAPSOGO	C5	decoupling SOG output
HSYNC1	C6	horizontal synchronization pulse input 1
VSYNC1	C7	vertical synchronization pulse input 1
CLPO	C8	clamp output

SYMBOL	BALL	DESCRIPTION
n.c.	C9	not connected
n.c.	C10	not connected
TCK	C11	scan test mode input
TDO	C12	scan test output
$V_{CCD(I2C)}$	C13	I^2C-bus lines digital supply voltage
n.c.	C14	not connected
n.c.	C15	not connected
n.c.	C16	not connected
GNDA	D1	analog ground
GNDA	D2	analog ground
CZ	D3	PLL filter input
CP	D4	PLL filter input
GNDA(CPO)	D5	CPO analog ground
CHSYNC1	D6	composite horizontal synchronization pulse input 1
VSYNC2	D7	vertical synchronization pulse input 2
HPDO	D8	hot plug detector output
n.c.	D9	not connected
n.c.	D10	not connected
$V_{CCO(TTL)}$	D11	TTL output digital supply voltage
GNDO(TTL)	D12	TTL output digital ground
GNDD(I2C)	D13	I^2C-bus lines digital ground
n.c.	D14	not connected
n.c.	D15	not connected
n.c.	D16	not connected
RIN2	E1	red channel analog input 2
GNDA	E2	analog ground
GNDA	E3	analog ground
GNDA	E4	analog ground
GNDD(TTL)	E7	TTL input digital ground
$V_{CCD(TTL)}$	E8	TTL input digital supply voltage
GNDD(SLC)	E9	SLC digital ground
$V_{CCD(SLC)}$	E10	SLC output digital supply voltage
n.c.	E13	not connected
n.c.	E14	not connected
n.c.	E15	not connected
n.c.	E16	not connected
GNDA	F1	analog ground
GNDA	F2	analog ground
RBOT	F3	red channel ladder decoupling input
GNDA	F4	analog ground
n.c.	F13	not connected

SYMBOL	BALL	DESCRIPTION
n.c.	F14	not connected
n.c.	F15	not connected
n.c.	F16	not connected
GIN1	G1	green channel analog input 1
GNDA	G2	analog ground
DEC	G3	main regulator decoupling input
V_{CCA}	G4	analog supply voltage
V_{CCA}	G5	analog supply voltage
n.c.	G12	not connected
n.c.	G13	not connected
n.c.	G14	not connected
n.c.	G15	not connected
n.c.	G16	not connected
GNDA	H1	analog ground
GNDA	H2	analog ground
GNDA	H3	analog ground
RCLPC	H4	red channel clamp capacitor input
V_{CCA}	H5	analog supply voltage
n.c.	H12	not connected
n.c.	H13	not connected
n.c.	H14	not connected
n.c.	H15	not connected
n.c.	H16	not connected
GIN2	J1	green channel analog input 2
GNDA	J2	analog ground
GBOT	J3	green channel ladder decoupling input
GNDA	J4	analog ground
GCLPC	J5	green channel clamp capacitor input
n.c.	J12	not connected
n.c.	J13	not connected
n.c.	J14	not connected
n.c.	J15	not connected
n.c.	J16	not connected
GNDA	K1	analog ground
GNDA	K2	analog ground
GNDA	K3	analog ground
BCLPC	K4	blue channel clamp capacitor input
V_{CCA}	K5	analog supply voltage
n.c.	K12	not connected
n.c.	K13	not connected
n.c.	K14	not connected

SYMBOL	BALL	DESCRIPTION
n.c.	K15	not connected
n.c.	K16	not connected
BIN1	L1	blue channel analog input 1
GNDA	L2	analog ground
BBOT	L3	blue channel ladder decoupling input
V_{CCA}	L4	analog supply voltage
n.c.	L13	not connected
n.c.	L14	not connected
n.c.	L15	not connected
n.c.	L16	not connected
GNDA	M1	analog ground
GNDA	M2	analog ground
AGCO	M3	AGC output
TEST	M4	test input
V_{CCO}	M7	data output digital supply voltage
V_{CCO}	M8	data output digital supply voltage
GNDO	M9	data output digital ground
GNDO	M10	data output digital ground
n.c.	M13	not connected
n.c.	M14	not connected
n.c.	M15	not connected
n.c.	M16	not connected
BIN2	N1	blue channel analog input 2
GNDA	N2	analog ground
GNDD(ADC)	N3	ADC digital ground
GNDD(ADC)	N4	ADC digital ground
BA2	N5	blue channel ADC output A bit 2
V_{CCO}	N6	data output digital supply voltage
GB4	N7	green channel ADC output B bit 4
GB0	N8	green channel ADC output B bit 0
GA4	N9	green channel ADC output A bit 4
GA0	N10	green channel ADC output A bit 0
GNDO	N11	data output digital ground
PWD	N12	power-down control input
n.c.	N13	not connected
n.c.	N14	not connected
n.c.	N15	not connected
n.c.	N16	not connected
$V_{CCD(ADC)}$	P1	ADC digital supply voltage
$V_{CCD(ADC)}$	P2	ADC digital supply voltage
BB1	P3	blue channel ADC output B bit 1

SYMBOL	BALL	DESCRIPTION
BA6	P4	blue channel ADC output A bit 6
BA3	P5	blue channel ADC output A bit 3
BOR	P6	blue channel ADC output bit out of range
GB5	P7	green channel ADC output B bit 5
GB1	P8	green channel ADC output B bit 1
GA5	P9	green channel ADC output A bit 5
GA1	P10	green channel ADC output A bit 1
RB6	P11	red channel ADC output B bit 6
RB3	P12	red channel ADC output B bit 3
RB0	P13	red channel ADC output B bit 0
RA5	P14	red channel ADC output A bit 5
RA2	P15	red channel ADC output A bit 2
ROR	P16	red channel ADC output bit out of range
BB6	R1	blue channel ADC output B bit 6
BB4	R2	blue channel ADC output B bit 4
BB2	R3	blue channel ADC output B bit 2
BA7	R4	blue channel ADC output A bit 7
BA4	R5	blue channel ADC output A bit 4
BA0	R6	blue channel ADC output A bit 0
GB6	R7	green channel ADC output B bit 6
GB2	R8	green channel ADC output B bit 2
GA6	R9	green channel ADC output A bit 6
GA2	R10	green channel ADC output A bit 2
RB7	R11	red channel ADC output B bit 7
RB4	R12	red channel ADC output B bit 4
RB1	R13	red channel ADC output B bit 1
RA6	R14	red channel ADC output A bit 6
RA3	R15	red channel ADC output A bit 3
RA0	R16	red channel ADC output A bit 0
BB7	T1	blue channel ADC output B bit 7
BB5	T2	blue channel ADC output B bit 5
BB3	T3	blue channel ADC output B bit 3
BB0	T4	blue channel ADC output B bit 0
BA5	T5	blue channel ADC output A bit 5
BA1	T6	blue channel ADC output A bit 1
GB7	T7	green channel ADC output B bit 7
GB3	T8	green channel ADC output B bit 3
GA7	T9	green channel ADC output A bit 7
GA3	T10	green channel ADC output A bit 3
GOR	T11	green channel ADC output bit out of range
RB5	T12	red channel ADC output B bit 5

SYMBOL	BALL	DESCRIPTION
RB2	T13	red channel ADC output B bit 2
RA7	T14	red channel ADC output A bit 7
RA4	T15	red channel ADC output A bit 4
RA1	T16	red channel ADC output A bit 1

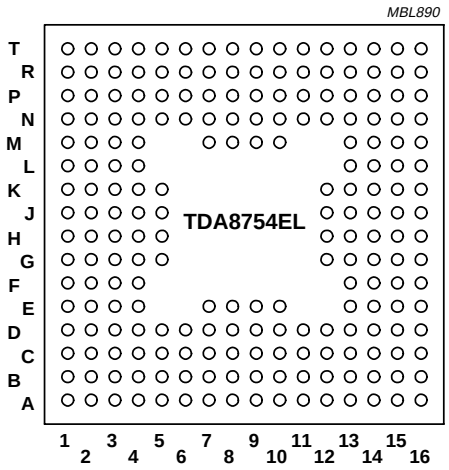


Fig.3 Pin configuration LBGA208 package.

8 FUNCTIONAL DESCRIPTION

This triple high-speed 8-bit ADC is designed to convert RGB/YUV signals coming from an analog source into digital data used by a LCD driver (pixel clock up to 270 MHz with analog source) or projections systems.

8.1 Power management

It is possible to put the TDA8754 in standby mode by setting bit STBY = 1 or to put the whole device in power-down mode by setting pin PWD to HIGH level.

8.1.1 STANDBY MODE

In standby mode, the status of the blocks is as follows:

- Activity detection, I²C-bus slave, sync separator and SOG are still active
- Pixel counter, ADCs, demultiplexers, AGC and clamp cells are inactive
- Output buffers to the RGB block (RGB 0 to 7, CKDATA, DEO, HSYNCO and VSYNCO) are in high-impedance state
- Output HPDO is still active
- Output buffers (ROR, BOR, GOR, CKREFO, CSYNCO, CLPO and FIELDO) are in a LOW-level state.

8.1.2 POWER-DOWN MODE

In power-down mode the status of the blocks is as follows:

- All digital inputs and outputs are in high-impedance state
- All blocks are inactive (I²C-bus, activity detection, ADCs, etc.)
- Analog output is left uncontrolled
- I²C-bus is left in high-impedance state.

8.2 Analog video input

The RGB/YUV video inputs are externally AC coupled and are internally DC polarized. The synchronization signals are also used by the device as input for the internal PLL and the automatic clamp.

8.2.1 ANALOG MULTIPLEXERS

The TDA8754 has two analog inputs (RGB input 1 and RGB input 2) selectable via the I²C-bus.

The sync management can be achieved in several ways:

- Choice between two analog inputs HSYNC and two analog inputs VSYNC
- Choice between two analog inputs CHSYNC
- Choice between two analog inputs SOG.

8.2.2 ACTIVITY DETECTION

When a signal is connected or disconnected on pins HSYNC1(2), CHSYNC1(2), VSYNC1(2) and SOG1(2), then bit HPDO is set to logic 1 and pin HPDO is set to HIGH to advise the user of a change. Bit HPDO is set to logic 0 and pin HPDO is set to LOW when register ACTIVITY2 has been read.

When the synchronization pulse on pin SOG is 3-level, the system will automatically be able to detect that a 3-level sync is present and will force bit 3LEVEL to logic 1. It is possible to disable this function with bit FTRILEVEL.

When an interlaced signal is detected, bit ACFIELD is set to logic 1. When the signal detected is progressive, this bit is set to logic 0. Any change in this bit results into setting bit HPDO = 1 and pin HPDO = HIGH.

A field detection unit is available on pin FIELDO which output is given by the sync separator. The field identity is given by pin FIELDO. This pin gives the field of interlaced signal input.

An automatic polarity detection is also available on pins HSYNC1(2), VSYNC1(2) and CHSYNC1(2). The output on pin HPDO is not affected by the change of polarity of these inputs.

8.2.3 ADC

The three ADCs are designed to convert R, G and B (or Y, U and V) signals at a maximum frequency of 270 Msps. The ADC input range is 1 V (p-p) full-scale and the pipeline delay is 2 ADC clock cycles from the input sampling to the data output.

The reference ladders regulators are integrated.

8.2.4 CLAMP

Three independent parallel clamping circuits are used to clamp the video input signals on programmable black levels. The clamp levels may be set from −24 to +136 LSBs in steps of 1 LSB. They are controlled by three 9-bit I²C-bus registers (OFFSETR, OFFSETG and OFFSETB).

The clamp pulse can be generated internally (based on the PLL clock reference) or can be externally applied on pin CLP.

By setting correctly the I²C-bus bits, it is possible to inhibit the clamp request with the Vsync signal. This inhibition will be effected by forcing logic 0 on the clamp request output. It should be noted that the clamp period can start on the falling edge of the clamp request and that the high level of the clamp request sets the ADC outputs in the blanking mode. This means that by forcing the clamp signal request to logic 0 by using Vsync, a falling edge may happen on the clamp request if this signal was at logic 1 before enforcing the inhibition. To avoid this, the user has to guarantee that the Vsync signal used for the clamp inhibition will not be set during a high level of the clamp request signal.

Remark: If signal Vsync is coming from the external pin VSYNC, this signal may be used to coast the PLL. In order to properly do the coast, the edge of signal Vsync (COAST) must not appear at the same time as the edge of signal Hsync. This condition is similar to the pin CLP inhibition condition.

8.2.5 AGC

Three independent variable gain amplifiers are used to provide, for each channel, a full-scale input signal to the 8-bit ADC. The gain adjustment range is designed in such a way that for an input range varying from 0.5 to 1 V (p-p), the output signal corresponds to the ADC full-scale input of 1 V (p-p).

8.3 HSOSEL, DEO and SCHCKREFO

Bit HSOSEL allows to have a full correlation phase behaviour between outputs CKDATA and HSYNCO when bit HSOSEL = 0 (Hsync from counter). If HSOSEL = 0 and bits PA4 to PA0 of register PHASE are changed to chose the best sampling time, the phase relationship between outputs CKDATA and HSYNCO will stay unchanged. After the video standard is determined, bit HSOSEL must be set to a logic 0 for normal operation mode.

To use the Hsync from the counter the registers HSYNCL, HBACKL, HDISPLMSB and HDISPLLSB should be set properly in order to create the correct HSYNCO and DEO output signals (see Figs.5 and 6), which is depending on video standard. Output signal DEO should be used to determine the first active pixel.

The demultiplexed mode should be used (bit DMX = 1) and the output flow is alternated between port A and port B in case the sampling frequency is over 140 Msps (clock frequency). It is necessary, in order to warrant that the outputs HSYNCO and DEO are always changing on CKDATA output rising edge (see Fig.7), that the values HSYNCL, HBACKL and HDISPL (see Fig.5) are even value. If an odd value is entered the outputs HSYNCO and DEO can change state during falling edge, which is not compliant with the $t_{h(o)}$ and $t_{d(o)}$ specified output timing.

Bit SCHCKREFO is used if in demultiplexed mode one pixel shift is needed in the DEO signal (to move the screen one vertical line). By setting bit SCHCKREFO from a logic 0 to a logic 1 a left move is obtained, also the timing relationship between HSYNCO, DEO and CKDATA stays unchanged. An even number of pixel moves is done by changing the value of HBACKL and HSYNCL. The correct combination of bits HBACKL, HSYNCL and SCHCKREFO places the first active pixel at the beginning of the screen with always the correct phase relationship between outputs DEO, HSYNCO and CKDATA.

Bit HSOSEL should be set to a logic 0 only after the PLL is stable, so only after the video standard has been found and correct PLL parameters have been set in the TDA8754. Bit HSOSEL should be set to a logic 1 to have a stable HSYNCO signal during the video recognition. The video standard can be recognized by using the signals FIELDO, VSYNCO and HSYNCO. The phase relation between CKDATA and HSYNCO (or DEO) is undefined if bit HSOSEL = 1.

8.4 PLL

The ADCs are clocked by either the internal PLL locked to the reference clock (Hsync from input or Hsync from sync separator) or to an external clock connected to pin CKEXT. This selection is performed via the I²C-bus by setting bit CKEXT. To use the external clock, bit CKEXT must be reset to logic 1.

The PLL phase frequency detector can be disconnected during the frame flyback (vertical blanking) or the unavailability of the Ckref signal by using the coast function. The coast signal can be derived from the VSYNC1(2) input, from the Vsync extracted by the sync separator or from the coast input. The coast function can be disabled with bit COE.

The coast signal may be active either HIGH or LOW by setting bit COS.

It is possible to control the phase of the ADC clock via the I^2C-bus with the included digital phase-shift controller. The phase register (5 bits) enables to shift the phase by steps of 11.25 deg.

The PLL also provides a CKDATA clock. This clock is synchronized with the data outputs whatever the output mode is.

It is possible to delay the CKDATA clock with a constant delay (t = 2 ns compared to the outputs) by setting bit CKDD = 1. Moreover, it is possible to invert this output by setting bit CKDATINV = 1.

When the PLL reference signal comes from the separator, the PLL rising edge must be preferably used in order to not use the PLL coast mode. It should be noted that the HSYNCO output of the sync separator is always a mostly low signal, whatever is the polarity of the composite sync input. The VSYNCO output signal of the sync separator is also mostly low signal. It is at a high state during the vertical blanking.

8.5 Sync-on-green

When the SOG input is selected (bit SOGSEL = 1), the SOG charge pump current bits SOGI[1:0] should be programmed in function of the input signal; see Table 1.

A hum remover is implemented in the SOG. It removes completely the hum perturbation on the first or second edge of the horizontal sync pulse for digital video input like VESA, and on the second edge only for analog video input signal like TV or HDTV.

The maximum hum perturbation is 250 mV (p-p) at 60 Hz to have a correct SOG functionality.

Table 1 Charge pump current programming; note 1

BITS SOGI[1:0]	MAXIMUM VALUE ΔTvideo / ΔTline	MAXIMUM VALUE ΔTsync / ΔTline	STANDARD
00	83.5 %	14.8 %	TV standards and non-VESA standards
01	86.0 %	12.6 %	all TV, HDTV and VESA standards
10	90.5 %	8.6 %	HDTV standards or non-VESA standards
11	test mode		

Note

1. Definitions:

   ΔTvideo = total time in 2 frames when video signal is strictly superior to black level.

   ΔTline = total time of 2 frames.

   ΔTsync = total time in 2 frames when the video signal is strictly inferior to black level.

8.6 Programmable coast

When the values of PRECOAST[2:0] = 0 and POSTCOAST[4:0] = 0, the coast pulse equals the Vsync input.

When an interlaced signal is used, the regenerated coast pulse width may vary from one frame to another of one Hsync pulse. In that case, the programmed value of PRECOAST[2:0] needs to be increased by one compared to the expected minimum number of Hsync coast pulses before the vertical sync signal.

8.7 Data enable

This signal qualifies the active data period on the horizontal line. Pin DEO = HIGH during the active display time and LOW during the blank time. The start of this signal can be adjusted with bits HSYNCL[9:0] and HBACKL[9:0]. The length of this signal can be adjusted with bits HDISPL[11:0].

8.8 Sync separator

The sync separator is compatible with TV, HDTV and VESA standards.

If the green video signal has composite sync on it (sync-on-green), the SOG function allows to separate the Chsync and the active video part. The Chsync signal coming from this SOG function is accessible through pin CSYNCO.

It is possible to extract the Hsync and the Vsync signals by using the sync separator from this (C)Hsync signal coming from SOG or coming from the (C)Hsync input.

This function is able to get rid of the additional synchronization pulses in vertical blanking like egalisation or serration pulses.

8.9 3-level

When the synchronization pulse of the input of the SOG is 3-level, the system will be able to detect that a 3-level sync is present and will advise the customer if a change is observed by setting bit HPDO = 1 and pin HPDO = HIGH. It is possible to disable this function with bit FTRILEVEL. When this automatic function is disabled, the manual mode will only influence the separator circuitry.

9 I²C-BUS REGISTER DESCRIPTION

9.1 I²C-bus formats

9.1.1 WRITE 1 REGISTER

Each register is programmed independently by giving its subaddress and its data content.

Table 2 I²C-bus sequence for writing 1 register

SDA LINE	DESCRIPTION
S	master starts with a start condition
Byte 1	master transmits device address (7 bits) plus write command bit ($R/\overline{W}$ = 0)
A	slave generates an acknowledge
Byte 2	master transmits programming mode and subregister address to write to
A	slave generates an acknowledge
Byte 3	master transmits data 1
A	slave generates an acknowledge
P	master generates a stop condition

Table 3 Byte format for writing 1 register

BIT	7	6	5	4	3	2	1	0
Byte 1	device address							$R/\overline{W}$
	A6	A5	A4	A3	A2	A1	A0	–
	1	0	0	1	1	0	X	0
Byte 2	programming mode			register subaddress				
	–	–	MODE	SA4	SA3	SA2	SA1	SA0
	X	X	0	–	–	–	–	–
Byte 3	data 1							
	D7	D6	D5	D4	D3	D2	D1	D0

Table 4 Write format bit description

BIT	SYMBOL	DESCRIPTION
Byte 1		
7 to 1	A[6:0]	**Device address**. The TDA8754 address is 1001 10X. Bit A0 relates with the voltage level on pin A0.
0	R/$\overline{W}$	**Write command bit.** If R/$\overline{W}$ = 0, then write action.
Byte 2		
7 to 6	–	not used
5	MODE	**Mode selection bit.** If MODE = 0, then each register can be written independently.
4 to 0	SA[4:0]	**Register subaddress.** Subaddress of the selected register (from 0 0000 to 1 1111).
Byte 3		
7 to 0	D[7:0]	**Data 1.** This value is written in the selected register.

9.1.2 WRITE ALL REGISTERS

All registers are programmed one after the other, by giving this initial condition (XX11 1111) as the subaddress state; thus, the registers are charged following the predefined sequence of 32 bytes (from subaddress 0 0000 to 1 1111).

Table 5 I^2C-bus sequence for writing all registers

SDA LINE	DESCRIPTION
S	master starts with a start condition
Byte 1	master transmits device address (7 bits) plus write command bit (R/$\overline{W}$ = 0)
A	slave generates an acknowledge
Byte 2	master transmits programming mode and subregister address to start writing to
A	slave generates an acknowledge
Byte 3	master transmits data 1
A	slave generates an acknowledge
:	:
Byte 34	master transmits data 32
A	slave generates an acknowledge
P	master generates a stop condition

Table 6 Byte format for writing all registers

BIT	7	6	5	4	3	2	1	0
Byte 1	device address							R/$\overline{W}$
	A6	A5	A4	A3	A2	A1	A0	–
	1	0	0	1	1	0	X	0
Byte 2	programming mode			register subaddress				
	–	–	MODE	SA4	SA3	SA2	SA1	SA0
	X	X	1	1	1	1	1	1
Byte (2 + n)	data n							
	D7	D6	D5	D4	D3	D2	D1	D0

Table 7 Write format bit description

BIT	SYMBOL	DESCRIPTION
Byte 1		
7 to 1	A[6:0]	**Device address**. The TDA8754 address is 1001 10X. Bit A0 relates with the voltage level on pin A0.
0	R/$\overline{W}$	**Write command bit.** If R/$\overline{W}$ = 0, then write action.
Byte 2		
7 to 6	–	not used
5	MODE	**Mode selection bit.** If MODE = 1, then all registers can be written one after the other.
4 to 0	SA[4:0]	**Register subaddress.** Initial condition is XX11 1111.
Byte (2 + n)		
7 to 0	D[7:0]	**Data n.** This value is written in register 00h + n.

9.1.3 READ REGISTER

Table 8 I^2C-bus sequence for reading one register

SDA LINE	DESCRIPTION
S	master starts with a start condition
Byte 1	master transmits device address (7 bits) plus write command bit (R/$\overline{W}$ = 0)
A	slave generates an acknowledge
Byte 2	master transmits programming mode and subregister address to read from
A	slave generates an acknowledge
Byte 3	master transmits read register subaddress
A	slave generates an acknowledge
Byte 4	master transmits device address (7 bits) plus read command bit (R/$\overline{W}$ = 1)
A	slave generates an acknowledge
Byte 5	slave transmits data to master
$\overline{A}$	master generates an not-acknowledge after reading the data byte
P	master generates a stop condition

Table 9 Byte format for reading register

BIT	7	6	5	4	3	2	1	0
Byte 1	device address							R/$\overline{W}$
	A6	A5	A4	A3	A2	A1	A0	–
	1	0	0	1	1	0	X	0
Byte 2	programming mode			register subaddress				
	–	–	MODE	SA4	SA3	SA2	SA1	SA0
	X	X	0	1	1	1	1	1
Byte 3	read subaddress							
	–	–	–	–	–	–	RA1	RA0
	0	0	0	0	0	0	–	–
Byte 4	device address							R/$\overline{W}$
	A6	A5	A4	A3	A2	A1	A0	–
	1	0	0	1	1	0	X	1
Byte 5	data 1							
	D7	D6	D5	D4	D3	D2	D1	D0

Table 10 Read format bit description

BIT	SYMBOL	DESCRIPTION
Byte 1		
7 to 1	A[6:0]	**Device address**. The TDA8754 address is 1001 10X. Bit A0 relates with the voltage level on pin A0.
0	R/$\overline{W}$	**Write command bit.** If R/$\overline{W}$ = 0, then write action.
Byte 2		
7 to 6	–	not used
5	MODE	**Mode selection bit.** If MODE = 0, then each register can be written independently.
4 to 0	SA[4:0]	**Register subaddress.** Subaddress of the read register (1 1111).
Byte 3		
7 to 0	RA[1:0]	**Read address.** This is the value of the read register to be selected.
Byte 4		
7 to 1	A[6:0]	**Device address**. The TDA8754 address is 1001 10X. Bit A0 relates with the voltage level on pin A0.
0	R/$\overline{W}$	**Read command bit.** If R/$\overline{W}$ = 1, then read action.
Byte 5		
7 to 0	D[7:0]	**Data 1.** The value from read register is sent from the slave to the master.

9.2 I²C-bus registers overview

Table 11 I²C-bus analog write registers

ADDR	NAME	MSB				BIT			LSB	DEFAULT VALUE
		7	6	5	4	3	2	1	0	
00h	OFFSETR	OR7	OR6	OR5	OR4	OR3	OR2	OR1	OR0	0000 0000
01h	COARSER	OR8	CR6	CR5	CR4	CR3	CR2	CR1	CR0	0100 0110
02h	FINER	–	–	–	–	–	FR2	FR1	FR0	XXXX X000
03h	OFFSETG	OG7	OG6	OG5	OG4	OG3	OG2	OG1	OG0	0000 0000
04h	COARSEG	OG8	CG6	CG5	CG4	CG3	CG2	CG1	CG0	0100 0110
05h	FINEG	–	–	–	–	–	FG2	FG1	FG0	XXXX X000
06h	OFFSETB	OB7	OB6	OB5	OB4	OB3	OB2	OB1	OB0	0000 0000
07h	COARSEB	OB8	CB6	CB5	CB4	CB3	CB2	CB1	CB0	0100 0110
08h	FINEB	–	–	–	–	–	FB2	FB1	FB0	XXXX X000
09h	SOG	DO	UP	FTRILEVEL	STRILEVEL	CKREFS	SOGSEL	SOGI1	SOGI0	0000 0001
0Ah	PLLCTRL	IP1	IP0	Z2	Z1	Z0	DR2	DR1	DR0	0101 1100
0Bh	PHASE	PA4	PA3	PA2	PA1	PA0	VCO2	VCO1	VCO0	0000 0101
0Ch	DIVMSB	CKEXT	SCH CKREFO	EPSI1	EPSI0	DI11	DI10	DI9	DI8	0000 0110
0Dh	DIVLSB	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0	1001 1000
0Eh	HSYNCL	HSYNCL9	HSYNCL8	HSYNCL7	HSYNCL6	HSYNCL5	HSYNCL4	HSYNCL3	HSYNCL2	0010 0100
0Fh	HBACKL	HSYNCL1	HSYNCL0	HBACKL9	HBACKL8	HBACKL7	HBACKL6	HBACKL5	HBACKL4	0000 1111
10h	HDISPLMSB	HBACKL3	HBACKL2	HBACKL1	HBACKL0	HDISPL11	HDISPL10	HDISPL9	HDISPL8	1000 0101
11h	HDISPLLSB	HDISPL7	HDISPL6	HDISPL5	HDISPL4	HDISPL3	HDISPL2	HDISPL1	HDISPL0	0000 0000
12h	COAST	PRE COAST2	PRE COAST1	PRE COAST0	POST COAST4	POST COAST3	POST COAST2	POST COAST1	POST COAST0	0000 0000
13h	HSYNCSEL	–	–	–	–	TESTCNT	BYSEPA	HSSEL	HSS	XXX X0100
14h	VSYNCSEL	–	–	–	TSTCOAST	COE	VSS	COSSEL2	COSSEL1	XXX0 0000
15h	CLAMP	–	HSOSEL	CLPSEL2	CLPSEL1	CLPH	CLPENL	ICLP	CLPT	X010 0000
16h	INVERTER	–	COS	CLPS	CKREFO INV	DEO INVRGB	HSO INVRGB	VSO INVRGB	FIELDO INV	X000 0000
17h	OUTPUT	RGBSEL	TEN	AGCSEL1	AGCSEL0	BLKEN	DMXRGB	ODDARGB	SHIFTRGB	0000 0000
18h	OUTPUTEN1	–	–	–	BOENRGB	AOENRGB	OROEN	TOUTERGB	TOUTSRGB	XXX1 1100

ADDR	NAME	MSB BIT LSB								DEFAULT VALUE
		7	6	5	4	3	2	1	0	
19h	OUTPUTEN2	CKROEN	CSOEN	DEOEN RGB	HSOEN RGB	HPDOEN	VSOEN RGB	CLPOEN	FIELDOEN	1111 1111
1Ah	CLKOUTPUT	–	–	–	CKSEL RGB	DLYCLK RGB	CKDAT INV	OUT OSCILL	CKOEN RGB	XXX0 0001
1Bh	INTOSC	–	–	–	–	–	–	SWITCH OSC	INTOSC OFF	XXXX XX00
1Ch	reserved									
1Dh	reserved									
1Eh	PWRMGT	–	–	–	–	SHCKDMX	SHCKADC	STBY	DVIRGB	XXXX 0000
1Fh	READADDR	–	–	–	–	–	–	ADDR1	ADDR0	XXXX XX00

Table 12 I^2C-bus analog read registers; note 1

ADDR	NAME	MSB BIT LSB								DEFAULT VALUE
		7	6	5	4	3	2	1	0	
1	VERSION	–	–	–	–	VER3	VER2	VER1	VER0	XXXX 0000
2	SIGN	–	–	POLVS2	POLVS1	POLCHS2	POLCHS1	POLHS2	POLHS1	XX00 0000
3	ACTIVITY1	ACVS2	ACVS1	ACSOG2	ACSOG1	ACCHS2	ACCHS1	ACHS2	ACHS1	0000 0000
4	ACTIVITY2	–	ASD	3LEVEL	ACFIELD	HPDO	ACVSSEP	ACRXC1	ACRXC0	X000 0000

Note

1. The read register address is specified with bits ADDR1 and ADDR0 of register READADDR.

9.3 Offset registers (R, G and B)

The offset registers contain a 9-bit value which controls the clamp level for the RGB channels. The 8 LSBs are in the offset registers and the 1 MSB is in the coarse gain control register. The relationship between the programming code and the level of the clamp code is given in Table 15. The default value is: clamp code = 0 and ADC output = 0.

Table 13 Offset registers (00h, 03h, 06h) bit allocation

REGISTER	7	6	5	4	3	2	1	0
OFFSETR (00h)	OR7	OR6	OR5	OR4	OR3	OR2	OR1	OR0
OFFSETG (03h)	OG7	OG6	OG5	OG4	OG3	OG2	OG1	OG0
OFFSETB (06h)	OB7	OB6	OB5	OB4	OB3	OB2	OB1	OB0
Default	0	0	0	0	0	0	0	0

Table 14 Offset registers (00h, 03h, 06h) bit description

BIT	SYMBOL	DESCRIPTION
OFFSETR (address: 00h)		
7 to 0	OR[7:0]	offset R channel; LSB in this register and MSB bit OR8 in register COARSER
OFFSETG (address: 03h)		
7 to 0	OG[7:0]	offset G channel; LSB in this register and MSB bit OG8 in register COARSEG
OFFSETB (address: 06h)		
7 to 0	OB[7:0]	offset B channel; LSB in this register and MSB bit OB8 in register COARSEB

Table 15 Coding for clamp level and ADC output

HEX VALUE	OR8	OR7	OR6	OR5	OR4	OR3	OR2	OR1	OR0	CLAMP CODE (DECIMAL)	ADC OUTPUT (CODE TRANSITION)
	OG8	OG7	OG6	OG5	OG4	OG3	OG2	OG1	OG0		
	OB8	OB7	OB6	OB5	OB4	OB3	OB2	OB1	OB0		
1 E9	1	1	1	1	0	1	0	0	0	–24	–24/–23
1 EA	1	1	1	1	0	1	0	0	1	–23	–23/–22
:										:	:
1 FF	1	1	1	1	1	1	1	1	1	–1	–1/0
0 00	0	0	0	0	0	0	0	0	0	0	0/1
0 01	0	0	0	0	0	0	0	0	1	+1	1/2
:										:	:
0 3F	0	0	0	1	1	1	1	1	1	63	63/64
0 40	0	0	1	0	0	0	0	0	0	64	64/65
:										:	:
0 78	0	0	1	1	1	1	0	0	0	120	120/121
0 79	0	0	1	1	1	1	0	0	1	121	121/122
:										:	:
0 80	0	1	0	0	0	0	0	0	0	128	128/129

HEX VALUE	OR8	OR7	OR6	OR5	OR4	OR3	OR2	OR1	OR0	CLAMP CODE (DECIMAL)	ADC OUTPUT (CODE TRANSITION)
	OG8	OG7	OG6	OG5	OG4	OG3	OG2	OG1	OG0		
	OB8	OB7	OB6	OB5	OB4	OB3	OB2	OB1	OB0		
:										:	:
0 86	0	1	0	0	0	0	1	1	0	134	134/135
0 87	0	1	0	0	0	0	1	1	1	135	135/136

9.4 Coarse registers (R, G and B)

The coarse gain of the AGC is controlled with 7 bits. The code gain can vary from 32 to 95; see Table 18.

Table 16 Coarse gain registers (01h, 04h, 07h) bit allocation

REGISTER	7	6	5	4	3	2	1	0
COARSER (01h)	OR8	CR6	CR5	CR4	CR3	CR2	CR1	CR0
COARSEG (04h)	OG8	CG6	CG5	CG4	CG3	CG2	CG1	CG0
COARSEB (07h)	OB8	CB6	CB5	CB4	CB3	CB2	CB1	CB0
Default	0	1	0	0	0	1	1	0

Table 17 Coarse gain registers (01h, 04h, 07h) bit description

BIT	SYMBOL	DESCRIPTION
COARSER (address: 01h)		
7	OR8	offset R channel; MSB bit of offset value
6 to 0	CR[6:0]	coarse gain of the AGC for R channel
COARSEG (address: 04h)		
7	OG8	offset G channel; MSB bit of offset value
6 to 0	CG[6:0]	coarse gain of the AGC for G channel
COARSEB (address: 07h)		
7	OB8	offset B channel; MSB bit of offset value
6 to 0	CB[6:0]	coarse gain of the AGC for B channel

Table 18 Coarse register

DECIMAL VALUE	CR6	CR5	CR4	CR3	CR2	CR1	CR0	V_i TO BE FULL-SCALE	GAIN ADC
	CG6	CG5	CG4	CG3	CG2	CG1	CG0		
	CB6	CB5	CB4	CB3	CB2	CB1	CB0		
32	0	1	0	0	0	0	0	1.000	1.000
33	0	1	0	0	0	0	1	0.992	1.008
:								:	:
63	0	1	1	1	1	1	1	0.753	1.328
64	1	0	0	0	0	0	0	0.746	1.340
65	1	0	0	0	0	0	1	0.738	1.355
:								:	:

DECIMAL VALUE	CR6	CR5	CR4	CR3	CR2	CR1	CR0	V_i TO BE FULL-SCALE	GAIN ADC
	CG6	CG5	CG4	CG3	CG2	CG1	CG0		
	CB6	CB5	CB4	CB3	CB2	CB1	CB0		
69	1	0	0	0	1	0	1	0.706	1.416
70	1	0	0	0	1	1	0	0.698	1.432
:								:	:
95	1	0	1	1	1	1	1	0.500	2.000

9.5 Fine registers (R, G and B)

Fine gain control is done with 3 bits allowing 8 intermediate values between two values of consecutive coarse gain.

Table 19 Fine gain registers (02h, 05h, 08h) bit allocation

REGISTER	7	6	5	4	3	2	1	0
FINER (02h)	–	–	–	–	–	FR2	FR1	FR0
FINEG (05h)	–	–	–	–	–	FG2	FG1	FG0
FINEB (08h)	–	–	–	–	–	FB2	FB1	FB0
Default	X	X	X	X	X	0	0	0

Table 20 Fine gain registers (02h, 05h, 08h) bit description

BIT	SYMBOL	DESCRIPTION
FINER (address: 02h)		
7 to 3	–	not used
2 to 0	FR[2:0]	fine gain of the AGC for R channel
FINEG (address: 05h)		
7 to 3	–	not used
2 to 0	FG[2:0]	fine gain of the AGC for G channel
FINEB (address: 08h)		
7 to 3	–	not used
2 to 0	FB[2:0]	fine gain of the AGC for B channel

Table 21 Fine gain control bits (example for coarse register value 32)

DECIMAL VALUE	FR2	FR1	FR0	FINE STEPS OF GAIN ADC
	FG2	FG1	FG0	
	FB2	FB1	FB0	
0	0	0	0	1.000
1	0	0	1	1.001
2	0	1	0	1.002
3	0	1	1	1.003
4	0	0	0	1.004

DECIMAL VALUE	FR2	FR1	FR0	FINE STEPS OF GAIN ADC
	FG2	FG1	FG0	
	FB2	FB1	FB0	
5	0	0	1	1.005
6	0	1	0	1.006
7	1	1	1	1.007

9.6 SOG register

Table 22 SOG (09h) bit allocation

BIT	7	6	5	4	3	2	1	0
Symbol	DO	UP	FTRILEVEL	STRILEVEL	CKREFS	SOGSEL	SOGI1	SOGI0
Default	0	0	0	0	0	0	0	1

Table 23 SOG (09h) bit description

BIT	SYMBOL	DESCRIPTION
7	DO	test bit for forcing charge pump current down 0 = default value 1 = forcing down
6	UP	test bit for forcing charge pump current up 0 = default value 1 = forcing up
5	FTRILEVEL	defines the 3-level function mode 0 = automatic 3-level 1 = level selection with bit STRILEVEL
4	STRILEVEL	forces the state of 3-level function 0 = not 3-level mode 1 = 3-level mode
3	CKREFS	enables the PLL Ckref signal to be selected 0 = same as input 1 = input inverted
2	SOGSEL	enables the reference PLL between HSYNC input and SOG input to be selected 0 = HSYNC input 1 = SOG input
1 to 0	SOGI[1:0]	defines the SOG charge pump current; values are given in % of sync pulse/line length 00 = 14,8 % maximum (TV standards) and non-VESA standards 01 = 12,6 % maximum (all standards) 10 = 8.6 % maximum (HDTV standards) and non-VESA standards 11 = 0 test mode

9.7 PLL control

Table 24 PLLCTRL (0Ah) bit allocation

BIT	7	6	5	4	3	2	1	0
Symbol	IP1	IP0	Z2	Z1	Z0	DR2	DR1	DR0
Default	0	1	0	1	1	1	0	0

Table 25 PLLCTRL (0Ah) bit description

BIT	SYMBOL	DESCRIPTION
7 to 6	IP[1:0]	charge pump current value to increase the bandwidth of the PLL 00 = 800 μA 01 = 1200 μA 10 = 1600 μA 11 = 2000 μA
5 to 3	Z[2:0]	internal resistance value for the VCO filter to be selected 000 = not used 001 = 1.56 kΩ 010 = 1.25 kΩ 011 = 1.00 kΩ 100 = 0.80 kΩ 101 = 0.64 kΩ 110 = 0.51 kΩ 111 = 0.41 kΩ
3 to 0	DR[2:0]	PLL temperature phase drift to be compensated. The optimized value of this register is XX. These bits add a delay on the clock reference input of the PLL as a function of the temperature of the die. 000 = +1.75 step phase 001 = –0.3 step phase 010 = –4.3 step phase 011 = –6.2 step phase 100 = –2.2 step phase

9.8 Phase register

Table 26 PHASE (0Bh) bit allocation

BIT	7	6	5	4	3	2	1	0
Symbol	PA4	PA3	PA2	PA1	PA0	VCO2	VCO1	VCO0
Default	0	0	0	0	0	1	0	1

Table 27 PHASE (0Bh) bit description

BIT	SYMBOL	DESCRIPTION
7 to 4	PA[4:0]	phase shift value for the clock pixel. See Table 28.
3 to 0	VCO[2:0]	VCO gain control. See Table 29.

Table 28 Phase registers bits

PA4	PA3	PA2	PA1	PA0	PHASE SHIFT (deg)
0	0	0	0	0	0
0	0	0	0	1	11.25
:	:	:	:	:	:
1	1	1	1	0	337.50
1	1	1	1	1	348.75

Table 29 VCO gain control

VCO2	VCO1	VCO0	VCO GAIN (MHz/V)	PIXEL CLOCK FREQUENCY (MHz)
0	0	0	13	12 to 22
0	0	1	30	22 to 45
0	1	0	60	45 to 62
0	1	1	60	62 to 85
1	0	0	105	85 to 120
1	0	1	105	120 to 176
1	1	0	135	176 to 270
1	1	1	no oscillation	–

9.9 PLL divider registers

Table 30 DIVMSB (0Ch) bit allocation

BIT	7	6	5	4	3	2	1	0
Symbol	CKEXT	SCH CKREFO	EPSI1	EPSI0	DI11	DI10	DI9	DI8
Default	0	0	0	0	0	1	1	0

Table 31 DIVMSB (0Ch) bit description

BIT	SYMBOL	DESCRIPTION
7	CKEXT	external clock selection 0 = internal PLL 1 = external clock
6	SCH CKREFO	shift of pixel counter reference (Ckref) with one clock pixel period 0 = not active 1 = active
5 to 4	EPSI[1:0]	enables the resynchronization edge of CKREFO to be selected; they are test bits 00 = default value for proper operation : 11 = tbf
3 to 0	DI[11:8]	PLL divider ratio. These are the 4 MSBs of the 12-bit value. See Table 34.

Table 32 DIVLSB (0Dh) bit allocation

BIT	7	6	5	4	3	2	1	0
Symbol	DI7	DI6	DI5	DI4	DI3	DI2	DI1	D0
Default	1	0	0	1	1	0	0	0

Table 33 DIVLSB (0Dh) bit description

BIT	SYMBOL	DESCRIPTION
7 to 0	DI[7:0]	PLL divider ratio. These are the 8 LSBs of the 12-bit value. See Table 34.

Table 34 PLL divider ratio

DI11	DI10	DI9	DI8	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0	PLL DIVIDER RATIO
0	0	0	0	0	1	1	0	0	1	0	0	100
:	:	:	:	:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	1	1	1	1	4095

9.10 Horizontal sync registers

Remark: The sum of HSYNCL[9:0] + HBACKL[9:0] + HDISPL[9:0] + 16 needs to be smaller than the PLL divider.

Table 35 HSYNCL, HBACKL and HDISPL bits allocation

BIT	7	6	5	4	3	2	1	0
Register address 0Eh								
Symbol	HSYNCL9	HSYNCL8	HSYNCL7	HSYNCL6	HSYNCL5	HSYNCL4	HSYNCL3	HSYNCL2
Default	0	0	1	0	0	1	0	0
Register address 0Fh								
Symbol	HSYNCL1	HSYNCL0	HBACKL9	HBACKL8	HBACKL7	HBACKL6	HBACKL5	HBACKL4
Default	0	0	0	0	1	1	1	1
Register address 10h								
Symbol	HBACKL3	HBACKL2	HBACKL1	HBACKL0	HDISPL11	HDISPL10	HDISPL9	HDISPL8
Default	1	0	0	0	0	1	0	1
Register address 11h								
Symbol	HDISPL7	HDISPL6	HDISPL5	HDISPL4	HDISPL3	HDISPL2	HDISPL1	HDISPL0
Default	0	0	0	0	0	0	0	0

Table 36 Sync registers (0Eh to 11h) bit description

BIT	SYMBOL	DESCRIPTION
–	HSYNCL[9:0]	length of the Hsync signal; in number of pixel clock cycles; minimum value is 16
–	HBACKL[9:0]	interval between the Hsync active edge and the first active pixel; in number of pixels; minimum value is 16
–	HDISPL[11:0]	number of active pixels for one line; length of the data enable signal; minimum value is 16

9.11 Coast register

Remark: When POSTCOAST[4:0] = PRECOAST[2:0] = 0, then the coast pulse equals the VSYNC input.

Table 37 COAST (12h) bit allocation

BIT	7	6	5	4	3	2	1	0
Symbol	PRE COAST2	PRE COAST1	PRE COAST0	POST COAST4	POST COAST3	POST COAST2	POST COAST1	POST COAST0
Default	0	0	0	0	0	0	0	0

Table 38 COAST (12h) bit description

BIT	SYMBOL	DESCRIPTION
7 to 5	PRE COAST[2:0]	programs the length (in numbers of pixel clocks) of the coast pulse before the edge of the vertical sync signal
4 to 0	POST COAST[4:0]	programs the length (in numbers of pixel clocks) of the coast pulse after the edge of the vertical sync signal

9.12 Horizontal sync selection register

Table 39 HSYNCSEL (13h) bit allocation

BIT	7	6	5	4	3	2	1	0
Symbol	–	–	–	–	TESTCNT	BYSEPA	HSSEL	HSS
Default	X	X	X	X	0	1	0	0

Table 40 HSYNCSEL (13h) bit description

BIT	SYMBOL	DESCRIPTION
7 to 4	–	not used
3	TESTCNT	this bit is used to test the pixel counter 0 = normal mode 1 = test mode
2	BYSEPA	enables the sync separator for the PLL reference to be bypassed 0 = Hsync from the separator 1 = bypass of the sync separator
1	HSSEL	enables either the HSYNC or CHSYNC input signal to be selected 0 = HSYNC input 1 = CHSYNC input
0	HSS	enables either the HSYNC or CHSYNC input signal to be inverted 0 = non-inverted 1 = inverted

9.13 Vertical sync selection register

Table 41 VSYNCSEL (14h) bit allocation

BIT	7	6	5	4	3	2	1	0
Symbol	–	–	–	TSTCOAST	COE	VSS	COSSEL2	COSSEL1
Default	X	X	X	0	0	0	0	0

Table 42 VSYNCSEL (14h) bit description

BIT	SYMBOL	DESCRIPTION
7 to 5	–	not used
4	TSTCOAST	switches a multiplexer to select the output signal on pin VSYNCO 0 = output of the separator function 1 = output of the coast function
3	COE	enables coast mode 0 = coast mode 1 = no coast mode
2	VSS	enables VSYNC input signal to be inverted 0 = non-inverted 1 = inverted
1	COSSEL2	selects signal for coast PLL mode 0 = signal selected with bit COSSEL1 1 = pin coast
0	COSSEL1	can be used for the coast PLL mode; see bit COSSEL2 0 = VSYNC input 1 = VSYNC from the sync separator

9.14 Clamp register

Table 43 CLAMP (15h) bit allocation

BIT	7	6	5	4	3	2	1	0
Symbol	–	HSOSEL	CLPSEL2	CLPSEL1	CLPH	CLPENL	ICLP	CLPT
Default	X	0	1	0	0	0	0	0

Table 44 CLAMP (15h) bit description

BIT	SYMBOL	DESCRIPTION
7	–	not used
6	HSOSEL	defines the signal on the output HSYNCO; see Section 8.3 0 = Hsync from the Hcounter 1 = Ckref is reference of the PLL
5	CLPSEL2	can be used to select the clamp signal 0 = Hsync signal generated by the pixel counter 1 = signal selected with bit CLPSEL1

BIT	SYMBOL	DESCRIPTION
4	CLPSEL1	can be used to select the clamp signal; see bit CLPSEL2 0 = PLL reference signal 1 = clamp input
3	CLPH	inhibits the clamp signal during the Vsynco or coast signal; see bit TSTCOAST (Table 42) 0 = clamp inhibited during Vsynco 1 = clamp active during Vsynco
2	CLPENL	defines if clamp input works on edge or on level 0 = on edge; for all frequencies (must be preferably chosen) 1 = on level; only for frequencies below 45 MHz to have proper clamp function
1	ICLP	dedicated for test mode; should be forced to logic 0
0	CLPT	defines if the test mode of the clamp is active 0 = not active 1 = active

9.15 Inverter register

Table 45 INVERTER (16h) bit allocation

BIT	7	6	5	4	3	2	1	0
Symbol	–	COS	CLPS	CKREFO INV	DEOINV RGB	HSOINV RGB	VSOINV RGB	FIELDO INV
Default	X	0	0	0	0	0	0	0

Table 46 INVERTER (16h) bit description

BIT	SYMBOL	DESCRIPTION
7	–	not used
6	COS	enables the COAST input signal to be inverted 0 = non-inverted 1 = inverted
5	CLPS	enables the CLAMP input signal to be inverted 0 = non-inverted 1 = inverted
4	CKREFOINV	enables the output CKREFO to be inverted 0 = non-inverted 1 = inverted
3	DEOINVRGB	enables the output DEO to be inverted 0 = non-inverted 1 = inverted
2	HSOINVRGB	enables the output HSYNCO to be inverted 0 = non-inverted 1 = inverted

BIT	SYMBOL	DESCRIPTION
1	VSOINVRGB	enables the output VSYNCO to be inverted 0 = non-inverted 1 = inverted
0	FIELDOINV	enables the output FIELDO to be inverted 0 = non-inverted 1 = inverted

9.16 Output register

Table 47 OUTPUT (17h) bit allocation

BIT	7	6	5	4	3	2	1	0
Symbol	RGBSEL	TEN	AGCSEL1	AGCSEL0	BLKEN	DMXRGB	ODDARGB	SHIFTRGB
Default	0	0	0	0	0	0	0	0

Table 48 OUTPUT (17h) bit description

BIT	SYMBOL	DESCRIPTION
7	RGBSEL	defines which RGB input will be used 0 = input 1 1 = input 2
6	TEN	enables the track and hold operating mode to be selected 0 = mode enable; must be set to logic 0 for proper operation 1 = mode disable
5 to 4	AGCSEL[1:0]	define the output on pin AGCO 00 = RAGC 01 = GAGC 10 = BAGC 11 = not used
3	BLKEN	inhibits the blanking mode during clamp 0 = blanking active; during the blanking period, the RGB outputs of the ADC are fixed at the values of registers OFFSETR, OFFSETG and OFFSETB if these values are greater or equal to 0, or forced to 0 if these values are negative. 1 = blanking not active
2	DMXRGB	determines whether all pixels go to port A or if pixels go alternately to port A and B. The maximum data rate for single port mode is 140 MHz and it is 270 MHz in dual port mode. 0 = port A 1 = port A and B
1	ODDARGB	defines the parity of the pixels 0 = even pixel on port A 1 = odd pixel on port A
0	SHIFTRGB	defines output on port A and B 0 = synchronous 1 = interleaved

9.17 Output enable register 1

Table 49 OUTPUTEN1 (18h) bit allocation

BIT	7	6	5	4	3	2	1	0
Symbol	–	–	–	BOENRGB	AOENRGB	OROEN	TOUTERGB	TOUTSRGB
Default	X	X	X	1	1	1	0	0

Table 50 OUTPUTEN1 (18h) bit description

BIT	SYMBOL	DESCRIPTION
7 to 5	–	not used
4	BOENRGB	enables output port B to be set to high-impedance 0 = active signal 1 = high-impedance
3	AOENRGB	enables output port A to be set to high-impedance 0 = active signal 1 = high-impedance
2	OROEN	enables outputs Out Of Range to be set to high-impedance 0 = active signal 1 = high-impedance
1	TOUTERGB	defines if the test mode of the output buffer is active or not 0 = mode normal 1 = mode test
0	TOUTSRGB	defines the state of the output in test mode 0 = forces output to LOW 1 = forces output to HIGH

9.18 Output enable register 2

Table 51 OUTPUTEN2 (19h) bit allocation

BIT	7	6	5	4	3	2	1	0
Symbol	CKROEN	CSOEN	DEOENRGB	HSOENRGB	HPDOEN	VSOENRGB	CLPOEN	FIELDOEN
Default	1	1	1	1	1	1	1	1

Table 52 OUTPUTEN2 (19h) bit description

BIT	SYMBOL	DESCRIPTION
7	CKROEN	enables the output CKREFO to be set to high-impedance 0 = active signal 1 = high-impedance
6	CSOEN	enables the output CSYNCO to be set to high-impedance 0 = active signal 1 = high-impedance

BIT	SYMBOL	DESCRIPTION
5	DEOENRGB	enables the output DEO to be set to high-impedance 0 = active signal 1 = high-impedance
4	HSOENRGB	enables the output HSYNCO to be set to high-impedance 0 = active signal 1 = high-impedance
3	HPDOEN	enables the output HPDO to be set to high-impedance 0 = active signal 1 = high-impedance
2	VSOENRGB	enables the output VSYNCO to be set to high-impedance 0 = active signal 1 = high-impedance
1	CLPOEN	enables the output CLPO to be set to high-impedance 0 = active signal 1 = high-impedance
0	FIELDOEN	enables the output FIELDO to be set to high-impedance 0 = active signal 1 = high-impedance

9.19 Clock output register

Table 53 CLKOUTPUT (1Ah) bit allocation

BIT	7	6	5	4	3	2	1	0
Symbol	–	–	–	CKSELRGB	DLYCLKRGB	CKDATINV	OUTOSCILL	CKOENRGB
Default	X	X	X	0	0	0	0	1

Table 54 CLKOUTPUT (1Ah) bit description

BIT	SYMBOL	DESCRIPTION
7 to 5	–	not used
4	CKSELRGB	enables the selection of the signal on the pin CKDATA 0 = clock of output buffers; signal Ckdata 1 = pixel clock of the converter; signal Ckadco
3	DLYCLKRGB	enables a delay of 2 ns to be added to the clock Ckdata 0 = no delay 1 = 2 ns delay
2	CKDATINV	enables the polarity of the output CKDATA to be inverted 0 = non-inverted 1 = inverted
1	OUTOSCILL	enables pin CKDATA to be switched with a multiplexer to have signal Ckdata or the internal oscillator on the output 0 = Ckdata 1 = for test

BIT	SYMBOL	DESCRIPTION
0	CKOENRGB	enables the output CKDATA to be set to high-impedance 0 = active signal 1 = high-impedance

9.20 Internal oscillator register

Table 55 INTOSC (1Bh) bit allocation

BIT	7	6	5	4	3	2	1	0
Symbol	–	–	–	–	–	–	SWITCHOSC	INTOSCOFF
Default	X	X	X	X	X	X	0	0

Table 56 INTOSC (1Bh) bit description

BIT	SYMBOL	DESCRIPTION
7 to 2	–	not used
1	SWITCHOSC	enables a multiplexer to be switched; signal insertion on the input of the separator and coast block, between the internal oscillator and pin CKEXT 0 = normal case; if this bit is switched from logic 1 to logic 0, then an internal reset of the coast, activity detection and sync separator is done 1 = test mode
0	INTOSCOFF	disables the internal oscillator for the separator function, the coast gate and activity detection 0 = active; if this bit is switched from logic 1 to logic 0, then an internal reset of the coast, activity detection and sync separator is done 1 = disabled

9.21 Power management register

Table 57 PWRMGT (1Eh) bit allocation

BIT	7	6	5	4	3	2	1	0
Symbol	–	–	–	–	SHCKDMX	SHCKADC	STBY	DVIRGB
Default	X	X	X	X	0	0	0	0

Table 58 PWRMGT (1Eh) bit description

BIT	SYMBOL	DESCRIPTION
7 to 4	–	not used
3	SHCKDMX	test bits; should be set to logic 0 for proper operation
2	SHCKADC	test bits; should be set to logic 1 for better performances
1	STBY	enables the RGB block to be forced into the standby mode, except activity detection, I^2C-bus registers. In the standby mode, all outputs are in high-impedance state, except pin HPDO which is still active. If the IC is in the power-down mode, this bit has no effect 0 = IC active 1 = standby mode
0	DVIRGB	this bit must be set to logic 0 for proper operation

9.22 Read register

Table 59 READADDR (1Fh) bit allocation

BIT	7	6	5	4	3	2	1	0
Symbol	–	–	–	–	–	–	ADDR1	ADDR0
Default	X	X	X	X	X	X	0	0

Table 60 READADDR (1Fh) bit description

BIT	SYMBOL	DESCRIPTION
7 to 2	–	not used
1 to 0	ADDR[1:0]	register address to be read 00 = read register 0 01 = read register 1 10 = read register 2 11 = read register 3

9.23 Version register

Table 61 VERSION (01h) bit allocation

BIT	7	6	5	4	3	2	1	0
Symbol	–	–	–	–	VER3	VER2	VER1	VER0
Default	X	X	X	X	0	0	0	0

Table 62 VERSION (01h) bit description

BIT	SYMBOL	DESCRIPTION
7 to 4	–	not used
3 to 0	VER[3:0]	version of the IC

9.24 Sign detection register

The sign bits are set at logic 0 when the input is a mostly low input signal.

Table 63 SIGN bit allocation

BIT	7	6	5	4	3	2	1	0
Symbol	–	–	POLVS2	POLVS1	POLCHS2	POLCHS1	POLHS2	POLHS1
Default	X	X	0	0	0	0	0	0

Table 64 SIGN bit description

BIT	SYMBOL	DESCRIPTION
7 to 6	–	not used
5	POLVS2	sign of VSYNC2 input 0 = non inverted 1 = inverted
4	POLVS1	sign of VSYNC1 input 0 = non inverted 1 = inverted
3	POLCHS2	sign of CHSYNC2 input 0 = non inverted 1 = inverted
2	POLCHS1	sign of CHSYNC1 input 0 = non inverted 1 = inverted
1	POLHS2	sign of HSYNC2 input 0 = non inverted 1 = inverted
0	POLHS1	sign of HSYNC1 input 0 = non inverted 1 = inverted

9.25 Activity detection register 1

Table 65 ACTIVITY1 bit allocation

BIT	7	6	5	4	3	2	1	0
Symbol	ACVS2	ACVS1	ACSOG2	ACSOG1	ACCHS2	ACCHS1	ACHS2	ACHS1
Default	0	0	0	0	0	0	0	0

Table 66 ACTIVITY1 bit description

BIT	SYMBOL	DESCRIPTION
7	ACVS2	activity of VSYNC2 input 0 = not active 1 = active
6	ACVS1	activity of VSYNC1 input 0 = not active 1 = active
5	ACSOG2	activity of SOGIN2 input 0 = not active 1 = active
4	ACSOG1	activity of SOGIN1 input 0 = not active 1 = active
3	ACCHS2	activity of CHSYNC2 input 0 = not active 1 = active
2	ACCHS1	activity of CHSYNC1 input 0 = not active 1 = active
1	ACHS2	activity of HSYNC2 input 0 = not active 1 = active
0	ACHS1	activity of HSYNC2 input 0 = not active 1 = active

9.26 Activity detection register 2

It should be noted that activity, sign and polarity detection will be correctly set after a maximum delay of: 6 frame periods + 50 ms.

Table 67 ACTIVITY2 bit allocation

BIT	7	6	5	4	3	2	1	0
Symbol	–	ASD	3LEVEL	ACFIELD	HPDO	ACVSSEP	ACRXC1	ACRXC0
Default	X	0	0	0	0	0	0	0

Table 68 ACTIVITY2 bit description

BIT	SYMBOL	DESCRIPTION
7	–	not used
6	ASD	indicates if parasite sync pulses have been detected 0 = not detected 1 = detected
5	3LEVEL	state of the sync separator input 0 = Hsync 1 = 3-level Hsync
4	ACFIELD	activity of the sync separator FIELDO output 0 = not active 1 = active
3	HPDO	copy of the HPDO output state 0 = stable state on input 1 = new input
2	ACVSSEP	activity of the sync separator (Vsync output) 0 = not active 1 = active
1	ACRXC1	test bit
0	ACRXC0	test bit

10 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		−0.5	+5.5	V
ΔV_{CC}	supply voltage differences		−0.5	+0.5	V
V_i	input voltage	referred to V_{SSA}	−0.5	+5.5	V
V_{TCK}	pin TCK input voltage	referred to V_{SSA}	−0.5	+4.5	V
I_o	output current		−	50	mA
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	ambient temperature		0	70	°C
T_{vj}	virtual junction temperature		−	150	°C
V_{esd}	electrostatic discharge voltage	HBM	−2000	+2000	V

11 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		
	LQFP144 package		45	K/W
	LBGA208 package		25	K/W

12 CHARACTERISTICS

Typical values are measured at $V_{CCA} = V_{CCA(SOG)}$ to GNDA(SOG) or $V_{CCA(R)}$ to GNDA(R) or $V_{CCA(G)}$ to GNDA(G) or $V_{CCA(B)}$ to GNDA(B) = 3.3 V; $V_{CCD} = V_{CCD(TTL)}$ to GNDD(TTL) or $V_{CCD(ADC)}$ to GNDD(ADC) or $V_{CCD(I2C)}$ to GNDD(I2C) or $V_{CCD(MCF)}$ to GNDD(MCF) or $V_{CCD(TTL)}$ to GNDD(TTL) or $V_{CCD(SLC)}$ to GNDD(SLC) = 3.3 V; $V_{CCO} = V_{CCO(BB)}$ to GNDO(BB) or $V_{CCO(BA)}$ to GNDO(BA) or $V_{CCO(GB)}$ to GNDO(GB) or $V_{CCO(GA)}$ to GNDO(GA) or $V_{CCO(RB)}$ to GNDO(RB) or $V_{CCO(RA)}$ to GNDO(RA) or $V_{CCO(CLK)}$ to GNDO(CLK) = 3.3 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		3.0	3.3	3.6	V
V_{CCD}	digital supply voltage		3.0	3.3	3.6	V
V_{CCO}	output stage supply voltage		3.0	3.3	3.6	V
I_{CCA}	analog supply current		−	180	−	mA
I_{CCD}	digital supply current		−	125	−	mA
I_{CCO}	output stage supply current		−	1	−	mA
ΔV_{CC}	supply voltage difference					
	V_{CCA} to V_{CCD}		−100	−	+100	mV
	V_{CCO} to V_{CCD}		−165	−	+165	mV
	V_{CCA} to V_{CCO}		−165	−	+165	mV
P_{tot}	total power dissipation		−	1.0	1.3	W
P	power dissipation	power-down mode	−	10	−	mW
		standby mode	−	120	−	mW

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
R, G and B amplifiers						
RGB INPUTS: PINS RIN1, GIN1, BIN1, RIN2, GIN2 AND BIN2						
$V_{i(p-p)}$	input voltage range (peak-to-peak value)		0.5	–	1.0	V
I_i	input current		–40	–	+40	μA
C_i	input capacitance		–	3	–	pF
R_i	input resistance		50	–	–	kΩ
AMPLIFIERS						
B	bandwidth	–3 dB; T_{amb} = 25 °C	–	410	–	MHz
G_c	coarse gain	minimum coarse gain; code = 32	–	0	–	dB
		maximum coarse gain; code = 95	–	6	–	dB
$\Delta G/\Delta T$	amplifier gain stability variation with temperature	minimum coarse gain; code = 32	–	2	–	%
$G_{E(rms)}$	full-scale channel-to-channel matching (RMS value)	minimum coarse gain; code = 32	–	–	2.5	%
R, G and B clamp						
N_{clamp}	clamp level accuracy	f_{CLK} = 25MHz	–	–	2	LSB
Phase-Locked Loop (PLL)						
PLL; see Table 69						
$J_{PLL(p-p)}$	long term PLL phase jitter (peak-to-peak value)	f_{clk} = 270 MHz; DR = 2160	–	390	480	ps
DR	divider ratio		100	–	4095	
f_{PLL}	output clock frequency		10	–	270	MHz
f_{ref}	reference clock frequency		15	–	150	kHz
$\Delta\varphi_{step}$	phase drift		–	–	2	step
φ_{step}	phase shift step		–	11.25	–	deg
Analog-to-Digital Converters (ADCs); minimum coarse gain						
$f_{s(max)}$	maximum sampling frequency		270	–	–	MHz
INL	integral non-linearity	f_{clk} = 270 MHz; f_i = 10 MHz	–	±0.6	±1.3	LSB
DNL	differential non-linearity	f_{clk} = 270 MHz; f_i = 10 MHz	–	±0.25	±0.6	LSB
ENOB	effective number of bits	f_{clk} = 270 MHz; f_i = 10 MHz	–	7.6	–	bits
α_{ct}	crosstalk	f_{clk} = 270 MHz	–	–	–45	dB
S/N	signal-to-noise ratio	f_{clk} = 270 MHz; f_i = 10 MHz	–	48	–	dB
SFDR	spurious free dynamic range	f_{clk} = 270 MHz; f_i = 10 MHz	48	55	–	dB
THD	total harmonic distortion	f_{clk} = 270 MHz; f_i = 10 MHz	–	-55	–48	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data timing; 10 pF load; see Fig.4						
$t_{d(o)}$	output delay		–	4	5.2	ns
$t_{h(o)}$	output hold time		1.9	–	–	ns
$t_{su(o)}$	output setup time		–	–	6.6	ns
LV-TTL digital inputs and outputs						
INPUT PINS CKEXT, COAST, VSYNC1, VSYNC2, HSYNC1, HSYNC2, CHSYNC1, CHSYNC2, PWD, A0, DIS, TCK AND CLP						
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	V_{CCD}	V
OUTPUT PINS RA[7:0], RB[7:0], GA[7:0], GB[7:0], BA[7:0], BB[7:0], ROR, BOR, GOR, CKDATA, TDO, DEO, HPDO, HSYNCO, VSYNCO, FIELDO, CLPO, CKREFO AND CSYNCO						
V_{OL}	LOW-level output voltage	I_{OH} = 1 mA	–	–	0.4	V
V_{OH}	HIGH-level output voltage	I_{OL} = 1 mA	2.4	–	–	V
Data clock output						
OUTPUT PIN CKDATA						
$f_{CKDATA(max)}$	maximum buffer frequency		–	140	–	MHz
Data outputs						
OUTPUT PINS RA[7:0], RB[7:0], GA[7:0], GB[7:0], BA[7:0], BB[7:0], ROR, BOR, GOR, DEO, HSYNCO AND CSYNCO						
$f_{data(max)}$	maximum buffer frequency		–	70	–	MHz
Hsync inputs						
INPUT PINS HSYNC1, HSYNC2, CHSYNC1 AND CHSYNC2						
$t_{W(Hsync)(min)}$	minimum pulse width		250	–	–	ns
$t_{W(Hsync)(max)}$	maximum pulse width	in % of total horizontal line	–	–	20	%
SOG inputs						
INPUT PINS SOGIN1 AND SOGIN2						
$V_{sync(G)}$	sync-on-green pulse amplitude		150	–	–	mV
$V_{sync(G)}$	high/low differential amplitude of 3-level pulse		–	–	20	%
I^2C-bus (fast mode; 5 V tolerant)						
PINS SCL AND SDA						
f_{SCL}	clock frequency		–	–	400	kHz
C_b	capacitive load		–	–	400	pF

Table 69 Examples of PLL settings and performance
$V_{CCA} = V_{CCD} = V_{CCO} = 3.3$ V; $T_{amb} = 25$ °C; note 1.

VIDEO STANDARD	f_{ref} (kHz)	f_{clk} (MHz)	DR	K_O (MHz/V)	C_Z (nF)	C_P (pF)	I_P (μA)	Z (Ω)	LONG-TERM TIME JITTER	
									RMS (ps)	p-p (ps)
VGA 60 Hz VESA: 640 × 480	31.469	25.175	800	30	220	680	1200	510	500	3000
SVGA 72 Hz VESA: 800 × 600	48.08	50	1040	60	220	680	1200	510	370	1980
XGA 75 Hz VESA: 1024 × 768	60.02	78.75	1312	60	220	680	1600	640	220	1320
SXGA 60 Hz VESA: 1280 × 1024	63.98	108	1688	105	220	680	1600	510	185	1110
SXGA 75 Hz VESA: 1280 × 1024	80.00	135	1688	105	220	680	1600	640	145	870
UXGA 60 Hz VESA: 1600 × 1200	75.00	162	2160	105	220	680	2000	640	135	810
UXGA 75 Hz VESA: 1600 × 1200	93.75	202.5	2160	135	220	680	1600	800	95	570
UXGA 85 Hz VESA: 1600 × 1200	106.25	229.5	2160	135	220	680	2000	640	85	510

Note

1. PLL long-term time jitter is measured at the end of the video line, where it is at its maximum.

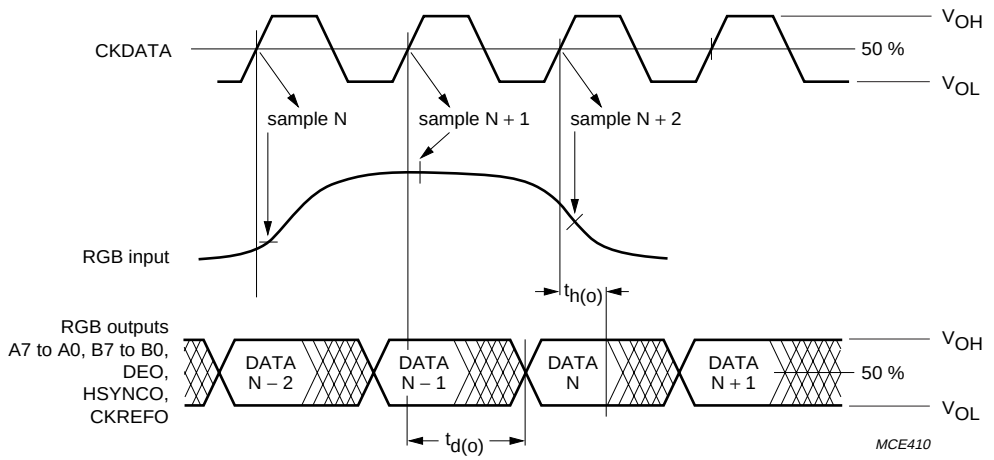
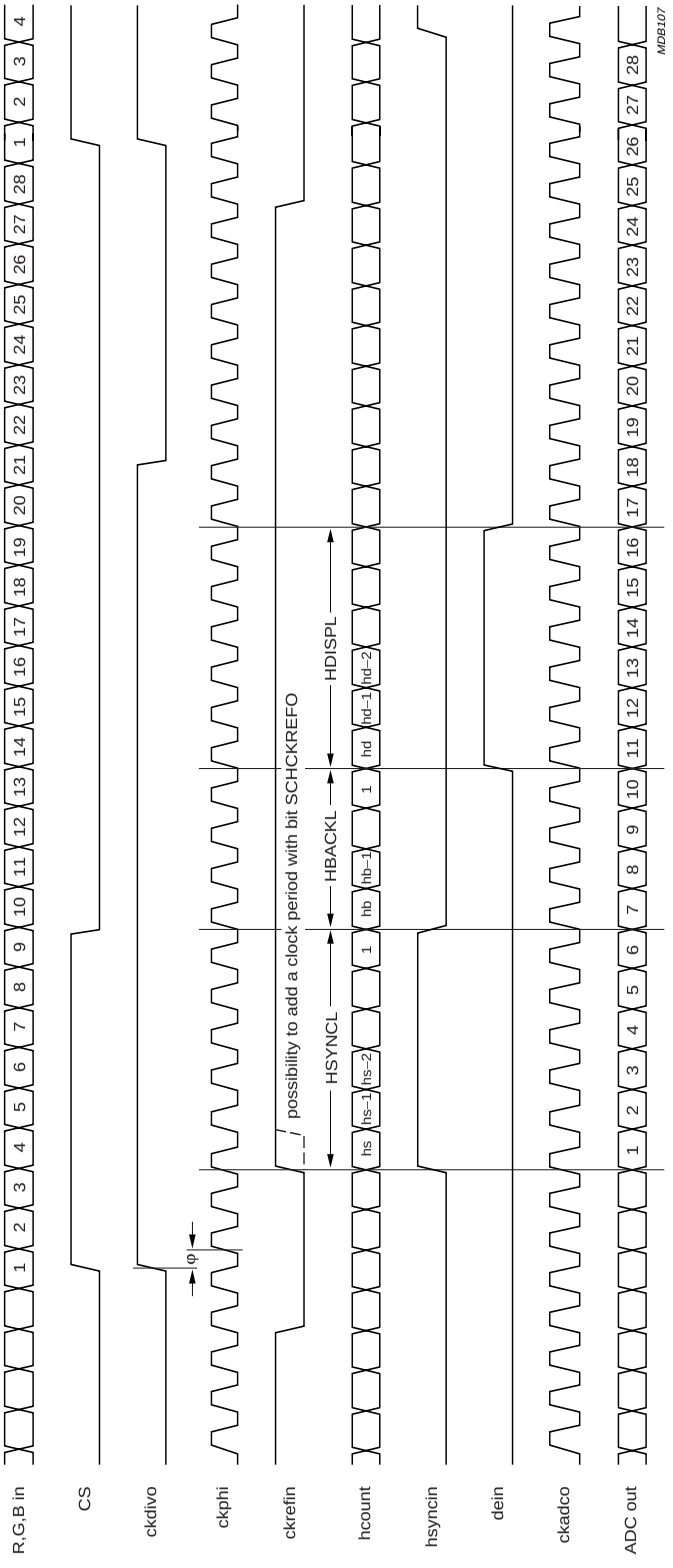


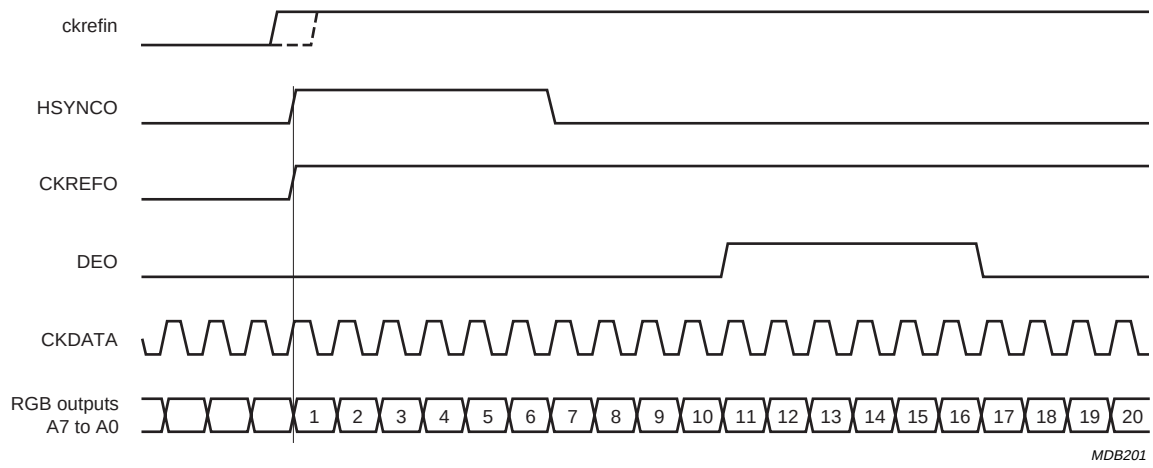
Fig.4 Data timing diagram.

13 TIMING



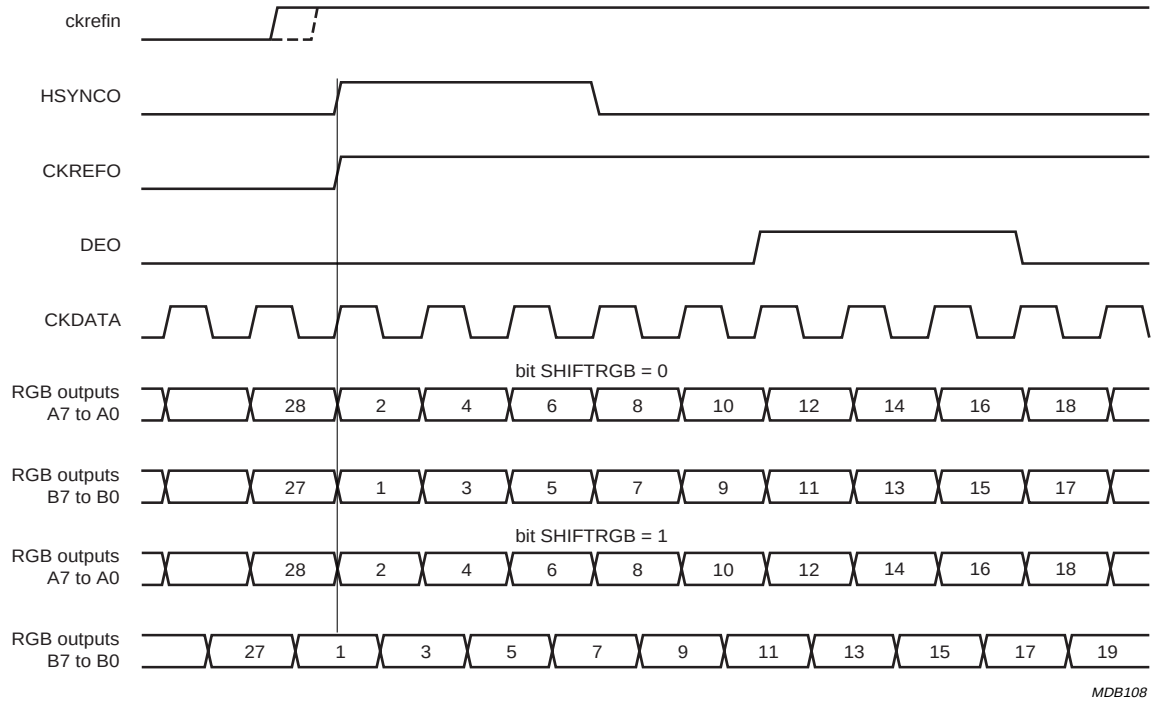
HSYNCL, HBACKL and HDISPL must be long 16 (minimum value in number of pixel clock cycles).

Fig.5 Timing diagram.



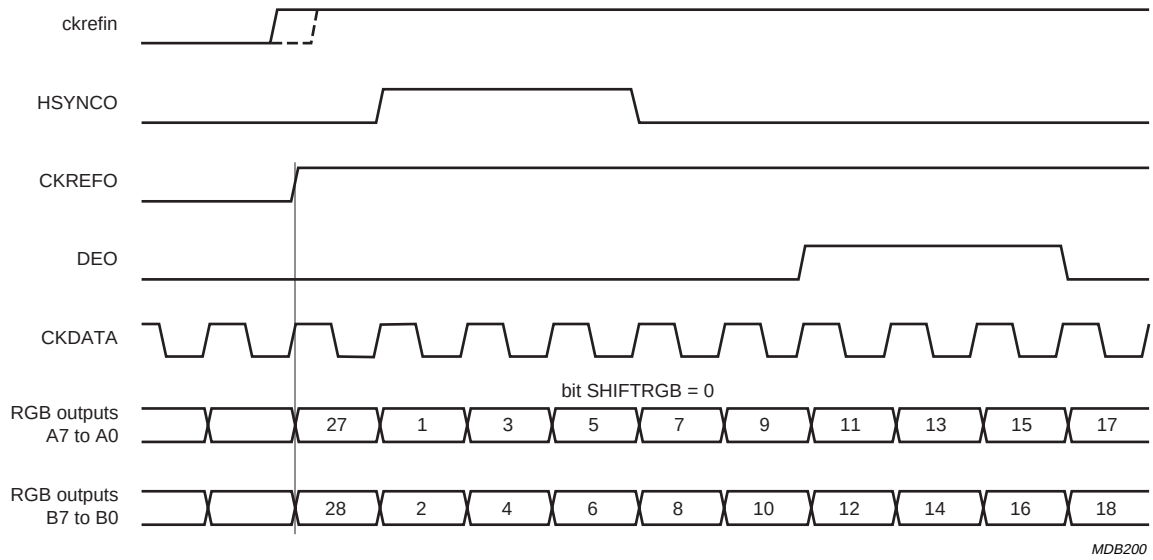
HSCYNCO, DEO, CKREFO and RGB outputs A7 to A0 are referred to the rising edge of ckrefin.
CKREFO is LOW during 8 clock pulses.

Fig.6 Output format port A.



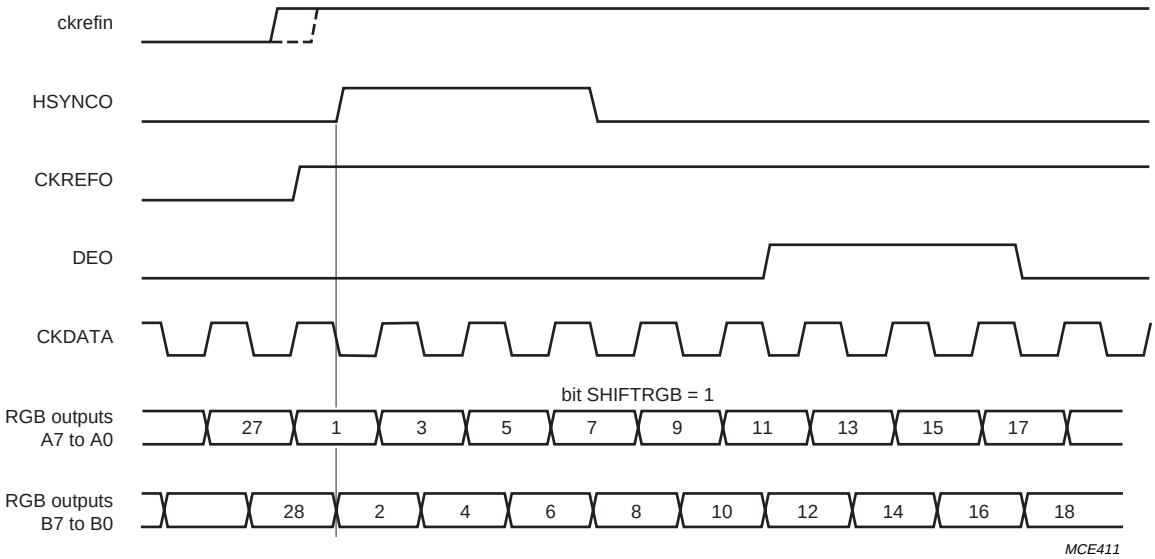
HSYNCO, DEO, CKREFO and RGB outputs A7 to A0 are referred to the rising edge of ckrefin.
CKREFO is LOW during 8 clock pulses.

Fig.7 Output formats ports A and B; even pixels port A and odd pixels port B.



HSYNCO, DEO, CKREFO and RGB outputs A7 to A0 are referred to the rising edge of ckrefin.
CKREFO is LOW during 8 clock pulses.

Fig.8 Output formats ports A and B; odd pixels port A; bit SHIFTRGB = 0.



HSYNCO, DEO, CKREFO and RGB outputs A7 to A0 are referred to the rising edge of ckrefin.
CKREFO is LOW during 8 clock pulses.

Fig.9 Output formats ports A and B; odd pixels port A; bit SHIFTRGB = 1.

14 APPLICATION INFORMATION

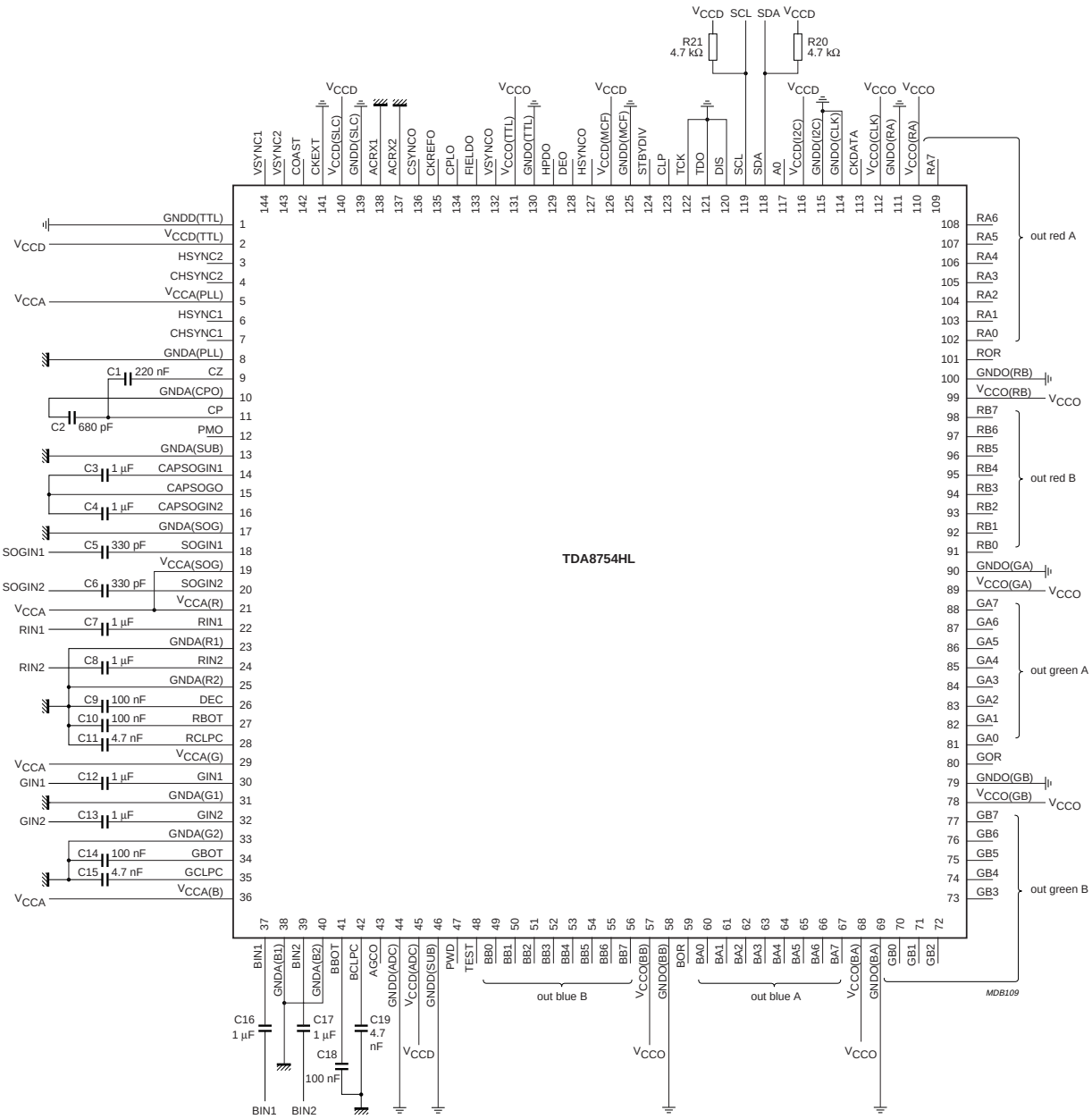
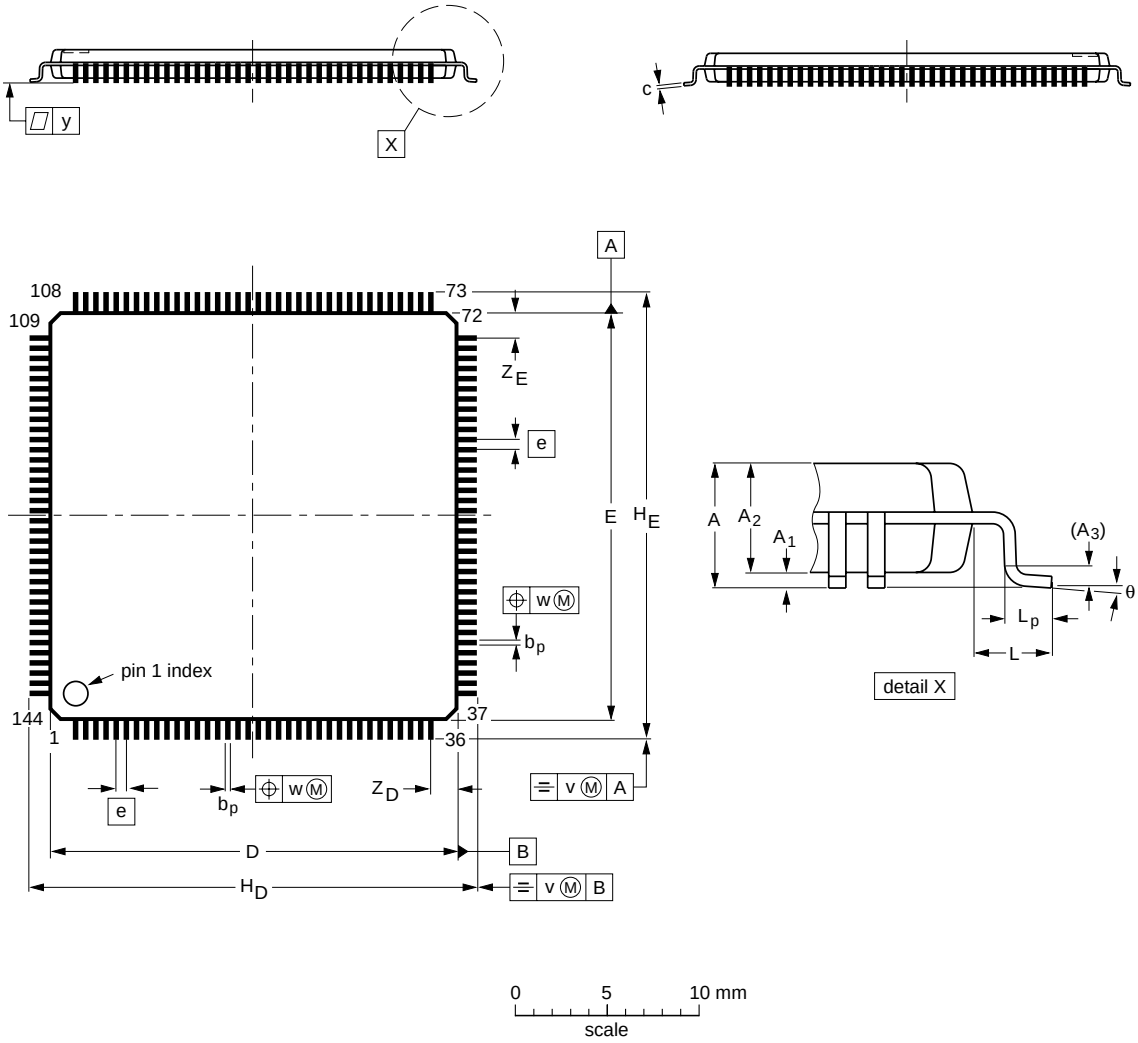


Fig.10 Application diagram.

15 PACKAGE OUTLINES

LQFP144: plastic low profile quad flat package; 144 leads; body 20 x 20 x 1.4 mm **SOT486-1**



DIMENSIONS (mm are the original dimensions)

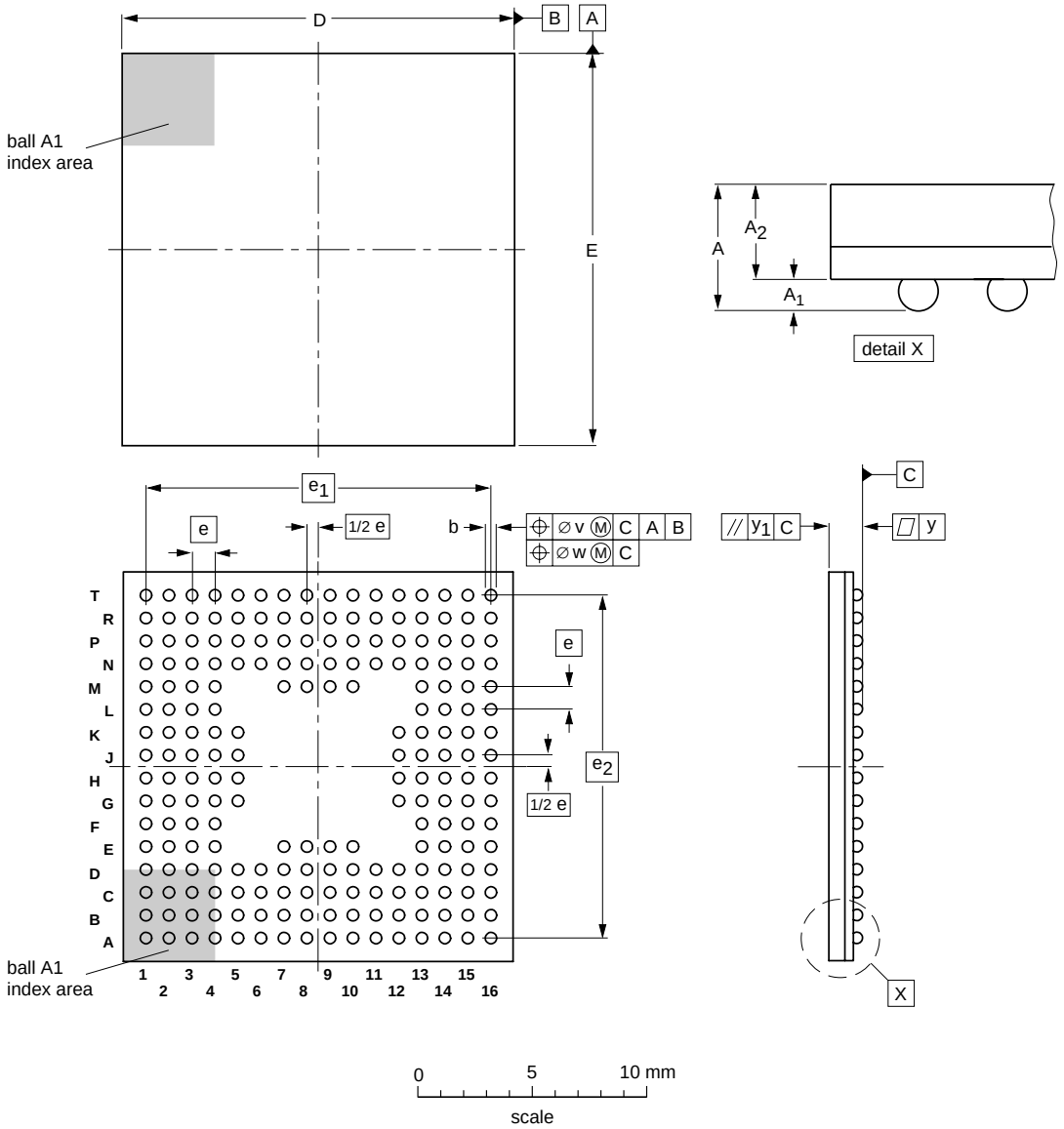
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	20.1 19.9	20.1 19.9	0.5	22.15 21.85	22.15 21.85	1	0.75 0.45	0.2	0.08	0.08	1.4 1.1	1.4 1.1	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT486-1	136E23	MS-026				~~00-03-14~~ 03-02-20

LBGA208: plastic low profile ball grid array package; 208 balls; body 17 x 17 x 1.05 mm **SOT774-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.65	0.45 0.35	1.20 0.95	0.55 0.45	17.2 16.8	17.2 16.8	1	15	15	0.25	0.1	0.12	0.35

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT774-1	- - -	MO-192	- - -			02-05-14

16 SOLDERING

16.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

16.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 220 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA and SSOP-T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 235 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

16.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

16.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

16.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, LBGA, LFBGA, SQFP, SSOP-T[3], TFBGA, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
PMFP[8]	not suitable	not suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
4. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
5. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
6. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
7. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
8. Hot bar or manual soldering is suitable for PMFP packages.

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I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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