PM4354

COMET-QUAD

ANSWERS TO FREQUENTLY ASKED QUESTIONS

APPLICATION NOTE

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[1] ANSI T1.102, “Digital Hierarchy: Electrical Interfaces,” 1992

[2] ANSI T1.107, “Digital Hierarchy: Formats Specification,” 1995

[3] ANSI T1.231, “Layer 1 In-Service Digital Transmission Performance Monitoring,” 1993

[4] ANSI T1.403, “Carrier to Customer Installation - DS-1 Metallic Interface Specification,” 1995

[5] AT&T PUB 54016, “Requirements For Interfacing Digital Terminal Equipment To Services Employing The Extended Superframe Format,” 1984

[6] AT&T TR 62411, “Accunet T1.5 - Service Description and Interface Specification,” December 1990

[7] AT&T TR 62411 Addendum 1, “Accunet T1.5 - Service Description and Interface Specification,” March 1991

[8] AT&T TR 62411 Addendum 2, “Accunet T1.5 - Service Description and Interface Specification,” October 1992

[9] Bellcore, GR-303-CORE, “IDLC System Generic Requirements, Objectives, and Interface,” 1997

[10] Bellcore, TA-NWT-000170, “Digital Cross-Connect System Requirements and Objectives,” 1993

[11] Bellcore, TA-TSY-000278, “Digital Data System; T1 Data Multiplexer,” Issue 1, November 1985

[12] Bellcore, TR-TSY-000008, “Digital Interface Between the SLC96 Digital Loop Carrier System and a Local Digital Switch,” Issue 2, August 1987

[13] ETSI ETS 300 011, “ISDN Primary Rate User-Network Interface Specification and Test Principles,” 1992

[14] ETSI ETS 300 011 A1, “ISDN Primary Rate User-Network Interface Specification and Test Principles,” 1992

[15] ETSI ETS 300 166, “Physical Characteristics of Interfaces at 2048 kbit/s,” 1994

[16] ETSI ETS 300 233, “Access Digital Section for ISDN Primary Rates,” 1992

[17] ETSI ETS 300 324-1, “Signaling Protocols and Switching (SPS); V interfaces at the Digital Local Exchange (LE) V5.1 Interface for the Support of Access Network (AN) Part 1: V5.1 Interface Specification,” February 1994

[18] ETSI ETS 300 347-1, “Signaling Protocols and Switching (SPS); V Interfaces at the Digital Local Exchange (LE) V5.2 Interface for the Support of Access Network (AN) Part 1: V5.2 Interface Specification,” September 1994

[19] ETSI CTR 4, “Integrated Services Digital Network (ISDN); Attachment requirements for terminal equipment to connect to an ISDN using ISDN primary rate access,” November 1995

[20] ETSI CTR 12, “Business Telecommunications (BT); Open Network Provision (ONP) technical requirements; 2 048 kbit/s digital unstructured leased lines (D2048U) Attachment requirements for terminal equipment interface,” December 1993

[21] ETSI CTR 13, “Business Telecommunications (BTC); 2 048 kbit/s digital structured leased lines (D2048S); Attachment requirements for terminal equipment interface,” January 1996

[22] FCC Part 68.308, “Signal Power Limitations,” 1993

[23] GO-MVIP, “Multi-Vendor Integration Protocol, MVIP-90,” Release 1.1

[24] ITU-T G.703, “Physical/Electrical Characteristics of Hierarchical Digital Interfaces,” Revision 1, 1991

[25] ITU-T G.704, “Synchronous Frame Structures Used at Primary and Secondary Hierarchical Levels,” Revision 1, 1991

[26] ITU-T G.823, “Control of Jitter and Wander Within Digital Networks based on the 2048 kbit/s Hierarchy,” 1994

[27] ITU-T I.431, “Primary Rate UNI Specification – Layer 1 Specification,” 1993

[28] PMC-Sierra, PMC-2000091, “COMET-QUAD Short Form Data Sheet”, Issue 1

[29] PMC-Sierra, PMC-1990315, “COMET-QUAD Long Form Data Sheet”, Issue 6

[30] PMC-Sierra, PMC-1991237, “COMET-QUAD Evaluator Board”, Issue 2

[31] TTC JJ-20.1, “PBX Y-Interface Specification,” 1995

[32] TTC JT-G703, “Physical/Electrical Characteristics of Hierarchical Digital Interfaces,” 1995

[33] TTC JT-G704, “Frame Structures on Primary and Secondary Hierarchical Digital Interfaces,” 1995

[34] TTC JT-G706, “Frame Synchronization and CRC Procedure,” 1995

[35] TTC JT-I431, “ISDN Primary Rate User-Network Interface Layer 1 - Specification,” 1995

[36] NTT, “Technical Reference for High-Speed Digital Leased Circuit Services,” Third Edition, 1990

2 DEFINITIONS

AIS	Alarm Indication Signal. This is a signal consisting of unframed all-ones serial digital data. It is transmitted when there is no good data to transmit (due to an upstream failure), and is useful for maintaining a timing reference to downstream equipment. This signal can be detected and transmitted by the COMET-QUAD.
AMI	Alternate Mark Inversion. This is a ternary coding scheme for electrical transmission of digital data. Each binary one that is transmitted is represented by a RZ pulse that is of opposite polarity of the preceding pulse. Each binary zero that is transmitted is represented by a space (no pulse).
ANSI	American National Standards Institute. This is a non-profit, non-government federation of standards-making and standards-using organizations. It publishes standards, but does not develop them. Compliance with an American National Standard is voluntary and does not preclude anyone from manufacturing, marketing, purchasing, or using products, processes, or procedures not conforming to the standards. More on ANSI can be found at their Web site: web.ansi.org/default_js.htm
B8ZS	Bipolar Eight Zero Substitution. This refers to a zero suppression scheme that replaces eight consecutive zeros with a decodable sequence of LCVs. Zero suppression is important to ensure proper operation of clock recovery circuits.
CAS	Channel-Associated Signaling. This is the term for the standardized (ITU-T G.704) signaling method consisting of a signaling multiframe carried in Timeslot 16 of the E1 frame.
CDRC	Clock and Data Recovery unit. This is PMC-Sierra's mnemonic to refer to the functional block in the T1XC which recovers the timing of the received signal, then uses that timing to sample the received data.

CHI	Concentration Highway Interface. This is a channelized timeslot backplane format originally defined on Lucent Technologies Microelectronics devices for T1 and E1 framing. The specification for the CHI can be downloaded from http://www.lucent.com/micro/isdn/isdndoc.html .
COMET-QUAD	This is PMC-Sierra's mnemonic for Four Channel Combined E1/T1/J1 Framer Transceiver. The marketing number for this device is PM4354.
CPU	Central Processing Unit.
CRC	Cyclic Redundancy Check. This is a scheme for error monitoring by making a Boolean cyclic polynomial calculation over a digital data payload. The transmitter transmits the results of this calculation, and the receiver compares this to it's own calculation. If there is a difference, it is assumed that one or more bits have been corrupted during transmission of the digital payload. Of the standardized DS1 formats, only ESF uses a CRC. Of the standardized E1 formats, the CRC-multiframe format uses a CRC.
D/A Converter	Digital-to-Analog Converter. This term is used generically to refer to a circuit that converts digital information into an analog signal. In the COMET-QUAD, a D/A Converter is used to create the transmitted line pulses.
DJAT	Digital Jitter Attenuator. This is PMC-Sierra's mnemonic for the functional block within the COMET-QUAD which attenuates phase jitter on a timing reference. It contains a digital PLL to create a jitter-attenuated clock, and a FIFO to absorb the phase jitter.
DRAM	Dynamic RAM.
DS0	Digital Service Level 0. A DS0 is an octet in a bitstream that is repeated at an 8 kHz frame rate to give a total bandwidth of 64 kbit/s. Sometimes the LSB of the octet is robbed for signaling purposes so only 56 kbit/s is available for user data.
DS1	Digital Service Level 1. This term refers to a standardized format for digital signals which is comprised of 24 DS0s plus one bit of overhead which is repeated at an 8 kHz frame rate to give a total bandwidth of 1544 kbit/s.

DS1	Digital Signal, Level 1. This term refers to a standardized (ANSI T1.107) format for transmitting serial digital data at 1.544Mbps.
DS2	Digital Service Level 2. This term refers to a standardized format for digital signals which is comprised of four DS1 signals asynchronously multiplexed plus overhead for a sum of 789 bits repeated at an 8 kHz frame rate to give a total bandwidth of 6312 kbit/s.
DS3	Digital Service Level 3. This term refers to a standardized format for digital signals which is comprised of seven DS2 signals asynchronously multiplexed plus overhead for a sum of 4760 bits sent at a 44.736 MHz bit rate. Note that the frame rate is not 8 kHz.
DSX-1	Digital Signal Cross-Connect, Level 1. This term refers to the interface at a digital cross-connect (a convenient central point of cross-connecting, rearranging, patching and testing digital equipment and facilities) operating at the DS1 level.
E1	European transmission format level 1. This term is used to describe systems signals conforming to the ITU-T 2048 kbit/s format and interface specifications.
E1XC	E1 Transceiver. This is PMC-Sierra's mnemonic for the PM6341 E1 framer/transceiver device.
ELST	Elastic Store. This is PMC-Sierra's mnemonic for the functional block within the COMET-QUAD that provides the elastic store function. The ELST is used for adapting the received data to the system backplane rate. Since these signals are not necessarily synchronized, they may slip with respect to each other. The function of the ELST is to control the slips such that they occur on the frame boundaries indicated on the backplane. For example, if the received data is faster than the system backplane then the ELST will drop full frames of data while maintaining the timeslot alignment on the backplane.
EMC	Electro-Magnetic Compatibility. This is a generic term used to refer to the ability of electronic equipment to operate in the presence of electro-magnetic forces as well as control of the electro-magnetic forces emanating from electronic equipment so that other equipment is not affected.

ESF	Extended Superframe Format. This is a standardized (ANSI T1.107) DS1 format. It makes use of the DS1 F-Bits to provide a 24-frame signaling multiframe, CRC error checking, and an out-of band maintenance channel.
F-Bit	Framing Bit. This term denotes the first bit of each DS1 frame that is used for carrying the framing overhead information. The specific use of this bit depends on the DS1 framing format.
FEAC	Far-End Alarm and Control. This term is applied to channels in a transmitted data stream that are reserved for carrying alarm and control information to and from the far-end equipment.
FEBE	Far-End Block Error. This term refers to standardized indicators that the far end equipment has received at least one bit error within a block of received data. In the E1 format, the E-bit of the CRC-4 multiframe structure (defined in ITU-T G.704) is used for FEBE indication.
FIFO	First-In First-Out buffer. This term refers to a digital buffer that outputs data in the same order as it was input.
Flag	A pre-defined pattern which marks the start and end of a data packet. For HDLC, the flag character is 01111110 (binary).
Frame Relay	This term is used in multiple contexts. It can refer to a switching technology, an interface standard or a set of data services. More on Frame Relay can be found at the Frame Relay Forum Web site: www.frforum.com
GPIC	General Purpose PCI Controller. This is PMC-Sierra's term for the functional block of the COMET-QUAD device which translates all transactions initiated by the RMAC and TMAC into activity onto a 32-bit PCI bus operating at up to 33 MHz.
HDB3	High-Density Bipolar of order 3. This is a zero suppression scheme that uses the intentional insertion of AMI LCVs to maintain a minimum transition density in the E1 signal. This function is important since it provides clear channel capability — the payload content is not restricted by the capabilities of the remote receiver's clock recovery unit.

HDLC	High-Level Data Link Control. A common message-based datalink protocol (OSI Layer 2) issued by ISO. Messages are delineated by flag characters and use a CRC frame check sequence for error detection.
IBIS	I/O Bus Interface Simulation. This is a standardized format for simulating I/O of digital logic devices. PMC-Sierra provides free IBIS models for most products, available from the PMC-Sierra Web site.
ISDN	Integrated Services Digital Network. This is a worldwide public telecommunications network that is implemented as a set of digital switches and paths supporting a broad range of services.
IPNS	ISDN PBX Network Specification. This is a forum with the mission “to promote the further worldwide proliferation of QSIG including its extension to other network technologies (e.g., IP, ATM, Frame Relay) with special consideration of quality and other critical characteristics of real-time communication.” More on the IPNS Forum can be found at their Web site: www.qsig.ie/index.htm
ITU-T	International Telecommunication Union - Telephony. This is a committee within a United Nations treaty organization. The charter is “to study and issue recommendations on technical, operating, and tariff questions relating to telegraphy and telephony.” Its primary objective is end-to-end compatibility of international telecommunications connections. More on the ITU-T can be found at their Web site: www.itu.ch
J1	Japanese transmission format level 1. This term is used to describe systems signals conforming to the TTC format and interface specifications for both 1544 kbit/s and 2048 kbit/s rates.
LCV	Line Code Violation. This term denotes a received bipolar pulse that violates the AMI, B8ZS, or HDB3 ternary coding scheme. LCV events are detected and accumulated by the COMET-QUAD.

LIU	Line Interface Circuit. This is a generic term used to refer to the circuitry in telecommunications equipment responsible for shaping the electrical signal for transmission on the transmission cable and responsible for recovering a clock from the received electrical signal on the cable. The LIU will usually implement a line-coding scheme (e.g. B8ZS or HDB3) as well as some performance monitoring, alarm, and diagnostic circuitry.
Long-Haul	This term applies to T1 interconnections over 100 Ω twisted pair cable that are more than the 655 feet specified in DSX-1 electrical interface specifications (e.g. ITU-T G.703). Cable distances up to 6000ft are typical of long-haul connections. ANSI T1.403 specifies that the signal attenuation that can be expected over a long-haul cable span is 22dB, although most long-haul receivers are designed to operate with attenuation up to 36dB.
LOS	Loss-of-Signal. This term refers to the state a clock recovery unit is in when there is no input signal. Since both DS1 and E1 require a minimum pulse density, the COMET-QUAD monitors for both digital and analog LOS. The COMET-QUAD declares digital LOS if the number of consecutive spaces (ZEROs) received exceeds a programmable threshold. The COMET-QUAD declares analog LOS by implementing the ITU-T G.775 analog LOS requirements based on the analog signal level.
MVIP	Multi-Vendor Interface Protocol. This is an industry standard for a TDM bus interface between a physical layer framing subsystem and a payload processing (or switch) subsystem. More on MVIP can be found at the GO-MVIP Web site: www.mvip.org
NRZ	Non-Return-to-Zero. This refers to the common electrical coding scheme for serial digital data. Logical ones are represented as a pulse that is high for the full bit period. Logical zeros are represented as no pulse for the full bit period. This scheme is useful for serial digital data that has an associated clock signal.
OOF	Out-Of-Frame alignment. This is the state a DS1 or E1 framer if it cannot find the frame alignment pattern within the received serial 1.544Mbps data.

PCM	Pulse-Coded Modulation. A term encompassing digital serial data which is encoded into electrical pulses. AMI, B8ZS, and HDB3 are PCM coding schemes.
PLL	Phase-Locked Loop. The generic term for a feedback system that generates a clock with a fixed (locked) phase/frequency relationship to some reference clock.
QSIG	QSIG is a protocol specified by the IPNS to link ISDN PBXs in a private telecommunications network. It has also found many other important applications such as: multi-vendor ISDN PBX based private networks, networking of remote ISDN PBXs interconnecting voice/fax/DP servers, providing network wide reach for applications supporting mobility in corporate networks Virtual Private Networks, broadband private networks, and trans-European trunked radio. Further information on QSIG can be found at the IPNS Web site: www.qsig.ie/qsig/index.htm
RJAT	Receive Jitter Attenuator. This is PMC-Sierra's mnemonic for the functional block within the COMET-QUAD which attenuates phase jitter on the receive timing reference. It contains a digital PLL to create a jitter-attenuated clock, and a FIFO to absorb the phase jitter.
RPSC	Receive Per-Channel Serial Controller. This is PMC-Sierra's mnemonic for the functional block of the COMET-QUAD which allows per-channel functions to be performed on the received PCM and signaling data, before being passed to the receive backplane.
RZ	Return-to-Zero. This refers to an electrical coding scheme for serial digital data. A logical ONE is represented as a pulse that is high for half the bit period then returns to low (zero) for the remainder of the bit period. A logical ZERO is represented as no pulse. This scheme is useful for serial digital data from which a clock must be recovered.
SF	Superframe Format. This is a standardized (ANSI T1.107) DS1 format. It makes use of the DS1 F-Bit to maintain a 12-frame signaling multiframe.

SIGX	Signaling Extractor. This is PMC-Sierra's mnemonic for the functional block of the COMET-QUAD that extracts and stores the received robbed-bit (channel-associated) signaling information. It also provides some per-channel functions on the received PCM data.
SLC®96	Subscriber Loop Carrier 96. This is a standardized[12] DS1 format. It is similar to SF, but makes use of the F-Bits such that it also carries a datalink. This datalink is used for concentrating up to four DS1 streams for an aggregate of 96 (4 x 24) 64kbps channels.
ST-BUS®	Standard Telecom Bus. This is a registered trademark of Mitel Corporation used to describe a TDM bus used for DS0 cross-connection. The ST-BUS is a subset of the MVIP bus.
T1	Transmission format level 1. This term is used loosely to describe systems carrying DS1-formatted signals electrically over cable.
T1DM	T1 Data Multiplexer. This is a standardized[9] DS1 format. It uses Timeslot 24 of the DS1 frame to pass additional framing information as well as a remote alarm and datalink.
T1XC	T1 Transceiver. This is PMC-Sierra's mnemonic for the PM4341A T1 framer/transceiver device.
TDM	Time-Division Multiplexed.
TJAT	Transmit Jitter Attenuator. This is PMC-Sierra's mnemonic for the functional block within the COMET-QUAD which attenuates phase jitter on the transmit timing reference. It contains a digital PLL to create a jitter-attenuated clock, and a FIFO to absorb the phase jitter.
TPSC	Transmit Per-Channel Serial Controller. This is PMC-Sierra's mnemonic for the functional block of the COMET-QUAD which allows per-channel functions to be performed on the PCM and signaling data from the transmit backplane, before transmission.
TRAN	Transmitter. This is PMC-Sierra's mnemonic for the functional block of the COMET-QUAD that inserts the DS1 or E1 framing overhead into the transmitted data stream. The TRAN can be configured to operate in unframed mode.

V5	V5. This is a standardized (ITU-T and ETSI) protocol suite for the connection of access networks to local exchange. The access network itself typically has public switched telephone network and ISDN interfaces (user ports) to the customer. The V5 interfaces are based on interfaces at 2048 kbit/s (E1).
XLPG	Transmit Line Pulse Generator. This is PMC-Sierra's mnemonic for the functional block of the COMET-QUAD that generates the transmit pulse shapes that drive the line interface. The XLPG provides the industry's highest resolution of pulse shape programmability.

3 BACKGROUND AND OVERVIEW

The PM4354 COMET-QUAD device is a four Channel Combined E1/T1/J1 Transceiver and Framer. It is suitable in long haul and short haul T1, J1 and E1 applications with a minimum of external circuitry.

The data sheet for COMET-QUAD (PMC-1990315) is an extensive document with detailed description of device's operation and registers.

This document gives the customer set of the most frequently asked questions with answers and reference literature for additional study.

If further clarification is required, please contact PMC-Sierra's technical support team at apps@pmc-sierra.com.

4 ANSWERS TO FREQUENTLY ASKED QUESTIONS

4.1 General Questions

Q1) Are there any reference designs or application notes available for the COMET-QUAD?

Yes, extensive design recommendations are provided in the reference designs and application notes available on the PMC-Sierra website (www.pmc-sierra.com):

1) There is an AAL1gator-8 Paper Reference Design (PMC-1991089) which shows an application of 2 COMET-QUADs with an AAL1gator-8 (an ATM segmentation and reassembly processor).

2) In addition, there is a S\UNI-IMA-8 Reference Design (PMC-2002117) which features two COMET-QUADs, one S\UNI-IMA-8, and one S\UNI-Duplex.3) There is also a COMET-QUAD Evaluator Board Design document (PMC-1991237) which details the design of our COMET-QUAD Evaluator board. This is a PCI card which installs in a PC and is controlled via Windows software. There is a PCI bridge on the card to allow the PC to directly make register read/writes to the COMET-QUAD.

These reference designs show the layout and necessary power-supply filtering for the COMET-QUAD. They also implement all necessary magnetics and line protection components.

Q2) Is there an evaluation platform for the COMET-QUAD?

There is a COMET-QUAD Evaluator Board (PMC-1991237) that is available for use on any PC running Windows 95/98 or NT/2000. The Evaluator card plugs into the any PCI slot, and provides full control of a COMET-QUAD device. The card features four T1/E1 jacks, an onboard oscillator, as well as external access for most I/O pins.

Windows application software is distributed with the Evaluator board, and includes the necessary device drivers to run in both a Windows 98 and a Windows-NT environment. The software is comprised of a graphical user interface (GUI), which provides the user with full register access and device status. The user can create and run TCL scripts, as well as make function calls from the COMET-QUAD device driver API.

Q3) What are the packaging options for the COMET-QUAD?

As of the publication date of this document, the COMET-QUAD is packaged in 208-ball Plastic Ball Grid Array (PBGA). This package type is designated with a –PI suffix. However, the packaging type will be changed in the near future to a pin-compatible 208-ball small thin Plastic Ball Grid Array (stPBGA). This new package type is designated with a –NI suffix.

Q4) Does the COMET-QUAD support industrial temperature range?

Yes, the COMET-QUAD supports industrial temperature range (-40C to 85C).

Q5) What is the power consumption of the COMET-QUAD?

The analog (3.3V) portions of the COMET-QUAD consume the majority of the power, compared with the digital 2.5V portions. The power consumption varies very widely depending on many factors, such as length of cable, ones-density of transmitted signal, and so forth.

The total power consumption can be calculated from the operating currents, P = IDDOP33 * VDD33 + IDDOP25 * VD25. Total power consumption includes on-chip power (dissipated as heat) and transmitted off-chip power.

In the “DC Characteristics” section of the datasheet, typical values for operating current are given (measured at 85°C ambient temperature, in T1 mode, transmitting 50% ones density, with short-haul 0-110 ft pulse waveform). Using these values, we can calculate a typical value for power consumption:

2.5V Power = 2.5V x 38mA = 95mW

3.3V Power = 3.3V x 441mA = 1455.3mW

Total Power: 1550.3 mW or approximately 1.55W

Q6) What are the major differences between COMET-QUAD and COMET?

The COMET-QUAD is nearly equivalent to four COMETs. It is capable of supporting four T1s, J1s, or E1s, whereas the COMET supports a single T1, J1, or E1. However, there are a few functional differences between using one COMET-QUAD and four COMETs:

- the COMET-QUAD’s line-side operates analog only. In other words, the LIU cannot be bypassed. In comparison, the COMET can operate in digital mode whereby the internal LIU is not used.

- the COMET-QUAD has only one RSYNC (receive recovered line-rate) output pin, which is shared between the four ports. The RSYNC pin presents the recovered timing from one of the four ports, selectable by the RSYNC_SEL[1:0] bits. Therefore, with the COMET-QUAD it is not possible to externally access the recovered timing of all four ports simultaneously.

- the COMET-QUAD has a single transmit line-rate input (CTCLK) shared between the four ports. This means that if all four transmit ports are timed to the external CTCLK pin, then the four ports will transmit synchronously. The only way to have each port independently-timed is if the transmit timing is sourced elsewhere, such as from the backplane BTCLK (in non H-MVIP mode) or from the recovered timing. The equivalent pin to CTCLK in the single COMET is labeled TCLKI.

- the COMET-QUAD provides full support for HMVIP multiplexing. It can internally multiplex the four receive streams into a single 8.192MHz HMVIP stream outputted on the MVBRD pin. Likewise, it can internally demultiplex four T1/E1 transmit streams from a 8.192MHz HMVIP stream presented on the MVBTD pin.

- In addition, the COMET-QUAD can support HMVIP multiplexing of CAS signaling using the CASBRD and CASBTD pins. COMET-QUAD provides similar support for CCS signaling utilizing the CCSBRD and CCSBTD pins.

- the COMET-QUAD has fewer HDLC transmitters/receivers per T1/E1 link. Whereas the COMET provides three HDLC transmitters/receivers for a single T1/E1 link, the COMET-QUAD provides one HDLC transmitter/receiver per T1/E1 link

4.2 Software Questions

Q7) Is there a Programmer's Guide available for the COMET-QUAD?

Yes, there is a Programmer's Guide available for the COMET-QUAD (PMC-2000151). Most software related questions are answered in this document.

Q8) Is a microcontroller required to control and monitor COMET-QUAD?

Yes. A microprocessor is required to initialize the COMET-QUAD. Immediately after power-up, the COMET-QUAD is not operational, and needs to be programmed via its microprocessor interface.

Q9) Is there a software driver available for the COMET-QUAD?

Yes, PMC-Sierra provides a software driver for COMET-QUAD. This software driver can be downloaded after registering on PMC-Sierra's Web site at www.pmc-sierra.com.

Q10) Can the COMET-QUAD be reset via software?

Yes, COMET-QUAD can be reset by software. The Programmer's Guide gives detailed information on how to reset the device. In fact the COMET-QUAD should always be reset by software after a power-up sequence (following a hardware reset) and at any other time required by the embedded processor. Software reset is achieved by writing into the register 00Eh. The RESET bit implements a software reset. If this bit has a value 1, the device is held reset. Note that the RESET bit is not self-clearing.

Holding the COMET-QUAD in a reset state effectively puts it into a low-power, stand-by mode.

After software or hardware reset, all the COMET-QUAD internal registers will be at the default values described in the COMET-QUAD data sheet (PMC-1990315).

Q11) How should the COMET-QUAD be powered-up?

All the 3.3V power pins (analog power) should ramp-up before the 2.5V pins (digital power). During the ramp-up, it is critical that the instantaneous voltage on the 2.5V pins never exceeds the instantaneous voltage on the 3.3V pins.

The point at which the power ramp-up is considered complete is defined when both the 2.5V power and 3.3V power have risen above the minimum input level thresholds specified in the "DC Characteristics" section of the COMET-QUAD Datasheet (PMC-1990315). These minimum thresholds are: 3.135V for the 3.3V power, and 2.3V for the 2.5V power.

After the ramp-up, there are three items that must be performed before the device is ready to use:

1) The RSTB (chip reset) must be driven active-low for a minimum of 100ns

2) The CSB (Chip Select) pin must be driven high concurrently with RSTB driven low at least once in order to clear any internal test modes. The most common way to accomplish this is to drive CSB high during the chip reset in step 1). Although there is no specified minimum time that CSB & /RSTB needs to be driven, 100ns will provide a safe margin.

3) The TRSTB (JTAG reset) must also be driven active-low for a minimum of 100ns in order to reset the JTAG state machine so that the I/O pins are in their correct operational configuration. This JTAG reset can be performed independently of the above two steps 1) and 2).

Q12) How should the COMET-QUAD be initialized?

Here is a brief list of steps one must remember when programming the COMET-QUAD. For further details on each step, please refer to the Programmer's Guide and Datasheet. These steps represent the minimum that needs to be programmed.

1) Select E1 or T1 in the Global Configuration registers (Q00h). All four ports must be configured to the same setting.

Note: The letter "Q" in the register address denotes the port being configured. Since there are four ports in the COMET-QUAD, this "Q" is substituted with either the value 0h, 1h, 2h, or 3h. Registers that are common to all four ports do not have the "Q" in their address.

2) Select the crystal frequency being supplied for XCLK. This is done in the CSU Configuration register (0D6h). In E1 mode, a 2.048MHz crystal must be selected. In T1 mode, either a 2.048MHz or 1.544MHz crystal may be chosen. Note that the setting here applies to all four ports.

3) Select the Line Encoding to be used. For the receive direction, configure the 'AMI' bit in the CDRC Configuration registers (Q10h). For the transmit direction, the relevant register depends on whether in T1 or E1 mode. For T1, configure the 'B8ZS' bit in the T1-XBAS Configuration register (Q54h). For E1, configure the 'AMI' bit in the E1-TRAN Configuration register (Q80h).

4) For framed operation, the framing format must be chosen. For T1, this is done by configuring the T1-XBAS (Q54h), which inserts the framing pattern in the transmit direction, and the T1-FRMR (Q48h), which recovers framing in the receive direction. For E1, one must configure the E1-TRAN (Q80h), which inserts the framing pattern, and the E1-FRMR (Q90h) which recovers the framing.

5) Select the source for the Transmit timing source in registers Q06h. Three sources are possible: BTCLK (Backplane), CTCLK, and recovered timing.

6) Configure the backplane interfaces in the BRIF registers (Q30h and Q31h) and the BTIF Configuration register (Q40h and Q41h). For both the BRIF and BTIF, one must select the backplane data rate, clock master slave, frame pulse master or slave, frame pulse type, clock edges, and so on.

7) Depending on the configuration of the backplane, the Elastic Stores may be needed. In general, the Elastic Stores are required whenever the backplane timing differs from the line-side timing in terms of rate and/or alignment. To enabled/disabled these blocks, use the 'TXELSTBYP' bit (registers Q06h) for the transmit direction and 'RXELSTBYP' (registers Q02h) for the receive direction. When using any Elastic Store, it must be configured for T1 or E1 operation via the 'IR' and 'OR' bits (in registers Q20h for TX-ELST, and Q1Ch for RX-ELST).

8) If either of the jitter-attenuators are being used (TJAT or RJAT), they need to be configured. Each have an N1/N2 divisor value that needs to be programmed for its internal PLL to function correctly. For TJAT, please refer to the table in the datasheet (under the register description for Q1Ah). For RJAT, set N1=N2= 2Fh for T1, or N1=N2= FFh for E1.

9) The RLPS (the analog receiver) requires a equalizer voltage reference value to be programmed into the 'EQ_VREF[5:0]' bits in registers QDCh. For T1, use the value 2Ch. For E1, use the value 3Dh.

10) Program the Receive Equalizer RAM table into the RLPS Indirect Registers. This table must be programmed in order to recover analog pulses.

11) Enable the Receive Equalizer by setting the 'EQEN' bit in registers QFFh to '1'. This will enable the equalizer by activating the feedback loop. The equalizer will begin to move up and down the Equalizer RAM table according to changes in the incoming signal level.

12) Program the Transmit Pulse Waveform into the XLPG Indirect Registers. There are 24x5 Indirect Registers that need to be programmed. Remember to also program the SCALE bits to the value indicated under each waveform table given in the datasheet. Lastly, it is recommended to leave the HIGHZ bit '1' until the entire configuration is complete.

13) Run the Fuse Stabilization procedure provided in the Programmer's Guide. If this isn't done, the transmit pulse waveform may vary quite significantly in amplitude.

14) Run the RPLS Optimization routine. This is a sequence of 29 writes, which is provided in the datasheet in the Operation section, under "Using the Line Receiver". This routine needs to be run only once, after configuring all four ports.

4.3 Modeling and Simulation Questions

Q13) Are IBIS models available for the COMET-QUAD?

Yes, the IBIS model for the COMET-QUAD is available for download on PMC-Sierra's website.

Q14) Are full-functional models available for the COMET-QUAD?

Full-functional models are not available for the COMET-QUAD.

4.4 Line Interface Questions

Q15) Can the COMET-QUAD terminate long-haul signals?

Yes, the COMET-QUAD's receiver is capable of recovering long-haul and short-haul signals. In the case of long-haul signals, the COMET-QUAD offers typical signal recovery of up to 43 dB of attenuation in E1 and up to 44dB of attenuation in T1. The guaranteed minimum performance is 32dB for E1 and 36dB for T1. These numbers are based on PIC-22 gauge cable emulation.

Q16) Does the COMET-QUAD meet line protection requirements?

Line protection is provided entirely by the protection components used with the COMET-QUAD, not by the COMET-QUAD itself. The protection components chosen in the Evaluator Board design (PMC-1991237) are compliant with the major standards such as Bellcore GR 1089-CORE, FCC Part 68 and UL 1459 & 1950

Q17) Does the COMET-QUAD meet T1, E1 and J1 jitter requirements?

Yes, the COMET-QUAD complies with T1, E1 and J1 jitter requirements.

Below mentioned jitter standards have been successfully tested:

- T1 Short and Long Haul Jitter Tolerance test complies with AT&T TR62411 and GR-499 CORE standards.
- E1/J1 Jitter Tolerance test complies with ITU-T G.823 and TBR 013 standards.
- T1 Long Haul Intrinsic Jitter test complies with ANSI T1.403 and ANSI T1.408 standards.

- T1 Short Haul Intrinsic Jitter test complies with AT&T TR62411 and ANSI T1.102 standards.
- E1/J1 Intrinsic Jitter test complies with ITU G.749, ITU-T G.823 and TBR 12 standards.

Q18) How does the COMET-QUAD meet return loss requirements on the line interface?

Return loss is the ratio, expressed in decibels, of signal power transmitted into a system to the power reflected. It can be considered as an echo that is reflected back by impedance changes in the link.

The COMET-QUAD has been designed to comply with return loss requirements of the following standards:

- ITU-T G.703
- JT-G703
- ETSI CTR4
- ETSI CTR13.

Return loss requirements are shown in Table 1.

Table 1 - Standardized T1/E1 Return Loss Requirements

		Interface Type			
		T1 100Ω	**E1 75Ω**	**E1 120Ω**	**J1 100Ω**
Receive Return Loss	Standard	None	ITU-T G.703	ETSI CTR4	JT-G703
	Requirement	N/A	≥ 15dB at 2048 kbit/s	≥ 12dB from 51 kbit/s to 102 kbit/s, ≥ 18dB from 102 kbit/s to 2048 kbit/s, ≥ 14dB 2048 kbit/s to 3072 kbit/s	≥ 15dB at 2048 kbit/s
Transmit Ret. Loss	Standard	None	None	ETSI CTR13	None

		Interface Type			
		T1 100Ω	**E1 75Ω**	**E1 120Ω**	**J1 100Ω**
	Requirement	N/A	N/A	≥ 6dB from 512 kbit/s to 102.4 kbit/s, ≥ 8dB from 102.4 kbit/s to 3072 kbit/s	N/A

Q19) Are the jitter attenuators on the COMET-QUAD "crystal-less" ?

The jitter-attenuators in the COMET-QUAD do not require any external "pullable" or "tunable" crystals. They are implemented instead with digital PLLs that adjust in discrete steps, and simply use an internal high-speed version of XCLK.

Q20) Why is a 110Ω impedance mentioned in the COMET-QUAD line interface circuit description?

The COMET-QUAD line interface circuitry has been designed to be a compromise between 100Ω T1/J1 cable and 120Ω E1 cable. Therefore, the recommended line interface circuit for those applications has an effective impedance of 110Ω.

There is no physical component of value 110Ω, rather the impedance matching relies on impedance "reflection" through the transformers. The effective impedance at the line side of the transformers is equal to the impedance at the chip side multiplied by the square of the turns ratio.

For example, in the receiver there is an 18.2Ω resistor placed differentially on the chip side of the transformer. This resistance drives the line through a 1:2.42 ratio transformer. The effective impedance is therefore approximately 110Ω.

Q21) Does the COMET-QUAD support the 75Ω E1 interface?

Yes, the COMET-QUAD supports the 75Ω E1 interface standardized in ITU-T G.703. The circuitry required for this interface is described in the COMET-QUAD data sheet.

Q22) Why does the COMET-QUAD reference design not show the 75Ω E1 interface?

For ISDN UNIs and access applications (as well as many other structured and unstructured E1 services) the120Ω interface is the only standardized interface.

Therefore, the COMET-QUAD Evaluation Board addresses the majority of the application space for E1 interfaces while highlighting the great advantage of the COMET-QUAD's software-selectability.

Using the COMET-QUAD, it is possible to design one board for sale in Europe, North America and Japan, with software selecting between the 100Ω T1/J1 and the 120Ω E1 — no need for relays or population options.

If it is desired to support the 75Ω E1 interface, then the corresponding circuitry (detailed in the COMET-QUAD data sheet, PMC-1990315) would need to be added to the circuitry of the Evaluation Board.

Q23) What transformer manufacturers does PMC-Sierra recommend for use with the COMET-QUAD ?

Manufacturer that PMC-Sierra has evaluated for use with the COMET-QUAD is:

- **Pulse**

Part number: T9021

12220 World Trade Drive
San Diego, CA 92128
Phone: (619) 674-8100
Fax: (619) 674-8262
Web: www.pulseeng.com

Since the COMET-QUAD requires the same turns ratio transformer as the COMET, transformers used for COMET can also be used for the COMET-QUAD. Transformers used on the COMET were from:

- **Halo Electronics**

Part number: TG23-1505N1

P.O. Box 5826
Redwood City, CA 94063
Phone: (650) 568-5800
Fax: (650) 568-6161
E-mail: HALOElect@aol.com
Web: www.haloelectronics.com

- **Midcom**

Part number: 50436

121 Airport Drive
P.O. Box 1330
Watertown, SD 57201-6330
Toll Free: 1-800-643-2661 (US and Canada)
Phone: (605) 886-4385
Fax: (605) 886-4486
Web: www.midcom-inc.com

- **Belfuse**

Part number: S553-6500-A7, S553-6500-A8, S553-6500-66 or S553-6500-45

206 Van Vorst Street
Jersey City
New Jersey 07302
Toll Free: 1-800-643-2661 (US and Canada)
Phone: (201) 432-0463
Fax: (201) 432-9542
Web: www.belfuse.com

Q24) How does the COMET-QUAD generate transmit pulse shapes?

The XLPG block contains current drivers (DACs), which drive current out TXTIP/TXRING to create a voltage across the external termination resistors. The “shape” of the pulse is programmed by the user into an internal RAM table (Indirect Registers), while the “amplitude” of the pulse is controlled with the SCALE[4:0] bits in the XLPG Configuration registers (register QF0h). The internal RAM creates the pulse by feeding time samples to the DACs. The SCALE[4:0] bits control the amplitude by controlling the number of DACs that placed in parallel to drive the TXTIP/TXRING. There are a maximum of 21 parallel DACs, so the SCALE[4:0] value can range anywhere from 0 (all DACs disabled, no pulses being driven) to 21 (15h).

The internal RAM consists of a 24x5 table. The 24 rows represent the 24 time samples used to generate the pulse shape. Sample 0 is transmitted first and sample 23 is transmitted last. The table is also composed of five columns, representing 5 Unit Intervals (UIs), or bit periods. UI#0 refers to the current bit period. UI#1 refers to the previous bit period. Similarly, UI#2 thru UI#4 refer to the three bit periods prior to UI#1. The five columns are conditionally summed together to create the time samples, depending if pulses exist in the corresponding UIs. If a pulse exists in the current bit period, each time sample is comprised of the value in the UI#0 column. If a pulse exists in the preceding bit period, then the subsequent column UI#1 is added to the time samples (this column represents the "leftover" portions of the previous pulse). Likewise for

UI#2, UI#3 and UI#4. This technique allows each individual pulse to spread over multiple bit periods -- up to 5 bit periods. This is particularly important in long-haul applications, where the pulse is shaped to concentrate its energy in the low frequency spectrum, which results in the tails of the pulses being very long. From this perspective, the UI#0 represents the beginning portion of the current pulse, while UI#1 thru UI#4 represent leftover portions (the "tails") of any preceding pulses.

Q25) Does the COMET-QUAD have a special transmit pulse shape to help meet AT&T TR62411 intrinsic jitter requirements?

Yes. The TR62411 pulse template is different than other T1 pulse templates (e.g. ANSI T1.403) because it is designed to ensure that there is no inter-symbol interference perceived as jitter effects on the transmitted pulse. Inter-symbol interference is one of three most important sources of pattern-dependent jitter. Wrong equalization of the incoming bit stream could change the shape of the equalized signal in a way that is dependent on the data pattern. When this misequalized signal is applied to the nonlinear element of the clock recovery circuit, it causes a phase variation in the extracted timing signal.

The datasheet provides a set of transmit pulse waveform tables specifically for TR62411. Also, note that TR62411 Jitter requirements may not be met if using a 2.048MHz crystal rather than a 1.544MHz crystal.

Q26) Is the RSYNC signal jitter attenuated?

Yes. In fact, RSYNC is always jitter-attenuated regardless of whether RJAT is bypassed. When RJAT is bypassed, it is removed from the datapath and will not affect the timing of the data presented to the backplane. However, it is still operational, and the RSYNC signal is taken from its output.

Q27) Can the COMET-QUAD internal LIU be placed in a tri-state condition?

Yes. When either the HIGHZ bit is set, or the SCALE[] bits are set to ‘00’, the TXTIP and TXRING pins become high-impedance. However, the TXCM common mode pins (which serve as the drain for the current generated by TXTIP and TXRING) are not high-impedance and need to be disconnected via a relay. This means that in a LIU redundancy application, where only one COMET-QUAD drives the transformers at any given time, the idle COMET-QUAD must have its TXCM pin disconnected via a relay.

It is also possible to internally tri-state the TXCM pin, but this requires placing the entire COMET-QUAD in a test mode.

Q28) Which register controls RSYNC signal recovery from any of the 4 links?

Register 0BBh controls the selection of RSYNC COMET-QUAD output. With the bits RSYNC_SEL[1:0] it's possible to select one of four quadrants as the source.

Q29) What happens to RSYNC when the link the COMET-QUAD is recovering clock from is lost?

Upon reception of Loss of Signal the RSYNC will be switched to XCLK or be held at high impedance as selected by RSYNC_MEM in the register 002h. For switching to another link it is necessary to reprogram register 0BBh.

4.5 Frame Format Questions

Q30) What are the differences between J1 and T1?

J1 refers to Japanese first order digital transmission systems. Unfortunately however, the term "J1" can refer to quite a number of interface variants. Here is an explanation of those variants.

In the past Japan has adopted both European and American formats. Therefore, there are some J1 interfaces that operate at the E1 rate of 2.048 Mbit/s rather than the T1 rate of 1.544 Mbit/s. The COMET-QUAD can support E1 formats, but was not specifically designed to meet Japanese standards for 2.048 Mbit/s.

For Japanese PBX interfaces, the TTC has created its own standards for a "Y-interface." In particular, JJ-20.11 states that the interface rate is 2.048 Mbit/s. However, there are many significant differences with respect to European E1. Firstly, the line coding used is CMI rather than HDB3. The basic frame alignment is indicated by CMI violations rather than a framing pattern in Timeslot 0. An 8-frame multiframe is used rather than a 16-frame multiframe. There are many other differences as well. The COMET-QUAD is not compatible with this interface.

For Japanese 2.048 Mbit/s ISDN PRI interfaces, the TTC has adopted ITU-T standards with JT-I431-b. This is exactly equivalent to European ISDN and is fully supported by the COMET-QUAD.

Within the 1.544 Mbit/s J1 application, Japan has a number of variants as described below.

For Japanese "Inter-Network" interfaces, the TTC has adopted the ITU-T standards with JT-G703, JT-G704, JT-G706 and JT-G733. However, these Japanese versions do differ significantly. Firstly, the Japanese want the output pulse shape to be measured at the output port, rather than at the distribution

frame. Also, the cable characteristic impedance is 110Ω rather than 100Ω. The Japanese interface only supports the use of ESF for inter-network interfaces, but they change the way the CRC-6 is calculated. The COMET-QUAD has been designed to be able to accommodate all of these differences, including framing in the presence of the alternate CRC-6.

For older Japanese inter-network interfaces a 1.544 Mbit/s format based on SF was used. This did differ from American T1 SF in that the yellow alarm was transmitted in the 12th F-Bit rather than in Bit 2 of all timeslots. This variant of the yellow alarm, often called the “Japanese yellow alarm" created difficulty for many American T1 framers. The COMET-QUAD however has an option to frame in the presence of the Japanese yellow alarm and is therefore compatible with this interface. The COMET-QUAD can also transmit the Japanese yellow alarm under software control.

For Japanese 1.544 Mbit/s ISDN PRI interfaces (the “I-interface”), the TTC has adopted the ITU-T standards with JT-I431. There are some minor differences with respect to American ISDN. The ESF datalink is not used. The CRC-6 is required to be checked as protection against mimic framing. The COMET-QUAD is compatible with these requirements.

The trend of Japanese standards is toward better harmonization with American and European standards. This implies that the COMET-QUAD will be compatible with most emerging J1 applications.

Q31) Does the COMET-QUAD meet ETSI framing and interworking requirements?

Yes, the COMET-QUAD automatically performs the framing and interworking requirements described in the following ETSI standards: ETS 300 011, ETS 300 233, TBR 004, TBR012, and TBR013.

Q32) Does the COMET-QUAD have a transmit elastic stores?

The COMET-QUAD has both a transmit elastic store (TX-ELST) and a receive elastic store (RX-ELST). This allows the backplane timing to be decoupled from the line-side timing in both the transmit direction and the receive direction.

Q33) When should the COMET-QUAD transmit elastic stores be used?

The transmit elastic-stores (TX-ELST) allow the timing of the backplane, and the timing of the transmit line-rate to be fully independent. Keep in mind that if the average frequency of the backplane is not equal to the average frequency of the transmitted line-rate, frame slips will occur.

Q34) Why does the COMET-QUAD have only four integrated HDLC controllers?

The reason is in utilization of the microprocessor bus. The microprocessor bus would be overloaded with V5.2 HDLC packets for all four quadrants. The COMET-QUAD supports V5.1 and V5.2 HDLC packets which can be transmitted and received over the H-MVIP interface. This feature required additional Common Channel Signaling (CCS) input and output on the COMET-QUAD. An external HDLC controller such as PMC-Sierra's FREEDM family of products should be used.

Q35) Does the COMET-QUAD support QSIG?

Yes. QSIG is a signaling system for interconnection of private integrated network exchanges in a corporate network. This signaling system is based on the ITU-T Q.93x and Q.95x recommendations and thus guarantees compatibility between the public and private ISDN.

QSIG has the same Layer 1 and Layer 2 of public ISDN signaling and thus uses the HDLC subset called LAPD in the D-Channel.

The COMET-QUAD internal HDLC controllers are capable of terminating the LAPD protocol carried in the D-Channel, and is therefore compatible with QSIG applications.

QSIG does differ from public ISDN signaling protocol at Layer 3, but that Layer is transparent to the COMET-QUAD.

More on QSIG can be found at the Web site: www.qsig.ie/qsig/index.htm.

Q36) Can I process frame relay packets using the COMET-QUAD integrated HDLC controllers?

No. The integrated HDLC controllers can only be trained on single timeslots and are intended for overhead processing such as facility data links and ISDN D-Channel. The high bandwidth of frame relay and the fact that many frame relay channels span multiple timeslots mean that external HDLC controllers should be used instead.

In particular, PMC-Sierra's PM7364 and PM7366 FREEDM family of products provide optimized HDLC processing for frame relay applications. The FREEDM products connect seamlessly to the COMET-QUAD using the NxDS0 backplane mode.

Q37) How do the COMET-QUAD PMON counters relate to ANSI T1.231 performance parameters?

Integrated services networks must support a variety of services such as voice, digital data and video. Each of these services has its own distinct operational characterstics and sensitivity to various errors in the network. Normally, the impairments in the network are not serious failures, but small degradations in performance.

Performance monitoring is thus required to capture these degradations and provide a basis for successful network maintenance. This type of monitoring refers to the set of functions and capabilities necessary for a network element to gather, store, threshold, and report performance data associated with its monitored entities. For DS1 the line and path entity indicators (L, P) apply.

Performance parameters are a set of primitives detectable from the monitored signal. Typical performance parameters are:

- LOS Second-Line (LOSS-L). This parameter is a count of 1-second intervals containing one or more LOS defects.

- Code Violation-Line (CV-L). This parameter is a count of both BPVs (Bipolar Violation) and EXZs (Excessive Zeros) occurring over the accumulation period. A BPV is the occurrence of a pulse of the same polarity as the previous pulse while an EXZ for an AMI coded signal is the occurrence of any zero string length greater than fifteen contiguous zeros. Impairment events are counted during the accumulation period which is 15 minutes for ANSI T1.231 standard.

- Errored Second-Line (ES-L). This parameter is a count of 1 second intervals with one or more BPVs, or one or more EXZs, or one or more LOS defects.

- Severly Errored Second-Line (SES-L). This parameter is a count of 1 second intervals with 1544 or more BPVs plus EXZs, or one or more LOS defects.

The purpose of the COMET-QUAD Performance Monitor counters (PMON) is to accumulate common performance parameters on intervals (up to one second). These parameters are under control of microprocessor. The PMON contains the following registers:

- Framing Bit Error Counter

- OOF/COFA/Far End Block Error Count (LSB and MSB)

- LCV Count (LSB and MSB)

- Bit Error/CRC Error Count (LSB and MSB)

Each quadrant in the COMET-QUAD has its own set of PMON registers. Writing any value to the Global PMON Update register (00Dh) will update all the PMON registers. The PMON registers can then be read until the polling interval is complete and the microprocessor updates the PMON again.

The PMON registers contain the raw defect counts collected in a one second interval. Therefore, software must process the PMON values and accumulate them in memory. Furthermore, the COMET-QUAD must be configured such that its PMON registers count appropriate events.

Here is a comparison of above mentioned T1.231 performance parameters and their relationship to the COMET-QUAD PMON counters.

- T1.231 LOSS-L (LOS second). In the COMET-QUAD the LOS is controlled by the LOS[1,0] bits in Register 010h. When set to LOS[1]=1 and LOS[0]=1, the COMET-QUAD will declare LOS defect when 175 continuous bit periods with no pulses are detected. The LOS defect is indicated with LOSV bit in Register 012H.

- T1.231 CV-L (Code Violation-Line). In the COMET-QUAD PMON there is an LCV counter. The COMET-QUAD contains a BPV bit in Register 003h that controls the definition of LCV. The default setting is BPV=0 which means that both BPV and EXZ events will be counted by the PMON LCV counter. Therefore, so long as BPV=0 then the LCV count in the COMET-QUAD will correspond to the CV-L parameter required by T1.231.

- T1.231 ES-L (Errored Second-Line). To report the ES-L parameter, your software must check both the COMET-QUAD LCV count and the LOSV status; if either are non-zero then ES-L occurred.

- T1.231 SES-L (Severely Errored Second-Line). This Line-related parameter is similar to ES-L except that your software would only check to see if the COMET-QUAD LCV count is greater or equal to 1544 or that the LOSV bit is set before declaring SES-L.

Therefore, the COMET-QUAD provides all the basic defect detection and counting required for T1.231 performance monitoring; however, in some cases software may be required to process this information and derive the standardized performance parameter definitions.

4.6 Backplane Interface Questions

Q38) What are the details of the COMET-QUAD H-MVIP backplane interface?

MVIP and H-MVIP are both backplane multiplexing formats that are used to reduce pin count between the COMET-QUAD and the system. MVIP multiplexes two T1s or E1s into 4.096MHz MVIP streams. H-MVIP is a higher-rate version of MVIP that multiplexes four T1/E1s into 8.192MHz streams. Both MVIP and H-MVIP frame-align the T1/E1 links, such that cross-connection of DS0 timeslots can be easily accomplished if desired.

With the original COMET, both MVIP and H-MVIP are supported. However because COMET is a single T1/E1 device, the multiplexing and demultiplexing of multiple T1/E1 streams needed to be done externally. In the COMETreference design (PMC-981210), this was done with a Mitel MVIP controller.

The COMET-QUAD provides full support for H-MVIP and hence can internally multiplex/demultiplex the H-MVIP streams (using its four local T1/E1 streams) directly to external pins.

The HMVIP interface comprises of, at minimum, two 8.192MHz HMVIP multiplexed streams. One carries the four transmit T1/E1 streams, while the other carries four receive T1/E1 streams.

There can optionally be an additional pair of HMVIP streams used to carry CAS signaling for the four T1/E1 links. A third pair of HMVIP streams can be used to carry CCS signaling for the four T1/E1 links.

All the HMVIP streams are timed by a common external clock and frame pulse. The clock operates at 8.192MHz. The frame pulse is 8kHz, and is sampled by a separate 4.096MHz clock. Every device connected to the HMVIP bus must be slave to the clock and frame pulse.

For the COMET-QUAD, the HMVIP pins are:

CMV8MCLK (Input) – the common externally provided 8.192MHz clock

CMVFPB (Input) – the common externally provided frame pulse

CMVFPC (Input) – the common external 4.096 clock for sampling the frame pulse

MVBTD (Input) – carries transmit data for four T1 or E1 streams (8.192MHz)

MVBRD (Output) – carries receive data for four T1 or E1 streams (8.192MHz)

CASBTD (Input) – carries CAS signaling for four T1/E1 transmit streams (8.192MHz)

CASBRD (Output) – carries CAS signaling for four T1/E1 receive streams (8.192MHz)

CCSBTD (Input) – carries CCS signaling for four T1/E1 transmit streams (8.192MHz)

CCSBRD (Output) – carries CCS signaling for four T1/E1 receive streams (8.192MHz). Note that this is the same pin as MVBRD, so it is not possible to have CCSBRD and MVBRD signals at the same time.

Q39) Can multiple COMET-QUAD devices share a single H-MVIP bus?

No. When using the COMET-QUAD's H-MVIP pins, the multiplexing/demultiplexing function is performed internal to the device and hence can only access the T1/E1 links local to the device.

Q40) What are the details of the COMET-QUAD CHI (Concentration Highway Interface) system backplane interface?

Framers from Lucent Technologies Microelectronics Group (formerly AT&T Microelectronics) have a flexible backplane interface that has some differences from the MVIP bus but generally serves the same purpose of frame aligning multiple ports to allow easy cross-connection of DS0 timeslots.

The specification for the CHI bus can be downloaded from Lucent's ISDN documentation Web page at http://www.lucent.com/micro/isdn/isdndoc.html.

The COMET-QUAD system backplane interface is fully compatible with the CHI bus.

Q41) How is the fractional NxDS0 interface on the COMET-QUAD used?

Some applications of T1, E1, and J1 only use a fraction of the payload available, for services termed "fractional." These fractional payloads are typically allocated in integral multiples of DS0's, for Nx64kbit/s service or Nx56kbit/s service.

The COMET-QUAD supports fractional services by providing a NxDS0 Backplane System Interface mode. In this mode, the COMET-QUAD will gap the backplane clocks during unused payload and overhead cycles, leaving the backplane clocks toggling only during desired payload timeslots. This enables direct connection to external serial controllers.

The NxDS0 mode in the COMET-QUAD is enabled using Transmit/Receive Backplane Nx64 kbit/s Mode Selection in the registers 030h and 040h respectively.

4.7 Layout and Board Design Questions

Q42) Is special treatment of the power supply necessary for the COMET-QUAD?

The COMET-QUAD contains sensitive analog circuitry (e.g. phase-locked loops, equalizers, D/A Converters and A/D Converters) and therefore it is necessary to ensure that the COMET-QUAD power supply is noise free and capable of providing required switching current.

The necessary power-filtering is provided in the COMET-QUAD Evaluator Board Design document (PMC-1991237). These filters have been thoroughly tested by PMC-Sierra, and must be followed. PMC-Sierra cannot guarantee proper operation if there is any deviation from the specified component values.

Q43) How do I ensure good signal integrity in my COMET-QUAD design?

The most common signal integrity issue in high-speed digital designs is signal reflection due to impedance mismatch. When the propagation time of a signal on an interconnection exceeds the edge rate, a feedback delay is created in the output driver causing an underdamped step response. This is seen as “ringing” on the signal edges, with corresponding overshoot and undershoot.

PMC-Sierra product inputs typically have an absolute maximum voltage rating of a diode drop (0.3V in case of COMET-QUAD) above the power supply voltage and an absolute minimum voltage rating of a diode drop below ground. If these ratings are exceeded then the COMET-QUAD is not guaranteed to operate correctly, in fact damage to the COMET-QUAD may occur. Therefore it is essential that signal reflections be minimized so that the overshoot and undershoot do not violate these ratings.

Signal reflections are minimized by ensuring that load impedance are matched to the characteristic impedance of the interconnection. There are many techniques for doing this, and the topic is beyond the scope of this document. The way that theCOMET-QUAD Evaluator Board accomplishes this impedance matching is by placing series termination (series resistors) on some of its connections. The values chosen for these resistors are specific to this board, so therefore cannot be copied.

Q44) What oscillator manufacturers does PMC-Sierra recommend for use with the COMET-QUAD?

Any reputable crystal oscillator manufacturer should be able to provide the required 1.544 MHz or 2.048 MHz oscillator (with the tolerance +/- 100 ppm or less) to source the COMET-QUAD XCLK input signal. Since this is a non-standard frequency, they will generally have to be custom cut. The 1100 series of custom-cut crystal oscillators is suitable and available from most manufacturers. The oscillator should output TTL (or TTL-compatible) levels.

Some manufacturers which PMC-Sierra has used in-house are: Champion Technologies, Connor-Winfield, Ecliptek Corporation, and Fox Corporation. These should be available from most electronic component distributors.

Custom cut oscillators can have very long lead times (16 weeks typical) so they should be ordered well in advance of when they will be needed.

Q45) Do the COMET-QUAD input clocks need to come from on-board oscillators?

No. As long as the input clocks to the COMET-QUAD meet the timing requirements specified in the COMET-QUAD data sheet, then it does not matter if the clock signal comes from an oscillator, a PLL, another logic device, or some other source.

In particular, clock inputs must meet:

set-up and hold requirements with respect to the clock;

duty cycle requirements;

frequency tolerance (in parts per million);

jitter requirement (jitter free XCLK).

Q46) Can the COMET-QUAD be damaged if the XCLK does not meet the minimum frequency requirement?

No. XCLK is a nominally jitter free clock at 1.544 MHz in T1 mode and 2.048 MHz in E1 mode. Deviations from above mentioned frequencies can cause incorrect operation of COMET-QUAD but cannot damage the device.

Q47) If I decide to use the recovered clock as my reference for the transmit path, and want to switch to the XCLK crystal reference clock automatically when LOS or ALOS condition occurs, what should I do?

- tie the RSYNC output pin to the CTCLK input pin

- choose which one of the four ports the RSYNC recovered timing comes from. This is specified with the RSYNC_SEL[1:0] bits in register 0BBh.

- choose CTCLK as the source of the transmit timing source for however many ports you wish. This is done by setting the PLLREF[1:0] bits in registers Q06h, to '11'. Note that all the selected ports will be have identical timing, which is synchronous to the RSYNC pin.

- ensure that 'RSYNC_MEM' (registers Q03h) is logic zero, so that RSYNC will switch to XCLK during LOS/ALOS conditions.

- use the RSYNC_ALOSB bit (registers Q00h) to specify whether LOS or ALOS will trigger RSYNC to switch to XCLK.Note: RSYNC is **always** jitter-attenuated, regardless of the setting of RJATBYP.

NOTES

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