Precision Six Supply Monitor

FEATURES

- **Ultralow Voltage Reset: V_{CC} = 0.5V Guaranteed***
- **Monitors Six Inputs Simultaneously: 5V, 3.3V, 2.5V, 1.8V, ADJ1, ADJ2 (LTC2908-A1) 3.3V, 2.5V, 1.8V, 1.5V, ADJ1, ADJ2 (LTC2908-B1)**
- **Guaranteed Threshold Accuracy: ±1.5% of Monitored Voltage Over Temperature**
- **Internal V_{CC} Auto Select**
- Power Supply Glitch Immunity
- 200ms Reset Time Delay
- Active Low Open-Drain $\overline{RST}$ Output
- Low Profile (1mm) SOT-23 (ThinSOT™) and Plastic (2mm × 3mm) DFN Packages

APPLICATIONS

- Network Servers
- Wireless Base Stations
- Optical Networking Systems
- Mulitvoltage Systems
- Desktop and Notebook Computers
- Handheld Devices

DESCRIPTION

The LTC®2908 is a six supply monitor for systems with a large number of supply voltages that require a precise and compact solution. The common reset output remains low until all six inputs have been in compliance for 200ms.

The LTC2908 features a tight 1.5% threshold accuracy over the entire operating temperature range (–40°C to 85°C) and glitch immunity to ensure reliable reset operation without false triggering. The open-drain $\overline{RST}$ output state is guaranteed to be in the correct state as long as V1 and/or V2 is 0.5V or greater.

The LTC2908 also features two adjustable inputs with a nominal threshold level at 0.5V. This product provides a precise, space-conscious, micropower and general purpose solution for any kind of system requiring supply monitors.

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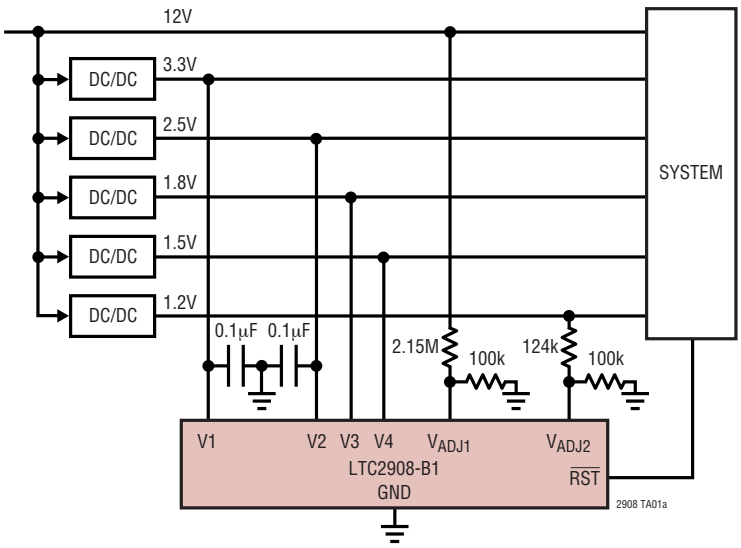
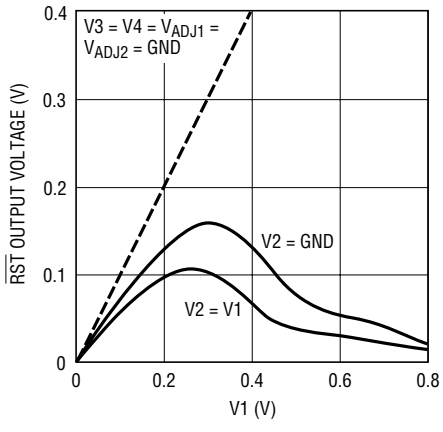
ThinSOT is a trademark of Linear Technology Corporation.
*Patent pending.

TYPICAL APPLICATION

Six Supply Monitor with 5% Tolerance (12V, 3.3V, 2.5V, 1.8V, 1.5V, 1.2V)



$\overline{RST}$ Output Voltage vs V1 with 10k Pull-Up Resistor to V1



ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

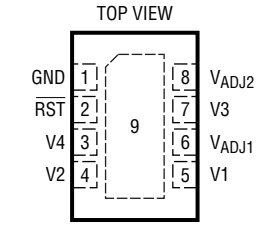
Terminal Voltages
- V1, V2, V3, V4 ..... –0.3V to 7V
- V_{ADJ1}, V_{ADJ2} ..... –0.3V to (V_{CC} + 0.3V)
- $\overline{RST}$ ..... –0.3V to 7V

Operating Temperature Range
- LTC2908C-A1/LTC2908C-B1 ..... 0°C to 70°C
- LTC2908I-A1/LTC2908I-B1 ..... –40°C to 85°C

Storage Temperature Range
- DFN Package .....–65°C to 125°C
- TSOT-23 Package .....–65°C to 150°C

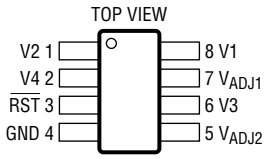
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



DDB8 PACKAGE
8-LEAD (3mm × 2mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 76°C/W
EXPOSED PAD (PIN 9)
(PCB CONNECTION OPTIONAL)

ORDER PART NUMBER
LTC2908CDDB-A1 LTC2908IDDB-A1 LTC2908CDDB-B1 LTC2908IDDB-B1
DDB8 PART MARKING
LBFD LBFF LBFG LBFH



TS8 PACKAGE
8-LEAD PLASTIC TSOT-23
T_{JMAX} = 125°C, θ_{JA} = 250°C/W

ORDER PART NUMBER
LTC2908CTS8-A1 LTC2908ITS8-A1 LTC2908CTS8-B1 LTC2908ITS8-B1
TS8 PART MARKING
LTBFJ LTBFK LTBFM LTBFN

Consult factory for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

(LTC2908-A1) The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{CC} = 5V, unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{RT50}	5V, 5% Reset Threshold	V1 Input Threshold	●	4.600	4.675	4.750	V
V_{RT33}	3.3V, 5% Reset Threshold	V2 Input Threshold	●	3.036	3.086	3.135	V
V_{RT25}	2.5V, 5% Reset Threshold	V3 Input Threshold	●	2.300	2.338	2.375	V
V_{RT18}	1.8V, 5% Reset Threshold	V4 Input Threshold	●	1.656	1.683	1.710	V
V_{RTADJ}	ADJ, 5% Reset Threshold	V_{ADJ1}, V_{ADJ2} Input Threshold	●	0.492	0.500	0.508	V

(LTC2908-B1) The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{CC} = 3.3V, unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{RT33}	3.3V, 5% Reset Threshold	V1 Input Threshold	●	3.036	3.086	3.135	V
V_{RT25}	2.5V, 5% Reset Threshold	V2 Input Threshold	●	2.300	2.338	2.375	V
V_{RT18}	1.8V, 5% Reset Threshold	V3 Input Threshold	●	1.656	1.683	1.710	V
V_{RT15}	1.5V, 5% Reset Threshold	V4 Input Threshold	●	1.380	1.403	1.425	V
V_{RTADJ}	ADJ, 5% Reset Threshold	V_{ADJ1}, V_{ADJ2} Input Threshold	●	0.492	0.500	0.508	V

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{CC} = 5V for the LT2908-A1 and V_{CC} = 3.3V for the LTC2908-B1, unless otherwise noted. (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Internal Operating Voltage	$\overline{RST}$ in Correct Logic State	●	0.5		6	V
I_{V1}	V1 Input Current	V1 = 5.0V (LTC2908-A1) (Note 4) V1 = 3.3V (LTC2908-B1)	● ●		26 24	50 50	µA µA
I_{V2}	V2 Input Current	V2 = 3.3V (LTC2908-A1) (Note 4) V2 = 2.5V (LTC2908-B1)	● ●		10 8	20 20	µA µA
I_{V3}	V3 Input Current	V3 = 2.5V (LTC2908-A1) V3 = 1.8V (LTC2908-B1)	● ●		2 2	5 5	µA µA
I_{V4}	V4 Input Current	V4 = 1.8V (LTC2908-A1) V4 = 1.5V (LTC2908-B1)	● ●		2 2	5 5	µA µA
I_{VADJ}	V_{ADJ1}, V_{ADJ2} Input Current	V_{ADJ1} = V_{ADJ2} = 0.55V	●			±15	nA
$t_{\overline{RST}}$	Reset Time-Out Period		●	160	200	260	ms
t_{UV}	V_X Undervoltage Detect to $\overline{RST}$ or RST	V_X Less Than Reset Threshold V_{RTX} by More Than 1%			250		µs
V_{OH}	Output Voltage High $\overline{RST}$ (Note 5)	$I_{\overline{RST}}$ = –1µA, V_{CC} = 5V (LTC2908-A1) I_{RST} = –1µA, V_{CC} = 3.3V (LTC2908-B1)	● ●	V_{CC} – 1.5 V_{CC} – 1.0			V V
V_{OL}	Output Voltage Low $\overline{RST}$	V_{CC} = 0.5V, $I_{\overline{RST}}$ = 5µA V_{CC} = 1.0V, $I_{\overline{RST}}$ = 100µA V_{CC} = 3.0V, $I_{\overline{RST}}$ = 2500µA	● ● ●		0.01 0.01 0.10	0.15 0.15 0.30	V V V

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The greater of V1, V2 is the internal supply voltage (V_{CC}).

Note 3: All currents into pins are positive; all voltages are referenced to GND unless otherwise noted.

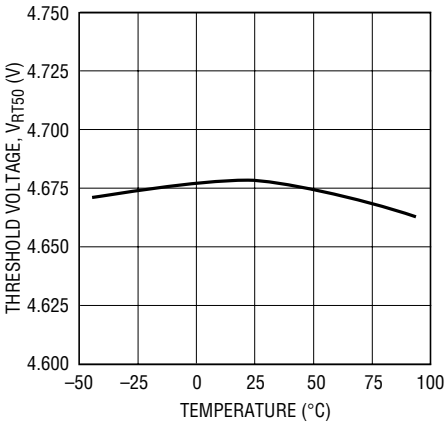
Note 4: Under typical operating conditions, most of the quiescent current is drawn from the V1 input. When V2 exceeds V1, V2 supplies most of the quiescent current.

Note 5: The output pin $\overline{RST}$ has an internal pull-up to V_{CC} of typically 6µA. However, an external pull-up resistor may be used when a faster rise time is required or for V_{OH} voltages greater than V_{CC}.

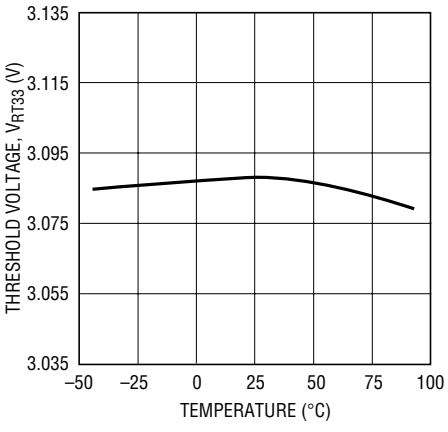
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at T_A = 25°C unless otherwise noted.

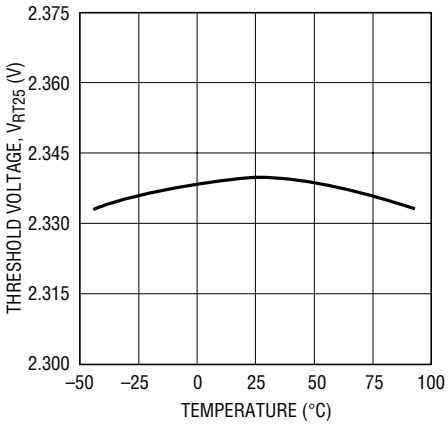
5V Threshold Voltage vs Temperature



3.3V Threshold Voltage vs Temperature



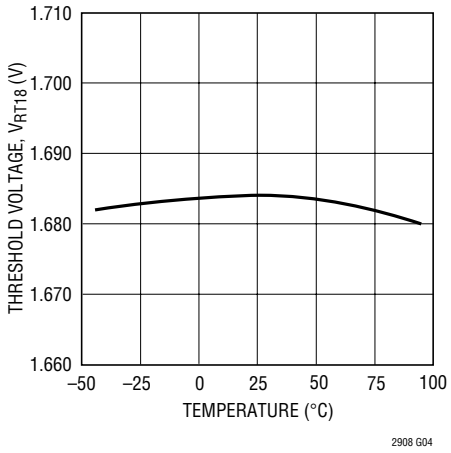
2.5V Threshold Voltage vs Temperature



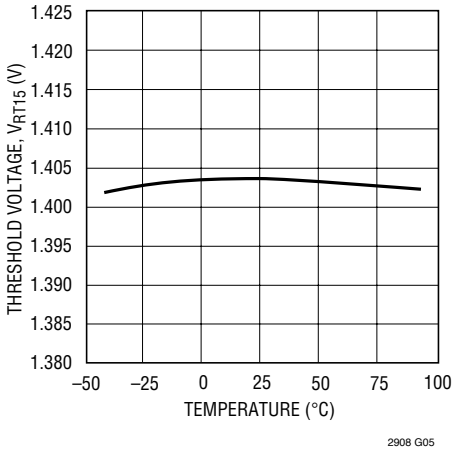
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at T_A = 25°C unless otherwise noted.

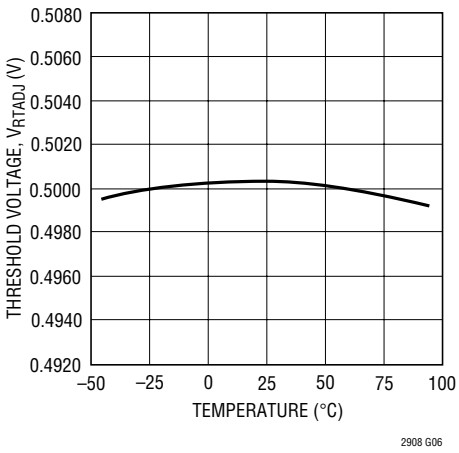
1.8V Threshold Voltage vs Temperature



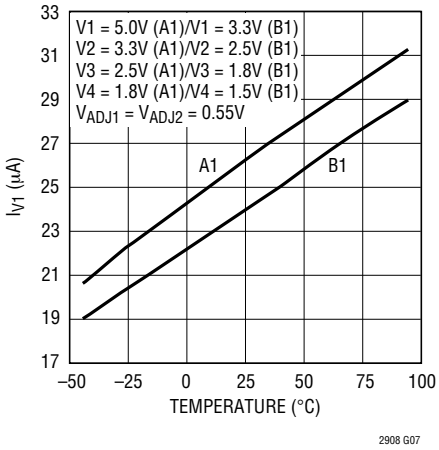
1.5V Threshold Voltage vs Temperature



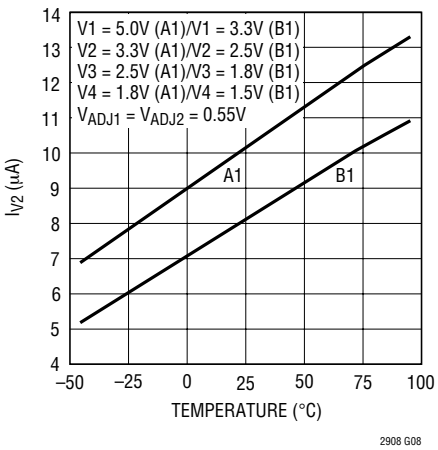
ADJ Threshold Voltage vs Temperature



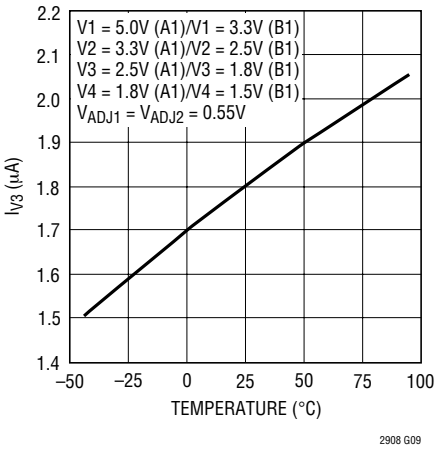
I_{V1} vs Temperature



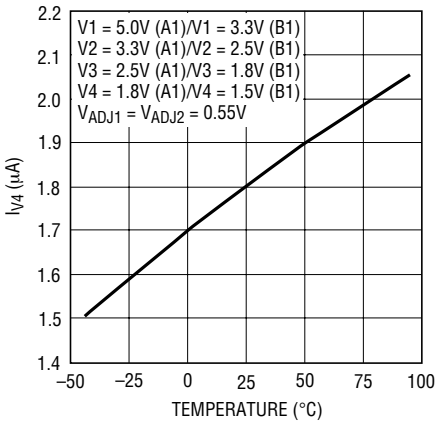
I_{V2} vs Temperature



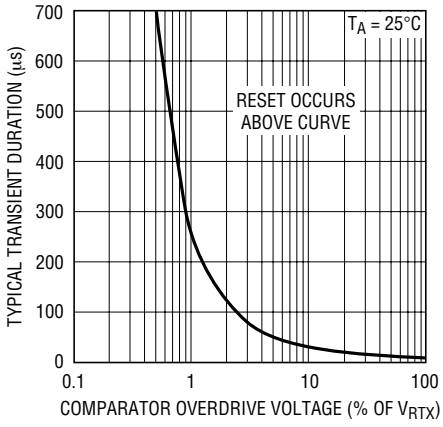
I_{V3} vs Temperature



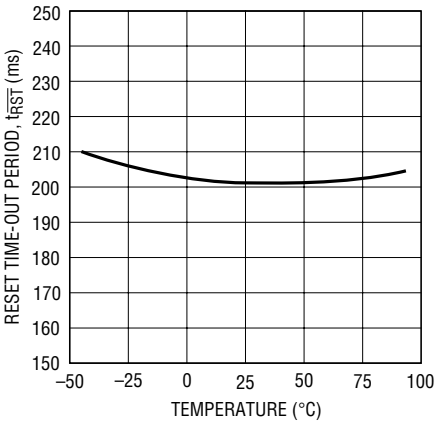
I_{V4} vs Temperature



Typical Transient Duration vs Comparator Overdrive



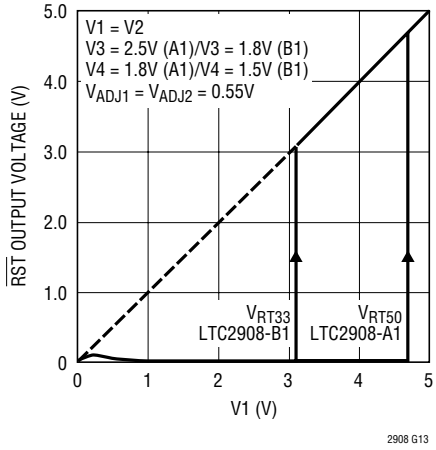
Reset Time-Out Period ($t_{\overline{RST}}$) vs Temperature



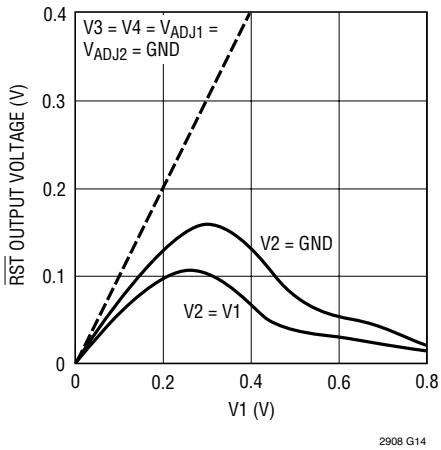
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at T_A = 25°C unless otherwise noted.

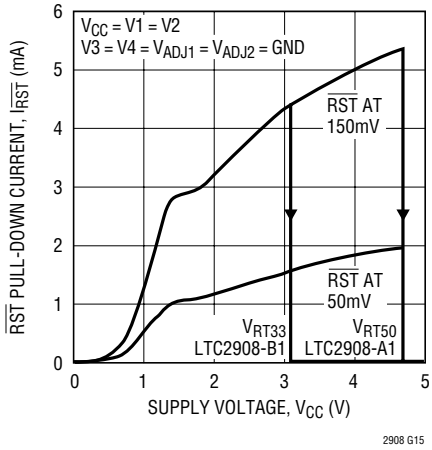
$\overline{RST}$ Output Voltage vs V1 with 10k Pull-Up Resistor to V1



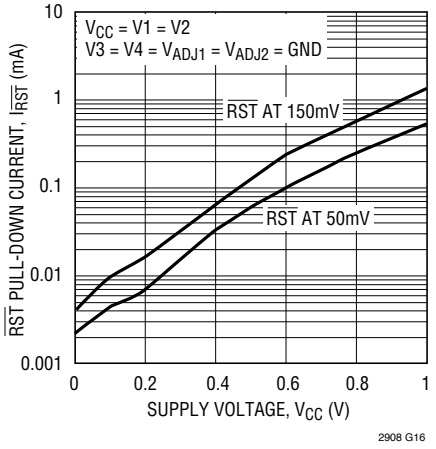
$\overline{RST}$ Output Voltage vs V1 with 10k Pull-Up Resistor to V1



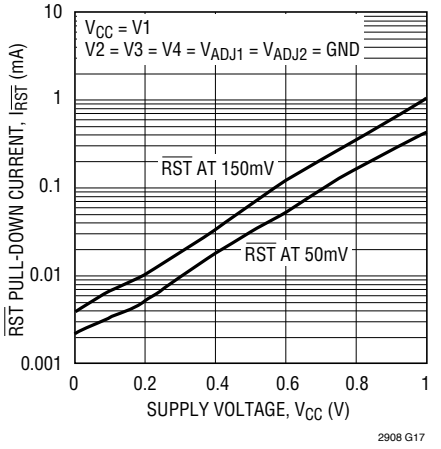
$\overline{RST}$ Pull-Down Current ($I_{\overline{RST}}$) vs Supply Voltage (V_{CC})



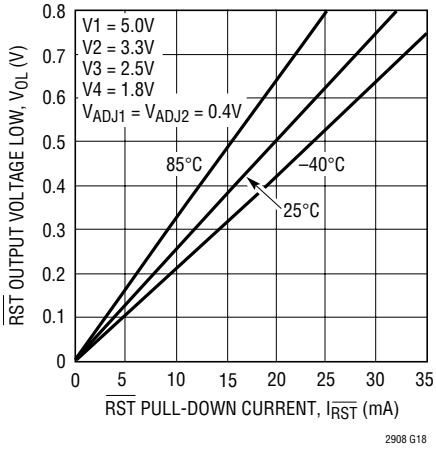
$\overline{RST}$ Pull-Down Current ($I_{\overline{RST}}$) vs Supply Voltage (V_{CC}) with Dual Channel Supply



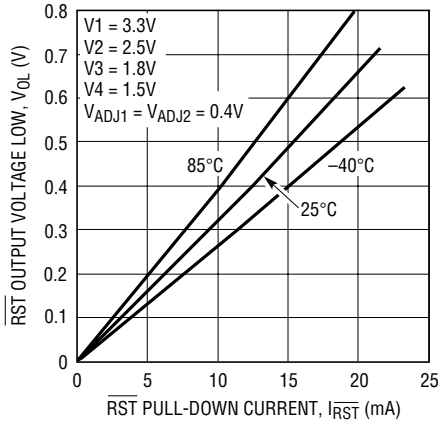
$\overline{RST}$ Pull-Down Current ($I_{\overline{RST}}$) vs Supply Voltage (V_{CC}) with Single Channel Supply



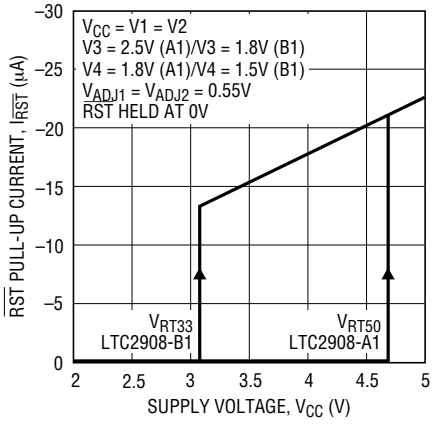
$\overline{RST}$ Output Voltage Low (V_{OL}) vs $\overline{RST}$ Pull-Down Current ($I_{\overline{RST}}$) LTC2908-A1



$\overline{RST}$ Output Voltage Low (V_{OL}) vs $\overline{RST}$ Pull-Down Current ($I_{\overline{RST}}$) LTC2908-B1

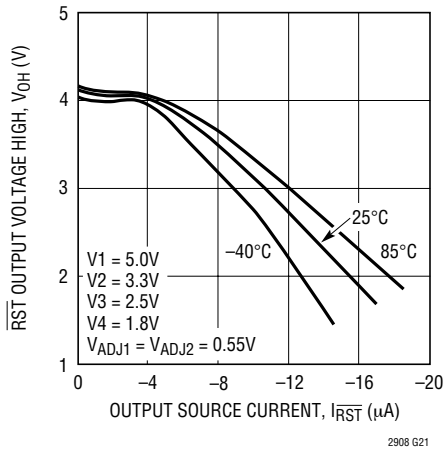


$\overline{RST}$ Pull-Up Current ($I_{\overline{RST}}$) vs Supply Voltage (V_{CC})

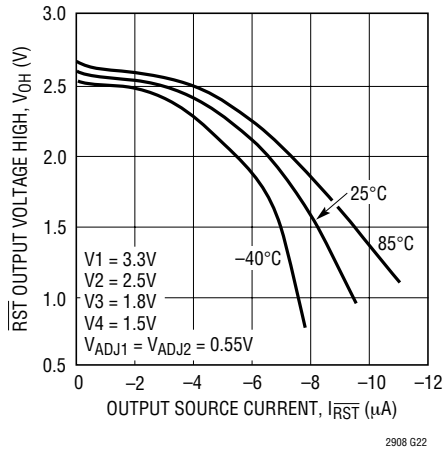


TYPICAL PERFORMANCE CHARACTERISTICS

$\overline{RST}$ Output Voltage High (V_{OH}) vs $\overline{RST}$ Output Source Current ($I_{\overline{RST}}$) LTC2908-A1



$\overline{RST}$ Output Voltage High (V_{OH}) vs $\overline{RST}$ Output Source Current ($I_{\overline{RST}}$) LTC2908-B1



PIN FUNCTIONS (TS8 Package/DDB8 Package)

V2 (Pin 1/Pin 4): Voltage Input 2. The greater of V1, V2 is also the internal V_{CC}. The operating voltage on this pin shall not exceed 6V. When in normal operation (V1 > V2), this pin draws approximately 8µA. When this pin is acting as the V_{CC} (V2 > V1), this pin draws an additional 15µA. Bypass this pin to ground with a 0.1µF (or greater) capacitor.

V4 (Pin 2/Pin 3): Voltage Input 4.

$\overline{RST}$ (Pin 3/Pin 2): Reset Logic Output. Pulls low when any voltage input is below the reset threshold and is held low for 200ms after all voltage inputs are above threshold. This pin has a weak pull-up to V_{CC} and may be pulled above V_{CC} using an external pull-up.

GND (Pin 4/Pin 1): Device Ground.

V_{ADJ2} (Pin 5/Pin 8): Adjustable Voltage Input 2. See Table 1 for recommended ADJ resistors values.

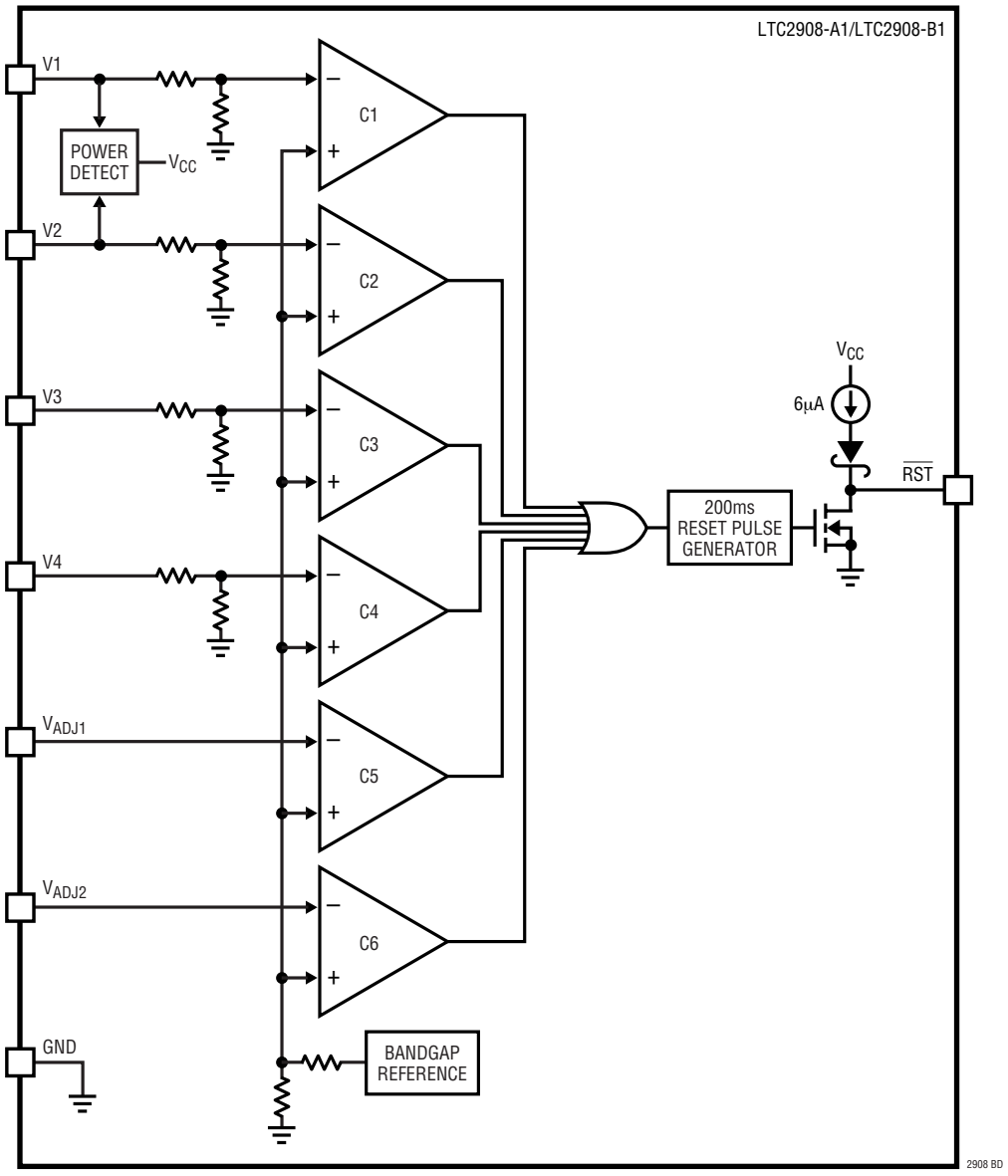
V3 (Pin 6/Pin 7): Voltage Input 3.

V_{ADJ1} (Pin 7/Pin 6): Adjustable Voltage Input 1. See Table 1 for recommended ADJ resistors values.

V1 (Pin 8/Pin 5): Voltage Input 1. The greater of V1, V2 is also the internal V_{CC}. The operating voltage on this pin shall not exceed 6V. When in normal operation (V1 > V2), this pin draws approximately 21µA. When this pin is not acting as the V_{CC} (V2 > V1), this pin draws approximately 8µA. Bypass this pin to ground with a 0.1µF (or greater) capacitor.

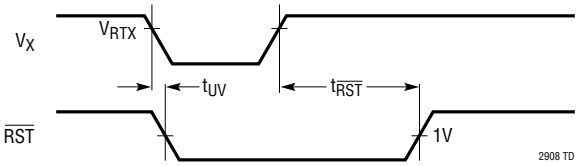
Exposed Pad (Pin 9, DDB8 Only): Exposed Pad may be left open or connected to device ground.

BLOCK DIAGRAM



TIMING DIAGRAM

V_X Monitor Timing



APPLICATIONS INFORMATION

Supply Monitoring

The LTC2908 is a low power, high accuracy, six input supply monitoring circuit with two adjustable inputs. The reset delay is set to a nominal of 200ms with an internal capacitor, eliminating the need for an external timing capacitor.

All input voltages must be above predetermined thresholds for the reset not to be invoked. The LTC2908 asserts the reset output during power-up, power-down and brown-out conditions on any one of the voltage inputs.

Ultralow Voltage Pull-Down on $\overline{RST}$

The LTC2908 issues a logic low on the $\overline{RST}$ output when any one of the inputs falls below its threshold. Ideally, the $\overline{RST}$ logic output would remain low with the input supply voltage down to zero volts. Most supervisors lack pull-down capability below 1V.

The LTC2908 power supply supervisor incorporates a novel low voltage pull-down circuit that can hold the $\overline{RST}$ line low with as little as 200mV of input supply voltage on V1 and/or V2 (see Figures 1 and 2). The pull-down circuit helps maintain a low impedance path to ground, reducing the risk of the $\overline{RST}$ node from floating to an indeterminate voltage.

Such an indeterminate voltage may trigger external logic causing erroneous reset operation(s). Furthermore, a mid-scale voltage level could cause external circuits to operate in the middle of their voltage transfer characteristic, consuming more quiescent current than normal. These conditions could cause serious system reliability problems.

Power-Up

During power-up, $\overline{RST}$ starts asserting low as soon as there is at least 200mV on V1 and/or V2. The $\overline{RST}$ pull-down capability is a function of V1 and V2 as shown in the Typical Performance Characteristics.

The greater of V1, V2 is the internal supply voltage (V_{CC}) that powers the other internal circuitry. Once all the V_X inputs rise above their thresholds, an internal timer is started. After the internal timer counts a 200ms delay time, $\overline{RST}$ weakly pulls high to V_{CC}.

Power-Down

On power-down, once any of the V_X inputs drop below their threshold, $\overline{RST}$ asserts logic low. V_{CC} of at least 0.5V guarantees a logic low of 0.15V at $\overline{RST}$.

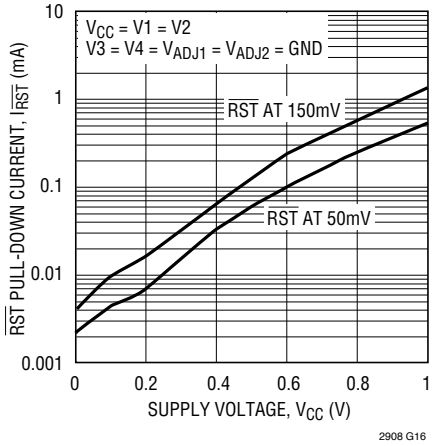


Figure 1. $\overline{RST}$ Pull-Down Current ($I_{\overline{RST}}$) vs Supply Voltage (V_{CC}) with Dual Channel Supply

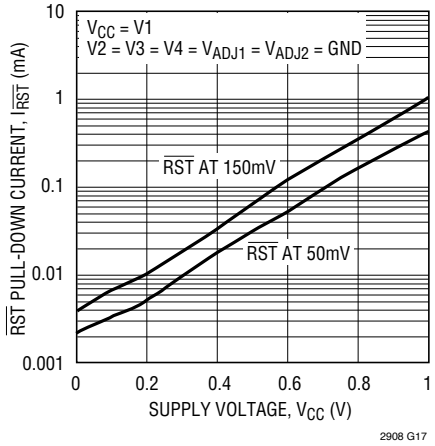


Figure 2. $\overline{RST}$ Pull-Down Current ($I_{\overline{RST}}$) vs Supply Voltage (V_{CC}) with Single Channel Supply

APPLICATIONS INFORMATION

Adjustable Input

The noninverting input on the V_{ADJ} comparator is set to 0.5V. And the high impedance inverting input directly ties to the V_{ADJ} pin.

In a typical application, this pin connects to a tap point on an external resistive divider between the positive voltage being monitored and ground. The following formula derives the value of the R1 resistor in the divider from a particular value of R2 and the desired trip voltage:

$$R1 = \left(\frac{V_{TRIP}}{0.5V} - 1\right) R2$$

R2 = 100k is recommended. Table 1 shows suggested 1% resistor values for various adjustable applications and their corresponding trip thresholds.

Table 1. Suggested 1% Resistor Values for the V_{ADJ} Inputs

V_{SUPPLY} (V)	V_{TRIP} (V)	R1 (kΩ)	R2 (kΩ)
12	11.25	2150	100
10	9.4	1780	100
8	7.5	1400	100
7.5	7	1300	100
6	5.6	1020	100
5	4.725	845	100
3.3	3.055	511	100
3	2.82	464	100
2.5	2.325	365	100
1.8	1.685	237	100
1.5	1.410	182	100
1.2	1.120	124	100
1.0	0.933	86.6	100
0.9	0.840	68.1	100
0.8	0.750	49.9	100
0.7	0.655	30.9	100
0.6	0.561	12.1	100

If an application has less than six supply voltages, the unused supervisor inputs should be tied to the closest higher supply voltage available.

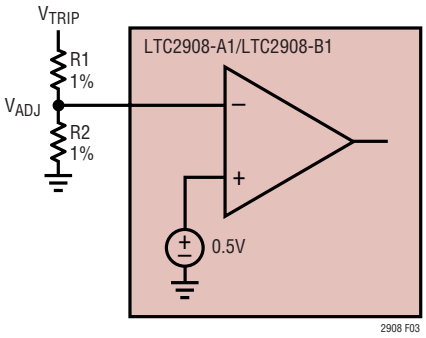


Figure 3. Setting the Adjustable Trip Point

Threshold Accuracy

Specifying system voltage margin for worst-case operation requires the consideration of three factors: power supply tolerance, IC supply voltage tolerance and supervisor reset threshold accuracy. Highly accurate supervisors ease the design challenge by decreasing the overall voltage margin required for reliable system operation. Consider a 5V system with a ±5% power supply tolerance band.

System ICs powered by this supply must operate reliably within this band (and a little more, as explained below). The bottom of the supply tolerance band, at 4.75V (5% below 5V), is the exact voltage at which a perfectly accurate supervisor generates a reset (see Figure 4). Such a perfectly accurate supervisor does not exist—the actual reset threshold may vary over a specified band (±1.5% for the LTC2908 supervisors). Figure 5 shows the typical relative threshold accuracy for all six inputs over temperature.

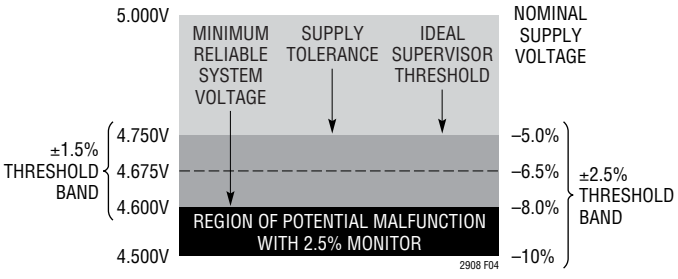


Figure 4. Threshold Band Diagram

APPLICATIONS INFORMATION

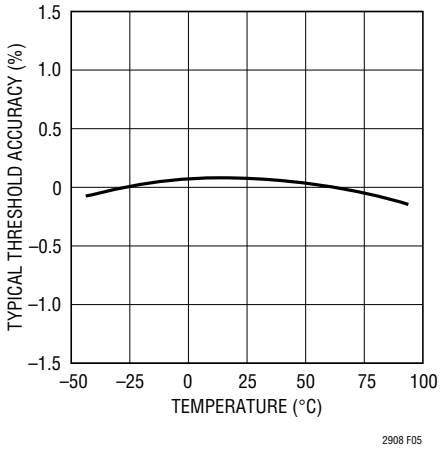


Figure 5. Typical Threshold Accuracy vs Temperature

With this variation of reset threshold in mind, the nominal reset threshold of the supervisor resides below the minimum supply voltage; just enough so that the reset threshold band and the power supply tolerance bands do not overlap. If the two bands overlap, the supervisor could generate a false or nuisance reset when the power supply remains within its specified tolerance band (for example at 4.8V).

Adding half of the reset threshold accuracy spread (1.5%) to the ideal 5% thresholds puts the LTC2908 thresholds at 6.5% (typ) below the nominal input voltage. For example, the 5V typical threshold is 4.675V, or 75mV below the ideal threshold of 4.750V. The guaranteed threshold lies in the band between 4.600V (8% below 5V) and 4.750V (5% below 5V) over temperature.

The powered system must work reliably down to the lowest voltage in the threshold band or risk malfunction before the reset line falls. In the 5V example, using the 1.5% accurate supervisor, the system ICs must work down to 4.60V (8% below 5V). System ICs working with a ±2.5% accurate supervisor must operate down to 4.50V (10% below 5V), increasing the required system voltage margin and the probability of system malfunction.

In any supervisory application, supply noise riding on the monitored DC voltage can cause spurious resets, particularly when the monitored voltage is near the reset threshold. A less desirable but common solution to this problem is to introduce hysteresis around the nominal threshold. Notice however, this hysteresis introduces an error term in the threshold accuracy. Therefore, a ±2.5% accurate monitor with ±1% hysteresis is equivalent to a ±3.5% monitor with no hysteresis.

Therefore, the LTC2908 takes a different approach to solving this problem of supply noise causing spurious reset. The first line of defense against this spurious reset is a first order lowpass filter at the output of the comparators. Therefore, each comparator output is integrated over time before triggering the output logic. Therefore, any kind of transient at the input of the comparator needs to be of sufficient magnitude and duration before it can trigger a change in the output logic.

The second line of defense is the 200ms delay time t_{RST}. This delay eliminates the effect of any supply noise, whose frequency is above 1/200ms = 5Hz, on the $\overline{RST}$ output.

When any one of the supply voltages drops below its threshold, the $\overline{RST}$ pin asserts low. When the supply recovers above its threshold, the reset-pulse-generator timer starts counting.

If all the supplies remain above their corresponding threshold when the timer finishes counting, the $\overline{RST}$ pin weakly pulls high. However, if any of the supplies falls below its threshold any time during the period when the timer is still counting, the timer resets and it starts fresh when all the supplies rise above their corresponding threshold.

Note that this second line of defense is only effective for a rising supply and does not affect the sensitivity of the system to a falling supply. Therefore, the first line of defense that works for both cases of rising and falling is necessary. These two approaches prevent spurious reset caused by supply noise without sacrificing the threshold accuracy.

Although all six comparators for the six inputs have built-in glitch filtering, use bypass capacitors on the V1 and V2 inputs because the greater of V1 or V2 supplies the V_{CC} for the part (a 0.1µF ceramic capacitor satisfies most applications). Apply filter capacitors on the V3, V4, V_{ADJ1} and V_{ADJ2} inputs in extremely noisy situations.

APPLICATIONS INFORMATION

$\overline{RST}$ Output Characteristics

The DC characteristics of the $\overline{RST}$ pull-up and pull-down strength are shown in the Typical Performance Characteristics section. The $\overline{RST}$ output has a weak internal pull-up to V_{CC} = Max(V1, V2) and a strong pull-down to ground.

The weak pull-up and strong pull-down arrangement allows this pin to have open-drain behavior while possessing several other beneficial characteristics.

The weak pull-up eliminates the need for external pull-up resistors when the rise time on these pins is not critical. On the other hand, the open-drain $\overline{RST}$ configuration allows for wired-OR connections and can be useful when more than one signal needs to pull down on the $\overline{RST}$ line.

As noted in the discussion of power-up and power-down, the circuits that drive $\overline{RST}$ are powered by V_{CC}. During fault condition, V_{CC} of at least 0.5V guarantees a maximum V_{OL} = 0.15V at $\overline{RST}$.

Output Rise and Fall Time Estimation

The following formula estimates the output fall time (90% to 10%) for a particular external load capacitance (C_{LOAD}):

$$t_{FALL} \approx 2.2 \bullet R_{PD} \bullet C_{LOAD}$$

where R_{PD} is the on-resistance of the internal pull-down transistor estimated to be typically 40Ω at room temperature (25°C) and C_{LOAD} is the external load capacitance on the pin. Assuming a 150pF load capacitance, the fall time is about 13ns.

The rise time on the $\overline{RST}$ pin is limited by a weak internal pull-up current source to V_{CC}. The following formula estimates the output rise time (10% to 90%) at the $\overline{RST}$ pin:

$$t_{RISE} \approx 2.2 \bullet R_{PU} \bullet C_{LOAD}$$

where R_{PU} is the on-resistance of the pull-up transistor. Notice that this pull-up transistor is modeled as a 6μA current source in the Block Diagram as a typical representation.

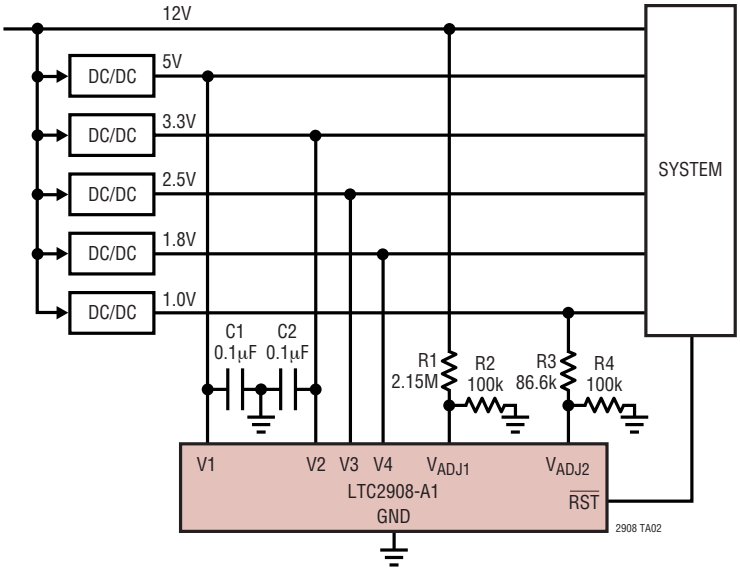
The on-resistance as a function of the V_{CC} = Max(V1, V2) voltage (for V_{CC} > 1V) at room temperature is estimated as follows:

$$R_{PU} = \frac{6 \bullet 10^5}{MAX(V1,V2) - 1V}\ \Omega$$

At V_{CC} = 3.3V, R_{PU} is about 260k. Using 150pF for load capacitance, the rise time is 86μs. A smaller external pull-up resistor may be used if the output needs to pull up faster and/or to a higher voltage. For example, the rise time reduces to 3.3μs for a 150pF load capacitance when using a 10k pull-up resistor.

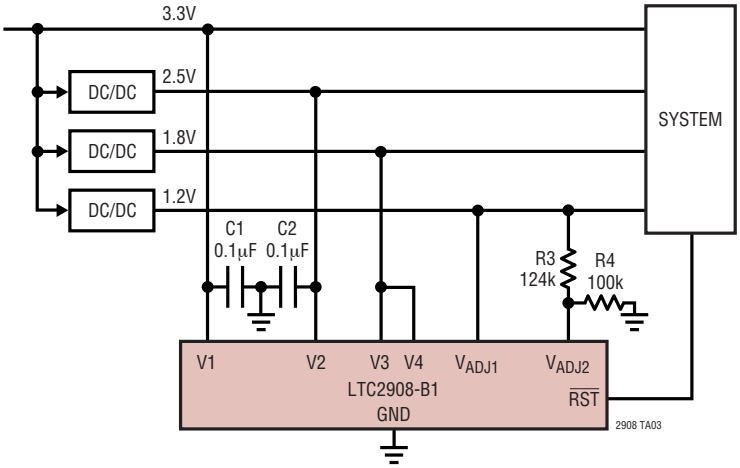
TYPICAL APPLICATIONS

Six Supply Monitor, 5% Tolerance, 12V, 5V, 3.3V, 2.5V, 1.8V, 1V



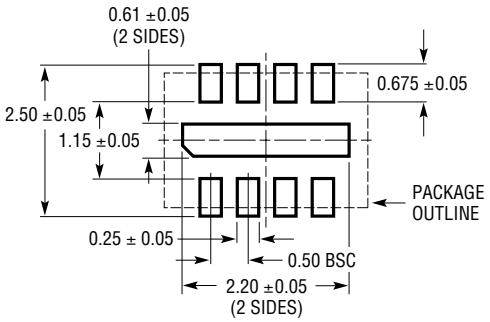
TYPICAL APPLICATIONS

Quad Supply Monitor with One Adjustable Input, 5% Tolerance, 3.3V, 2.5V, 1.8V, 1.2V

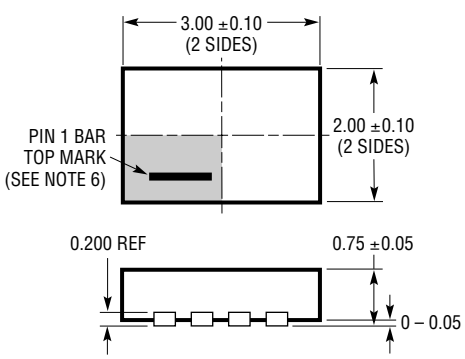


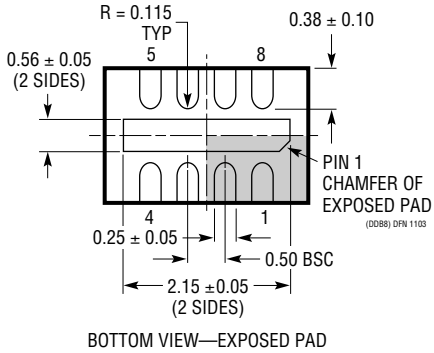
PACKAGE DESCRIPTION

DDB Package
8-Lead Plastic DFN (3mm × 2mm)
(Reference LTC DWG # 05-08-1702)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



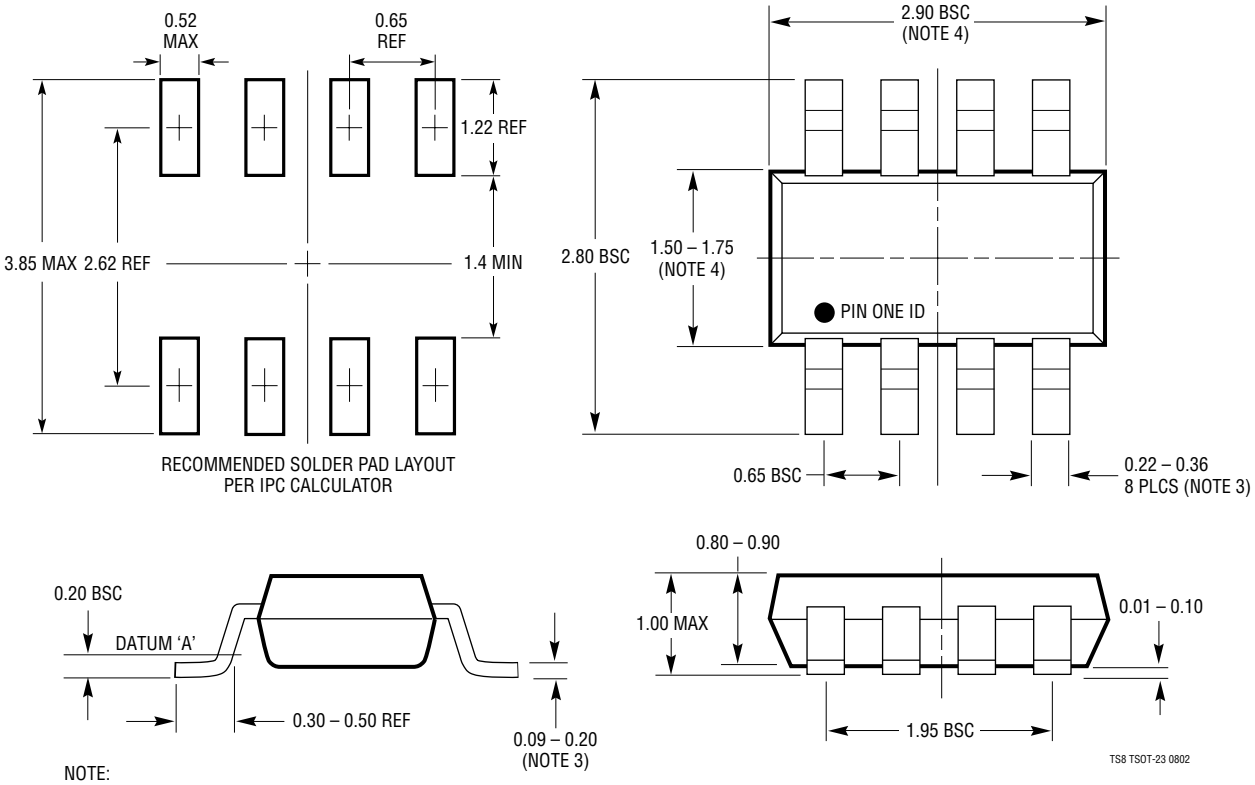


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO VERSION (WECD-1) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

TS8 Package
8-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1637)

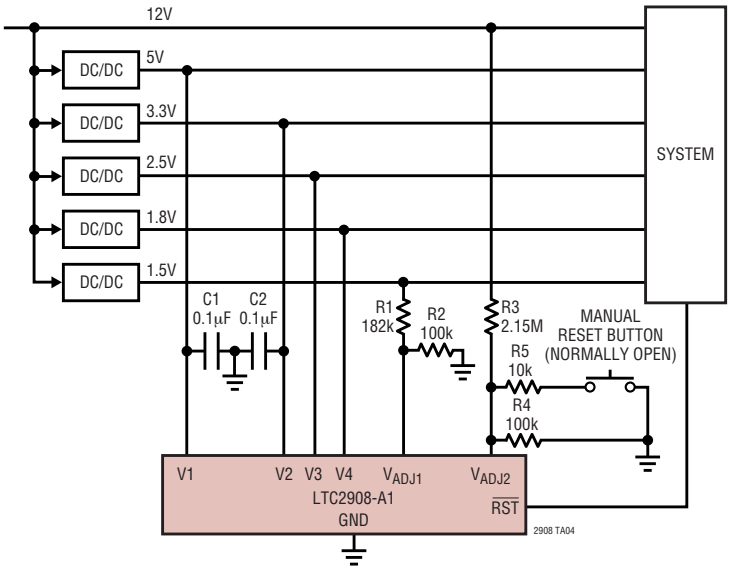


NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

Six Supply Monitor with Manual Reset Button, 5% Tolerance, 12V, 5V, 3.3V, 2.5V, 1.8V, 1.5V



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC690	5V Supply Monitor, Watchdog Timer and Battery Backup	4.65 Threshold
LTC694-3.3	3.3V Supply Monitor, Watchdog Timer and Battery Backup	2.9V Threshold
LTC699	5V Supply Monitor and Watchdog Timer	4.65 Threshold
LTC1232	5V Supply Monitor, Watchdog Timer and Pushbutton Reset	4.37V/4.62V Threshold
LTC1326/LTC1326-2.5	Micropower Precision Triple Supply Monitor for 5V/2.5V, 3.3V and ADJ	4.725V, 3.118V, 1V Threshold (±0.75%)
LTC1536	Precision Triple Supply Monitor for PCI Applications	Meets PCI t_{FAIL} Timing Specifications
LTC1726-2.5/LTC1726-5	Micropower Triple Supply Monitor for 2.5V/5V, 3.3V and ADJ	Adjustable $\overline{\text{RESET}}$ and Watchdog Time-Outs
LTC1727-2.5/LTC1727-5	Micropower Triple Supply Monitor with Open-Drain Reset	Individual Monitor Outputs in MSOP
LTC1728-1.8/LTC1728-3.3	Micropower Triple Supply Monitor with Open-Drain Reset	5-Lead SOT-23 Package
LTC1728-2.5/LTC1728-5	Micropower Triple Supply Monitor with Open-Drain Reset	5-Lead SOT-23 Package
LTC1985-1.8	Micropower Triple Supply Monitor with Push-Pull Reset Output	5-Lead SOT-23 Package
LTC2900	Programmable Quad Supply Monitor	Adjustable RESET, 10-Lead MSOP and DFN Packages
LTC2901	Programmable Quad Supply Monitor	Adjustable RESET and Watchdog Timer, 16-Lead SSOP Package
LTC2902	Programmable Quad Supply Monitor	Adjustable RESET and Tolerance, 16-Lead SSOP Package
LTC2903	Precision Quad Supply Monitor	6-Lead SOT-23 Package
LTC2904	Three-State Programmable Precision Dual Supply Monitor	Adjustable Tolerance, 8-Lead SOT-23 and DFN Packages
LTC2905	Three-State Programmable Precision Dual Supply Monitor	Adjustable RESET and Tolerance, 8-Lead SOT-23 and DFN Packages
LTC2906	Dual Supply Monitor with One Pin Selectable Threshold and One Adjustable Input	0.5V Adjustable Threshold and Three Supply Tolerances, 8-Lead SOT-23 and DFN Packages
LTC2907	Dual Supply Monitor with One Pin Selectable Threshold and One Adjustable Input	0.5V Adjustable Threshold, RESET and Three Supply Tolerances, 8-Lead SOT-23 and DFN Packages

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