DATA SHEET

PCA9550

2-bit I^2C LED driver with programmable blink rates

Product data
Supersedes data of 2002 Dec 13

2003 May 02

PHILIPS

FEATURES

- 2 LED drivers (on, off, flashing at a programmable rate)
- 2 selectable, fully programmable blink rates (frequency and duty cycle) between 0.15625 and 40 Hz (6.4 and 0.025 seconds)
- Input/output not used as LED drivers can be used as regular GPIOs
- Internal oscillator requires no external components
- I^2C-bus interface logic compatible with SMBus
- Internal power-on reset
- Noise filter on SCL/SDA inputs
- Active-LOW reset input
- 2 open drain outputs directly drive LEDs to 25 mA
- Controlled edge rates to minimize ground bounce
- No glitch on power-up
- Supports hot insertion
- Low stand-by current
- Operating power supply voltage range of 2.3 V to 5.5 V
- 0 to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 150 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: SO8, TSSOP8

DESCRIPTION

The PCA9550 LED Blinker blinks LEDs in I^2C-bus and SMBus applications where it is necessary to limit bus traffic or free up the I^2C Master's (MCU, MPU, DSP, chipset, etc.) timer. The uniqueness of this device is the internal oscillator with two programmable blink rates. To blink LEDs using normal I/O Expanders like the PCF8574 or PCA9554, the bus master must send repeated commands to turn the LED on and off. This greatly increases the amount of traffic on the I^2C-bus and uses up one of the master's timers. The PCA9550 LED Blinker instead requires only the initial set up command to program BLINK RATE 1 and BLINK RATE 2 (i.e., the frequency and duty cycle). From then on, only one command from the bus master is required to turn each individual open drain output ON, OFF, or to cycle at BLINK RATE 1 or BLINK RATE 2. Maximum output sink current is 25 mA per bit and 50 mA per package.

Any bits not used for controlling the LEDs can be used for General Purpose Parallel Input/Output (GPIO) expansion.

The active-LOW hardware reset pin ($\overline{RESET}$) and Power On Reset (POR) initializes the registers to their default state, all zeroes, causing the bits to be set HIGH (LED off).

One hardware address pin on the PCA9550 allows two devices to operate on the same bus.

PIN CONFIGURATION

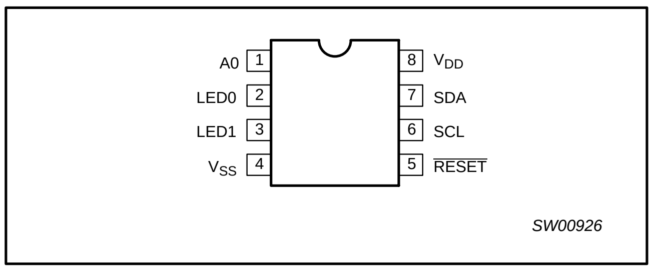


Figure 1. Pin configuration

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	A0	Address input 0
2	LED0	LED driver 0
3	LED1	LED driver 1
4	V_{SS}	Supply ground
5	$\overline{RESET}$	Active-LOW reset input
6	SCL	Serial clock line
7	SDA	Serial data line
8	V_{DD}	Supply voltage

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	TOPSIDE MARK	DRAWING NUMBER
8-Pin Plastic SO	-40 to +85 °C	PCA9550D	PCA9550	SOT96-1
8-Pin Plastic TSSOP	-40 to +85 °C	PCA9550DP	9550	SOT505-1

Standard packing quantities and other packaging data is available at www.philipslogic.com/packaging.

I^2C is a trademark of Philips Semiconductors Corporation.

BLOCK DIAGRAM

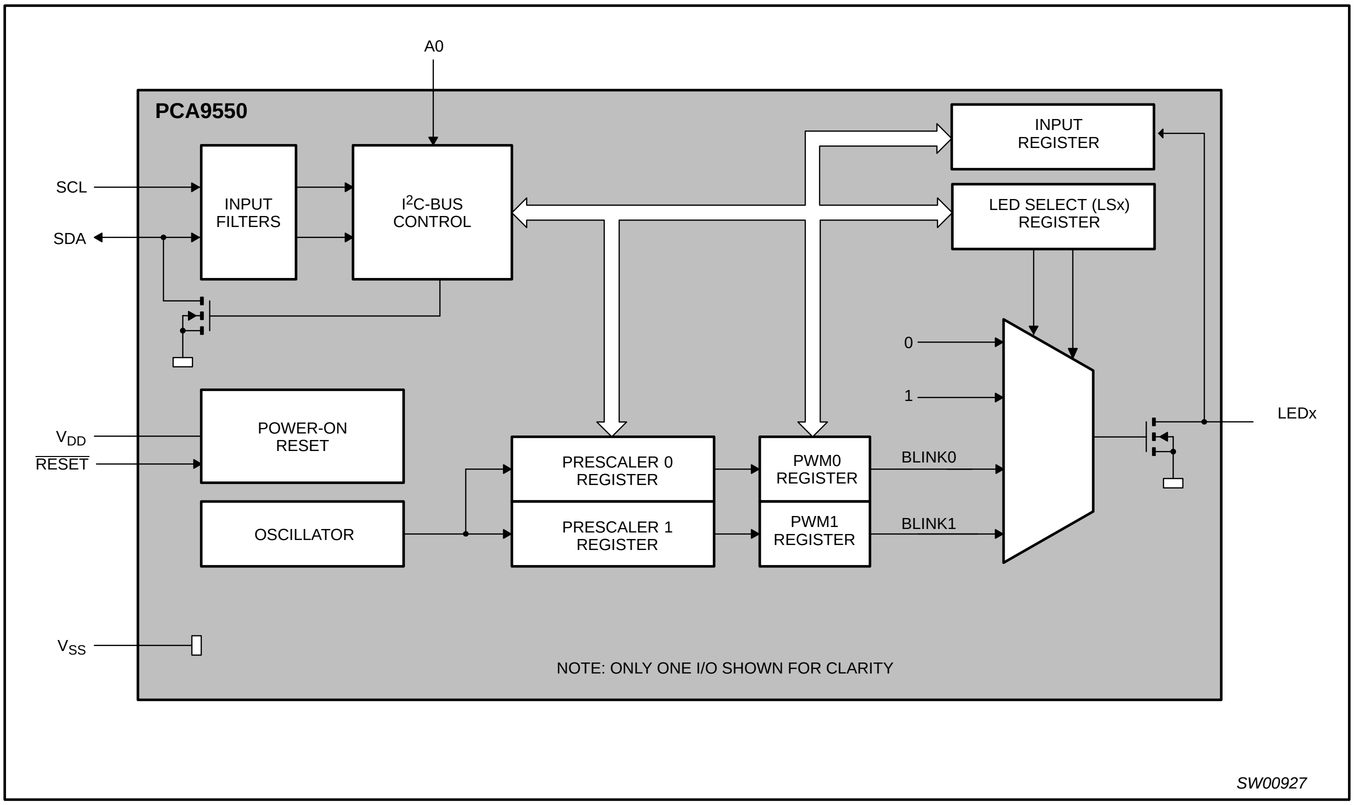


Figure 2. Block diagram

DEVICE ADDRESSING

Following a START condition the bus master must output the address of the slave it is accessing. The address of the PCA9550 is shown in Figure 3. To conserve power, no internal pull-up resistor is incorporated on the hardware selectable address pin and it must be pulled HIGH or LOW.

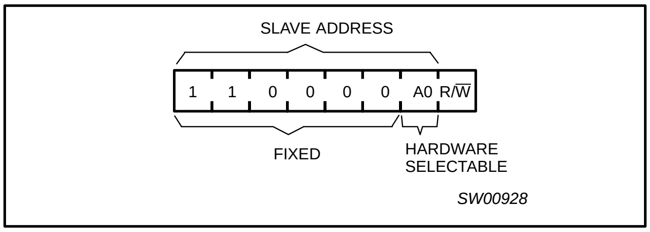


Figure 3. Slave address

The last bit of the address byte defines the operation to be performed. When set to logic 1 a read is selected while a logic 0 selects a write operation.

CONTROL REGISTER

Following the successful acknowledgement of the slave address, the bus master will send a byte to the PCA9550 which will be stored in the Control Register.

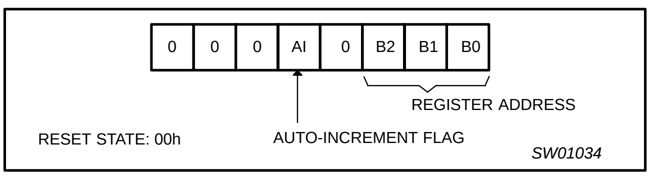


Figure 4. Control register

CONTROL REGISTER DEFINITION

B2	B1	B0	REGISTER NAME	TYPE	REGISTER FUNCTION
0	0	0	INPUT	READ	INPUT REGISTER
0	0	1	PSC0	READ/ WRITE	FREQUENCY PRESCALER 0
0	1	0	PWM0	READ/ WRITE	PWM REGISTER 0
0	1	1	PSC1	READ/ WRITE	FREQUENCY PRESCALER 1
1	0	0	PWM1	READ/ WRITE	PWM REGISTER 1
1	0	1	LS0	READ/ WRITE	LED SELECTOR

REGISTER DESCRIPTION

The lowest 3 bits are used as a pointer to determine which register will be accessed.

If the auto-increment flag is set, the three low order bits of the Control Register are automatically incremented after a read or write. This allows the user to program the registers sequentially. The contents of these bits will rollover to '000' after the last register is accessed.

When auto-increment flag is set (AI = 1) and a read sequence is initiated, the sequence must start by reading a register different from the input register (B2 B1 B0 $\neq$ 0 0 0).

Only the 3 least significant bits are affected by the AI flag.

Unused bits must be programmed with zeroes.

INPUT — INPUT REGISTER

bit	7	6	5	4	3	2	1	0
default	0	0	0	0	0	0	X	X

The INPUT register reflects the state of the device pins. Writes to this register will be acknowledged but will have no effect.

PSC0 — FREQUENCY PRESCALER 0

bit	7	6	5	4	3	2	1	0
default	1	1	1	1	1	1	1	1

PSC0 is used to program the period of the PWM output.

The period of BLINK0 $= \frac{(PSC0 + 1)}{38}$

PWM0 — PWM REGISTER 0

bit	7	6	5	4	3	2	1	0
default	1	0	0	0	0	0	0	0

The PWM0 register determines the duty cycle of BLINK0. The outputs are LOW (LED off) when the count is less than the value in PWM0 and HIGH when it is greater. If PWM0 is programmed with 00h, then the PWM0 output is always LOW.

The duty cycle of BLINK0 is: $\frac{256 - PWM0}{256}$

PSC1 — FREQUENCY PRESCALER 1

bit	7	6	5	4	3	2	1	0
default	1	1	1	1	1	1	1	1

PSC1 is used to program the period of PWM output.

The period of BLINK1 $= \frac{(PSC1 + 1)}{38}$

PWM1 — PWM REGISTER 1

bit	7	6	5	4	3	2	1	0
default	1	0	0	0	0	0	0	0

The PWM1 register determines the duty cycle of BLINK1. The outputs are LOW (LED off) when the count is less than the value in PWM1 and HIGH when it is greater. If PWM1 is programmed with 00h, then the PWM1 output is always LOW.

The duty cycle of BLINK1 is: $\frac{256 - PWM1}{256}$

LS0 — LED SELECTOR

					LED 1		LED 0	
bit	7	6	5	4	3	2	1	0
default	1	1	1	1	0	1	0	1

The LSx LED select registers determine the source of the LED data.

- 00 = Output is set LOW (LED on)
- 01 = Output is set Hi-Z (LED off - default)
- 10 = Output blinks at PWM0 rate
- 11 = Output blinks at PWM1 rate

POWER-ON RESET

When power is applied to V_{DD}, an internal Power-On Reset holds the PCA9550 in a reset state until V_{DD} has reached V_{POR}. At this point, the reset condition is released and the PCA9550 registers are initialized to their default states, all the outputs in the off state.

EXTERNAL RESET

A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin LOW for a minimum of t_W. The PCA9550 registers and I²C state machine will be held in their default state until the $\overline{\text{RESET}}$ input is once again HIGH.

This input requires a pull-up resistor to V_{DD}.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 5).

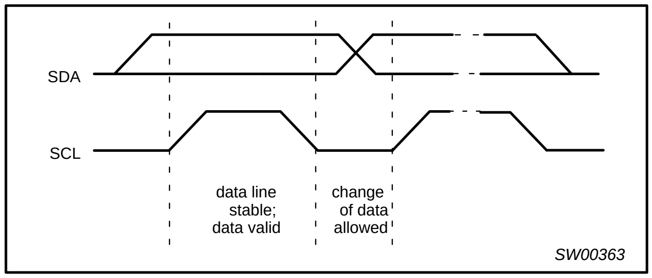


Figure 5. Bit transfer

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P) (see Figure 6).

System configuration

A device generating a message is a transmitter: a device receiving is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves (see Figure 7).

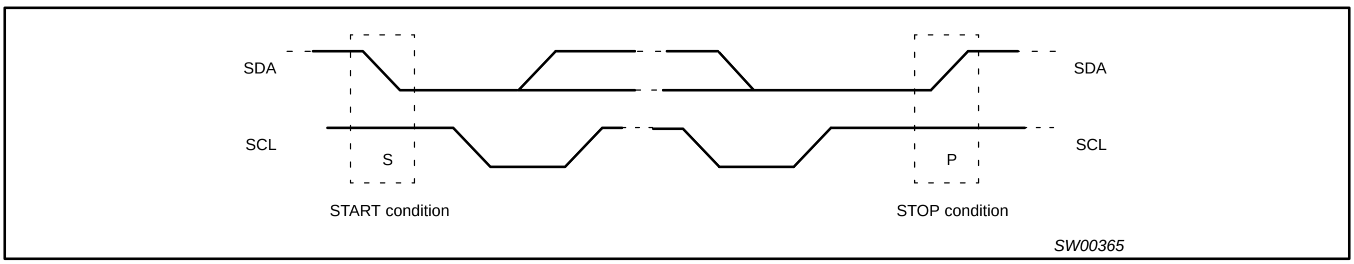


Figure 6. Definition of start and stop conditions

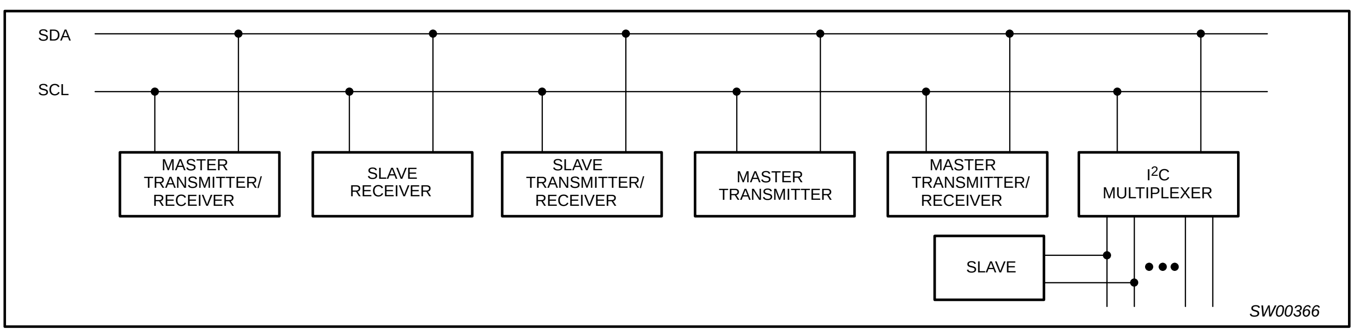


Figure 7. System configuration

Acknowledge

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

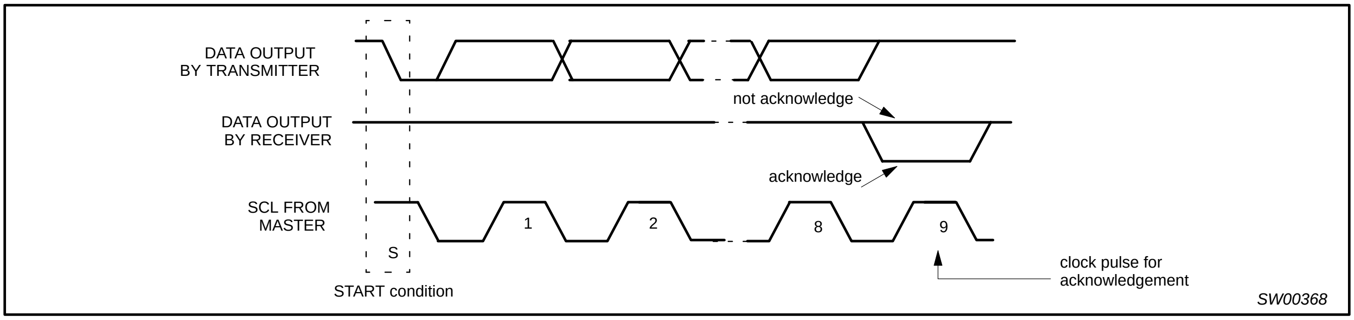


Figure 8. Acknowledgement on the I²C-bus

Bus transactions

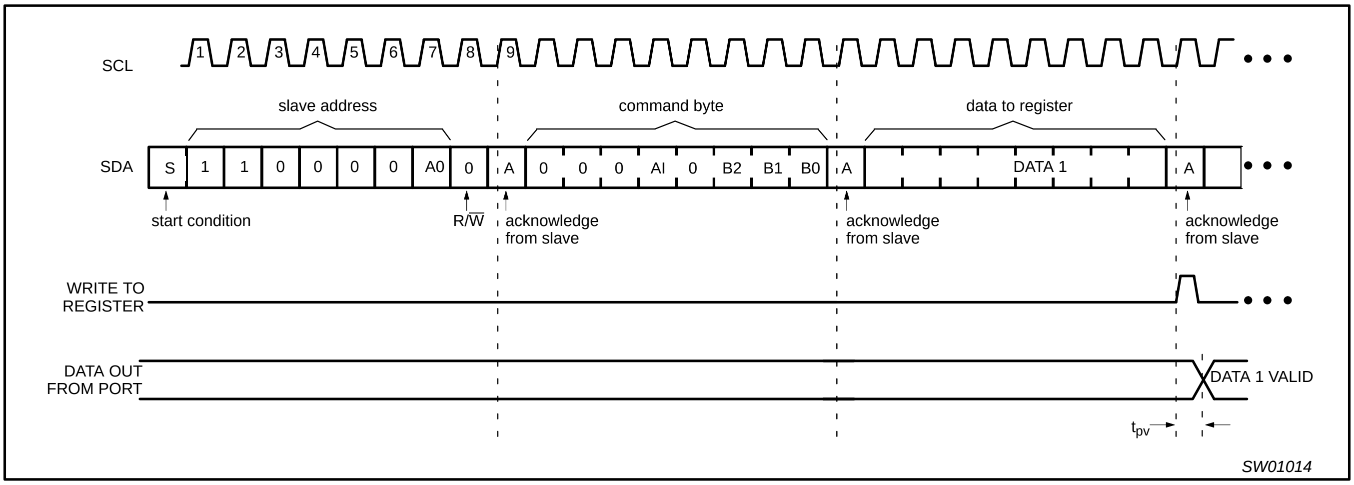


Figure 9. WRITE to register

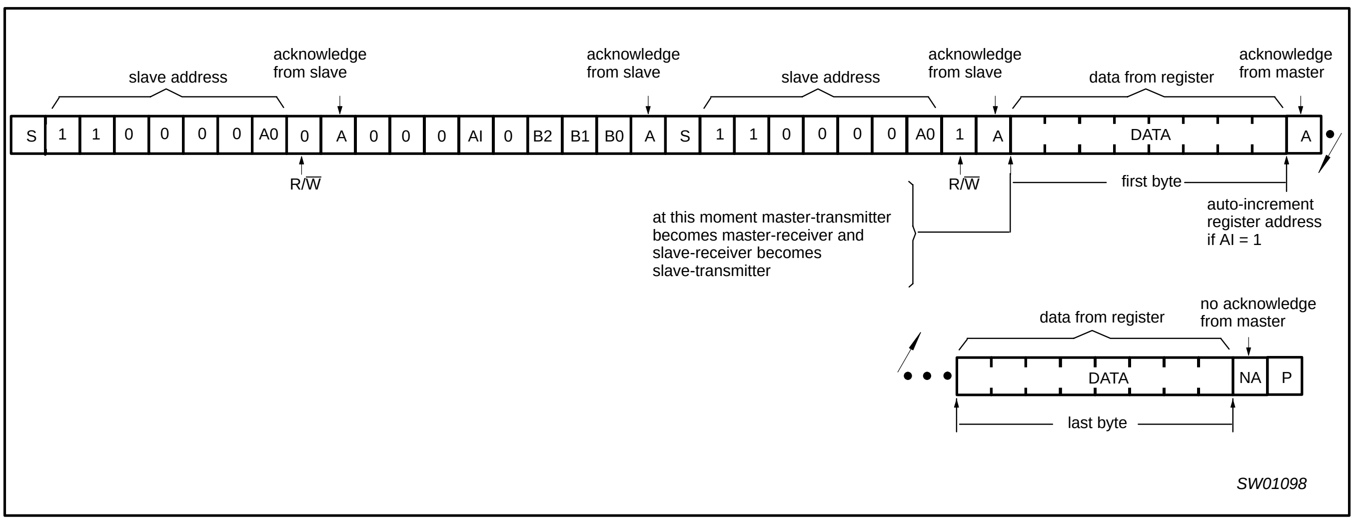
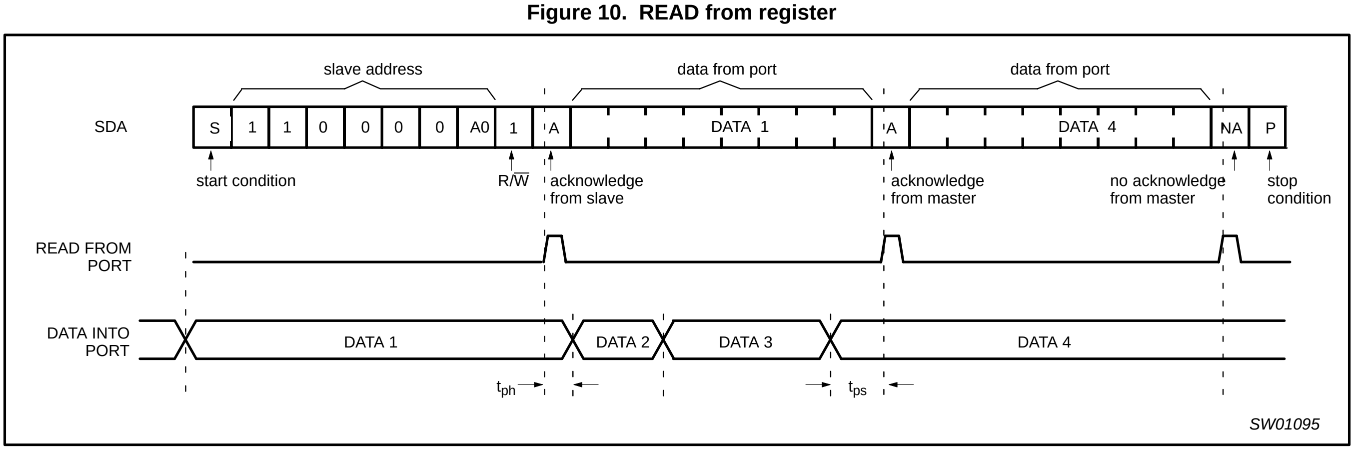


Figure 10. READ from register



NOTES:
1. This figure assumes the command byte has previously been programmed with 00h.

Figure 11. READ input port register

APPLICATION DATA

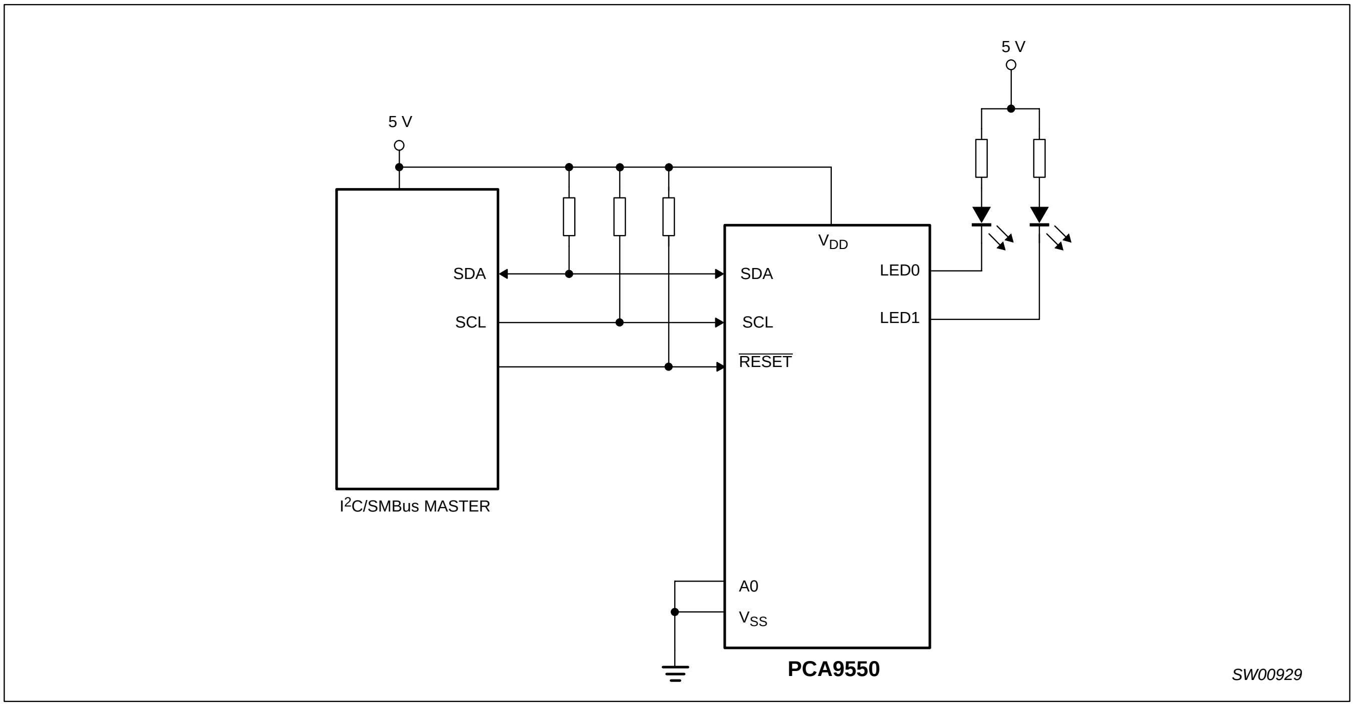


Figure 12. Typical application

Minimizing I_{DD} when the I/O is used to control LEDs

When the I/Os are used to control LEDs, they are normally connected to V_{DD} through a resistor as shown in Figure 12. Since the LED acts as a diode, when the LED is off the I/O V_{IN} is about 1.2 V less than V_{DD}. The supply current, I_{DD}, increases as V_{IN} becomes lower than V_{DD} and is specified as ΔI_{DD} in the DC characteristics table.

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V_{DD} when the LED is off. Figure 13 shows a high value resistor in parallel with the LED. Figure 14 shows V_{DD} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_{IN} at or above V_{DD} and prevents additional supply current consumption when the LED is off.

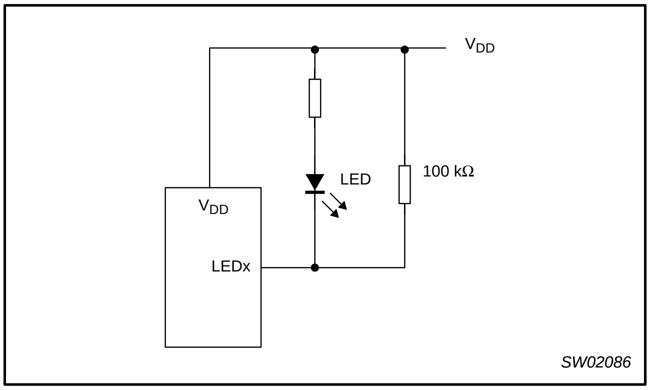


Figure 13. High value resistor in parallel with the LED

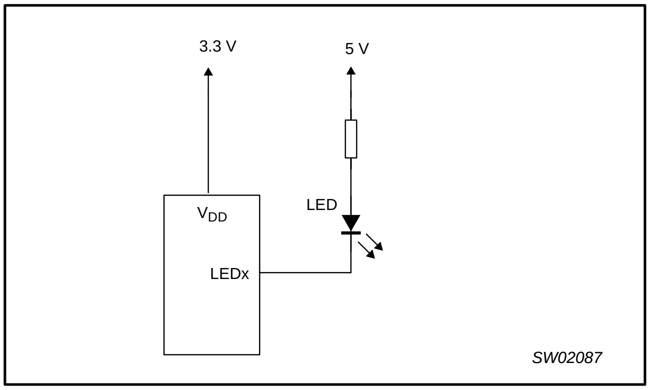


Figure 14. Device supplied by a lower voltage

Programming example

The following example will show how to set LED0 to blink at 1 Hz at a 50% duty cycle. LED1 will be set to blink at 4 Hz, 25% duty cycle.

Table 1.

	I^2C-bus
Start	S
PCA9550 address with A0 = LOW	COh
PSC0 subaddress + auto-increment	11h
Set prescaler PSC0 to achieve a period of 1 second: $\text{Blink period} = 1 = \frac{PSC0 + 1}{38}$ PSC0 = 37	25h
Set PWM0 duty cycle to 50%: $\frac{256 - PWM0}{256} = 0.5$ PWM0 = 128	80h
Set prescaler PCS1 to achieve a period of 0.25 seconds: $\text{Blink period} = 0.25 = \frac{PSC1 + 1}{38}$ PSC1 = 9	09h
Set PWM1 output duty cycle to 25%: $\frac{256 - PWM1}{256} = 0.25$ PWM1 = 192	C0h
Set LED0 to PWM0 and set LED1 to blink at PWM1	OEh
Stop	P

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{DD}	Supply voltage		-0.5	6.0	V
$V_{I/O}$	DC voltage on an I/O		V_{SS} - 0.5	5.5	V
$I_{I/O}$	DC output current on an I/O		—	±25	mA
I_{SS}	Supply current		—	50	mA
P_{tot}	Total power dissipation		—	400	mW
T_{stg}	Storage temperature range		-65	+150	°C
T_{amb}	Operating ambient temperature		-40	+85	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC24 under ”*Handling MOS devices*”.

DC CHARACTERISTICS

V_{DD} = 2.3 to 5.5 V; V_{SS} = 0 V; T_{amb} = -40 to +85 °C; unless otherwise specified. TYP at 3.3 V and 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supplies						
V_{DD}	Supply voltage		2.3	—	5.5	V
I_{DD}	Supply current	Operating mode; V_{DD} = 5.5 V; no load; $V_I = V_{DD}$ or V_{SS}; f_{SCL} = 100 kHz	—	350	500	µA
I_{stb}	Standby current	Standby mode; V_{DD} = 5.5 V; no load; $V_I = V_{DD}$ or V_{SS}; f_{SCL} = 0 kHz	—	1.9	3.0	µA
ΔI_{DD}	Additional standby current	Standby mode; V_{DD} = 5.5 V; Every LED I/O at V_{IN} = 4.3 V; f_{SCL} = 0 kHz	—	—	200	µA
V_{POR}	Power-on reset voltage	No load; $V_I = V_{DD}$ or V_{SS}	1.4	1.7	2.2	V
Input SCL; input/output SDA						
V_{IL}	LOW-level input voltage		-0.5	—	0.3 V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7 V_{DD}	—	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4V	3	6.5	—	mA
I_L	Leakage current	$V_I = V_{DD} = V_{SS}$	-1	—	+1	µA
C_I	Input capacitance	$V_I = V_{SS}$	—	3.7	5	pF
I/Os						
V_{IL}	LOW-level input voltage		-0.5	—	0.8	V
V_{IH}	HIGH-level input voltage		2.0	—	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; V_{DD} = 2.3 V; Note 1	9	—	—	mA
		V_{OL} = 0.4 V; V_{DD} = 3.0 V; Note 1	11	—	—	mA
		V_{OL} = 0.4 V; V_{DD} = 5.0 V; Note 1	14	—	—	mA
		V_{OL} = 0.7 V; V_{DD} = 2.3 V; Note 1	14	—	—	mA
		V_{OL} = 0.7 V; V_{DD} = 3.0 V; Note 1	18	—	—	mA
		V_{OL} = 0.7 V; V_{DD} = 5.0 V; Note 1	24	—	—	mA
I_L	Input leakage current	V_{DD} = 3.6 V; V_I = 0 or V_{DD}	-1	—	1	µA
C_{IO}	Input/output capacitance		—	2.1	5	pF
Select Inputs A0 / $\overline{\text{RESET}}$						
V_{IL}	LOW-level input voltage		-0.5	—	0.8	V
V_{IH}	HIGH-level input voltage		2.0	—	5.5	V
I_{LI}	Input leakage current		-1	—	1	µA
C_I	Input capacitance	$V_I = V_{SS}$	—	2.3	5	pF

NOTE:
1. Each I/O must be externally limited to a maximum of 25 mA and the device must be limited to a maximum current of 50 mA.

AC SPECIFICATIONS

SYMBOL	PARAMETER	STANDARD MODE I²C-BUS		FAST MODE I²C-BUS		UNITS
		MIN	MAX	MIN	MAX	
f_{SCL}	Operating frequency	0	100	0	400	kHz
t_{BUF}	Bus free time between STOP and START conditions	4.7	—	1.3	—	µs
$t_{HD;STA}$	Hold time after (repeated) START condition	4.0	—	0.6	—	µs
$t_{SU;STA}$	Repeated START condition set-up time	4.7	—	0.6	—	µs
$t_{SU;STO}$	Set-up time for STOP condition	4.0	—	0.6	—	µs
$t_{HD;DAT}$	Data in hold time	0	—	0	—	ns
$t_{VD;ACK}$	Valid time for ACK condition[2]	—	600	—	600	ns
$t_{VD;DAT}$ (L)	Data out valid time[3]	—	600	—	600	ns
$t_{VD;DAT}$ (H)	Data out valid time[3]	—	1500	—	600	ns
$t_{SU;DAT}$	Data set-up time	250	—	100	—	ns
t_{LOW}	Clock LOW period	4.7	—	1.3	—	µs
t_{HIGH}	Clock HIGH period	4.0	—	0.6	—	µs
t_F	Clock/Data fall time	—	300	$20 + 0.1\ C_b$[1]	300	ns
t_R	Clock/Data rise time	—	1000	$20 + 0.1\ C_b$[1]	300	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filters	—	50	—	50	ns
Port Timing						
t_{PV}	Output data valid	—	200	—	200	ns
t_{PS}	Input data set-up time	100	—	100	—	ns
t_{PH}	Input data hold time	1	—	1	—	µs
Reset						
t_W	Reset pulse width	6	—	6	—	ns
t_{REC}	Reset recovery time	0	—	0	—	ns
t_{RESET}[4,5]	Time to reset	400	—	400	—	ns

NOTES:
1. C_b = total capacitance of one bus line in pF.
2. $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.
3. $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.
4. Resetting the device while actively communicating on the bus may cause glitches or errant STOP conditions.
5. Upon reset, the full delay will be the sum of t_{RESET} and the RC time constant of the SDA bus.

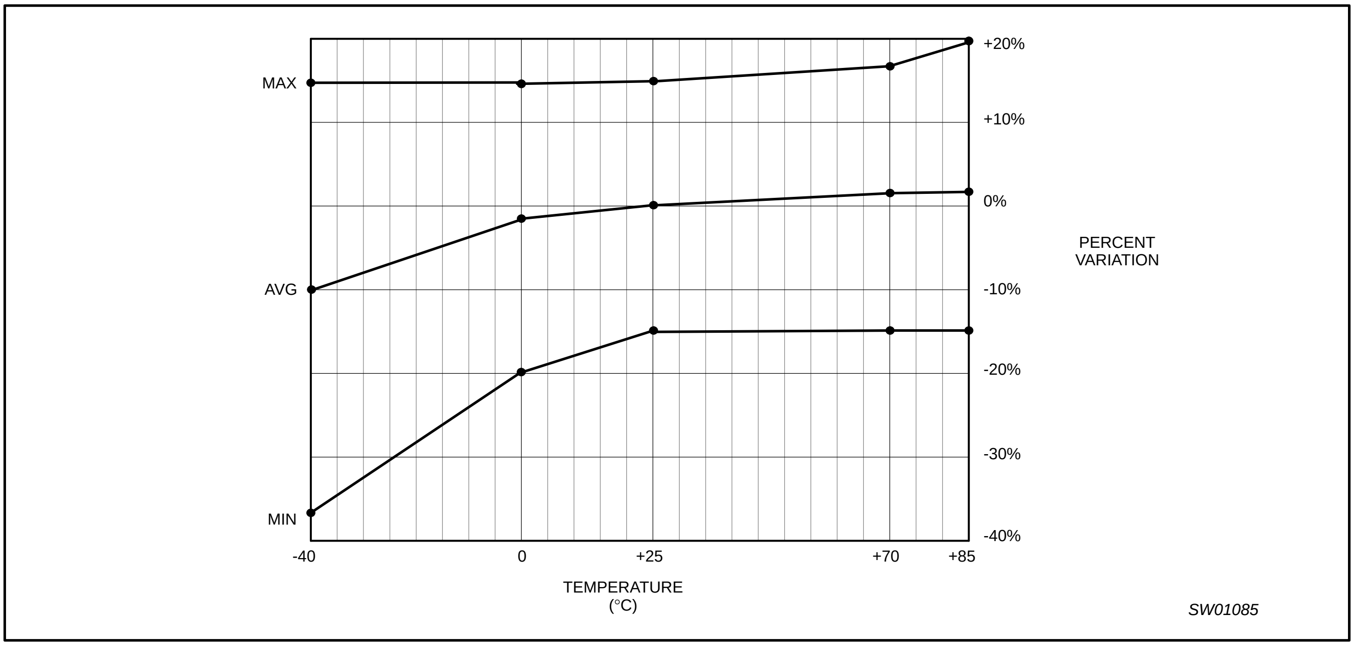


Figure 15. Typical frequency variation over process at V_{DD} = 2.3 V to 3.0 V

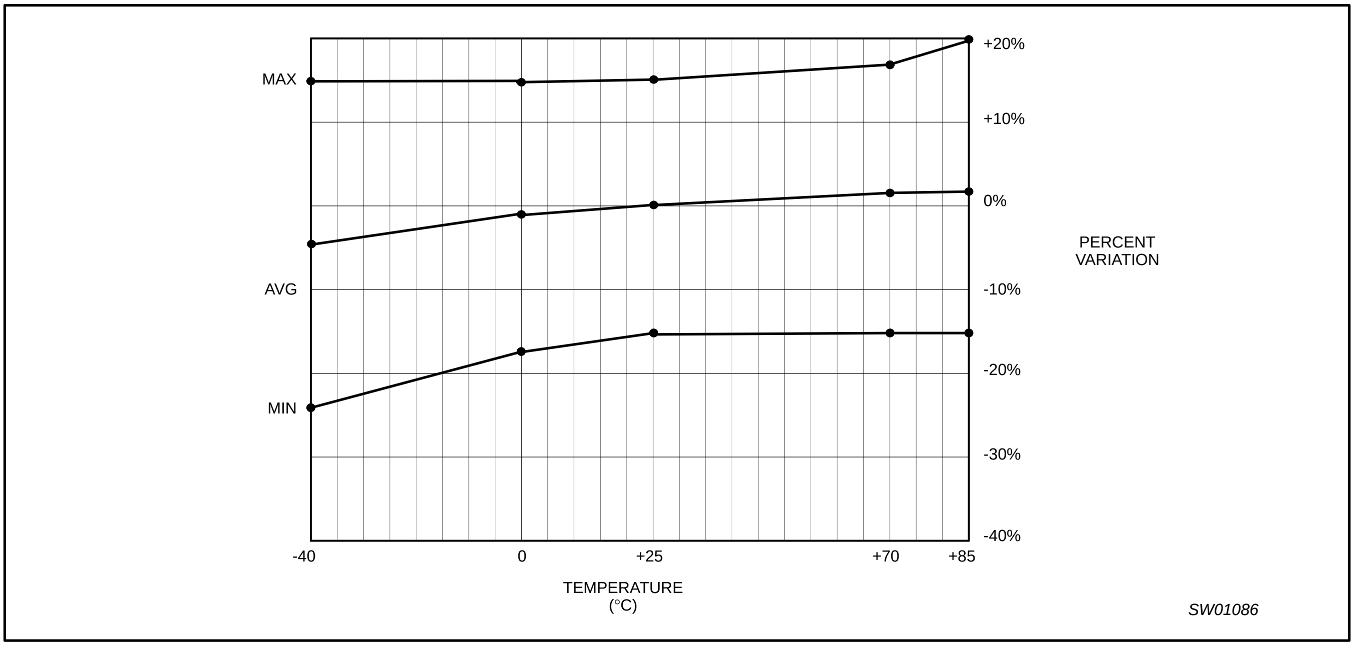


Figure 16. Typical frequency variation over process at V_{DD} = 3.0 V to 5.5 V

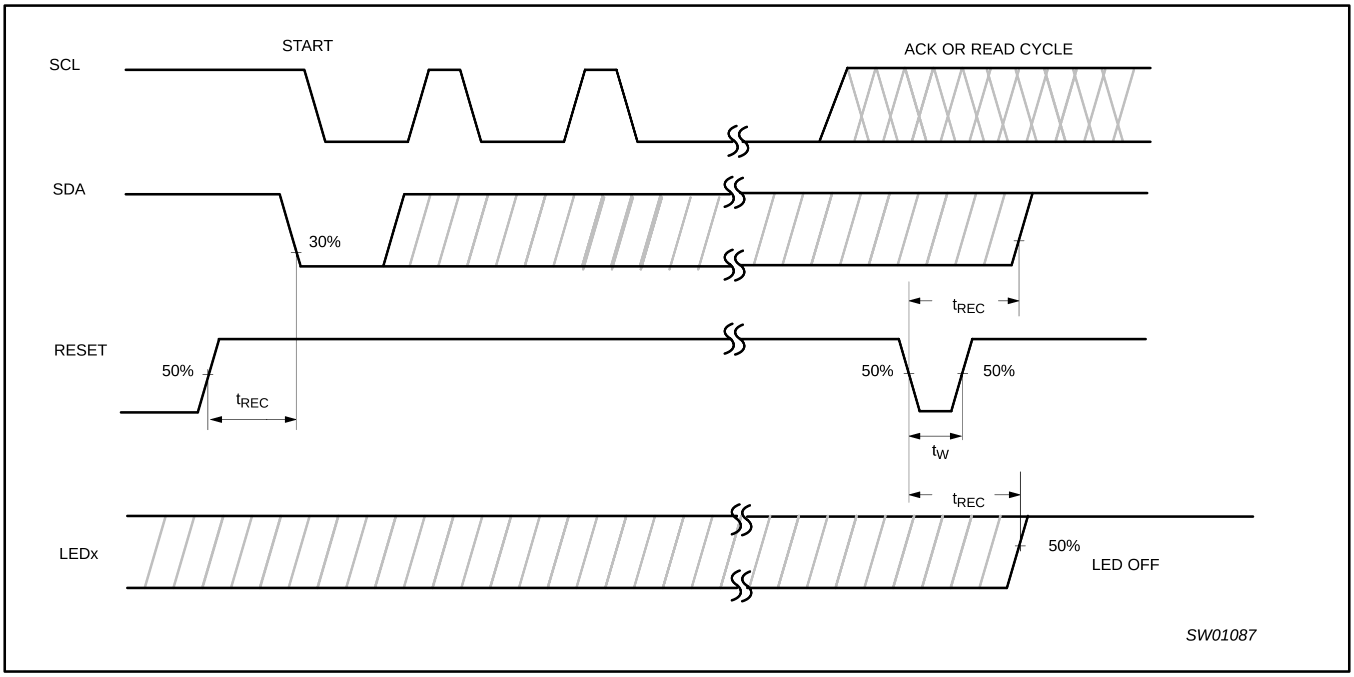


Figure 17. Definition of $\overline{\text{RESET}}$ timing

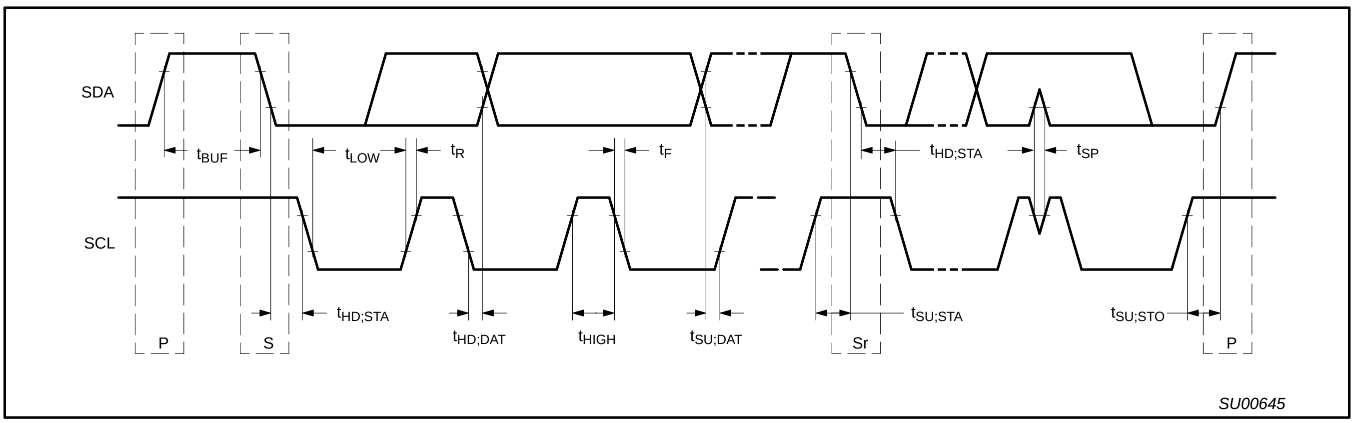
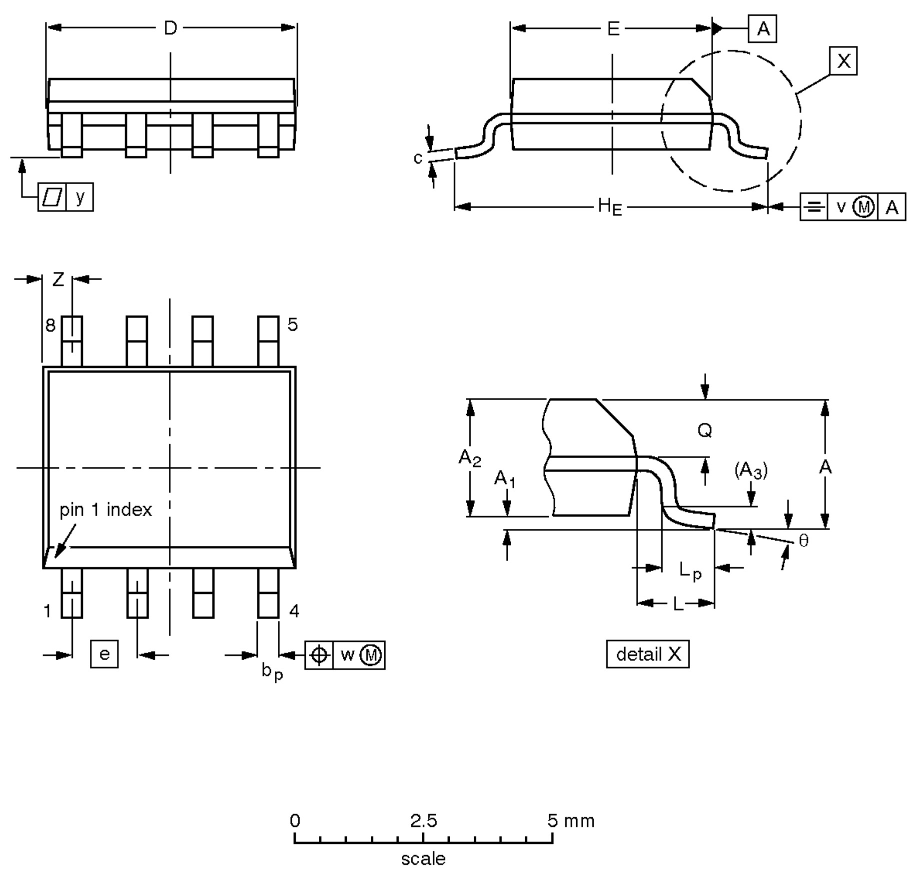


Figure 18. Definition of timing

SO8: plastic small outline package; 8 leads; body width 3.9 mm SOT96-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

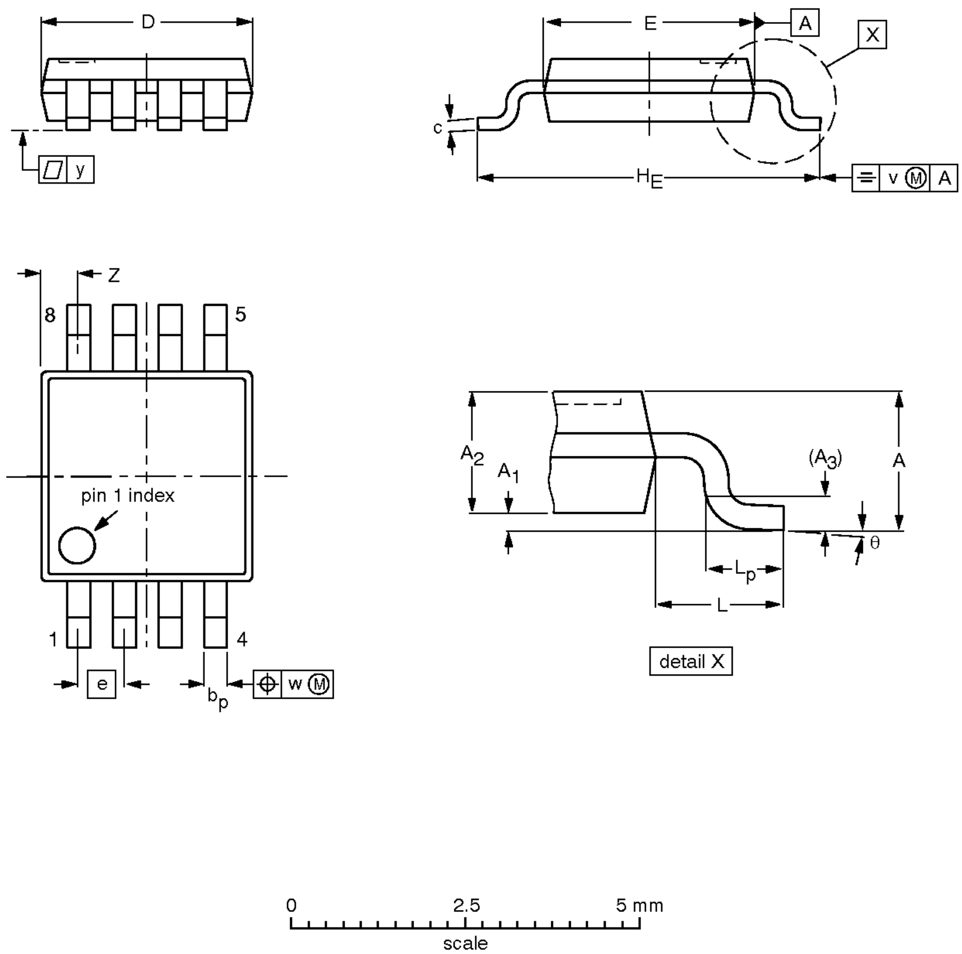
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**

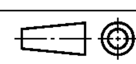


DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.10 2.90	3.10 2.90	0.65	5.10 4.70	0.94	0.70 0.40	0.1	0.1	0.1	0.70 0.35	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT505-1						99-04-09

REVISION HISTORY

Rev	Date	Description
_2	20030502	**Product data (9397 750 11461); ECN 853-2396 29859 dated 24 April 2003. Supersedes data of 2002 Dec 13 (9397 750 10857).** Modifications: • Correction to voltage in typical application drawing • Update maximum current per bit and per device • Adjust maximum and minimum curves to ±15% on frequency variation graphs.
_1	20021213	Product data (9397 750 10857); ECN 853-2396 29264 of 09 December 2002.

Purchase of Philips I^{2}C components conveys a license under the Philips' I^{2}C patent to use the components in the I^{2}C system provided the system conforms to the I^{2}C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

Data sheet status

Level	Data sheet status[1]	Product status[2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Contact information

For additional information please visit
http://www.semiconductors.philips.com. Fax: **+31 40 27 24825**

For sales offices addresses send e-mail to:
sales.addresses@www.semiconductors.philips.com.

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