Data Sheet | October 1998 | File Number 1384.2

3A, 450V and 500V, 3 Ohm, N-Channel Power MOSFETs

These are N-Channel enhancement mode silicon gate power field effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA17405.

Ordering Information

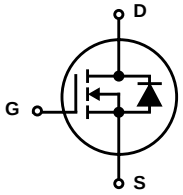
PART NUMBER	PACKAGE	BRAND
RFM3N45	TO-204AA	RFM3N45
RFM3N50	TO-204AA	RFM3N50
RFP3N45	TO-220AB	RFP3N45
RFP3N50	TO-220AB	RFP3N50

NOTE: When ordering, use the entire part number.

Features

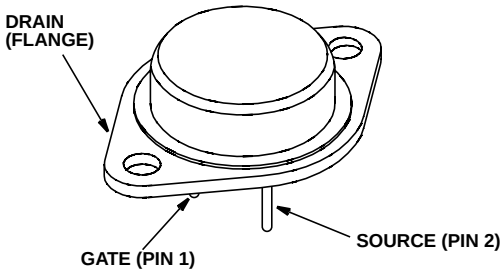
- 3A, 450V and 500V
- $r_{DS(ON)} = 3\Omega$
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol

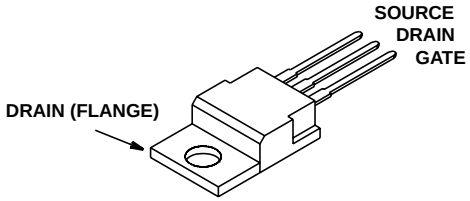


Packaging

JEDEC TO-204AA



JEDEC TO-220AB



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

	RFM3N45	RFM3N50	RFP3N45	RFP3N50	UNITS
Drain to Source Breakdown Voltage (Note 1) . . . . . V_{DS}	450	500	450	500	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1) . . . . . V_{DGR}	450	500	450	500	V
Continuous Drain Current . . . . . I_D	3	3	3	3	A
Pulsed Drain Current (Note 3) . . . . . I_{DM}	5	5	5	5	A
Gate to Source Voltage . . . . . V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation . . . . . P_D	75	75	60	60	W
Linear Derating Factor	0.6	0.6	0.48	0.48	$W/^oC$
Operating and Storage Temperature . . . . . T_J, T_{STG}	-55 to 150	-55 to 150	-55 to 150	-55 to 150	^oC
Maximum Temperature for Soldering					
Leads at 0.063in (1.6mm) from Case for 10s . . . . . T_L	300	300	300	300	^oC
Package Body for 10s, See Techbrief 334 . . . . . T_{pkg}	260	260	260	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250µA, V_{GS} = 0V				
RFM3N45, RFP3N45			450	-	-	V
RFM3N50, RFP3N50			500	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250µA, (Figure 7)	2.0	-	4.0	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, V_{GS} = 0V	-	-	1	µA
		V_{DS} = 0.8 x Rated BV_{DSS}, V_{GS} = 0V, $T_C = 125^oC$	-	-	25	µA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V	-	-	±100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	I_D = 3A, V_{GS} = 10V, (Figures 5, 6)	-	-	3	Ω
Drain to Source On Voltage (Note 2)	$V_{DS(ON)}$	I_D = 3A, V_{GS} = 10V	-	-	9.0	V
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 250V, $I_D \approx$ 1.5A, R_G = 50Ω, V_{GS} = 10V R_L = 165Ω (Figures 10, 11, 12)	-	30	45	ns
Rise Time	t_r		-	40	60	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	90	135	ns
Fall Time	t_f		-	50	75	ns
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz	-	-	750	pF
Output Capacitance	C_{OSS}		-	-	150	pF
Reverse Transfer Capacitance	C_{RSS}		-	-	100	pF
Thermal Resistance, Junction to Case	$R_{\theta JC}$					
RFM3N45, RFM3N50			-	-	1.67	$^oC/W$
RFP3N45, RFP3N50			-	-	2.083	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	I_{SD} = 1.5A	-	-	1.4	V
Reverse Recovery Time	t_{rr}	I_{SD} = 4A, dI_{SD}/dt = 100A/µs	-	800	-	ns

NOTES:

2. Pulse test: pulse width ≤ 300µs, duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by maximum junction temperature.

Typical Performance Curves Unless Otherwise Specified

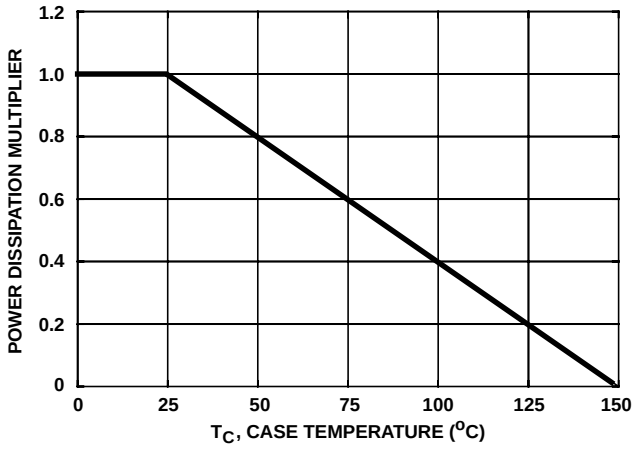


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

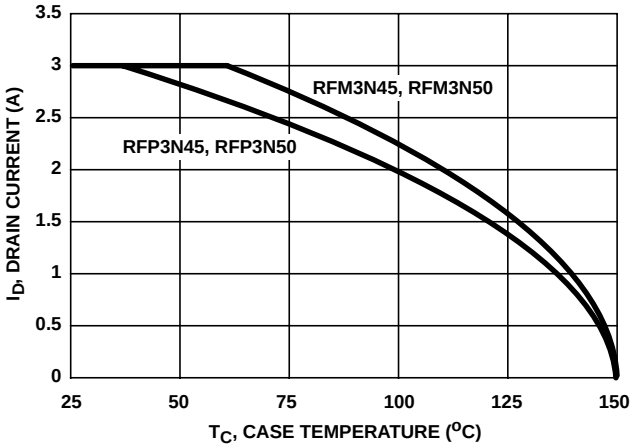


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

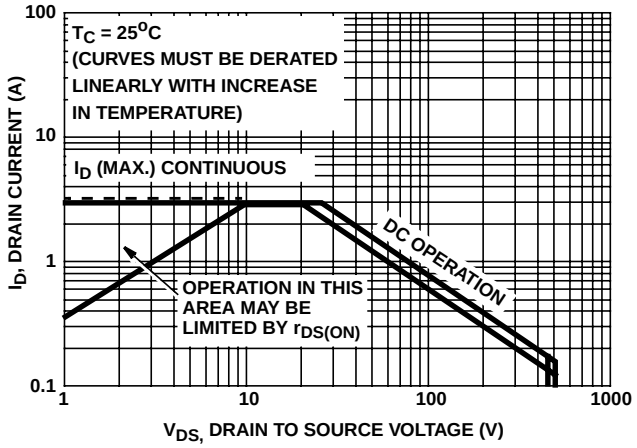


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

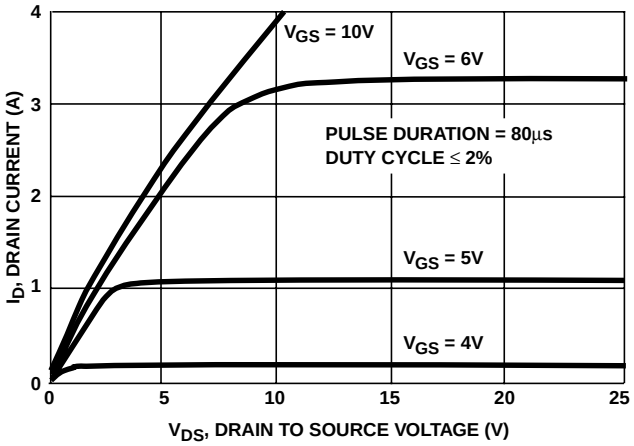


FIGURE 4. SATURATION CHARACTERISTICS

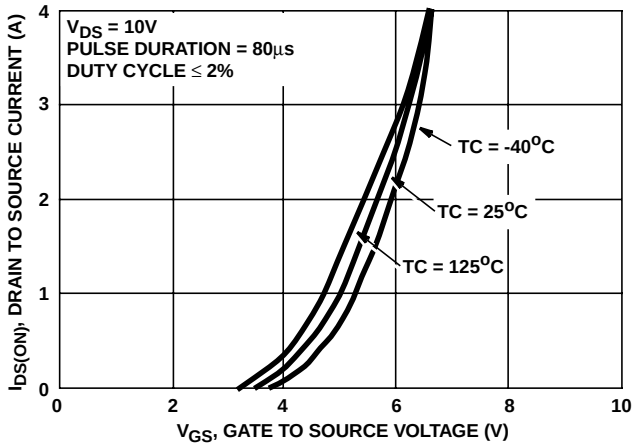


FIGURE 5. TRANSFER CHARACTERISTICS

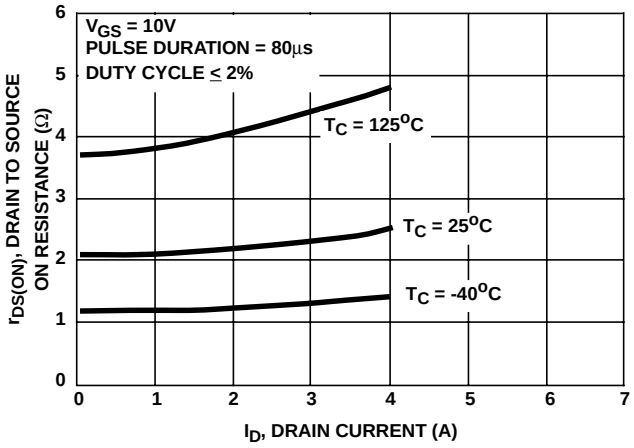


FIGURE 6. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

Typical Performance Curves Unless Otherwise Specified **(Continued)**

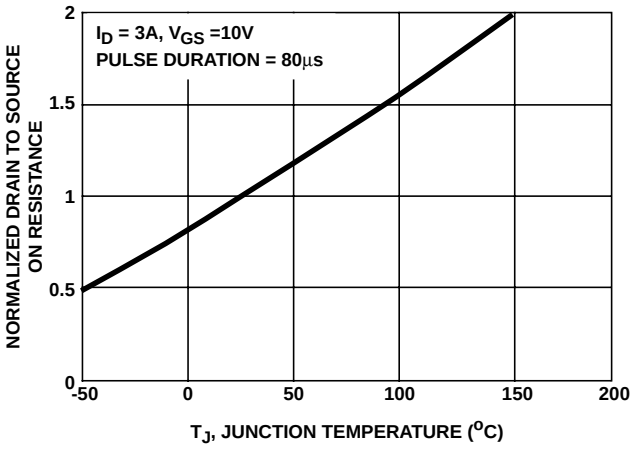


FIGURE 7. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

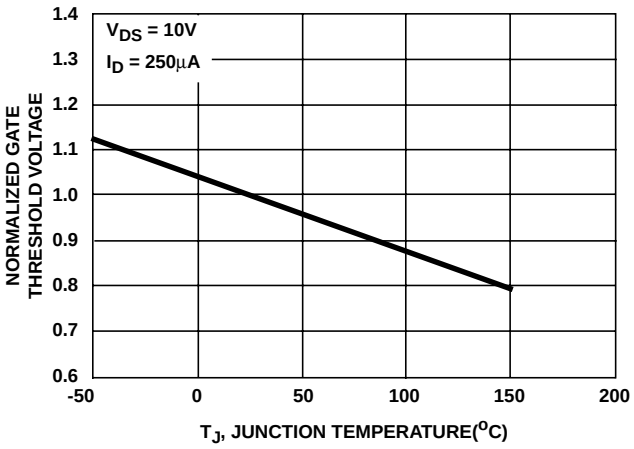


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

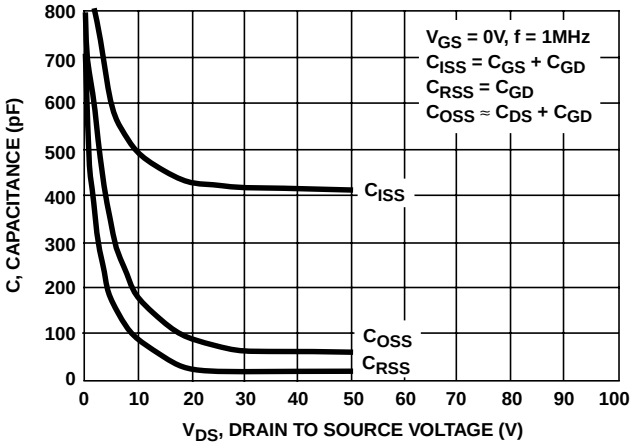
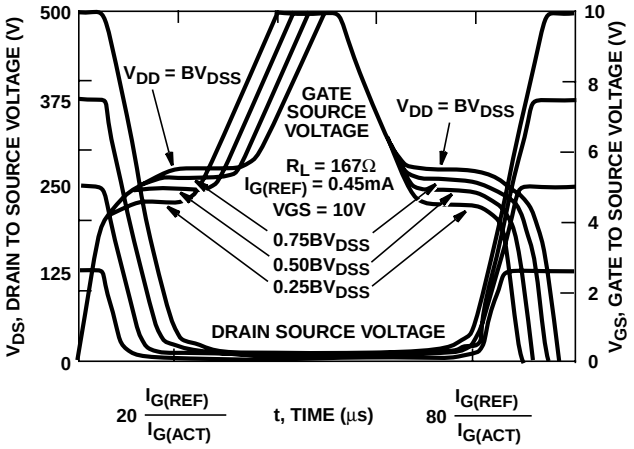


FIGURE 9. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Harris Application Notes AN7254 and AN7260.

FIGURE 10. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

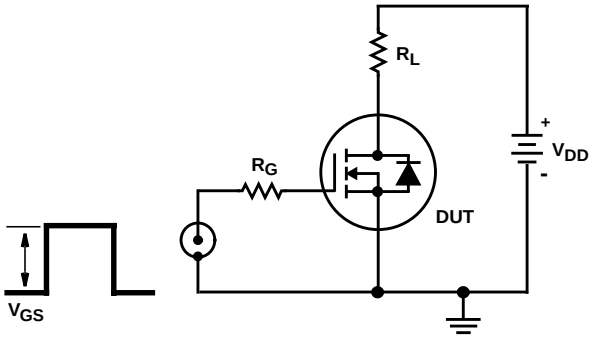


FIGURE 11. SWITCHING TIME TEST CIRCUIT

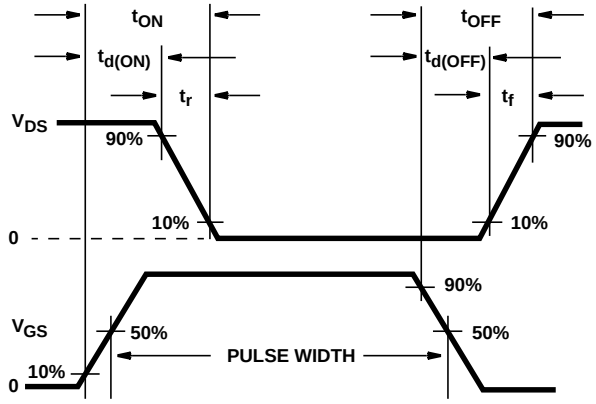


FIGURE 12. RESISTIVE SWITCHING WAVEFORMS

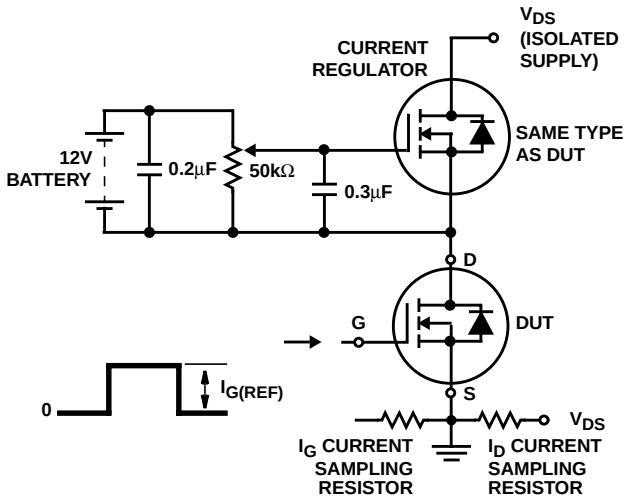


FIGURE 13. GATE CHARGE TEST CIRCUIT

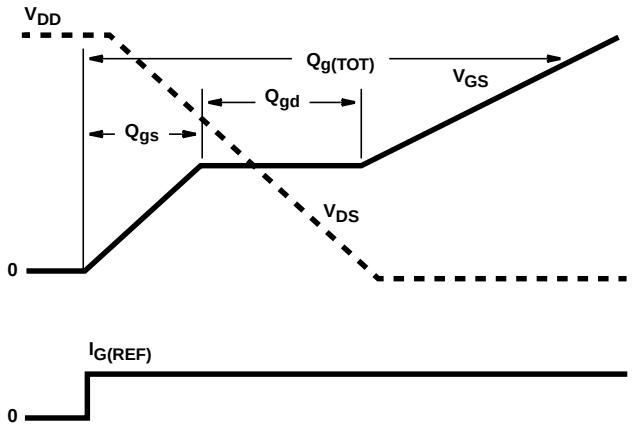


FIGURE 14. GATE CHARGE WAVEFORMS

Data Sheet | October 1998 | File Number 1384.2

3A, 450V and 500V, 3 Ohm, N-Channel Power MOSFETs

These are N-Channel enhancement mode silicon gate power field effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA17405.

Ordering Information

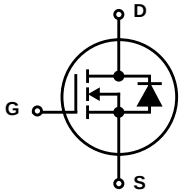
PART NUMBER	PACKAGE	BRAND
RFM3N45	TO-204AA	RFM3N45
RFM3N50	TO-204AA	RFM3N50
RFP3N45	TO-220AB	RFP3N45
RFP3N50	TO-220AB	RFP3N50

NOTE: When ordering, use the entire part number.

Features

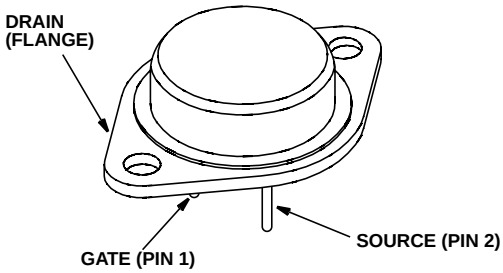
- 3A, 450V and 500V
- $r_{DS(ON)} = 3\Omega$
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol

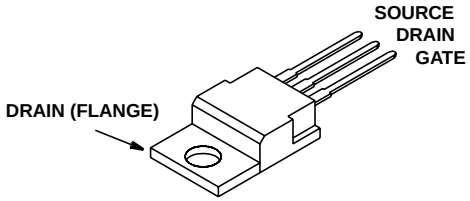


Packaging

JEDEC TO-204AA



JEDEC TO-220AB



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

	RFM3N45	RFM3N50	RFP3N45	RFP3N50	UNITS
Drain to Source Breakdown Voltage (Note 1) . . . . . V_{DS}	450	500	450	500	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1) . . . . . V_{DGR}	450	500	450	500	V
Continuous Drain Current . . . . . I_D	3	3	3	3	A
Pulsed Drain Current (Note 3) . . . . . I_{DM}	5	5	5	5	A
Gate to Source Voltage . . . . . V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation . . . . . P_D	75	75	60	60	W
Linear Derating Factor	0.6	0.6	0.48	0.48	$W/^oC$
Operating and Storage Temperature . . . . . T_J, T_{STG}	-55 to 150	-55 to 150	-55 to 150	-55 to 150	^oC
Maximum Temperature for Soldering					
Leads at 0.063in (1.6mm) from Case for 10s . . . . . T_L	300	300	300	300	^oC
Package Body for 10s, See Techbrief 334 . . . . . T_{pkg}	260	260	260	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250µA, V_{GS} = 0V				
RFM3N45, RFP3N45			450	-	-	V
RFM3N50, RFP3N50			500	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250µA, (Figure 7)	2.0	-	4.0	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, V_{GS} = 0V	-	-	1	µA
		V_{DS} = 0.8 x Rated BV_{DSS}, V_{GS} = 0V, $T_C = 125^oC$	-	-	25	µA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V	-	-	±100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	I_D = 3A, V_{GS} = 10V, (Figures 5, 6)	-	-	3	Ω
Drain to Source On Voltage (Note 2)	$V_{DS(ON)}$	I_D = 3A, V_{GS} = 10V	-	-	9.0	V
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 250V, $I_D \approx$ 1.5A, R_G = 50Ω, V_{GS} = 10V R_L = 165Ω (Figures 10, 11, 12)	-	30	45	ns
Rise Time	t_r		-	40	60	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	90	135	ns
Fall Time	t_f		-	50	75	ns
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz	-	-	750	pF
Output Capacitance	C_{OSS}		-	-	150	pF
Reverse Transfer Capacitance	C_{RSS}		-	-	100	pF
Thermal Resistance, Junction to Case	$R_{\theta JC}$					
RFM3N45, RFM3N50			-	-	1.67	$^oC/W$
RFP3N45, RFP3N50			-	-	2.083	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	I_{SD} = 1.5A	-	-	1.4	V
Reverse Recovery Time	t_{rr}	I_{SD} = 4A, dI_{SD}/dt = 100A/µs	-	800	-	ns

NOTES:

2. Pulse test: pulse width ≤ 300µs, duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by maximum junction temperature.

Typical Performance Curves Unless Otherwise Specified

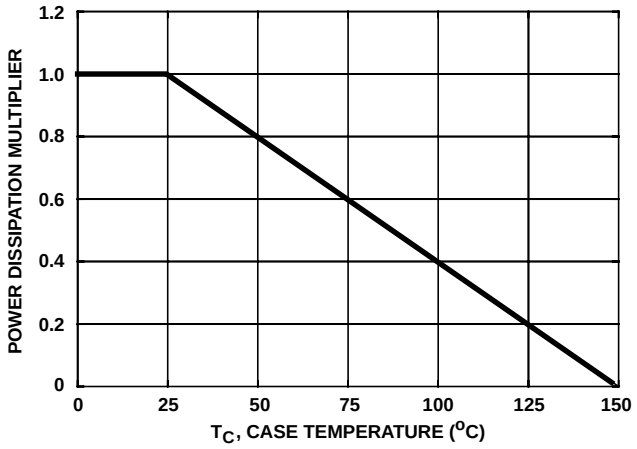


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

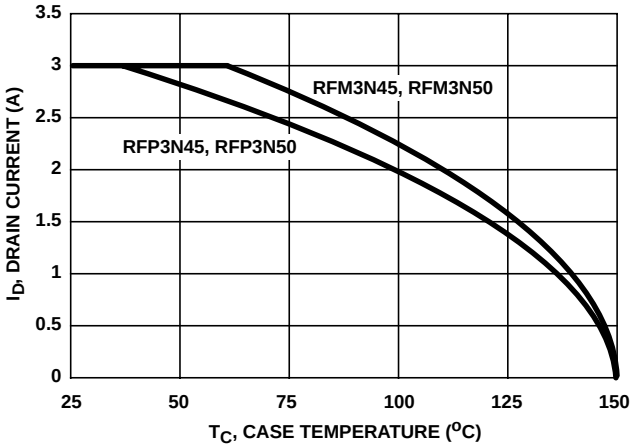


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

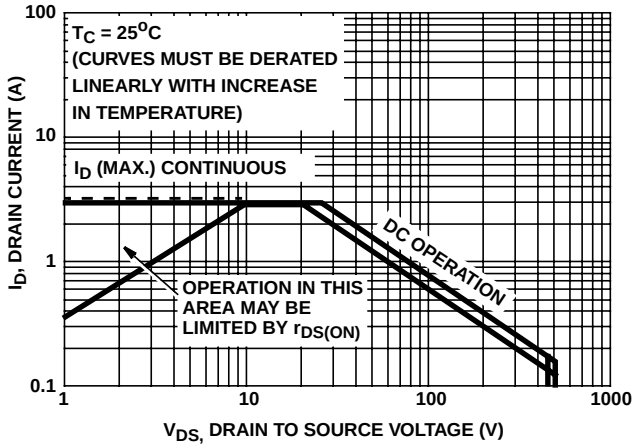


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

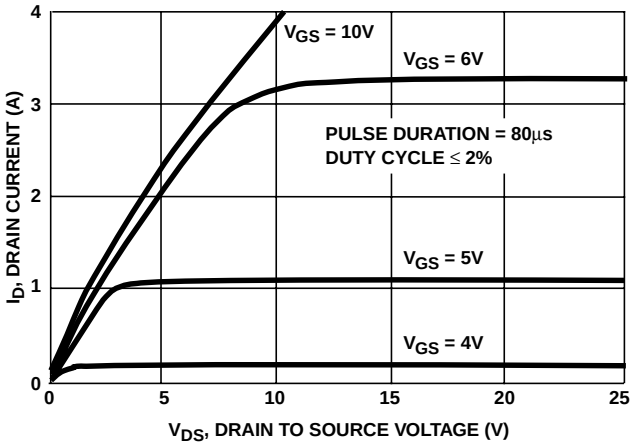


FIGURE 4. SATURATION CHARACTERISTICS

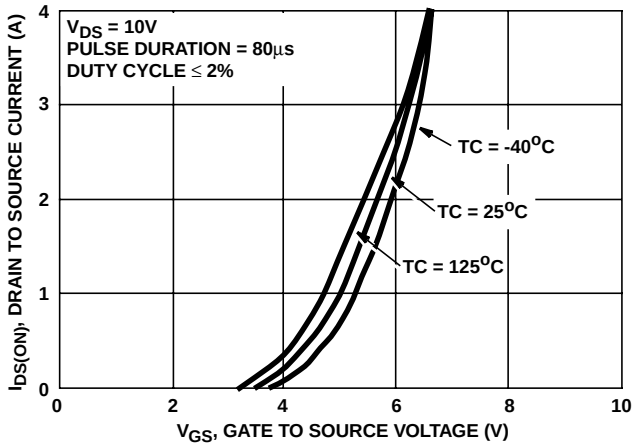


FIGURE 5. TRANSFER CHARACTERISTICS

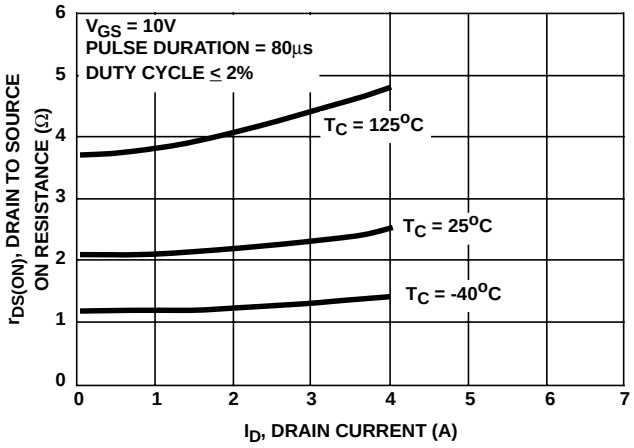


FIGURE 6. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

Typical Performance Curves Unless Otherwise Specified **(Continued)**

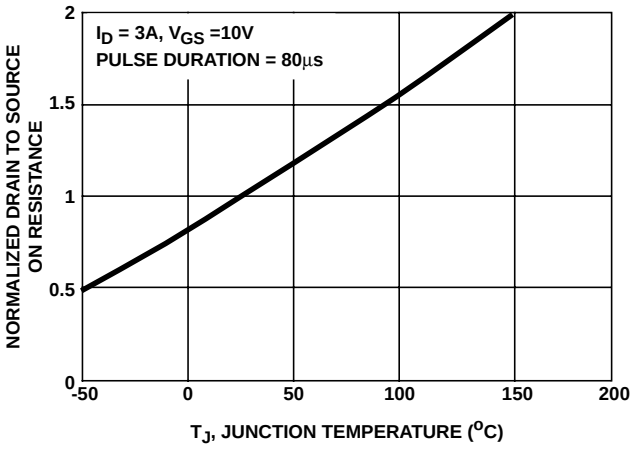


FIGURE 7. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

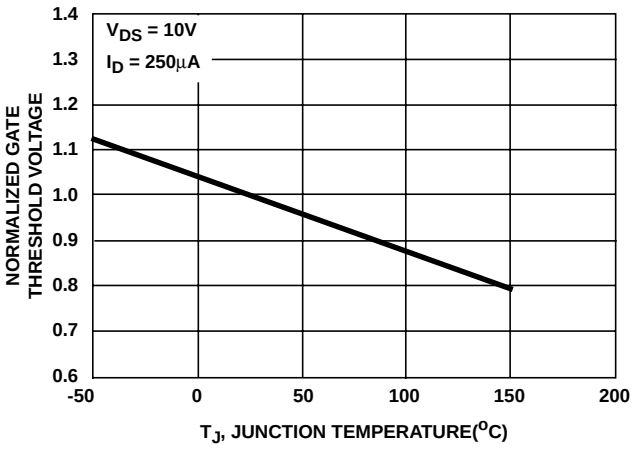


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

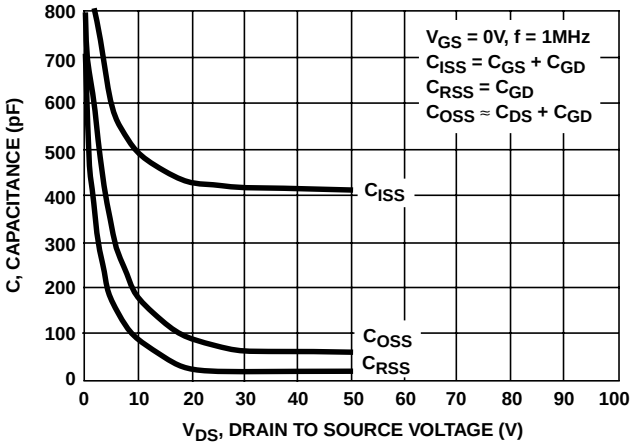
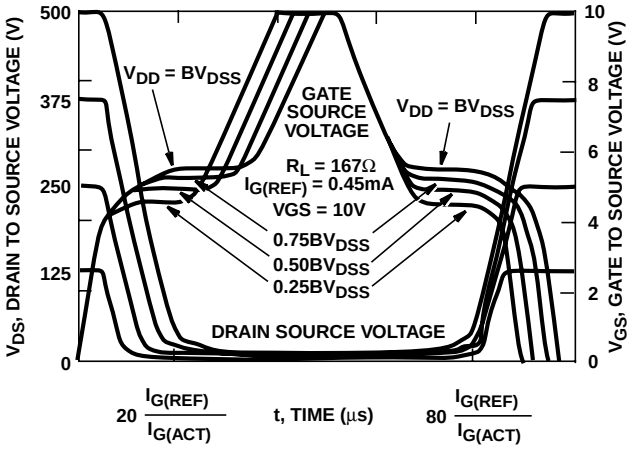


FIGURE 9. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Harris Application Notes AN7254 and AN7260.

FIGURE 10. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

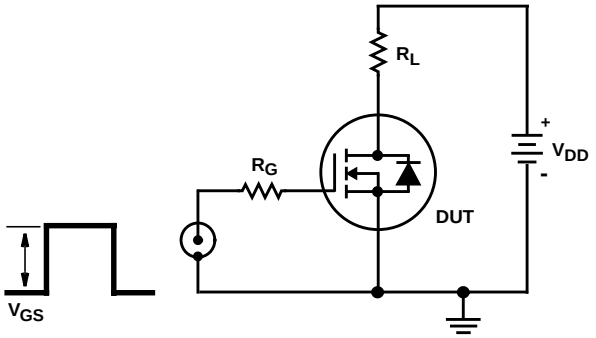


FIGURE 11. SWITCHING TIME TEST CIRCUIT

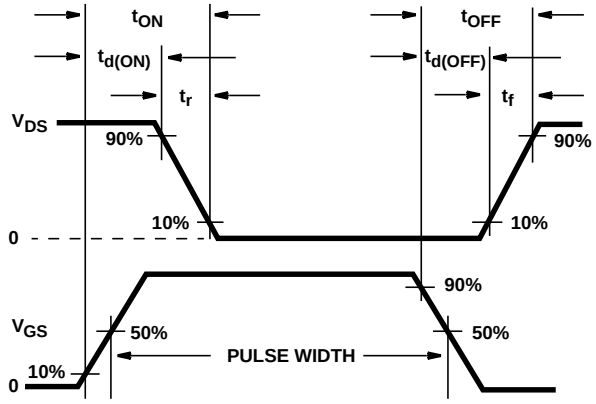


FIGURE 12. RESISTIVE SWITCHING WAVEFORMS

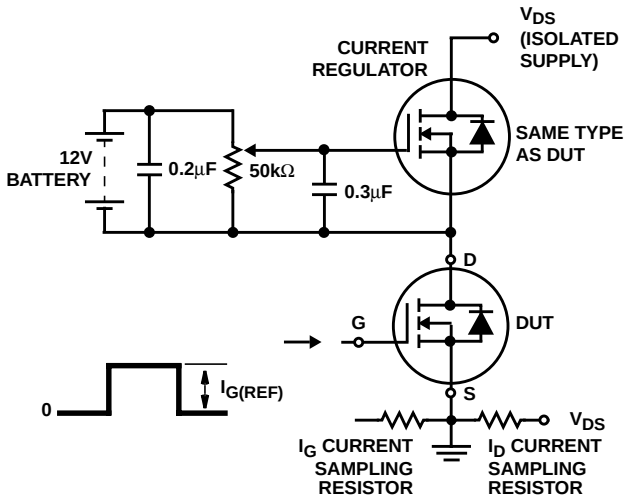


FIGURE 13. GATE CHARGE TEST CIRCUIT

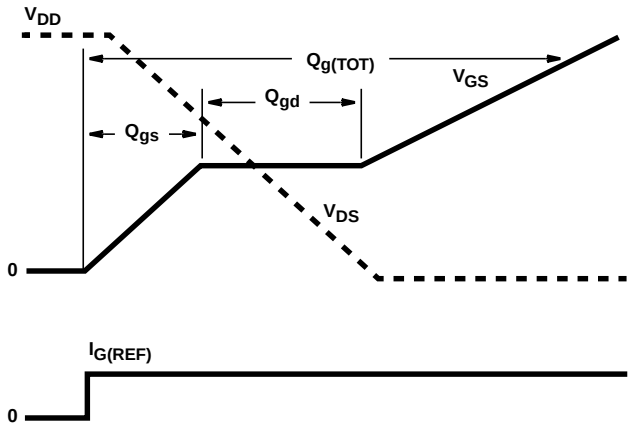


FIGURE 14. GATE CHARGE WAVEFORMS