

**TC74LVX157F, TC74LVX157FN, TC74LVX157FT**

**QUAD 2-CHANNEL MULTIPLEXER**

The TC74LVX157 is a high speed CMOS QUAD 2-CHANNEL MULTIPLEXER fabricated with silicon gate C<sup>2</sup>MOS technology.

Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation. This device is suitable for low voltage and battery operated systems.

This device consist of four 2-input digital multiplexers with common select and strobe inputs.

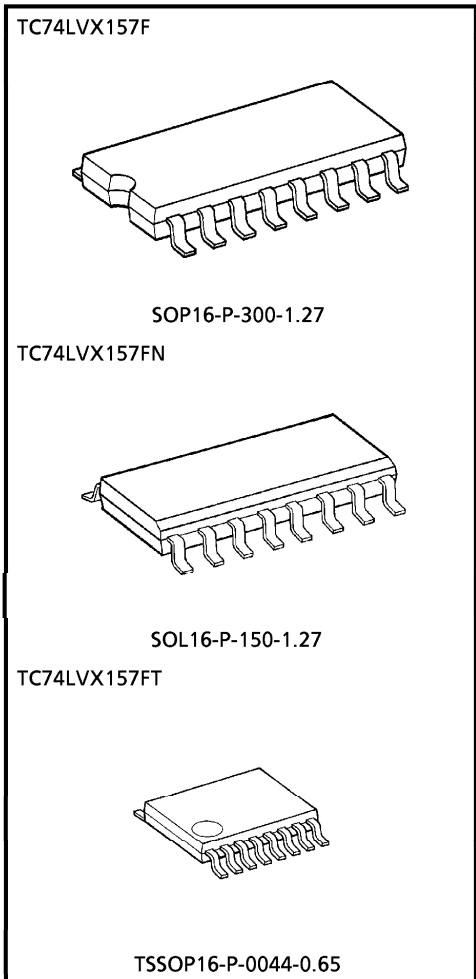
When the  $\overline{\text{STROBE}}$  input is held "H" level, selection of data is inhibited and all the outputs become "L" level. The SELECT decoding determines whether the A or B inputs get routed to their corresponding Y outputs.

An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

**FEATURES**

- High speed :  $t_{pd} = 5.1\text{ns}$  (Typ.) ( $V_{CC} = 3.3\text{V}$ )
- Low power dissipation :  $I_{CC} = 4\mu\text{A}$  (Max.) ( $T_a = 25^\circ\text{C}$ )
- Input voltage level :  $V_{IL} = 0.8\text{V}$  (Max.) ( $V_{CC} = 3\text{V}$ )  
 $V_{IH} = 2.0\text{V}$  (Min.) ( $V_{CC} = 3\text{V}$ )
- Power down protection is provided on all inputs.
- Balanced propagation delays :  $t_{pLH} \approx t_{pHL}$
- Low noise :  $V_{OLP} = 0.5\text{V}$  (Max.)
- Pin and function compatible with 74HC157

(Note) The JEDEC SOP (FN) is not available in Japan.

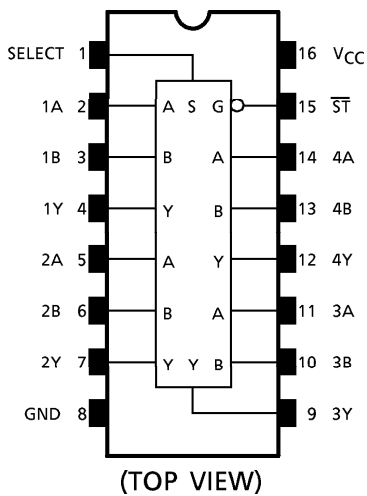


Weight  
 SOP16-P-300-1.27 : 0.18g (Typ.)  
 SOL16-P-150-1.27 : 0.12g (Typ.)  
 TSSOP16-P-0044-0.65 : 0.06g (Typ.)

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**PIN ASSIGNMENT**

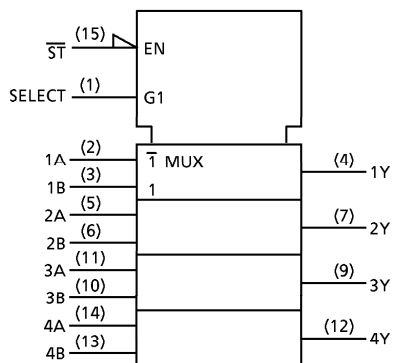


**TRUTHTH TABLE**

INPUTS				OUTPUTS
ST-bar	SELECT	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

X : Don't Care

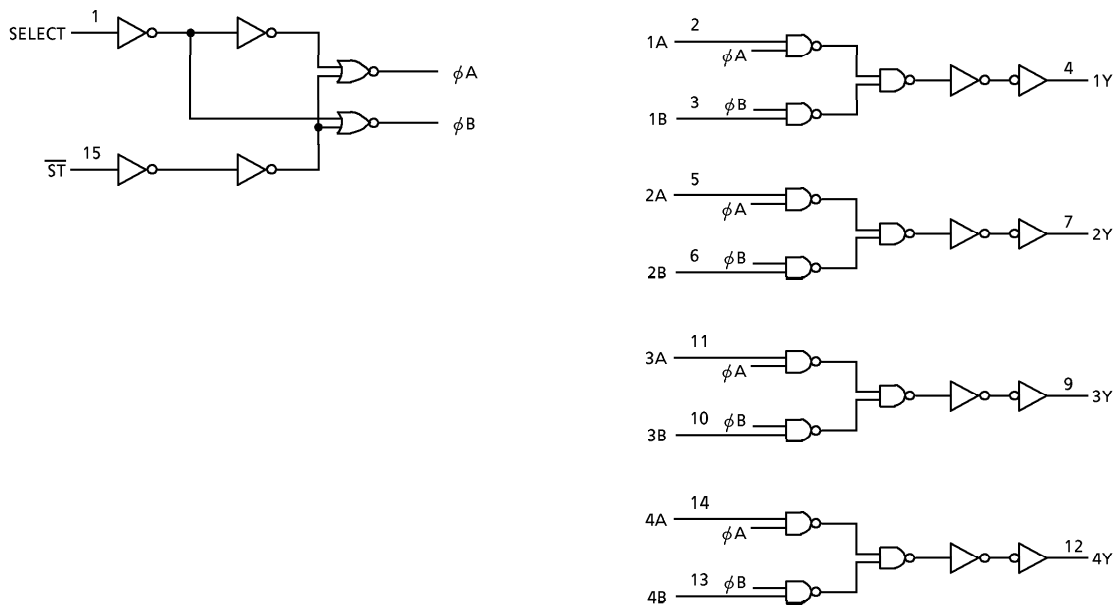
**IEC LOGIC SYMBOL**



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**SYSTEM DIAGRAM**



**MAXIMUM RATINGS**

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage Range	$V_{CC}$	-0.5~7.0	V
DC Input Voltage	$V_{IN}$	-0.5~7.0	V
DC Output Voltage	$V_{OUT}$	-0.5~ $V_{CC}$ +0.5	V
Input Diode Current	$I_{IK}$	-20	mA
Output Diode Current	$I_{OK}$	±20	mA
DC Output Current	$I_{OUT}$	±25	mA
DC $V_{CC}$ /Ground Current	$I_{CC}$	±50	mA
Power Dissipation	$P_D$	180	mW
Storage Temperature	$T_{stg}$	-65~150	°C

**RECOMMENDED OPERATING CONDITIONS**

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	$V_{CC}$	2.0~3.6	V
Input Voltage	$V_{IN}$	0~5.5	V
Output Voltage	$V_{OUT}$	0~ $V_{CC}$	V
Operating Temperature	$T_{opr}$	-40~85	°C
Input Rise And Fall Time	$dt/dv$	0~100	ns/V

**ELECTRICAL CHARACTERISTICS**

DC characteristics

PARAMETER		SYM-BOL	TEST CONDITION		V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40~85°C		UNIT			
						MIN.	TYP.	MAX.	MIN.	MAX.				
Input Voltage	"H" Level	V <sub>IH</sub>			2.0	1.5	—	—	1.5	—	V			
					3.0	2.0	—	—	2.0	—				
					3.6	2.4	—	—	2.4	—				
	"L" Level	V <sub>IL</sub>			2.0	—	—	0.5	—	0.5				
					3.0	—	—	0.8	—	0.8				
					3.6	—	—	0.8	—	0.8				
Output Voltage	"H" Level	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>		I <sub>OH</sub> = -50 μA	2.0	1.9	2.0	—	1.9	—	V		
					I <sub>OH</sub> = -50 μA	3.0	2.9	3.0	—	2.9	—			
					I <sub>OH</sub> = -4mA	3.0	2.58	—	—	2.48	—			
	"L" Level	V <sub>OL</sub>			V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>		I <sub>OL</sub> = 50 μA	2.0	—	0.0	0.1		—	0.1
							I <sub>OL</sub> = 50 μA	3.0	—	0.0	0.1		—	0.1
							I <sub>OL</sub> = 4mA	3.0	—	—	0.36		—	0.44
Input Leakage Current		I <sub>IN</sub>	V <sub>IN</sub> = 5.5V or GND				3.6	—	—	±0.1	—	±1.0	μA	
Quiescent Supply Current		I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND				3.6	—	—	4.0	—	40.0	μA	

AC characteristics (Input  $t_r = t_f = 3\text{ns}$ )

PARAMETER	SYM-BOL	TEST CONDITION			Ta = 25°C			Ta = -40~85°C		UNIT
			V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (A, B-Y)	t <sub>pLH</sub>		2.7	15	—	6.6	12.5	1.0	15.5	ns
				50	—	9.1	16.0	1.0	19.0	
	3.3 ± 0.3		15	—	5.1	7.9	1.0	9.5		
			50	—	7.6	11.4	1.0	13.0		
Propagation Delay Time (SELECT-Y)	t <sub>pLH</sub>		2.7	15	—	8.9	16.9	1.0	20.5	ns
				50	—	11.4	20.4	1.0	24.0	
	3.3 ± 0.3		15	—	7.0	11.0	1.0	13.0		
			50	—	9.5	14.5	1.0	16.5		
Propagation Delay Time (ST-Y)	t <sub>pLH</sub>		2.7	15	—	9.1	17.6	1.0	20.5	ns
				50	—	11.6	21.1	1.0	24.0	
	3.3 ± 0.3		15	—	7.2	11.5	1.0	13.5		
			50	—	9.7	15.0	1.0	17.0		
Output To Output Skew	t <sub>osLH</sub>	(Note 1)	2.7	50	—	—	1.5	—	1.5	ns
	t <sub>osHL</sub>		3.3 ± 0.3	50	—	—	1.5	—	1.5	
Input Capacitance	C <sub>IN</sub>	(Note 2)			—	4	10	—	10	pF
Power Dissipation Capacitance	C <sub>PD</sub>	(Note 3)			—	20	—	—	—	pF

(Note 1) Parameter guaranteed by design.

$$(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$$

(Note 2) Parameter guaranteed by design.

(Note 3) C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr.}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per bit)}$$

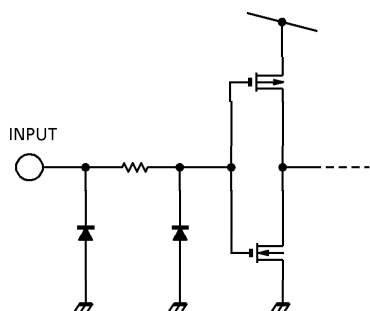
And the total C<sub>PD</sub> when n pcs. of gate operate can be gained by the following equation :

$$C_{PD}(\text{total}) = 13 + 7 \cdot n$$

Noise characteristics (Ta = 25°C, Input tr = tf = 3ns, CL = 50pF)

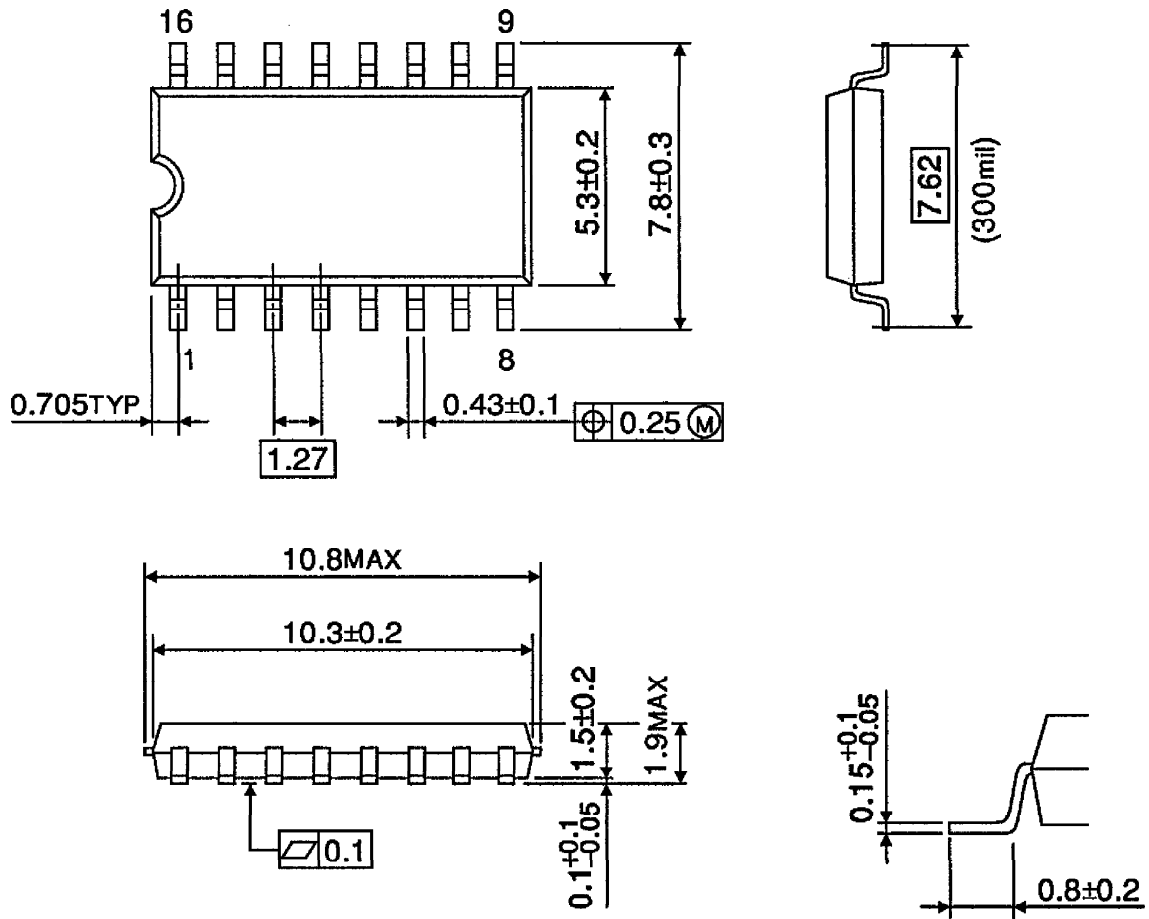
PARAMETER	SYMBOL	TEST CONDITION	VCC (V)	TYP.	LIMIT	UNIT
			3.3			
Quiet Output Maximum Dynamic VOL	VOLP		3.3	0.3	0.5	V
Quiet Output Minimum Dynamic VOL	VOLV		3.3	-0.3	-0.5	V
Minimum High Level Dynamic Input Voltage	VIHD		3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	VILD		3.3	—	0.8	V

**INPUT EQUIVALENT CIRCUIT**



OUTLINE DRAWING  
SOP16-P-300-1.27

Unit : mm

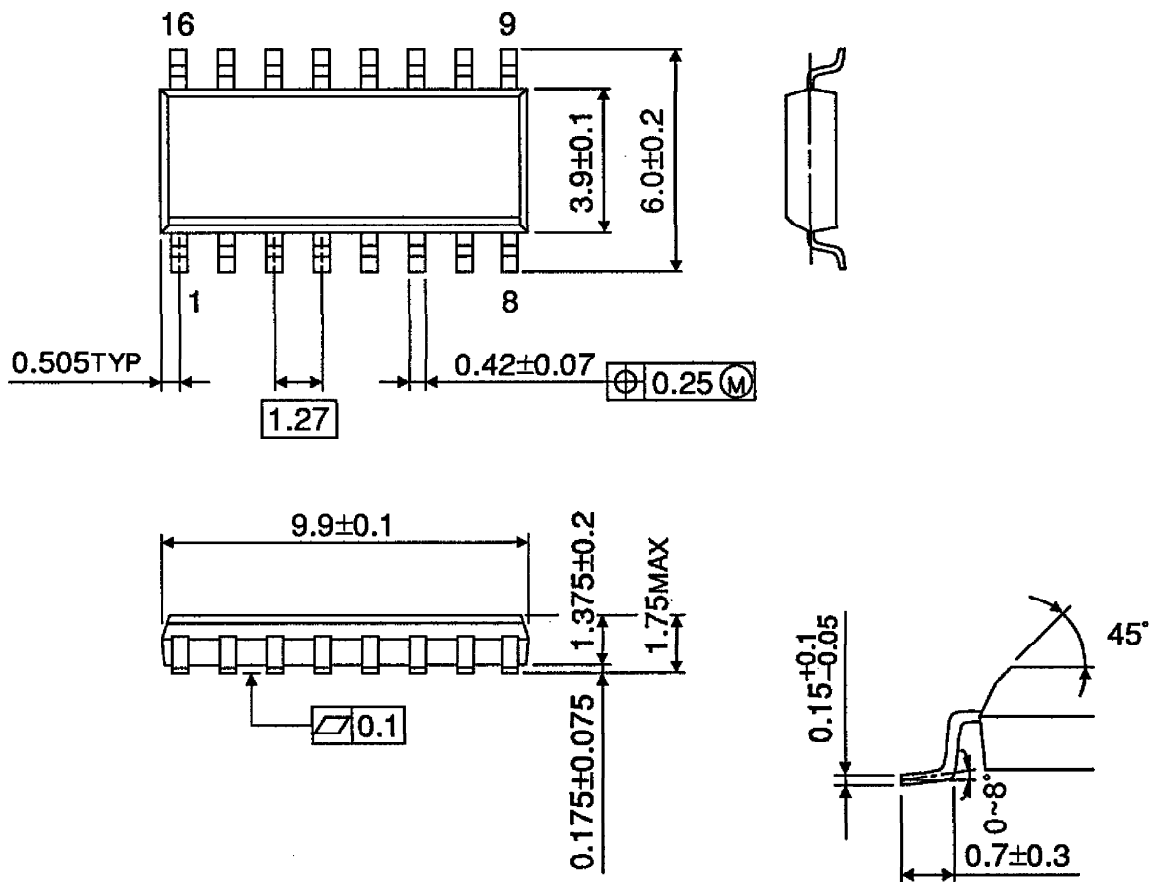


Weight : 0.18g (Typ.)

**OUTLINE DRAWING**  
SOL16-P-150-1.27

Unit : mm

(Note) This package is not available in Japan.

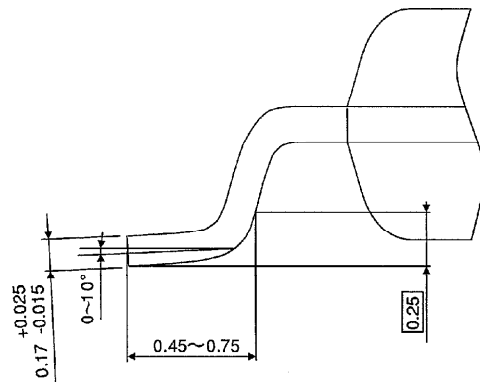
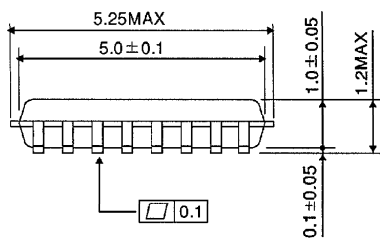
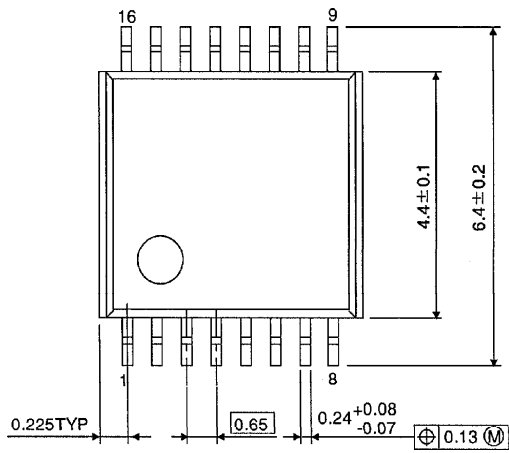


Weight : 0.12g (Typ.)



**OUTLINE DRAWING**  
TSSOP16-P-0044-0.65

Unit : mm



Weight : 0.06g (Typ.)