SIEMENS

3.3V 8M x 64-Bit SDRAM Module — HYS64V8000GU-10
3.3V 8M x 72-Bit SDRAM Module — HYS72V8000GU-10

168 pin unbuffered DIMM Modules

- 168 Pin JEDEC Standard, Unbuffered 8 Byte Dual-In-Line SDRAM Modules for PC main memory applications
- 1 bank 8M x 64, 8M x 72 organisation
- Optimized for byte-write non-parity or ECC applications
- Fully PC66 layout compatible
- JEDEC standard Synchronous DRAMs (SDRAM)
- Performance:

		-10
f_{CK}	Max. Clock frequency	66 MHz @ CL=2 100 MHz @ CL=3
t_{AC}	Max. access time from clock	8 ns @ CL=2 7 ns @ CL=3

- Single +3.3V(± 0.3V) power supply
- Programmable $\overline{\text{CAS}}$ Latency, Burst Length and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- Decoupling capacitors mounted on substrate
- All inputs, outputs are LVTTL compatible
- Serial Presence Detect with E^2PROM
- Utilizes eight / nine 8M x 8 SDRAMs in TSOPII-54 packages
- 4096 refresh cycles every 64 ms
- Gold contact pad
- Card Size: 133,35mm x 25,40mm x 4,00 mm

The HYS64(72)V8000GU-10 are industry standard 168-pin 8-byte Dual in-line Memory Modules (DIMMs) which are organised as 8M x 64 and 8M x 72 high speed memory arrays designed with Synchronous DRAMs (SDRAMs) for non-parity and ECC applications. The DIMMs use eight 8M x 8 SDRAMs for the 8M x 64 organisation and an additional SDRAM for the 8M x 72 organisation. Decoupling capacitors are mounted on the PC board.

The DIMMs have a serial presence detect, implemented with a serial E ^{2}PROM using the two pin I^{2}C protocol. The first 128 bytes are utilized by the DIMM manufacturer and the second 128 bytes are available to the end user.

All SIEMENS 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 133,35 mm long footprint.

Ordering Information

Type	Ordering Code	Package	Descriptions
HYS 64V8000GU-10		L-DIM-168-23	PC66 8M x 64 SDRAM module
HYS 72V8000GU-10		L-DIM-168-23	PC66 8M x 72 SDRAM module

Pin Names

A0-A11	Address Inputs(RA0 ~ RA11 / CA0 ~ CA8)
BA0,BA1	Bank Selects
DQ0 - DQ63	Data Input/Output
CB0-CB7	Check Bits (x72 organisation only)
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read / Write Input
$\overline{CKE0}$	Clock Enable
CLK0, CLK1	Clock Input
DQMB0 - DQMB7	Data Mask
$\overline{CS0}$ - $\overline{CS3}$	Chip Select
Vcc	Power (+3.3 Volt)
Vss	Ground
SCL	Clock for Presence Detect
SDA	Serial Data Out for Presence Detect
N.C.	No Connection

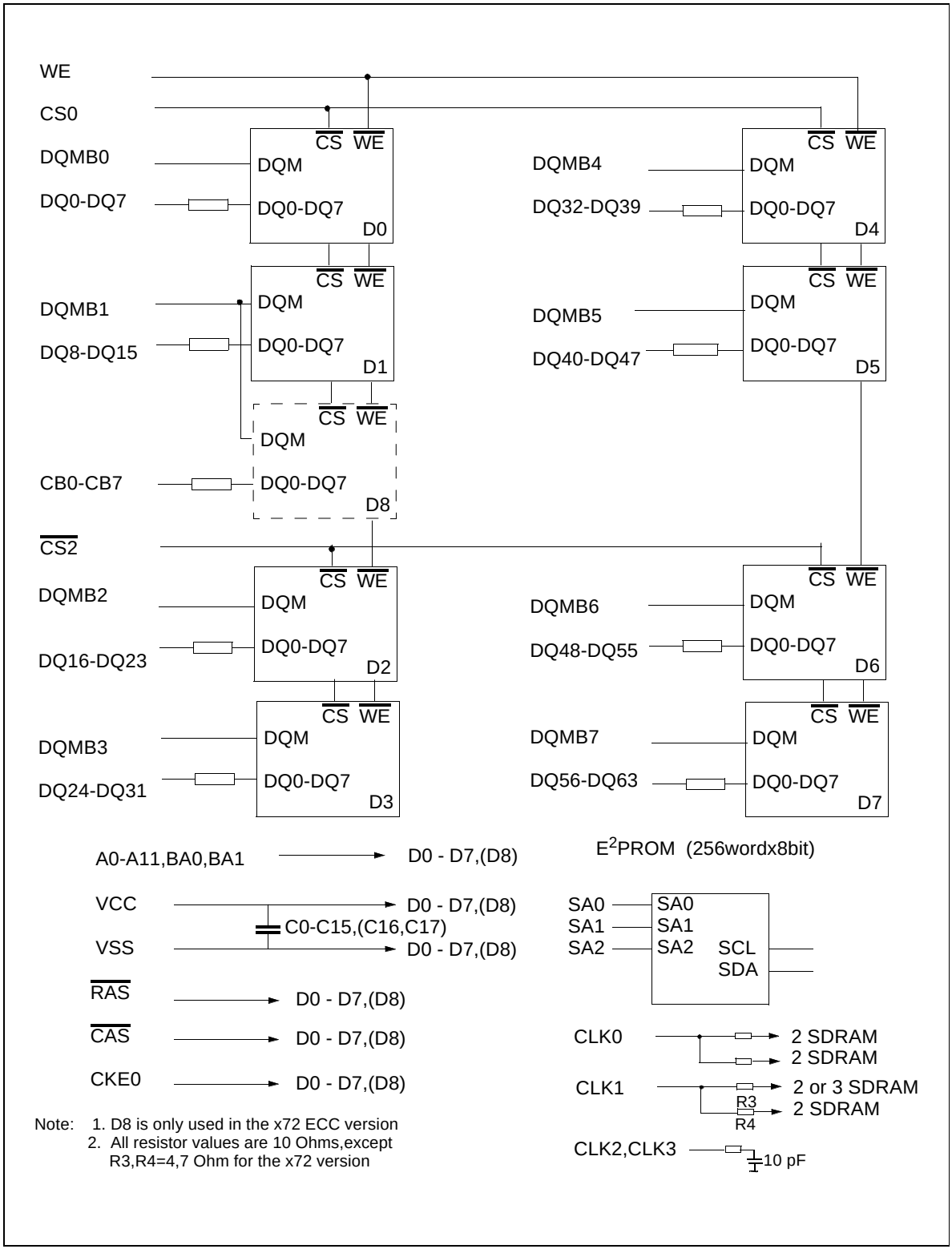
Address Format:

	Part Number	Rows	Columns	Bank Select	Refresh	Period	Interval
8M x 64	HYS 64V8000GU	12	9	2	4k	64 ms	15,6 µs
8M x 72	HYS 72V8000GU	12	9	2	4k	64 ms	15,6 µs

Pin Configuration

PIN #	Symbol	PIN #	Symbol		PIN #	Symbol	PIN #	Symbol
1	VSS	43	VSS		85	VSS	127	VSS
2	DQ0	44	DU		86	DQ32	128	CKE0
3	DQ1	45	CS2		87	DQ33	129	NC
4	DQ2	46	DQMB2		88	DQ34	130	DQMB6
5	DQ3	47	DQMB3		89	DQ35	131	DQMB7
6	VCC	48	DU		90	VCC	132	NC
7	DQ4	49	VCC		91	DQ36	133	VCC
8	DQ5	50	NC		92	DQ37	134	NC
9	DQ6	51	NC		93	DQ38	135	NC
10	DQ7	52	NC (CB2)		94	DQ39	136	CB6
11	DQ8	53	NC (CB3)		95	DQ40	137	CB7
12	VSS	54	VSS		96	VSS	138	VSS
13	DQ9	55	DQ16		97	DQ41	139	DQ48
14	DQ10	56	DQ17		98	DQ42	140	DQ49
15	DQ11	57	DQ18		99	DQ43	141	DQ50
16	DQ12	58	DQ19		100	DQ44	142	DQ51
17	DQ13	59	VCC		101	DQ45	143	VCC
18	VCC	60	DQ20		102	VCC	144	DQ52
19	DQ14	61	NC		103	DQ46	145	NC
20	DQ15	62	DU		104	DQ47	146	DU
21	NC (CB0)	63	NC		105	NC (CB4)	147	NC
22	NC (CB1)	64	VSS		106	NC (CB5)	148	VSS
23	VSS	65	DQ21		107	VSS	149	DQ53
24	NC	66	DQ22		108	NC	150	DQ54
25	NC	67	DQ23		109	NC	151	DQ55
26	VCC	68	VSS		110	VCC	152	VSS
27	WE	69	DQ24		111	CAS	153	DQ56
28	DQMB0	70	DQ25		112	DQMB4	154	DQ57
29	DQMB1	71	DQ26		113	DQMB5	155	DQ58
30	CS0	72	DQ27		114	NC	156	DQ59
31	DU	73	VCC		115	RAS	157	VCC
32	VSS	74	DQ28		116	VSS	158	DQ60
33	A0	75	DQ29		117	A1	159	DQ61
34	A2	76	DQ30		118	A3	160	DQ62
35	A4	77	DQ31		119	A5	161	DQ63
36	A6	78	VSS		120	A7	162	VSS
37	A8	79	CLK2		121	A9	163	CLK3
38	A10	80	NC		122	BA0	164	NC
39	BA1	81	NC		123	A11	165	SA0
40	VCC	82	SDA		124	VCC	166	SA1
41	VCC	83	SCL		125	CLK1	167	SA2
42	CLK0	84	VCC		126	NC	168	VCC

Note : Pinnames in brackets are for the x72 ECC versions



Note: 1. D8 is only used in the x72 ECC version
2. All resistor values are 10 Ohms,except R3,R4=4,7 Ohm for the x72 version

Block Diagram for 8M x 64/72 SDRAM DIMM modules

DC Characteristics

T_A = 0 to 70 °C; V_{SS} = 0 V; $V_{DD,}V_{DDQ}$ = 3.3 V ± 0.3 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input high voltage	V_{IH}	2.0	Vcc+0.3	V
Input low voltage	V_{IL}	– 0.5	0.8	V
Output high voltage (I_{OUT} = – 2.0 mA)	V_{OH}	2.4	–	V
Output low voltage (I_{OUT} = 2.0 mA)	V_{OL}	–	0.4	V
Input leakage current, any input (0 V < V_{IN} < 3.6 V, all other inputs = 0 V)	$I_{I(L)}$	– 40	40	µA
Output leakage current (DQ is disabled, 0 V < V_{OUT} < V_{CC})	$I_{O(L)}$	– 40	40	µA

Capacitance

T_A = 0 to 70 °C; V_{DD} = 3.3 V ± 0.3 V, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min. (x64)	max. (x72)	
Input capacitance (A0 to A11, BS0, BS1 $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{I1}	45	55	pF
Input capacitance (CS0 - CS3)	C_{I2}	20	25	pF
Input capacitance (CLK0 - CLK3)	C_{I3}	38	38	pF
Input capacitance (DQMB0 - DQMB7)	C_{I4}	13	13	pF
Input / Output capacitance (DQ0-DQ63,CB0-CB7)	C_{IO}	12	12	pF
Input Capacitance (SCL,SA0-2)	C_{sc}	8	8	pF
Input/Output Capacitance	C_{sd}	10	10	pF

Operating Currents (T_A = 0 to 70°C, VCC = 3.3V ± 0.3V

(Recommended Operating Conditions unless otherwise noted)

Parameter & Test Condition		Symb.	x64	x72		Note
			max.			
OPERATING CURRENT trc=trcmin., tck=tckmin. Active-precharge command cycling, without burst operation	1 bank operation	ICC1	880	990	mA	7
PRECHARGE STANDBY CURRENT in Power Down Mode	tck = min.	ICC2P	24	27	mA	7
$\overline{CS}$ =VIH (min.), CKE<=Vil(max)	tck = Infinity	ICC2PS	16	18	mA	
PRECHARGE STANDBY CURRENT in Non-Power Down Mode	tck = min.	ICC2	400	450	mA	7
$\overline{CS}$ = VIH (min.), CKE>=Vih(min)	tck = Infinity	ICC2S	40	45	mA	
NO OPERATING CURRENT	CKE>=VIh(min.)	ICC3	560	630	mA	
tck = min., $\overline{CS}$ = VIH(min), active state (max. 4 banks)	CKE<=VIl(max.) (Power down mode)	ICC3P	64	72	mA	
BURST OPERATING CURRENT tck = min., Read/Write command cycling		ICC4	1240	1395	mA	7,8
AUTO REFRESH CURRENT tck = min., Auto Refresh command cycling		ICC5	1040	1170	mA	7
SELF REFRESH CURRENT Self Refresh Mode, CKE=0.2V		ICC6	16	18	mA	

Notes:

7. These parameters depend on the cycle rate and these values are measured by the cycle rate under the .....minimum value of tck and trc. Input signals are changed one time during tck.

8. These parameter depend on output loading. Specified values are obtained with output open.

AC Characteristics 1)2)3)
T_A = 0 to 70 °C; V_{SS} = 0 V; V_{CC} = 3.3 V ± 0.3 V, t_T = 1 ns

Parameter	Symbol	Limit Values		Unit	
		-10			
		min	max		
Clock and Clock Enable					
Clock Cycle Time					
$\overline{CAS}$ Latency = 3	t_{CK}	10	–	ns	
$\overline{CAS}$ Latency = 2		15	–	ns	
Clock Frequency					
$\overline{CAS}$ Latency = 3	t_{CK}	–	100	MHz	
$\overline{CAS}$ Latency = 2		–	66	MHz	
Access Time from Clock					
$\overline{CAS}$ Latency = 3	t_{AC}	–	7	ns	4
$\overline{CAS}$ Latency = 2		–	8	ns	
Clock High Pulse Width	t_{CH}	3	–	ns	
Clock Low Pulse Width	t_{CL}	3	–	ns	
Transition time	t_T	0.5	10	ns	
Setup and Hold Times					
Command Setup Time	t_{CS}	2.5	–	ns	5
Address Setup Time	t_{AS}	2.5	–	ns	5
Data In Setup Time	t_{DS}	2.5	–	ns	5
CKE Setup Time	t_{CKS}	2.5	–	ns	5
Command Hold Time	t_{CH}	1	–	ns	5
Address Hold Time	t_{AH}	1	–	ns	5
Data In Hold Time	t_{DH}	1	–	ns	5
CKE Hold Time	t_{CKH}	1	–	ns	5
Common Parameters					
Row to Column Delay Time	t_{RCD}	30	–	ns	6
Row Active Time	t_{RAS}	60	100k	ns	6
Row Cycle Time	t_{RC}	90	–	ns	6
Row Precharge Time	t_{RP}	30	–	ns	6

Parameter	Symbol	Limit Values		Unit	
		-10			
		min	max		
Activate(a) to Activate(b) Command period	t_{RRD}	20	–	ns	6
$\overline{CAS}$(a) to $\overline{CAS}$(b) Command period	t_{CCD}	1	–	CLK	
Mode Register Set-up time	t_{RSC}	20	–	ns	
Power Down Mode Entry Time	t_{SB}	0	10	ns	
Refresh Cycle					
Refresh Period (4096 cycles)	t_{REF}	–	64	ms	
Self Refresh Exit Time	t_{SREX}	10			
Read Cycle					
Data Out Hold Time	t_{OH}	3	–	ns	
Data Out to Low Impedance Time	t_{LZ}	0	–	ns	
Data Out to High Impedance Time	t_{HZ}	3	10	ns	8
DQM Data Out Disable Latency	t_{DQZ}	2	–	CLK	
Write Cycle					
Write Recovery Time					
$\overline{CAS}$ Latency = 3	t_{WR}	10	–	ns	
$\overline{CAS}$ Latency = 2		15	–	ns	
DQM Write Mask Latency	t_{DQW}	0	–	CLK	

Notes:

1. The specified values are valid when addresses are changed no more than once during tck(min.) and when No Operation commands are registered on every rising clock edge during tRC(min).
2. The specified values are valid when data inputs (DQs) are stable during tRC(min.).
3. An initial pause of 100µs is required after power-up, then a Precharge All Banks command must be given followed by 8 Auto Refresh (CBR) cycles before the Mode Register Set Operation can begin.
4. AC timing tests have V_{il} = 0.4 V and V_{ih} = 2.4 V with the timing referenced to the 1.4 V crossover point. The transition time is measured between V_{ih} and V_{il}. All AC measurements assume t_T=1ns with the AC output load circuit shown.

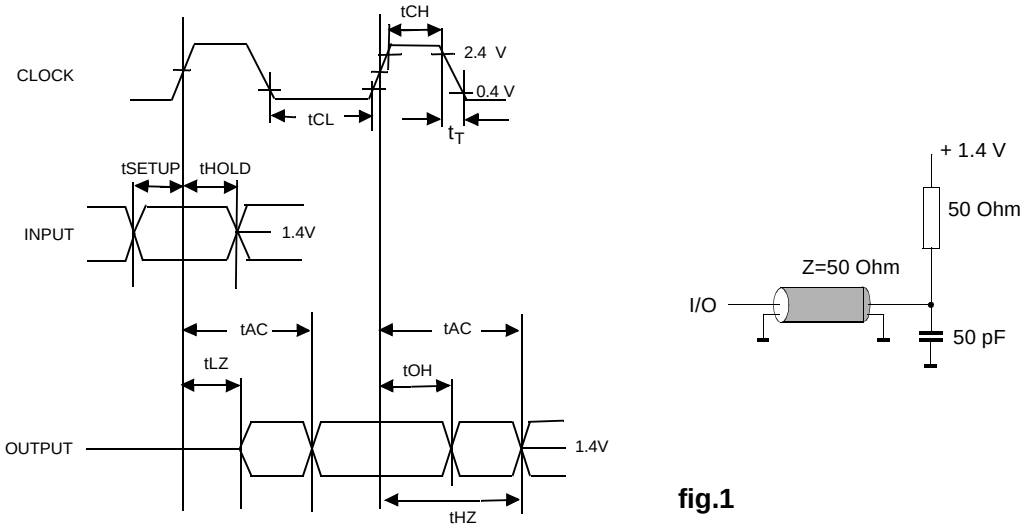


fig.1

5. If clock rising time is longer than 1 ns, a time (t_T/2 -0.5) ns has to be added to this parameter.
6. If t_T is longer than 1 ns, a time (t_T -1) ns has to be added to this parameter.
7. Any time that the refresh Period has been exceeded, a minimum of two Auto (CBR) Refresh commands must be given to "wake-up" the device.
8. Self Refresh Exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to tRC is satisfied once the Self Refresh Exit command is registered.
9. Referenced to the time which the output achieves the open circuit condition, not to output voltage levels.

A serial presence detect storage device - E^2PROM - is assembled onto the module. Information about the module configuration, speed, etc. is written into the E^2PROM device during module production using a serial presence detect protocol (I^2C synchronous 2-wire bus)

SPD-Table:

Byte#	Description	SPD Entry Value	Hex	
			x64 -10	x72 -10
0	Number of SPD bytes	128	80	80
1	Total bytes in Serial PD	256	08	08
2	Memory Type	SDRAM	04	04
3	Number of Row Addresses (without BS bits)	12	0C	0C
4	Number of Column Addresses (for x 8 SDRAM)	9	09	09
5	Number of DIMM Banks	1	01	01
6	Module Data Width	64 / 72	40	48
7	Module Data Width (cont'd)	0	00	00
8	Module Interface Levels	LVTTL	01	01
9	SDRAM Cycle Time at CL=3	10 ns	A0	A0
10	SDRAM Access time from Clock at CL=3	7.0 ns	70	70
11	Dimm Config (Error Det/Corr.)	none / ECC	00	02
12	Refresh Rate/Type	Self-Refresh, 15.6µs	80	80
13	SDRAM width, Primary	x8	08	08
14	Error Checking SDRAM data width	n/a / x8	00	08
15	Minimum clock delay for back-to-back random column address	t_{ccd} = 1 CLK	01	01
16	Burst Length supported	1, 2, 4, 8 & full page	8F	8F
17	Number of internal SDRAM banks	4	04	04
18	Supported CAS Latencies	$\overline{CAS}$ latencies = 2,3	06	06
19	CS Latencies	CS latency = 0	01	01
20	WE Latencies	Write latency = 0	01	01
21	SDRAM DIMM module attributes	non buffered/non reg.	00	00
22	SDRAM Device Attributes :General	Vcc tol +/- 10%	06	06
23	SDRAM Cycle Time at CL = 2	15 ns	F0	F0
24	SDRAM Acces TIme from Clock at CL=2	8.0 ns	80	80
25	SDRAM Cycle Time at CL = 1	not supported	FF	FF
26	SDRAM Acces TIme from Clock at CL=1	not supported	FF	FF
27	Minimum Row Precharge Time	30 ns	1E	1E
28	Minimum Row Active to Row Active delay tRRD	20 ns	14	14

SPD-Table (cont'd)

Byte#	Description	SPD Entry Value	Hex	
			x64 -10	x72 -10
29	Minimum RAS to CAS delay tRCD	30 ns	1E	1E
30	Minimum RAS pulse width tRAS	45 ns	2D	2D
31	Module Bank Density (per bank)	64 MByte	10	10
32-61	Superset information (may be used in future)		FF	FF
62	SPD Revision	Revision 1.2a	12	12
63	Checksum for bytes 0 - 62		7A	8C
64-127	Manufacturer's information (optional) (FFh if not used)		FF	FF
128+	Unused storage locations		FF	FF

L-DIM-168-23
SDRAM DIMM Module package