L9214A/G
Low-Cost Ringing SLIC

Introduction

The Agere Systems Inc. L9214 is a subscriber line interface circuit that is optimized to provide a very low-cost solution for short- and medium-loop applications. This device provides the complete set of line interface functionality, including power ringing needed to interface to a subscriber loop. This device has the capability to operate with a V_{CC} supply of 3.3 V or 5 V and is designed to minimize external components required at all device interfaces.

Features

- Low-cost solution
- Onboard ringing generation with software adjustable crest factor switching
- Flexible V_{CC} options:
  — 3.3 V or 5 V V_{CC}
  — No –5 V required
- Power control options:
  — Power control resistor
  — Automatic battery switch to minimize off-hook power
- Eight operating states:
  — Scan mode for minimal power dissipation
  — Forward and reverse battery active
  — On-hook transmission states
  — Ring mode
  — Disconnect mode
- Low on-hook power:
  — 25 mW scan mode
  — 165 mW active mode
- Two SLIC gain options to minimize external components in codec interface
- Loop start, ring trip, and ground key detectors
- Programmable current limit
- On-hook and scan mode line voltage clamp
- Thermal protection
- 48-pin MLCC, 32-pin PLCC, and 28-pin SOG (Please contact your Agere Sales Representative for availability) packages

Applications

- Voice over Internet Protocol (VoIP)
- Cable Modems
- Terminal Adapters (TA)
- Wireless Local Loop (WLL)
- *Telcordia Technologies*™ GR-909 Access
- Network Termination (NT)
- PBX
- Key Systems

Description

This device is optimized to provide battery feed, ringing, and supervision on short- and medium-loop plain old telephone service (POTS) loops. Supported round trip loop length is up to 1000 Ω.

This device provides power ring to the subscriber by the use of line reversal to create either a sine wave ringing signal with a PWM input or a trapezoidal ringing signal with a selectable crest factor from a square wave input. It provides forward and reverse battery feed states, on-hook transmission, a low-power scan state, and a forward disconnect state.

The device requires a V_{CC} and line feed battery to operate. V_{CC} may be either a 3.3 V or a 5 V supply. The ringing signal is derived from the high-voltage battery. An automatic battery switch is included to allow for use of a second lower voltage battery in the off-hook mode, thus minimizing short-loop off-hook power consumption and dissipation. If the user desires single battery operation, a power resistor is required to reduce the power dissipation in the SLIC.

Loop closure, ring trip, and ground key detectors are available. The loop closure detector has a fixed threshold with hysteresis. The ring trip detector and ground key detector threshold and time constants are externally set.

The dc current limit is programmed by an external resistor, the maximum current limit determined by the Vcc supply.

The overhead voltage for this device is fixed and the device is capable of supporting 3.17 dB into a 600 Ω load with minimal overhead.

The device is offered with two gain options. This allows for an optimized codec interface, with minimal external components regardless of whether a first-generation or a programmable third-generation codec is used.

Table of Contents

Table of Contents (continued)

Figures

Tables

Features

- Onboard balanced trapezoidal ringing generation, 40 Vrms, 1.2 crest factor:
  - — 3 REN ring load (2330 Ω + 24 μF), 600 Ω loop
  - — 2 REN ring load (3500 Ω + 16 μF), 1000 Ω loop
  - — 2 REN ring load (3500 Ω + 1.8 μF), 500 Ω loop
  - — No ring relay
  - — No bulk ring generator required
  - — 15 Hz to 70 Hz ring frequency supported
- Power supplies requirements:
  - — V_{CC} talk battery and ringing battery required
  - — No –5 V supply required
  - — No high-voltage positive supply required
- Flexible Vcc options:
  - — 3.3 V or 5 V V_{CC} operation
  - — 3.3 V or 5 V V_{CC} interchangeable and transparent to users
- Power control options:
  - — Automatic battery switch
  - — Power control resistor
- Minimal external components required
- Ten operating states:
  - — Forward active, fast polarity reversal
  - — Reverse active, fast polarity reversal
  - — Forward active, slow polarity reversal
  - — Reverse active, slow polarity reversal
  - — Scan
  - — Disconnect
  - — Ringing, line forward with high slope
  - — Ringing, line reverse with high slope
  - — Ringing, line forward with low slope
  - — Ringing, line reverse with low slope
- Unlatched parallel data control interface
- Low SLIC power:
  - — Scan 24 mW (V_{CC} = 5.0 V)
  - — Forward/reverse active 148 mW (V_{CC} = 5.0 V)
  - — Scan 17 mW (V_{CC} = 3.3 V)
  - — Forward/reverse on-hook 135 mW (V_{CC} = 3.3 V)
- Supervision:
  - — Loop start, fixed threshold with hysteresis
  - — Ring trip filtering, fixed threshold not a function of battery voltage, user adjustable with an external resistor
  - — Common-mode current for ground key applications, user-adjustable threshold
- Adjustable current limit:
  - — 10 mA to 45 mA programming range at 5 V Vcc
  - — 10 mA to 35 mA programming range at 3.3 V Vcc
- Overhead voltage:
  - — Automatically adjusted in active mode
  - — Clamped <56.5 V in scan and on-hook modes
- Thermal shutdown protection with hysteresis
- Longitudinal balance:
  - — ETSI/ITU-T balance
  - — GR-909
- Meter pulse compatible
- ac interface:
  - — Two SLIC gain options to minimize external components required for interface to first- or third-generation codecs
  - — Sufficient dynamic range for direct coupling to codec output
- 28-pin SOG, 32-pin PLCC, and 48-pin MLCC package options
- 90 V CBIC-S technology

Description

The L9214 is designed to provide battery feed, ringing, and supervision functions on short and medium plain old telephone service (POTS) loops. Supported round-trip loop length is up to 1000 Ω of wiring resistance plus handset or ringing load. This device is designed to minimize power in all operating states.

The L9214 offers eight operating states. The device assumes use of a lower-voltage talk battery, a higher-voltage ringing battery and a single V_{CC} supply.

The L9214 requires only a positive V_{CC} supply. No –5 V supply is needed. The L9214 can operate with a V_{CC} of either 5.0 V or 3.3 V, allowing for greater user flexibility. The choice of V_{CC} voltage is transparent to the user; the device will function with either supply voltage connected.

Two batteries may be used:

1. A high-voltage ring battery (V_{BAT1}). V_{BAT1} is a maximum –70 V and is used for power ringing, scan, and on-hook transmission modes. This supply is current limited to the maximum power ringing current of approximately 90 mApeak.
2. A lower-voltage talk battery (V_{BAT2}). V_{BAT2} is normally used for active mode powering.

Alternatively, operation may be from a single high-voltage battery supply with a power control resistor to reduce the power dissipation in the SLIC.

Description (continued)

Forward and reverse battery active modes are used for off-hook conditions. Since this device is designed for short- and medium-loop applications, the lower-voltage V_{BAT2} is normally applied during the forward and reverse active states. Battery reversal is quiet, without breaking the ac path. The rate of battery reversal may be ramped to control switching time.

The magnitude of the overhead voltage in the forward and reverse active modes allows for an undistorted signal of 3.17 dBm into 600 Ω. The ring trip detector is turned off during active modes to conserve power.

On-hook transmission is not permitted in the scan mode. In this mode, the tip ring voltage is derived from the higher V_{BAT1} rather than V_{BAT2}.

In the scan and active modes, the overhead voltage is set such that the tip/ring open loop voltage is 42.5 V minimum for a primary battery of 63 V to 70 V for compatibility with maintenance termination units (MTUs). Also, the maximum voltage with respect to ground (tip or ring to ground) is 56.5 V to comply with *UL*™ 1950/60950 ANNEX M.2 method B and *IEC*® 60950 (quiet interval of ringing). If the primary battery is below –63 V, the magnitude of the tip/ring open circuit voltage is approximately 17 V less than the battery.

To minimize on-hook power, a low-power scan mode is available. In this mode, all functions except off-hook supervision are turned off to conserve power. On-hook transmission is not allowed in the scan mode.

A forward disconnect mode is provided, where all circuits are turned off and power is denied to the loop.

The device offers a ring mode, in which a power ring signal is provided to the tip/ring pair. During the ring mode, the user, by use of the input states, performs line reversals at the required frequency, which generates the power ringing signal. This signal may be applied continuously but is normally cadenced to meet country-specific requirements. The input states are normally set to an active state when power ringing is halted to enable on-hook transmission. The ring trip detector and common-mode current detector are active during the ring mode. The user may adjust the crest factor of the ring signal by selecting one of the two slew rates. The two rates, high or low, allow the designer to chose one set of external capacitors to meet the crest factor range of 1.2 to 1.6 over a 3:1 frequency range by software control alone. For increased power efficiency, the crest factor should be kept as low as possible.

With maximum V_{BAT1}, the L9214 has sufficient power to ring a 3 REN (2310 Ω + 24 μF) ringing load into 600 Ω of physical wiring resistance. With maximum V_{BAT1}, the L9214 has sufficient power to ring a 2 REN (3500 Ω + 16 μF) ringing load into <1000 Ω of physical wiring resistance. Loop ranges may be expanded by applying a lower crest factor trapezoidal input waveform.

This feature eliminates the need for a separate external ring relay, associated external circuitry, and a bulk ringing generator. See the Applications section of this data sheet for more information.

Where PPM is required, it is injected into the audio receive pins (ac-coupled). PPM shaping must be done externally and the PPM level must be within the 1.12 Vrms (3.17 dBm, 600 Ω) level set by the amplifier overhead in the active state.

Both the ring trip and loop closure supervision functions are included. The loop closure has a fixed typical 10 mA on- to off-hook threshold in the active and scan mode. In either case, there is a 2 mA hysteresis. The ring trip detector requires a simple filter at the input. The ring trip threshold internally at a given battery voltage is fixed, but the threshold can be adjusted through an external voltage divider. Typical ring trip threshold is 20.1 mA for a –65 V V_{BAT1}.

A common-mode current detector for tip or ring ground detection is included for ground key applications. The threshold is user programmable via external resistors. See the Applications section of this data sheet for more information on supervision functions.

Description (continued)

Longitudinal balance is consistent with European ETSI and North American GR-909 requirements. Specifications are given in Table 10.

Data control is via a parallel unlatched control scheme.

The dc current limit is programmable in the active modes by use of an external resistor connected between DCOUT and I_{PROG}. Design equations for this feature are given in the dc Loop Current Limit section within the Applications section of this data sheet.

Programming range is 15 mA to 45 mA with V_{CC} = 5.0 V and 15 mA to 35 mA with V_{CC} = 3.3 V. Programming accuracy is ±10% over this current range.

Circuitry is added to the L9214 to minimize the inrush of current from the V_{CC} supply and to the battery supply during an on- to off-hook transition, thus saving in power supply design cost. See the Applications section of this data sheet for more information.

Transmit and receive gains have been chosen to minimize the number of external components required in the SLIC-codec ac interface, regardless of the choice of codec.

The L9214 uses a voltage feed-current sense architecture; thus, the transmit gain is a transconductance. The L9214 transconductance is set via a single external resistor, and this device is designed for optimal performance with a transconductance set at 300 V/A.

The L9214 offers an option for a single-ended to differential receive gain of either 8 or 2. These options are mask programmable at the factory and are selected by choice of product code.

A receive gain of 8 is more appropriate when choosing a first-generation type codec where termination impedance, hybrid balance, and overall gains are set by external analog filters. The higher gain is typically required for synthesization of complex termination impedance.

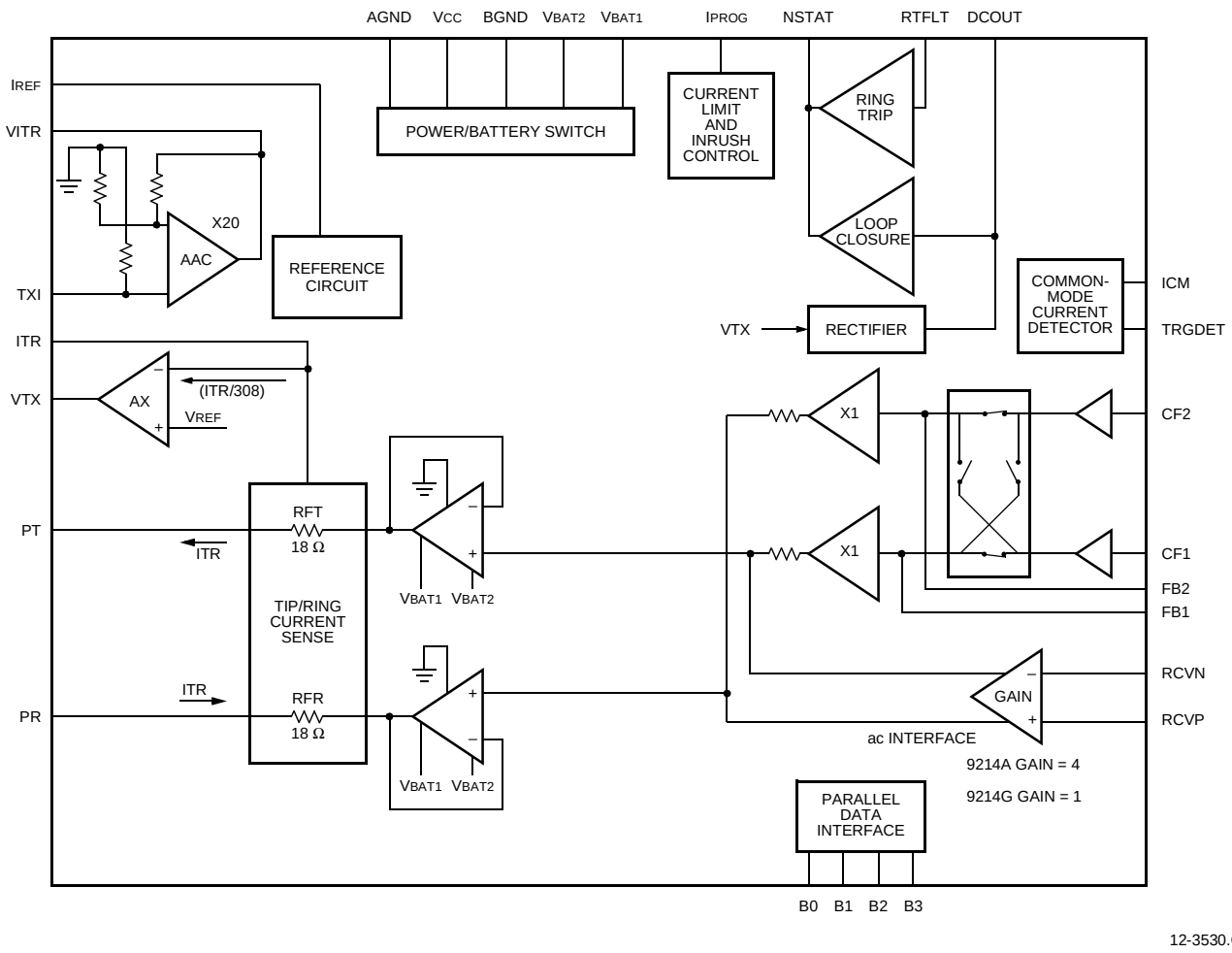
A receive gain of 2 is more appropriate when choosing a third-generation type codec. Third-generation codecs will synthesize termination impedance and set hybrid balance and overall gains. To accomplish these functions, third-generation codecs typically have both analog and digital gain filters. For optimal signal to noise performance, it is best to operate the codec at a higher gain level. If the SLIC then provides a high gain, the SLIC output may be saturated causing clipping distortion of the signal at tip and ring. To avoid this situation, with a higher gain SLIC, external resistor dividers are used. These external components are not necessary with the lower gain offered by the L9214. See the Applications section of this data sheet for more information.

The L9214 is internally referenced to 1.5 V. The SLIC output VITR is referenced to AGND; therefore, it must be ac-coupled to the codec input. However, the SLIC inputs RCVP/RCVN are floating inputs. If there is not feedback from RCVP/RCVN to VITR, RCVP/RCVN may be directly coupled to the codec output. If there is feedback from RCVP/RCVN to VITR, RCVP/RCVN must be ac coupled to the codec output.

The L9214 is thermally protected to guard against faults. Upon reaching the thermal shutdown temperature, the device will enter an all-off mode. Upon cooling, the device will re-enter the state it was in prior to thermal shutdown. Hysteresis is built in to prevent oscillation.

The L9214 is packaged in the 28-pin SOG, 32-pin PLCC and 48-pin MLCC surface-mount packages. The L9214A is set for gain of eight applications, and the L9214G is set for gain of two applications.

Architecture Diagram



12-3530.C (F)

Figure 1. Architecture Diagram

Pin Information

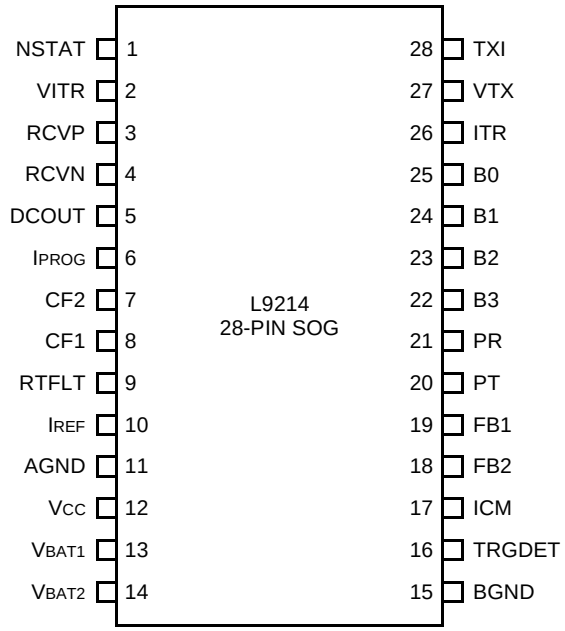


Figure 2. 28-Pin SOG Diagram

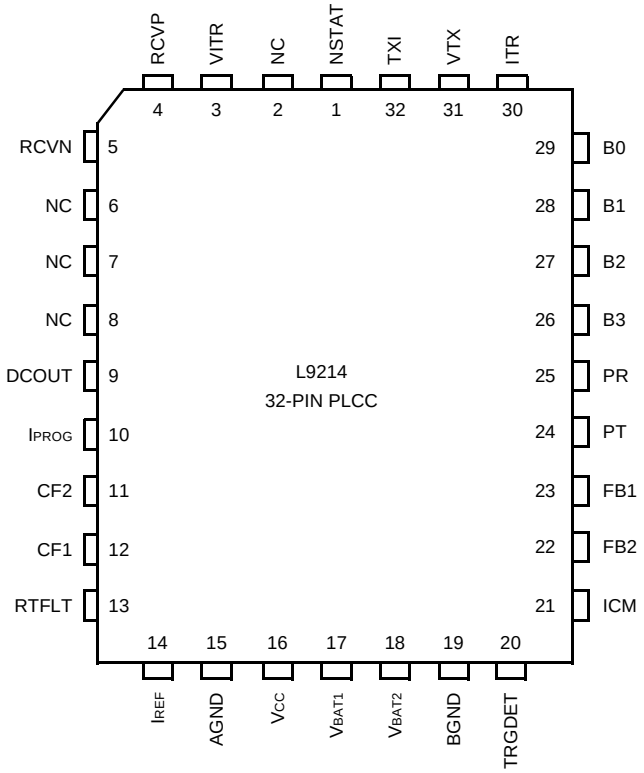
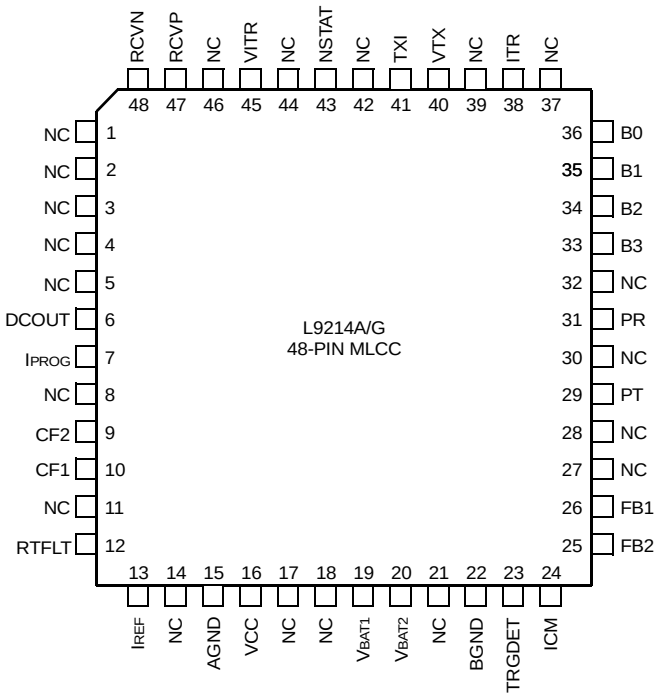


Figure 3. 32-Pin PLCC Diagram

Pin Information (continued)



12-3361f(F)

Figure 4. 48-Pin MLCC Diagram

Pin Information (continued)

Table 1. Pin Descriptions

28-Pin SOG	32-Pin PLCC	48-Pin MLCC	Symbol	Type	Name/Function
1	1	43	NSTAT	O	**Loop Closure Detector Output—Ring Trip Detector Output.** When low, this logic output indicates that an off-hook condition exists or ringing is tripped.
—	—	5, 14, 18, 28, 32, 39, 42, 44	NC	—	**No Connection.** May be used as a tie point.
—	2, 6, 7, 8	1—4, 8, 11, 17, 21, 27, 30, 37, 46	NC	—	**No Connection.** May not be used as a tie point.
2	3	45	VITR	O	**Transmit ac Output Voltage.** Output of internal AAC amplifier. This output is a voltage that is directly proportional to the differential ac tip/ring current.
3	4	47	RCVP	I	**Receive ac Signal Input (Noninverting).** This high-impedance input controls to ac differential voltage on tip and ring. This node is a floating input.
4	5	48	RCVN	I	**Receive ac Signal Input (Inverting).** This high-impedance input controls to ac differential voltage on tip and ring. This node is a floating input.
5	9	6	DCOUT	O	**dc Output Voltage.** This output is a voltage that is directly proportional to the absolute value of the differential tip/ring current. This is used to set the dc current limit and the ring trip threshold.
6	10	7	I_{PROG}	I	**Current-Limit Program Input.** A resistor is connected from this pin to DCOUT to program the dc current limit for the device.
7	11	9	CF2	—	**Filter Capacitor.** Connect a capacitor from this node to ground.
8	12	10	CF1	—	**Filter Capacitor.** Connect a capacitor from this node to CF2.
9	13	12	RTFLT	—	**Ring Trip Filter.** Connect this lead to DCOUT via a resistor and to AGND with a capacitor or a resistor capacitor combination, depending on the ringing type, to filter the ring trip circuit to prevent spurious responses.
10	14	13	I_{REF}	I	**SLIC Internal Reference Current.** Connect a resistor between this pin and AGND to generate an internal reference current.
11	15	15	AGND	GND	**Analog Signal Ground.**
12	16	16	V_{CC}	PWR	**Analog Power Supply.** User choice of 5 V or 3.3 V nominal power supply.
13	17	19	V_{BAT1}	PWR	**Battery Supply 1.** High-voltage battery.
14	18	20	V_{BAT2}	PWR	**Battery Supply 2.** Low-voltage battery or power control resistor.
15	19	22	BGND	GND	**Battery Ground.** Ground return for the battery supplies.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

28-Pin SOG	32-Pin PLCC	48-Pin MLCC	Symbol	Type	Name/Function
16	20	23	TRGDET	O	**Tip/Ring Ground Detect.** When high, this open collector output indicates the presence of a ring ground or a tip ground. This supervision output may be used in ground key or common-mode fault detection applications.
17	21	24	ICM	I	**Common-Mode Current Sense.** To program tip or ring ground sense threshold, connect a resistor to V_{CC} and connect a capacitor to AGND to filter 50/60 Hz. If unused, the pin is connected to ground.
18	22	25	FB2	—	**Polarity Reversal Slowdown Capacitor.** Connect a capacitor from this node for controlling rate of battery reversal. Also used for ringing, this pin cannot be left open.
19	23	26	FB1	—	**Polarity Reversal Slowdown Capacitor.** Connect a capacitor from this node for controlling rate of battery reversal. Also used for ringing, this pin cannot be left open.
20	24	29	PT	I/O	**Protected Tip.** The input to the loop sensing circuit and output drive of the tip amplifier. Connect to loop through overvoltage and overcurrent protection.
21	25	31	PR	I/O	**Protected Ring.** The input to the loop sensing circuit and output drive of the ring amplifier. Connect to loop through overvoltage and overcurrent protection.
22	26	33	B3	I	**State Control Input.**
23	27	34	B2	I	**State Control Input.**
24	28	35	B1	I	**State Control Input.**
25	29	36	B0	I	**State Control Input.**
26	30	38	ITR	I	**Transmit Gain.** Input to AX amplifier. Connect a resistor from this node to VTX to set transmit gain. Gain shaping for termination impedance with a COMBO I codec is also achieved with a network from this node to VTX.
27	31	40	VTX	O	**ac/dc Output Voltage.** Output of internal AX amplifier. The voltage at this pin is directly proportional to the differential tip/ring current.
28	32	41	TXI	I	**ac/dc Separation.** Input to internal AAC amplifier. Connect a 0.1 µF capacitor from this pin to VTX.

Operating States

Table 2. Control States

B3	B2	B1	B0	State
0	0	0	0	Disconnect
0	0	0	1	Ringing, (line reverse with high slope)
0	0	1	0	Unused*
0	0	1	1	Ringing, (line forward with high slope)
0	1	0	0	Disconnect
0	1	0	1	Reverse active and on-hook, fast polarity reversal
0	1	1	0	Scan
0	1	1	1	Forward active and on-hook, fast polarity reversal
1	0	0	0	Disconnect
1	0	0	1	Ringing, (line reverse with low slope)
1	0	1	0	Unused*
1	0	1	1	Ringing, (line forward with low slope)
1	1	0	0	Disconnect
1	1	0	1	Reverse active and on-hook, slow polarity reversal
1	1	1	0	Scan
1	1	1	1	Forward active and on-hook, slow polarity reversal

* In this state, all supervision functions are disabled, on hook transmission is disabled, pin PT is positive with respect to PR, V_{BAT1} is applied to tip/ring, and the tip to ring voltage will be equivalent to the scan state.

State Definitions

Forward Active (Fast Polarity Reversal)

Off-hook

- Pin PT is positive with respect to PR.
- V_{BAT2} is applied to tip/ring drive amplifiers for the majority of loop lengths. This may also be derived from V_{BAT1} through a power control resistor.
- Loop closure and common-mode detect are active.
- Ring trip detector is turned off to conserve power.
- Overhead is set for undistorted transmission of +3.17 dBm into 600 Ω.

On-hook

- Pin PT is positive with respect to PR.
- V_{BAT1} is applied to tip/ring drive amplifiers. The tip to ring on-hook differential voltage will be between –42.5 V and –56.5 V with a primary battery of –65 V.
- Loop closure and common-mode detect are active.
- Ring trip detector is turned off to conserve power.
- On-hook transmission is enabled.
- Overhead is set to nominal 17.0 V for undistorted transmission of 0 dBm into 600 Ω.

Forward Active (Slow Polarity Reversal)

Off-hook

- Same as the forward active (fast polarity reversal) state, but with slower polarity reversal.

On-hook

- Same as the forward active (fast polarity reversal) state, but with slower polarity reversal.

State Definitions (continued)

Reverse Active (Fast Polarity Reversal)

Off-hook

- Pin PR is positive with respect to PT.
- V_{BAT2} is applied to tip/ring drive amplifiers via the soft battery switch for the majority of loop lengths. This may also be derived from V_{BAT1} through a power control resistor.
- Loop closure and common-mode detect are active.
- Ring trip detector is turned off to conserve power.
- Overhead is set to nominal 4.0 V for undistorted transmission of 0 dBm into 600 Ω and may be increased automatically for larger signal levels.

On-hook

- Pin PR is positive with respect to PT.
- V_{BAT1} is applied to tip/ring drive amplifiers. The tip to ring on-hook differential voltage will be between –42.5 V and –56.5 V with a primary battery of –65 V.
- Loop closure and common-mode detect are active.
- Ring trip detector is turned off to conserve power.
- On-hook transmission is enabled.
- Overhead is set to nominal 17.0 V for undistorted transmission of 0 dBm into 600 Ω.

Reverse Active (Slow Polarity Reversal)

Off-hook

- Same as the reverse active (fast polarity reversal) state, but with slower polarity reversal.

On-hook

- Same as the reverse active (fast polarity reversal) state, but with slower polarity reversal.

Scan

- Except for loop closure, all circuits (including ring trip and common-mode detector) are powered down.
- On-hook transmission is disabled.
- Pin PT is positive with respect to PR, and V_{BAT1} is applied to tip/ring.
- The tip to ring on-hook differential voltage will be between –42.5 V and –56.5 V with a –65 V primary battery.

Disconnect

- The tip/ring amplifiers and all supervision are turned off.
- The SLIC goes into a high-impedance state.
- NSTAT is forced high (on-hook).

Ring

- Ringing controlled digitally or by a PWM input signal
- Power ring signal is applied to tip and ring.
- Software-selectable slew rate, fast or slow.
- Ring trip supervision and common-mode current supervision are active; loop closure is inactive.
- Overhead voltage is reduced to typically 2.5 V and current limit set at I_{PROG} is disabled.
- Current is limited by saturation current of the amplifiers themselves, typically 72 mA peak at 125 °C.

Thermal Shutdown

- Not controlled via truth table inputs.
- This mode is caused by excessive heating of the device, such as may be encountered in an extended power-cross situation.

Absolute Maximum Ratings (at T_A = 25 °C)

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Typ	Max	Unit
dc Supply (V_{CC})	—	–0.5	—	7.0	V
Battery Supply (V_{BAT1})	—	—	—	–80	V
Battery Supply (V_{BAT2})	—	—	—	V_{BAT1}	V
Logic Input Voltage	—	–0.5	—	V_{CC} + 0.5	V
Logic Output Voltage	—	–0.5	—	V_{CC} + 0.5	V
Operating Temperature Range	—	–40	—	125	°C
Storage Temperature Range	—	–40	—	150	°C
Relative Humidity Range	—	5	—	95	%
Ground Potential Difference (BGND to AGND)	—	—	—	±1	V

Note: The IC can be damaged unless all ground connections are applied before, and removed after, all other connections. Furthermore, when powering the device, the user must guarantee that no external potential creates a voltage on any pin of the device that exceeds the device ratings. For example, inductance in a supply lead could resonate with the supply filter capacitor to cause a destructive overvoltage.

Table 3. Typical Operating Characteristics

Parameter	Min	Typ	Max	Unit
5 V dc Supplies (V_{CC})	—	5.0	5.25	V
3 V dc Supplies (V_{CC})	2.97	3.3	—	V
High Office Battery Supply (V_{BAT1})	–63	–65	–70	V
Auxiliary Office Battery Supply (V_{BAT2})	–15	–21	V_{BAT1}	V
Operating Temperature Range (28-pin SOG)	0	25	70	°C
Operating Temperature Range (32-pin PLCC)	–40	25	85	°C

Table 4. Thermal Characteristics

Parameter	Min	Typ	Max	Unit
Thermal Protection Shutdown (Tjc)	150	165	—	°C
28-pin SOG Thermal Resistance Junction to Ambient (θ_{JA})[1, 2]:				
Natural Convection 2S2P Board	—	70	—	°C/W
Wind Tunnel 200 Linear Feet per Minute (LFPM) 2S2P Board	—	59	—	°C/W
32-pin PLCC Thermal Resistance Junction to Ambient (θ_{JA})[1, 2]:				
Natural Convection 2S2P Board	—	35.5	—	°C/W
Natural Convection 2S0P Board	—	50.5	—	°C/W
Wind Tunnel 100 Linear Feet per Minute (LFPM) 2S2P Board	—	31.5	—	°C/W
Wind Tunnel 100 Linear Feet per Minute (LFPM) 2S0P Board	—	42.5	—	°C/W
48-pin MLCC Thermal Resistance Junction to Ambient (θ_{JA})[1, 2]	—	38	—	°C/W

1. This parameter is not tested in production. It is guaranteed by design and device characterization.
2. Airflow, PCB board layers, and other factors can greatly affect this parameter.

Electrical Characteristics

Table 5. Environmental Characteristics

Parameter	Min	Typ	Max	Unit
Temperature Range (28-pin SOG)	0	—	70	°C
Temperature Range (32-pin PLCC and 48-pin MLCC)	–40	—	85	°C
Humidity Range[1]	5	—	95[1]	%RH

1. Not to exceed 26 grams of water per kilogram of dry air.

Table 6. 5.0 V Supply Currents

V_{BAT1} = –65 V, V_{BAT2} = –21 V, V_{CC} = 5.0 V.

Parameter	Min	Typ	Max	Unit
Supply Currents (scan state; no loop current):				
I_{VCC}	—	2.90	3.80	mA
I_{VBAT1}	—	0.09	0.20	mA
I_{VBAT2}	—	0.04	0.07	mA
Supply Currents (forward/reverse active; no loop current, V_{BAT1} applied):				
I_{VCC}	—	4.8	6.00	mA
I_{VBAT1}	—	1.5	1.95	mA
I_{VBAT2}	—	1.0	1.20	mA
Supply Currents (disconnect mode):				
I_{VCC}	—	1.60	2.20	mA
I_{VBAT1}	—	0.02	0.10	mA
I_{VBAT2}	—	0.01	0.02	mA
Supply Currents (ringing mode, no load applied):				
I_{VCC}	—	4.40	5.0	mA
I_{VBAT1}	—	1.70	2.2	mA
I_{VBAT2}	—	0.57	0.7	mA

Table 7. 5.0 V Powering

V_{BAT1} = –65 V, V_{BAT2} = –21 V, V_{CC} = 5.0 V.

Parameter	Min	Typ	Max	Unit
Power Dissipation (scan state; no loop current)	—	21	33	mW
Power Dissipation (forward/reverse active; no loop current, V_{BAT1} applied)	—	143	182	mW
Power Dissipation (disconnect mode)	—	10	18	mW
Power Dissipation (ring mode; no load applied)	—	144	183	mW

Note: Refer to the power control description in the Applications section to calculate power dissipation in the forward/reverse off-hook state.

Electrical Characteristics (continued)

Table 8. 3.3 V Supply Currents

V_{BAT1} = –65 V, V_{BAT2} = –21 V, V_{CC} = 3.3 V.

Parameter	Min	Typ	Max	Unit
Supply Currents (scan state; no loop current):				
I_{VCC}	—	2.30	3.00	mA
I_{VBAT1}	—	0.09	0.18	mA
I_{VBAT2}	—	0.04	0.07	mA
Supply Currents (forward/reverse active; no loop current, V_{BAT1} applied):				
I_{VCC}	—	4.40	5.30	mA
I_{VBAT1}	—	1.50	1.90	mA
I_{VBAT2}	—	0.97	1.20	mA
Supply Currents (disconnect mode):				
I_{VCC}	—	1.20	1.70	mA
I_{VBAT1}	—	0.02	0.10	mA
I_{VBAT2}	—	0.01	0.02	mA
Supply Currents (ringing mode, no load applied):				
I_{VCC}	—	4.00	4.75	mA
I_{VBAT1}	—	1.64	2.16	mA
I_{VBAT2}	—	0.54	0.60	mA

Table 9. 3.3 V Powering

V_{BAT1} = –65 V, V_{BAT2} = –21 V, V_{CC} = 3.3 V.

Parameter	Min	Typ	Max	Unit
Power Dissipation (scan state; no loop current)	—	14	23	mW
Power Dissipation (forward/reverse active; no loop current, V_{BAT1} applied)	—	132	166	mW
Power Dissipation (disconnect mode)	—	5	13	mW
Power Dissipation (ring mode; no loop current)	—	131	169	mW

Note: Refer to the power control description in the Applications section to calculate power dissipation in the forward/reverse off-hook state.

Electrical Characteristics (continued)

Table 10. Two-Wire Port

Parameter	Min	Typ	Max	Unit
Tip or Ring Drive Current = dc + Longitudinal + Signal Currents	72	—	—	mApeak
Tip or Ring Drive Current = Ringing + Longitudinal	37	—	—	mApeak
Signal Current	5	—	—	mArms
Longitudinal Current Capability per Wire (Longitudinal current is independent of dc loop current.)	8.5	15	—	mArms
Ringing Current (R_{LOAD} = 2330 Ω + 24 µF)	25	—	—	mApeak
Ringing Current (R_{LOAD} = 3500 Ω + 1.8 µF)	12	—	—	mApeak
Ringing Current Limit (R_{LOAD} = 100 Ω)	—	—	90	mApeak
dc Loop Current—I_{LIM} (R_{LOOP} = 500 Ω):				
Programming Range (V_{CC} = 5.0 V)	15	—	45	mA
Programming Range (V_{CC} = 3.3 V)	15	—	35	mA
dc Current Variation (current limit 15 mA to 45 mA)	—	—	±10	%
dc Loop Current (R_{LOOP} = 100 Ω, on to off hook transition)	—	—	350	mApeak
t < 20 ms	—	—	100	mA
dc Loop Current (R_{LOOP} = 100 Ω, on to off hook transition)	—	—	—	
t < 50 ms	—	—	150%	I_{LIM}
dc Feed Resistance, 2 x R_F (excluding protection resistors)	25	36	50	Ω
Loop Resistance Range*, (0 dB overload into 600 Ω)				
I_{LOOP} = 20 mA, V_{BAT2} = –24 V, 50 Ω (2 x R_F), 60 Ω (2 x R_P), 300 Ω R_{LOOP} plus Handset	840	—	—	Ω
I_{LOOP} = 25 mA, V_{BAT1} = –65 V, 50 Ω (2 x R_F), 60 Ω (2 x R_P), 1000 Ω R_{LOOP} plus Handset	1540	—	—	Ω
Open Loop Voltages, |V_{BAT1}| = –63 V to –70 V:				
Scan/On-Hook Transmission Mode:				
|PT – PR| – Differential	42.5	48	—	V
|PT| or |PR| Referenced to BGND	—	—	56.5	V
Ring Mode, |V_{BAT1}| = –63 V to –70 V:				
|PT – PR| – Differential, (open loop ring voltage)	40	—	—	Vrms
Loop Closure Threshold:				
Scan/Active/On-hook Transmission Modes	—	10	—	mA
Loop Closure Threshold Hysteresis:	—	2	—	mA
Ground Key:				
Differential Detector Threshold	5	8	10	mA
Detection	50	—	—	ms
Longitudinal to Metallic Balance at PT/PR				
Test Method per Figure 8, 1 kHz† 58 dB minimum, 60 dB typical:				
300 Hz to 600 Hz	55	58	—	dB
600 Hz to 3.4 kHz	55	58	—	dB
Metallic to Longitudinal (harm) Balance:				
200 Hz to 1000 Hz	40	—	—	dB
100 Hz to 4000 Hz	40	—	—	dB
PSRR 500 Hz—3000 Hz:				
V_{BAT1}, V_{BAT2}	40	—	—	dB
V_{CC} (3.3 V operation)	25	—	—	dB

* Values guaranteed by design, not subject to production test.
† Corresponds to 55 dB minimum with 1%, 30 Ω resistors per Q552 (11/96) Section 2.1.2 and *IEEE*® 455.

Electrical Characteristics (continued)

Table 11. Analog Pin Characteristics

Parameter	Min	Typ	Max	Unit
TXI (input impedance)	—	100	—	kΩ
Output Offset (VTX)	—	±5	—	mV
Output Offset (VITR)	—	±70	—	mV
Output Drive Current (VTX)	—	±500	—	µA
Output Drive Current (VITR)	—	±250	—	µA
Output Voltage Swing (VTX) (V_{CC} = 5.0 V)	±3.7	—	+5/–8	V
Output Voltage Swing (VITR) (V_{CC} = 5.0 V)	—	—	±3.1	V
Output Short-circuit Current (VTX)	—	±5	—	mA
Output Short-circuit Current (VITR)	—	±6	—	mA
Output Load Resistance (VTX and VITR)	10	—	—	kΩ
Output Load Capacitance (VTX)	—	—	20	pF
Output Load Capacitance (VITR)	—	—	50	pF
RCVN and RCVP:				
Input Voltage Range (V_{CC} = 5.0 V)	0	—	V_{CC} – 0.5	V
Input Voltage Range (V_{CC} = 3.3 V)	0	—	V_{CC} – 0.3	V
Input Bias Current	—	—	±1.5	µA

Electrical Characteristics (continued)

Table 12. ac Feed Characteristics

Parameter	Min	Typ	Max	Unit
ac Termination Impedance[1]	150	600	1400	Ω
Total Harmonic Distortion (200 Hz—4 kHz)[2]:				
Off-hook	—	—	0.3	%
On-hook	—	—	1.0	%
Transmit Gain (f = 1004 Hz, 1020 Hz)[3]:				
PT/PR Current to VITR	291	300	309	V/A
Receive Gain[4] (f = 1004 Hz to 1020 Hz):				
RCVP or RCVN to PT—PR (gain of 8 option, L9214A)	7.6	8	8.4	—
RCVP or RCVN to PT—PR (gain of 2 option, L9214G)	1.9	2	2.1	—
Gain vs. Frequency (transmit and receive)[2], 600 Ω Termination (Q.552), 1004 Hz, 1020 Hz reference:				
200 Hz—300 Hz	–0.30	0	0.05	dB
300 Hz—3.4 kHz	–0.05	0	0.05	dB
3.4 kHz—3.6 kHz	–1.50	0	0.05	dB
3.6 kHz—20 kHz	–3.00	–0.1	–0.05	dB
20 kHz—266 kHz	—	—	–2.0	dB
Gain vs. Level (transmit and receive)[2], 0 dBV Reference (Q.552):				
–55 dB to +3.0 dB	–0.05	0	0.05	dB
Idle-channel Noise (tip/ring) 600 Ω Termination:				
Psophometric	—	–82	–77	dBmp
C-Message	—	8	13	dBrnC
3 kHz Flat	—	—	20	dBrn
Idle-channel Noise (VTX) 600 Ω Termination:				
Psophometric	—	–82	–77	dBmp
C-Message	—	8	13	dBrnC
3 kHz Flat	—	—	20	dBrn

1. Set externally either by discrete external components or a third- or fourth-generation codec. Any complex impedance R1 + R2 || C between 150 Ω and 1400 Ω can be synthesized.
2. This parameter is not tested in production. It is guaranteed by design and device characterization.
3. VITR transconductance depends on the resistor from ITR to VTX. This gain assumes an ideal 4750 Ω, the recommended value. Positive current is defined as the differential current flowing from PT to PR.
4. Tested per Figure 9. The gain reading is adjusted by the ratio of 696/660 to account for the 36 Ω nominal ac feed resistance.

Electrical Characteristics (continued)

Table 13. Logic Inputs and Outputs (V_{CC} = 5.0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltages:					
Low Level	V_{IL}	–0.5	0.4	0.7	V
High Level	V_{IH}	2.0	2.4	V_{CC}	V
Input Current:					
Low Level (V_{CC} = 5.25 V, V_I = 0.4 V)	I_{IL}	—	—	±250	µA
High Level (V_{CC} = 5.25 V, V_I = 2.4 V)	I_{IH}	—	—	±250	µA
Output Voltages (open collector with internal pull-up resistor):					
Low Level (V_{CC} = 4.75 V, I_{OL} = 200 µA)	V_{OL}	0	0.2	0.4	V
High Level (V_{CC} = 4.75 V, I_{OH} = –10 µA)	V_{OH}	2.4	—	V_{CC}	V

Table 14. Logic Inputs and Outputs (V_{CC} = 3.3 V)

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltages:					
Low Level	V_{IL}	–0.5	0.2	0.5	V
High Level	V_{IH}	2.0	2.5	V_{CC}	V
Input Current:					
Low Level (V_{CC} = 3.46 V, V_I = 0.4 V)	I_{IL}	—	—	±250	µA
High Level (V_{CC} = 3.46 V, V_I = 2.4 V)	I_{IH}	—	—	±250	µA
Output Voltages (open collector with internal pull-up resistor):					
Low Level (V_{CC} = 3.13 V, I_{OL} = 200 µA)	V_{OL}	0	0.2	0.5	V
High Level (V_{CC} = 3.13 V, I_{OH} = –5 µA)	V_{OH}	2.2	—	V_{CC}	V

Table 15. Ringing Specifications

Parameter	Min	Typ	Max	Unit
Ring Signal Isolation: PT/PR to VITR Ring Mode	—	60	—	dB
Ringing Voltage (5 REN 1386 Ω + 40 µF load, 200 Ω loop, 2 x 30 Ω protection resistors, –69 V battery, 1.2 crest factor)[1]	40	—	—	Vrms
Ringing Voltage (3 REN 2330 Ω + 24 µF load, 600 Ω loop, 2 x 30 Ω protection resistors, –69 V battery, 1.2 crest factor)[1]	40	—	—	Vrms
Ringing Voltage (2 REN 3500 Ω + 16 µF load, 1000 Ω loop, 2 x 30 Ω protection resistors, –69 V battery, 1.2 crest factor)[1]	40	—	—	Vrms
Ringing Voltage (2 REN 3500 Ω + 1.8 µF load, 500 Ω loop, 2 x 30 Ω protection resistors, –69 V battery, 1.2 crest factor)[2]	40	—	—	Vrms
Ring Signal Distortion:				
5 REN 1386 Ω, 40 µF Load, 200 Ω Loop	—	5	—	%
3 REN 2330 Ω, 24 µF Load, 600 Ω Loop	—	5	—	%
2 REN 3500 Ω, 16 µF Load, 1000 Ω Loop	—	5	—	%
2 REN 3500 Ω, 1.8 µF Load, 500 Ω Loop	—	5	10	%

1. Voltage is measured across both resistive and capacitive elements of the ringer load.
2. Voltage is measured only across the resistive element of the ringer load.

Electrical Characteristics (continued)

Table 16. Ring Trip (3 REN Configuration)

Parameter	Min	Typ	Max	Unit
Ring Trip (NSTAT = 0): Loop Resistance (total)	0	—	1000	Ω
Ring Trip (NSTAT = 1): Loop Resistance (total)	10	—	—	kΩ
Ringer Load	—	—	2330 Ω + 24 µF	—
Trip Time (f = 20 Hz)	—	—	130	ms

Ringing will not be tripped by the following loads:

- 100 Ω resistor in series with a 2 µF capacitor applied across tip and ring. Ring frequency = 17 Hz to 23 Hz.
- 10 kΩ resistor in parallel with a 4 µF capacitor applied across tip and ring. Ring frequency = 17 Hz to 23 Hz.

Table 17. Ring Trip (5 REN Configuration)

Parameter	Min	Typ	Max	Unit
Ring Trip (NSTAT = 0): Loop Resistance (total)	0	—	600	Ω
Ring Trip (NSTAT = 1): Loop Resistance (total)	10	—	—	kΩ
Ringer Load	—	—	1386 Ω + 40 µF	—
Trip Time (f = 20 Hz)	—	—	150	ms

Ringing will not be tripped by the following loads:

- 100 Ω resistor in series with a 2 µF capacitor applied across tip and ring. Ring frequency = 17 Hz to 23 Hz.
- 10 kΩ resistor in parallel with a 6 µF capacitor applied across tip and ring. Ring frequency = 17 Hz to 23 Hz.

Note: Refer to the application section for further description of the 3 REN configuration vs. 5 REN configuration.

Test Configurations

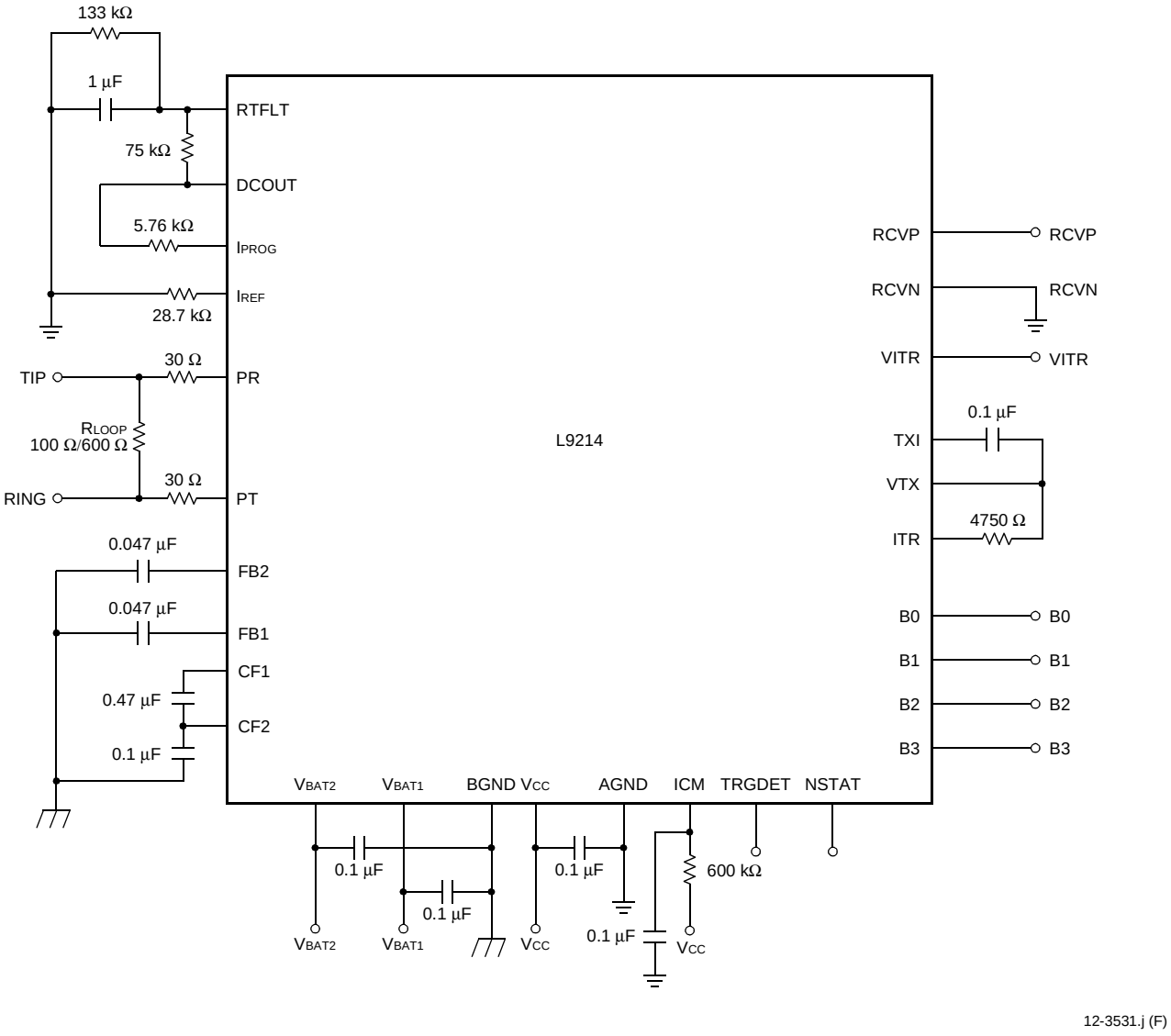


Figure 5. Basic Test Circuit, V_{CC} = 3.3 V (3 REN Configuration)

Test Configurations (continued)

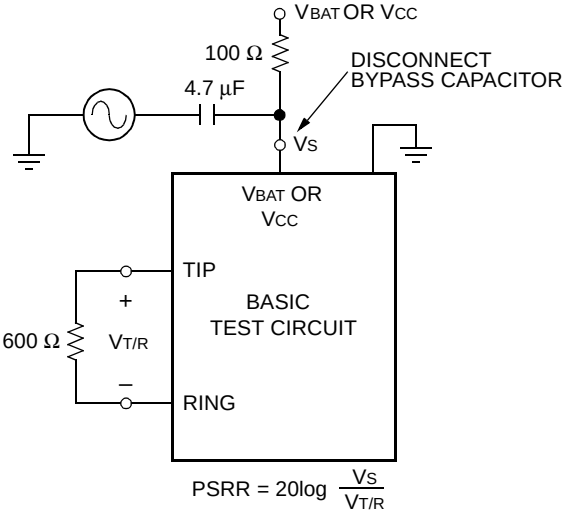


Figure 6. Metallic PSRR

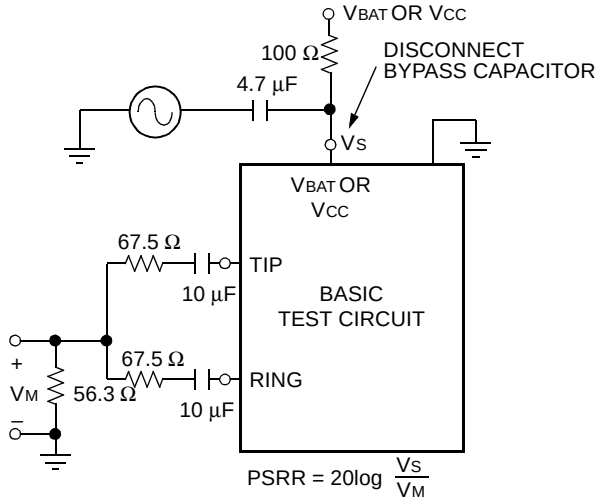


Figure 7. Longitudinal PSRR

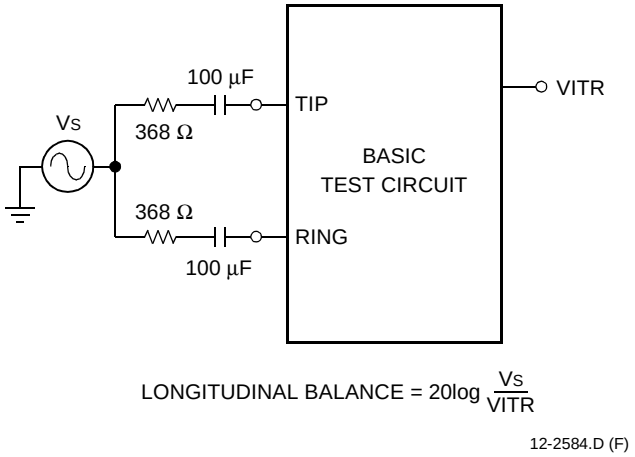


Figure 8. Longitudinal Balance

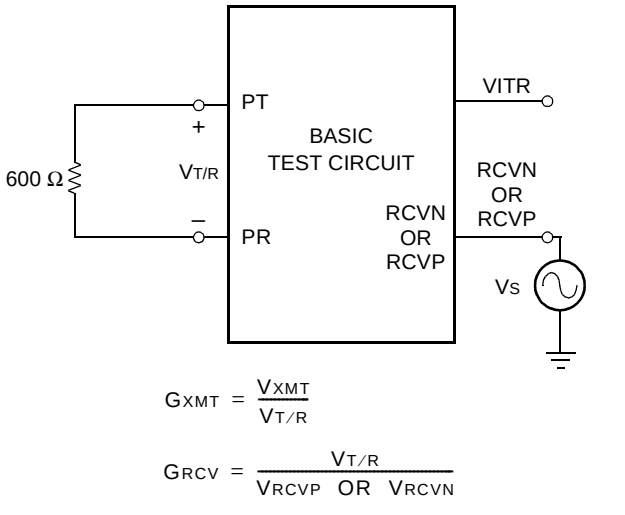


Figure 9. ac Gains

Applications

Power Control

Under normal device operating conditions, power dissipation must be controlled to prevent the device temperature from rising too close to the thermal shutdown point. Power dissipation is highest with higher battery voltages, higher current limit, and under shorter dc loop conditions. Additionally, higher ambient temperature will reduce thermal margin. Increasing the number of PC board layers and increasing airflow around the device are typical ways of improving thermal margin.

The maximum recommended junction temperature for the L9214 is 150 °C. The junction temperature is:

$T_j = T_{AMBIENT} + \theta_{JA} * P_{SLIC}$

The thermal impedance of this device depends on the package type as well as number of PCB layers and airflow. The thermal impedance of the 28-pin SOG package is somewhat higher than the 32-pin PLCC package. The 28-pin SOG package in still air with a single-sided PCB is rated at 70 °C/W. The 32-pin PLCC package thermal impedance with no airflow on a four-layer PCB is estimated at 37 °C/W.

The power handling capability of the package is:

$P_{SLIC} = (150\ °C - T_{AMBIENT})/\theta_{JA}$

which is a minimum of 0.93 W for the 28-pin SOG package with a single-sided PCB and no airflow and as much as 2.15 W for the 32-pin PLCC package with a multilayer PCB.

This device is intended to operate with a high-voltage primary battery of –63 V to –70 V. Under short-loop conditions, an internal soft battery switch shunts most (all but I_{BIAS} = 3.5 mA) of the loop current to an auxiliary battery of lower absolute voltage (typically –21 V). Where single battery operation is required, an external power control resistor can be connected from the V_{BAT2} pin to V_{BAT1} and all but 3.5 mA of the loop current will flow through the power control resistor.

The power dissipated in the device is best illustrated by an example. Assume V_{BAT1} is –65 V, V_{BAT2} is –21 V, and the current limit is is I_{LOOP}.

Let I_{Q1} and I_{Q2} be the quiescent currents drawn from V_{BAT1} and V_{BAT2} respectively (the current drawn from the battery when the phone is on-hook). Let I_{BIAS} be the additional current drawn from V_{BAT1} when the phone is off-hook.

$I_{BIAS} = I_{VBAT1(off\text{-}hook)} - I_{Q1}$

Typically I_{BIAS} is 3.5 mA. This additional V_{BAT1} current contributes to the loop current and the remaining loop current is supplied by V_{BAT2}, so that

$I_{VBAT2} = I_{Q2} + I_{LOOP} - I_{BIAS}$

I_{VCC} is the current drawn from V_{CC} and is relatively constant as the phone goes off hook.

The total power from the power supplies is:

$P_{TOTAL} = \{[(I_{Q1} + I_{BIAS}) * V_{BAT1}] + [(I_{Q2} + I_{LOOP} - I_{BIAS}) * V_{BAT2}] + [(I_{VCC}) * V_{CC}]\}$

The maximum values of I_{Q1} and I_{Q2} are 1.95 mA and 1.20 mA respectively from Table 4.

If the current limit is set to 25 mA, given the current limit tolerance of 10%, the maximum current limit is 27.5 mA. Also, assume 20 Ω of wire resistance, 30 Ω of protection resistance, and 200 Ω for the handset

$P_{TOTAL} = \{[(1.95\ mA + 3.5\ mA) * (65\ V)] + [(1.20\ mA + 27.5\ mA - 3.5\ mA) * (21\ V)] + [(6\ mA) * (5\ V)]$
$= 913.45\ mW$

The power delivered to the loop and the protection resistors (P_{LOOP}) is:

$P_{LOOP} = \{(I_{LOOP})^2 * [(2 * R_{PROTECTION}) + (R_{WIRE}) + (R_{PHONE})]\} = \{(27.5\ mA)^2 * [(2 * 30\ \Omega) + (20\ \Omega) + 200\ \Omega)]\} = 212\ mW$

Thus, the total power dissipated by the SLIC is:

P_D of SLIC = Total power (P_{TOTAL}) – power delivered to loop and protection resistors (P_{LOOP}).

$P_D = 913.45\ mW - 212\ mW$
$= 701.45\ mW$ for this example.

Since the minimum power handling capability of the 28-pin SOG package is 0.93 W, in this case either package type is acceptable even with a single-sided PCB. At higher battery voltages, higher ambient temperature, and higher current limit, the required thermal impedance drops and the 32-pin PLCC package, more PCB layers, or some airflow might be required.

Another case to consider is the case of the power control resistor. In this case, the effective V_{BAT2} voltage is:

$V_{BAT2} = V_{BAT1} - R_{PWR} * (I_{LOOP} - I_{BIAS} + I_{Q2})$

For the case of the 27.5 mA maximum current limit, choosing R_{PWR} = 1.75 kΩ would give V_{BAT2} = –21 V and the same SLIC power as above. The power in the resistor would be:

$P_{RPWR} = (I_{LOOP} - I_{BIAS} + I_{Q2})^2 * R_{PWR} = 1.11\ W$

Choosing a larger R_{PWR} would result in lower V_{BAT2} and lower SLIC power, but more power in the resistor. Similarly, choosing a smaller R_{PWR} results in higher V_{BAT2}, higher SLIC power, and less power in the resistor.

Applications (continued)

dc Loop Current Limit

In the active modes, dc current limit is programmable via an external resistor. The resistor is connected between I_{PROG} and DCOUT. The loop current limit (I_{LOOP}) with 100 Ω load is related to the R_{IPROG} programming resistor by:

I_{LOOP} (mA) = 4 mA/kΩ * R_{IPROG} (kΩ) + 2 mA

Note that the overall current-limit accuracy achieved will be affected by the specified accuracy of the internal SLIC current-limit circuit and the accuracy of the external resistor.

The above equation describes the active mode steady-state current-limit response. There will be a transient response of the current-limit circuit upon an on- to off-hook transition. Typical active mode transient current-limit response is given in Table 18.

Table 18. Typical Active Mode On- to Off-Hook Tip/Ring Current-Limit Transient Response

Parameter	Value	Unit
dc Loop Current: Active Mode R_{LOOP} = 100 Ω On- to Off-hook Transition t < 20 ms	I_{LOOP} + 60	mA
dc Loop Current: Active Mode R_{LOOP} = 100 Ω On- to Off-hook Transition t < 30 ms	I_{LOOP} + 20	mA
dc Loop Current: Active Mode R_{LOOP} = 100 Ω On- to Off-hook Transition t < 50 ms	I_{LOOP}	mA

Overhead Voltage

Active Mode

The overhead is preprogrammed in the active mode.

Note that overhead is not symmetrical with respect to tip and ring. Under default conditions, the tip to ground voltage is 2.1 V to 2.6 V and the ring to battery overhead is 14.5 V typical.

The default overhead provides sufficient headroom for on-hook transmission of a +3.17 dBm signal into 600 Ω.

+3.17 dBm = 10 log ($Vrms^2$ / P_0 * $R_{600\ \Omega}$)

dBm = 10 log ($Vrms^2$ / 0.001 W * 600 Ω)

$$+3.17\ \text{dBm} = 10 \log \frac{Vrms^2}{0.6(IV \times R)}$$

Vrms = 1.12 V and Vpeak = 1.58 V are supported.

Scan Mode

If the magnitude of the primary battery is greater than a nominal –63 V, the magnitude of the open-loop tip to ring voltage is clamped to between –42.5 V and –56.5 V.

Again, the overhead is not symmetrical with respect to tip and ring. With the magnitude of the primary battery greater than a nominal –63 V, the tip to ground voltage is clamped between –0.1 V and –0.6 V and the ring to ground voltage is clamped between –42.5 V and –56.5 V. If the magnitude of the primary battery is less than a nominal –63 V, the tip to ground voltage is –0.1 V to –0.6 V and the ring to battery voltage is typically 17 V less than V_{BAT1}.

On-Hook Transmission Mode

If the magnitude of the primary battery is greater than 63 V, the magnitude of the open-loop tip to ring voltage will be greater than 42.5 V. If the magnitude of the primary battery is less than 63 V, the open-loop voltage may be less than 42.5 V and is approximately 17 V less than the magnitude of the primary battery voltage. For primary battery voltages less than 70 V, the magnitude of the ring to ground voltage will be less than 56.5 V.

Again, the overhead is not symmetrical with respect to tip and ring. The tip voltage to ground is between –2 V and –4.5 V and the ring to primary voltage is 14.5 V typical.

Applications (continued)

Overhead Voltage (continued)

Ring Mode

In the ring mode, to maximize ringing loop length, the overhead is decreased to the saturation of the tip ring drive amplifiers, a nominal 4 V. The tip to ground voltage is 1 V, and the ring to V_{BAT1} voltage is 3 V.

The AX amplifier at VTX is active during the ring mode, differential ring current may be sensed at VTX during the ring mode.

Loop Range

The dc loop range for medium-loop applications is calculated using:

$$R_L = \frac{(|V_{BAT1}| - V_{OHH})}{I_{LOOP}} - 2R_P - R_{dc}$$

The dc loop range for short-loop applications is calculated using:

$$R_L = \frac{(|V_{BAT2}| - V_{OHL})}{I_{LOOP}} - 2R_P - R_{dc}$$

where:
V_{OHH} = 19.5 (2.5 V + 17 V) and
V_{OHL} = 3.4 V (2.5 V + 0.9 V)

and where:

R_L = loop resistance, not including protection resistors.
R_P = protection resistor value.
Rdc = SLIC internal dc feed resistance.
$|V_{BAT1}|$ and $|V_{BAT2}|$ = battery voltage magnitude.
I_{LOOP} = loop current.
V_{OHH} = overhead voltage when power is drawn from V_{BAT1}.
V_{OHL} = overhead voltage when power is drawn from V_{BAT2}.

The point of change over between V_{BAT2} and V_{BAT1} occurs at:

$|V_{BAT2}| - (0.9 + 2.5)\ V > [(2R_P + R_{DC} + R_L) * I_{LOOP}]\ V$

V_{BAT2} is typically applied under off-hook conditions for power conservation and SLIC thermal considerations. The L9214 is intended for short- and medium-loop applications and, therefore, will always be in current limit during off-hook conditions. However, note that the ringing loop length rather than the dc loop length will be the factor to determine operating loop length. Where V_{BAT2} is insufficient to support the loop length, the power will be taken from V_{BAT1}.

Battery Reversal Rate

The rate of battery reverse is controlled or ramped by capacitors FB1 and FB2. A chart showing FB1/FB2 values versus typical ramp time is given below. Leave FB1 and FB2 open if it is not desired to ramp the rate of battery reversal.

Table 19. FB1/FB2 Values vs. Typical Ramp Time at V_{BAT1} = –65 V

C_{FB1}/C_{FB2}	Transition Time Fast, B3 = 0	Transition Time Slow, B3 = 1
0.01 µF	7 ms	20 ms
0.1 µF	75 ms	220 ms
0.22 µF	145 ms	440 ms
0.47 µF	300 ms	900 ms
1.0 µF	600 ms	1.8 s
1.22 µF	750 ms	2.25 s
1.3 µF	830 ms	2.5 s
1.4 µF	900 ms	2.7 s
1.6 µF	1070 ms	3.2 s

Supervision

The L9214 offers the loop closure and ring trip supervision functions. Internal to the device, the outputs of these detectors are multiplexed into a single package output, NSTAT. Additionally, a common-mode current detector for tip or ring ground detection is included for ground key applications.

Loop Closure

The loop closure has a fixed typical 10 mA on- to off-hook threshold in the active mode and a fixed 10 mA on- to off-hook threshold from the scan mode. In either case, there is a 2 mA hysteresis with V_{CC} = 5.0 V and with V_{CC} = 3.3 V.

Ring Trip

The ring trip detector requires an external filter at the input, minimizing external components. An R + R//C combination of 75 kΩ and 133 kΩ // 1 µF, for a filter pole at 3.3 Hz, is recommended for a 3 REN configuration. For a 5 REN configuration, a 150 kΩ and 100 kΩ // 1 µF (for a filter pole at 2.65 Hz) combination is recommended.

The ring trip threshold is internally fixed and is independent of battery voltage. The threshold, I_{RT} = 20.1 mA.

Tip or Ring Ground Detector

In the ground key or ground start applications a common-mode current detector is used to indicate either a tip- or ring-ground has occurred (ground key) or an off-hook has occurred (ground start). The detection threshold is set by connecting a resistor from ICM to V_{CC}.

1000 * V_{CC}/R_{ICM} (kΩ) = I_{TH} (mA)

where:

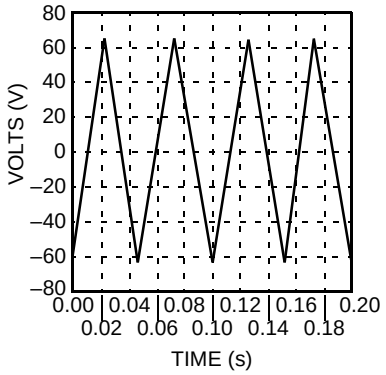
R_{ICM} > 80 kΩ @ V_{CC} = 3.3 V
R_{ICM} > 150 kΩ @ V_{CC} = 5.0 V

Additionally, a filter capacitor across R_{ICM} will set the time constant of the detector. No hysteresis is associated with this detector.

Power Ring

The device offers a ring mode, in which a power ring signal is provided to the tip/ring pair. The standard method of ringing is to perform trapezoidal ringing by use of the state input pins. It is possible to select either fast or slow slew rates to alter the crest factor of the ringing signal. This allows designers to set the external capacitors to a specific factor and change the ringing frequency under software control while maintaining the crest factor between 1.2 and 1.6 for the trapezoidal signal.

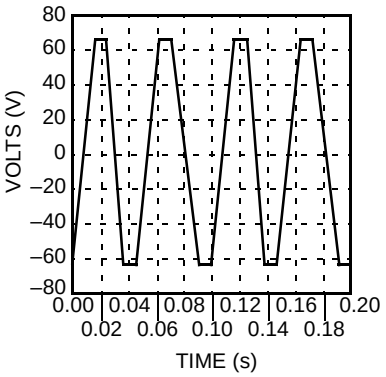
During the ring mode, it is also possible to supply a pulse-width modulated, PWM, signal into the device's B1 input. This signal is used to produce the power ring signal. This signal must be removed during nonring mode states. The user may input any crest factor ring signal using this method; thus, the device will support a sine wave (crest factor 1.414) or a lower or higher crest factor input for increased power efficiency ring signal. Various crest factors are shown below.



12-3346a (F)

Note: Slew rate = 5.65 V/ms; trise = tfall = 23 ms; pwidth = 2 ms; period = 50 ms.

Figure 10. Ringing Waveform Crest Factor = 1.6



12-3347a (F)

Note: Slew rate = 10.83 V/ms; trise = tfall = 12 ms; pwidth = 13 ms; period = 50 ms.

Figure 11. Ringing Waveform Crest Factor = 1.2

Supervision (continued)

Power Ring (continued)

The ring signal will appear balanced on tip and ring. That is, the ring signal is applied on both tip and ring, with the signal on tip 180° out of phase from the signal on ring. This operation is shown in Figure 12 below.

Ringing loop range is calculated as follows:

$V_{RINGLOAD} = \{(V_{BATTERY} – 4)/\text{Crest Factor}\} * \{R_{LOAD}/(R_{LOAD} + R_{LOOP} + 2 \times R_{PROTECTION})\}$

As a practical example, calculate the maximum dc loop length, assuming the following conditions:

Minimum required ring voltage = 40 Vrms
$V_{BATTERY}$ = –67 V
Trapezoidal ringing, crest factor = 1.2
Protection resistors = 30 Ω each
Ring Load = 2 North American REN = 3500 Ω + 16 µF
Ringing frequency = 25 Hz

First, calculate the equivalent ringing load resistance at 25 Hz.

$R_{LOAD} = \{(3500\ \Omega)^2 + (2 * \pi * 25 * 16E{-}6)^{-2}\}^{0.5}$

$R_{LOAD} = 3522\ \Omega$

$40\ \text{Vrms} = \{(67 – 4)/1.2)\}\ \{3522\ \Omega/(R_{LOOP} + 3522\ \Omega + 60\ \Omega)\}$

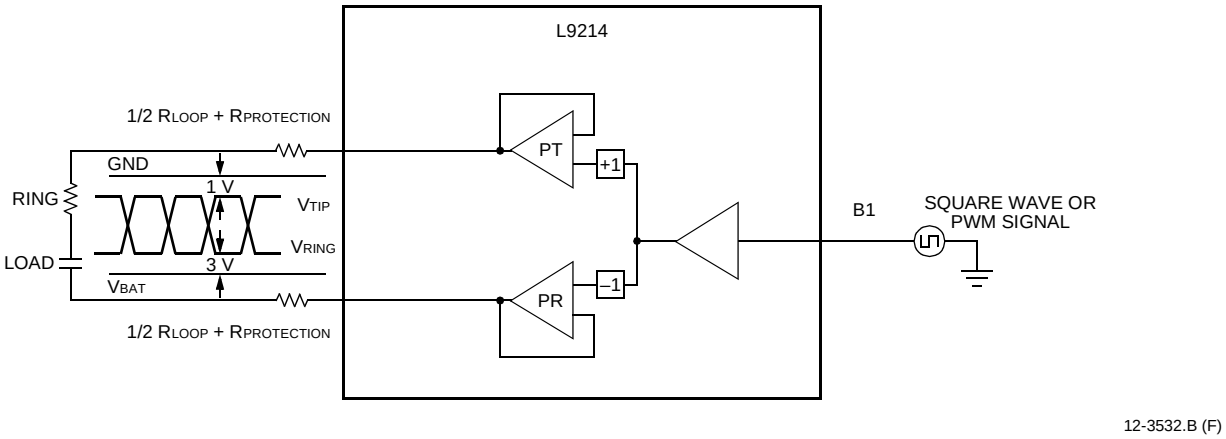
$R_{LOOP} = 1040\ \Omega$

Effects such as power supply tolerance and crest factor tolerance can affect this calculation.

Crest factor is estimated by the formula:

$$= \frac{1}{\sqrt{1 - \frac{(4 \times f \times C_{FB} \times \langle |V_{BAT1}| - V_{OHH} \rangle)}{3 \times I_{CS}}}}$$

Where:
f = ringing frequency; $C_{FB} = (C_{FB1} + C_{FB2})/2$;
Ics = 30 µA with B3 = 1 and 90 µA with B3 = 0;
V_{OHH} = 4 V



12-3532.B (F)

Figure 12. Ring Operation

Periodic Pulse Metering (PPM)

Periodic pulse metering (PPM), also referred to as teletax (TTX), is applied to the audio input of the L9214. When in the active state, this signal is presented to the tip/ring subscriber loop along with the audio signal. The L9214 assumes that a shaped PPM signal is applied to the audio input.

ac Applications

ac Parameters

There are four key ac design parameters. **Termination impedance** is the impedance looking into the 2-wire port of the line card. It is set to match the impedance of the telephone loop in order to minimize echo return to the telephone set. **Transmit gain** is measured from the 2-wire port to the PCM highway, while **receive gain** is done from the PCM highway to the transmit port. Transmit and receive gains may be specified in terms of an actual gain, or in terms of a transmission level point (TLP), that is the actual ac transmission level in dBm. Finally, the **hybrid balance** network cancels the unwanted amount of the receive signal that appears at the transmit port.

Codec Types

At this point in the design, the codec needs to be selected. The interface network between the SLIC and codec can then be designed. Below is a brief codec feature summary.

First-Generation Codecs

These perform the basic filtering, A/D (transmit), D/A (receive), and μ-law/A-law companding. They all have an op amp in front of the A/D converter for transmit gain setting and hybrid balance (cancellation at the summing node). Depending on the type, some have differential analog input and output stages, +5 V only or ±5 V operation, and μ-law/A-law selectability. These are available in single and quad designs. This type of codec requires continuous time analog filtering via external resistor/capacitor networks to set the ac design parameters. An example of this type of codec is the Agere T7504 quad 5 V only codec.

This type of codec tends to be the most economical in terms of piece part price, but tends to require more external components than a third-generation codec. The ac parameters are fixed by the external R/C network so software control of ac parameters is difficult.

Third-Generation Codecs

This class of devices includes all ac parameters set digitally under microprocessor control. Depending on the device, it may or may not have data control latches. Additional functionality sometimes offered includes tone plant generation and reception, PPM generation, test algorithms, and echo cancellation. Again, this type of codec may be 3.3 V, 5 V only, or ±5 V operation, single-, quad-, or 16-channel, and μ-law/A-law or 16-bit linear coding selectable. Examples of this type of codec are the Agere T8535/6 (5 V only, quad, standard features), T8537/8 (3.3 V only, quad, standard features), T8533/4 (5 V only, quad with echo cancellation), and the T8531/32 (5 V only, eight- or 16-channel).

ac Interface Network

The ac interface network between the L9214 and the codec will vary depending on the codec selected. With a first-generation codec, the interface between the L9214 and codec actually sets the ac parameters. With a third-generation codec, all ac parameters are set digitally, internal to the codec; thus, the interface between the L9214 and this type of codec is designed to avoid overload at the codec input in the transmit direction and to optimize signal to noise ratio (S/N) in the receive direction.

Because the design requirements are very different with a first- or third-generation codec, the L9214 is offered with two different receive gains. Each receive gain was chosen to optimize, in terms of external components required, the ac interface between the L9214 and codec.

With a first-generation codec, the termination impedance is set by providing gain shaping through a feedback network from the SLIC VITR output to the SLIC RCVN/RCVP inputs. The L9214 provides a transconductance from T/R to VITR in the transmit direction and a single-ended to differential gain from either RCVN or RCVP to T/R in the receive direction. Assuming a short from VITR to RCVN or RCVP, the maximum impedance that is seen looking into the SLIC is the product of the SLIC transconductance times the SLIC receive gain, plus the protection resistors. The various specified termination impedance can range over the voiceband as low as 300 Ω up to over 1000 Ω. Thus, if the SLIC gains are too low, it will be impossible to synthesize the higher termination impedances. Further, the termination that is achieved will be far less than what is calculated by assuming a short for SLIC output to SLIC input.

ac Applications (continued)

ac Interface Network (continued)

In the receive direction, in order to control echo, the gain is typically a loss, which requires a loss network at the SLIC RCVN/RCVP inputs, which will reduce the amount of gain that is available for termination impedance. For this reason, a high-gain SLIC is required with a first-generation codec.

With a third-generation codec, the line card designer has different concerns. To design the ac interface, the designer must first decide upon all termination impedance, hybrid balances, and transmission level point (TLP) requirements that the line card must meet. In the transmit direction, the only concern is that the SLIC does not provide a signal that is too hot and overloads the codec input. Thus, for the highest TLP that is being designed to, given the SLIC gain, the designer, as a function of voiceband frequency, must ensure the codec is not overloaded. With a given TLP and a given SLIC gain, if the signal will cause a codec overload, the designer must insert some sort of loss, typically a resistor divider, between the SLIC output and codec input.

Note also that some third-generation codecs require the designer to provide an inherent resistive termination via external networks. The codec will then provide gain shaping, as a function of frequency, to meet the return loss requirements. This feedback will increase the signal at the codec input and increase the likelihood that a resistor divider is needed in the transmit direction. Further stability issues may add external components or excessive ground plane requirements to the design.

In the receive direction, the issue is to optimize the S/N. Again, the designer must consider all the TLPs. The idea is, for all desired TLPs, to run the codec at or as close as possible to its maximum output signal, to optimize the S/N. Remember noise floor is constant, so the hotter the signal from the codec, the better the S/N. The problem is if the codec is feeding a high-gain SLIC, either an external resistor divider is needed to knock the gain down to meet the TLP requirements, or the codec is not operated near maximum signal levels, thus compromising the S/N.

Thus, it appears that the solution is to have a SLIC with a low gain, especially in the receive direction. This will allow the codec to operate near its maximum output signal (to optimize S/N), without an external resistor divider (to minimize cost).

To meet the unique requirements of both type of codecs, the L9214 offers two receive gain choices. These receive gains are mask programmable at the factory and are offered as two different code variations. For interface with a first-generation codec, the L9214 is offered with a receive gain of 8. For interface with a third-generation codec, the L9214 is offered with a receive gain of 2. In either case, the transconductance in the transmit direction or the transmit gain is 300 Ω, (300 V/A).

This selection of receive gain gives the designer the flexibility to maximize performance and minimize external components, regardless of the type of codec chosen.

Design Examples

First-Generation Codec ac Interface Network—Resistive Termination

The following reference circuit shows the complete SLIC schematic for interface to the Agere T7504 first-generation codec for a resistive termination impedance. For this example, the ac interface was designed for a 600 Ω resistive termination and hybrid balance with transmit gain and receive gain set to 0 dBm. For illustration purposes, no PPM injection was assumed in this example.

This is a lower feature application example and uses single battery operation, fixed overhead, current limit, and loop closure threshold.

Resistor R_{GN} is optional. It compensates for any mismatch of input bias voltage at the RCVN/RCVP inputs. If it is not used, there may be a slight offset at tip and ring due to mismatch of input bias voltage at the RCVN/RCVP inputs. It is very common to simply tie RCVN directly to ground in this particular mode of operation. If used, to calculate RGN, the impedance from RCVN to ac ground should equal the impedance from RCVP to ac ground.

ac Applications (continued)

Design Examples (continued)

Example 1, Real Termination

The following design equations refer to the circuit in Figure 13. Use these to synthesize real termination impedance.

Termination Impedance:

$$z_T = \frac{V_{T/R}}{-I_{T/R}}$$

$$z_T = 36\ \Omega + 2R_P + \frac{2400}{1 + \frac{R_{T1}}{R_{GP}} + \frac{R_{T1}}{R_{RCV}}}$$

Receive Gain:

$$g_{rcv} = \frac{V_{T/R}}{V_{FR}}$$

$$g_{rcv} = \frac{8}{\left(1 + \frac{R_{RCV}}{R_{T1}} + \frac{R_{RCV}}{R_{GP}}\right)\left(1 + \frac{Z_T}{Z_{T/R}}\right)}$$

Transmit Gain:

$$g_{tx} = \frac{V_{GSX}}{V_{T/R}}$$

$$g_{tx} = \frac{-R_X}{R_{T2}} \times \frac{300}{Z_{T/R}}$$

Hybrid Balance:

$$h_{bal} = 20\log\left(\frac{R_X}{R_{HB}} - g_{tx} \times g_{rcv}\right)$$

$$h_{bal} = 20\log\left(\frac{V_{GSX}}{V_{FR}}\right)$$

To optimize the hybrid balance, the sum of the currents at the VFX input of the codec op amp should be set to 0. The expression for ZHB becomes the following:

$$R_{HB}(k\Omega) = \frac{R_X}{g_{tx} \times g_{rcv}}$$

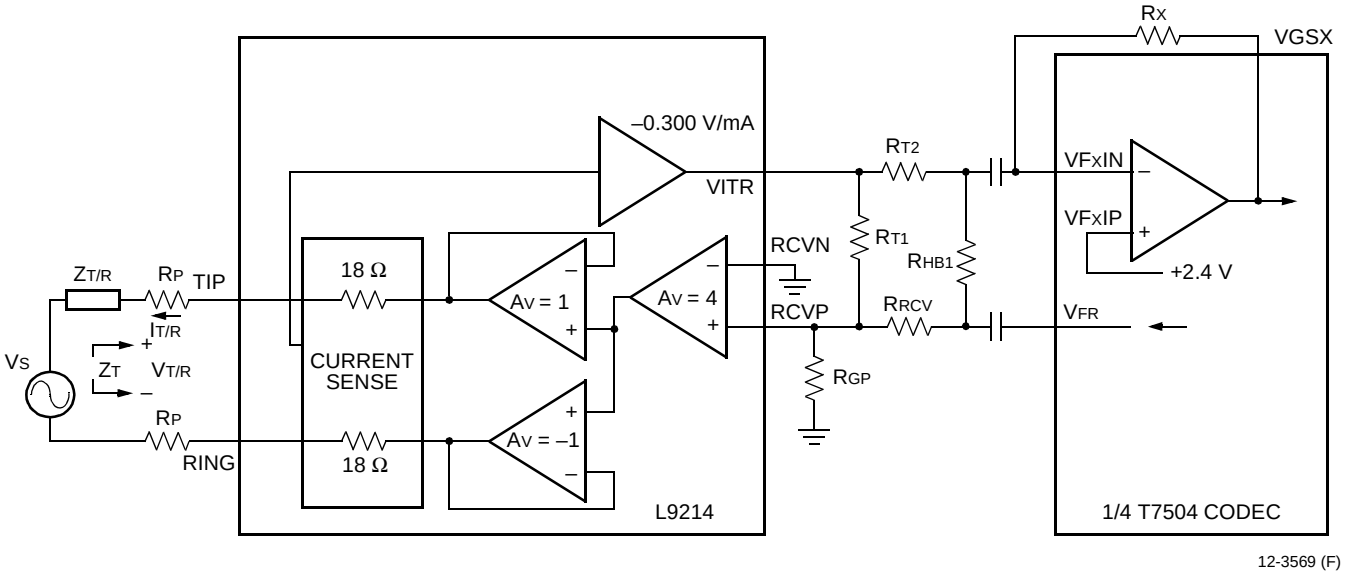


Figure 13. ac Equivalent Circuit

ac Applications (continued)

Design Examples (continued)

Example 1, Real Termination (continued)

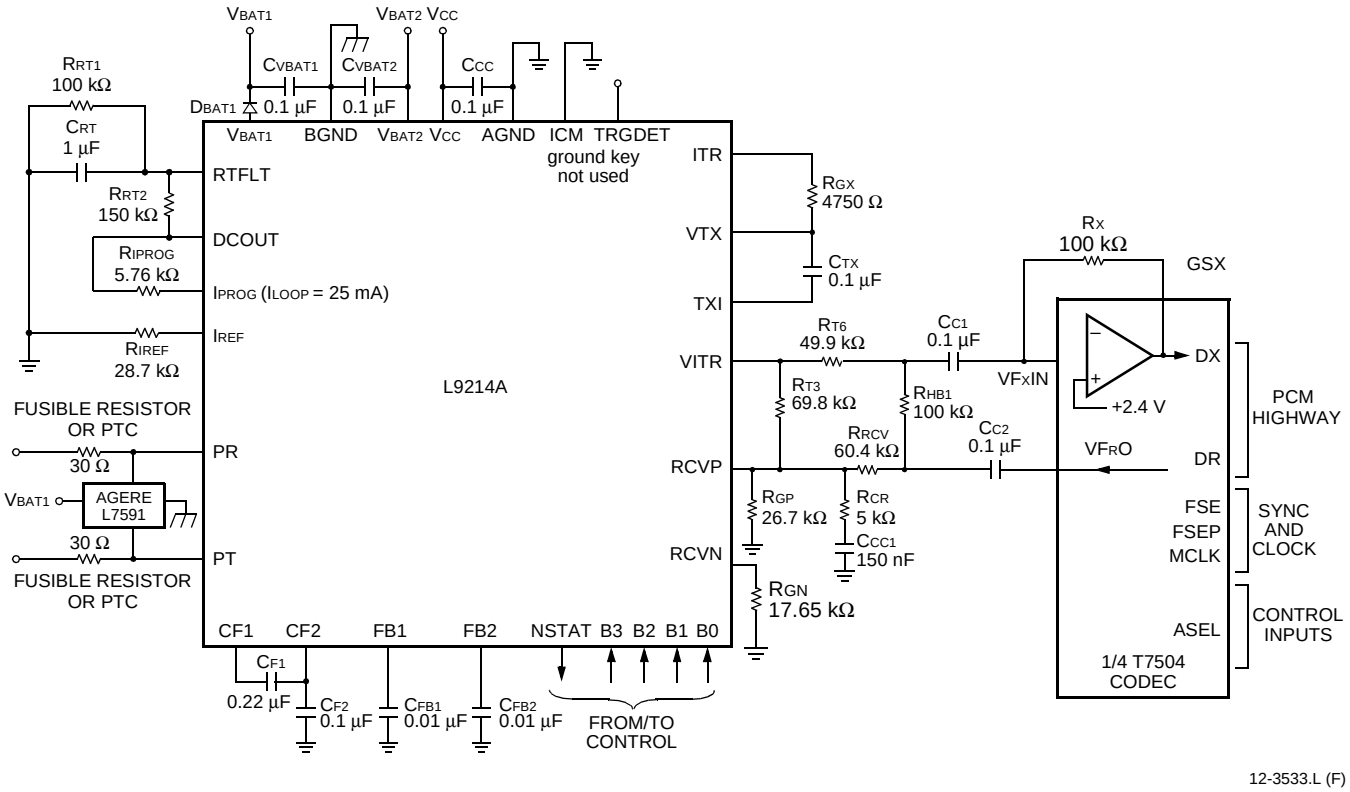


Figure 14. Agere T7504 First-Generation Codec; Resistive Termination (5 REN Configuration)

ac Applications (continued)

Design Examples (continued)

Example 1, Real Termination (continued)

Table 20. L9214 Parts List for Agere T7504 First-Generation Codec; Resistive Termination

Name	Value	Tolerance	Rating	Function
Fault Protection				
R_{PT}	30 Ω	1%	Fusible or PTC	Protection resistor.
R_{PR}	30 Ω	1%	Fusible or PTC	Protection resistor.
Protector	Agere L7591	—	—	Secondary protection.
Power Supply				
C_{VBAT1}	0.1 µF	20%	100 V	V_{BAT} filter capacitor.
C_{VBAT2}	0.1 µF	20%	50 V	V_{BAT} filter capacitor. $\|V_{BAT2}\| < \|V_{BAT1}\|$.
D_{BAT1}	1N4004	—	—	Reverse current.
C_{CC}	0.1 µF	20%	10 V	V_{CC} filter capacitor.
C_{F1}	0.22 µF	20%	100 V	Filter capacitor.
C_{F2}	0.1 µF	20%	100 V	Filter capacitor.
dc Profile				
R_{IPROG}	5.76 kΩ	1%	1/16 W	With R_{IREF}, fixes dc current limit.
R_{IREF}	28.7 kΩ	1%	1/16 W	With R_{IPROG}, fixes dc current limit.
Ringing/Ring Trip				
C_{RT}	1.0 µF	20%	10 V	Ring trip filter capacitor.
R_{RT1}	100 kΩ	1%	1/16 W	Ring trip filter resistor.
R_{RT2}	150 kΩ	1%	1/16 W	Ring trip filter resistor.
C_{FB1}	0.01 µF	20%	100 V	With C_{FB2}, slows rate of battery reversal. Sets crest factor of balanced power ring signal.
C_{FB2}	0.01 µF	20%	100 V	With C_{FB1}, slows rate of battery reversal. Sets crest factor of balanced power ring signal.
ac Interface				
R_{GX}	4750 Ω	1%	1/16 W	Sets T/R to VITR transconductance.
R_{CR}	5 kΩ	5%	1/16 W	Compensation resistor.
C_{CC1}	150 pF	20%	10 V	Compensation capacitor.
C_{TX}	0.1 µF	20%	10 V	ac/dc separation.
C_{C1}	0.1 µF	20%	10 V	dc blocking capacitor.
C_{C2}	0.1 µF	20%	10 V	dc blocking capacitor.
R_{T3}	69.8 kΩ	1%	1/16 W	With R_{GP} and R_{RCV}, sets termination impedance and receive gain.
R_{T6}	49.9 kΩ	1%	1/16 W	With R_X, sets transmit gain.
R_X	100 kΩ	1%	1/16 W	With R_{T6}, sets transmit gain.
R_{HB1}	100 kΩ	1%	1/16 W	With R_X, sets hybrid balance.
R_{RCV}	60.4 kΩ	1%	1/16 W	With R_{GP} and R_{T3}, sets termination impedance and receive gain.
R_{GP}	26.7 kΩ	1%	1/16 W	With R_{RCV} and R_{T3}, sets termination impedance and receive gain.
R_{GN} Optional	17.6 kΩ	1%	1/16 W	Optional. Compensates for input offset at RCVN/RCVP.

Note: T_X = 0 dBm, R_X = 0 dBm, termination impedance = 600 Ω, hybrid balance = 600 Ω.

ac Applications (continued)

Design Examples (continued)

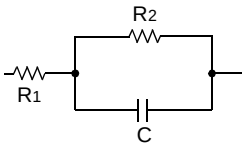
First-Generation Codec ac Interface Network—Complex Termination

The following reference circuit shows the complete SLIC schematic for interface to the Agere T7504 first-generation codec for the German complex termination impedance. For this example, the ac interface was designed for a 220 Ω + (820 Ω || 115 nF) complex termination and hybrid balance with transmit gain and receive gain set to 0 dBm.

Complex Termination Impedance Design Example

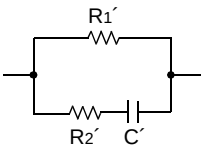
The gain shaping necessary for a complex termination impedance may be done by shaping across the Ax amplifier at nodes ITR and VTX.

Complex termination is specified in the form:



5-6396(F)

To work with this application, convert termination to the form:



5-6398(F)

where:

$R_1' = R_1 + R_2$

$R_2' = \frac{R_1}{R_2}(R_1 + R_2)$

$C' = \left(\frac{R_2}{R_1 + R_2}\right)^2 C$

ac Interface Using First-Generation Codec

$R_{GX}/R_{TGS}/C_{GS}$ (Z_{TG}): These components give gain shaping to get good gain flatness. These components are a scaled version of the specified complex termination impedance.

Note for pure (600 Ω) resistive terminations, components R_{TGS} and C_{GS} are not used. Resistor R_{GX} is used and is still 4750 Ω.

R_X/R_{T6}: With other components set, the transmit gain (for complex and resistive terminations) R_X and R_{T6} are varied to give specified transmit gain.

$R_{T3}/R_{RCV}/R_{GP}$: For both complex and resistive terminations, the ratio of these resistors sets the receive gain. For resistive terminations, the ratio of these resistors sets the return loss characteristic. For complex terminations, the ratio of these resistors sets the low-frequency return loss characteristic.

$C_N/R_{N1}/R_{N2}$: For complex terminations, these components provide high-frequency compensation to the return loss characteristic.

For resistive terminations, these components are not used and RCVN is connected to ground via a resistor.

R_{HB}: Sets hybrid balance for all terminations.

Set Z_{TG}—gain shaping:

$Z_{TG} = R_{GX} || R_{TGS} + C_{GS}$ which is a scaled version of $Z_{T/R}$ (the specified termination resistance) in the $R_1' || R_2' + C'$ form.

R_{GX} must be 4750 Ω to set SLIC transconductance to 300 V/A.

$R_{GX} = 4750\ \Omega$

At dc, C_{GS} and C' are open.

$R_{GX} = M \times R_1'$

where M is the scale factor.

$M = \frac{4750}{R_1'}$

It can be shown:

$R_{TGS} = M \times R_2'$

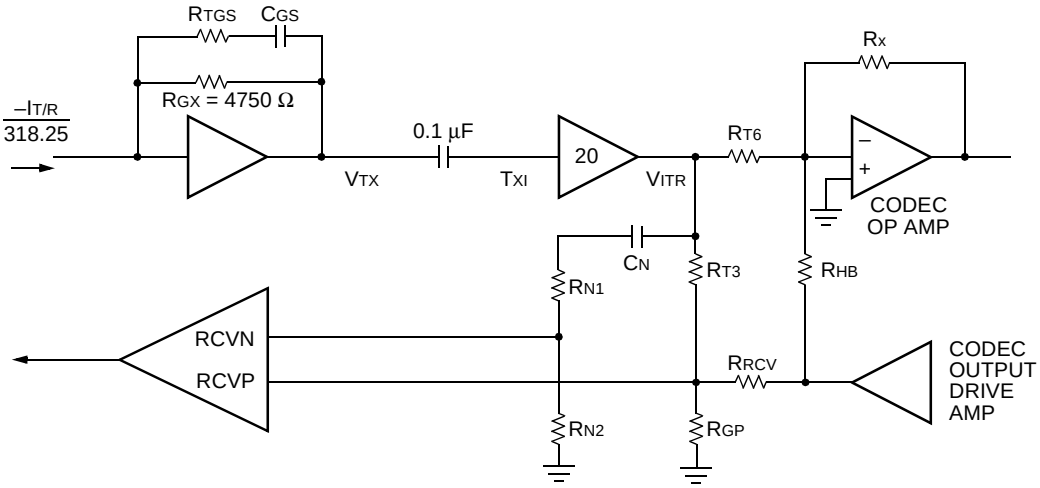
and

$C_{TGS} = \frac{C'}{M}$

ac Applications (continued)

Design Examples (continued)

ac Interface Using First-Generation Codec (continued)



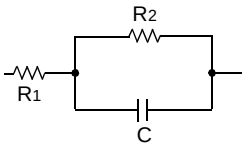
5-6400.H (F)

Figure 15. Interface Circuit Using First-Generation Codec (Blocking Capacitors Not Shown)

Transmit Gain

Transmit gain will be specified as a gain from T/R to PCM, T_X (dB). Since PCM is referenced to 600 Ω and assumed to be 0 dB, and in the case of T/R being referenced to some complex impedance other than 600 Ω resistive, the effects of the impedance transformation must be taken into account.

Again, specified complex termination impedance at T/R is of the form:



5-6396(F)

First, calculate the equivalent resistance of this network at the midband frequency of 1000 Hz.

$$R_{EQ} = \sqrt{\left(\frac{(2\pi f)^2 C_1^2 R_1 R_2^2 + R_1 + R_2}{1 + (2\pi f)^2 R_2^2 C_1^2}\right)^2 + \left(\frac{2\pi f R_2^2 C_1^2}{1 + (2\pi f)^2 R_2^2 C_1^2}\right)^2}$$

Using R_{EQ}, calculate the desired transmit gain, taking into account the impedance transformation:

$$T_X\ (\text{dB}) = T_{X\ (\text{specified[dB]})} + 20\log\sqrt{\frac{600}{R_{EQ}}}$$

$T_{X\ (\text{specified[dB]})}$ is the specified transmit gain. 600 Ω is the impedance at the PCM, and R_{EQ} is the impedance at Tip and ring. $20\log\sqrt{\frac{600}{R_{EQ}}}$ represents the power loss/gain due to the impedance transformation.

Note in the case of a 600 Ω pure resistive termination at T/R $20\log\sqrt{\frac{600}{R_{EQ}}} = 20\log\sqrt{\frac{600}{600}} = 0$.

Thus, there is no power loss/gain due to impedance transformation and $T_X\ (\text{dB}) = T_{X\ (\text{specified[dB]})}$.

Finally, convert T_X (dB) to a ratio, g_{tx}:

$T_X\ (\text{dB}) = 20\log g_{tx}$

The ratio of R_X/R_{T6} is used to set the transmit gain:

$$\frac{R_X}{R_{T6}} = g_{tx} \bullet \frac{318.25}{20} \bullet \frac{1}{M}$$ with a quad Agere codec such as T7504:

$R_X < 200\ k\Omega$

ac Applications (continued)

Design Examples (continued)

ac Interface Using First-Generation Codec (continued)

Receive Gain

Ratios of R_{RCV}, R_{T3}, R_{GP} will set both the low-frequency termination and receive gain for the complex case. In the complex case, additional high-frequency compensation, via C_N, R_{N1}, and R_{N2}, is needed for the return loss characteristic. For resistive termination, C_N, R_{N1}, and R_{N2} are not used and RCVN is tied to ground via a resistor.

Determine the receive gain, g_{rcv}, taking into account the impedance transformation in a manner similar to transmit gain.

$$R_X\,(dB) = R_{X\,(specified[dB])} + 20\log\sqrt{\frac{R_{EQ}}{600}}$$

$$R_X\,(dB) = 20\log g_{rcv}$$

Then:

$$g_{rcv} = \frac{4}{1 + \frac{R_{RCV}}{R_{T3}} + \frac{R_{RCV}}{R_{GP}}}$$

and low-frequency termination

$$Z_{TER(low)} = \frac{2400}{1 + \frac{R_{T3}}{R_{GP}} + \frac{R_{T3}}{R_{RCV}}} + 2R_P + 36\ \Omega$$

$Z_{TER(low)}$ is the specified termination impedance assuming low frequency (C or C´ is open).

R_P is the series protection resistor.

36 Ω is the typical internal feed resistance.

These two equations are best solved using a computer spreadsheet.

Next, solve for the high-frequency return loss compensation circuit, C_N, R_{N1}, and R_{N2}:

$$C_N R_{N2} = \frac{2R_P}{2400}\ C_G\ R_{TGP}$$

$$R_{N1} = R_{N2}\left[\frac{2400}{2R_P}\left(\frac{R_{TGS}}{R_{TGP}}\right) - 1\right]$$

There is an input offset voltage associated with nodes RCVN and RCVP. To minimize the effect of mismatch of this voltage at T/R, the equivalent resistance to ac ground at RCVN should be approximately equal to that at RCVP. Refer to Figure 16 (with dc blocking capacitors). To meet this requirement, $R_{N2} = R_{GP} \parallel R_{T3}$.

Hybrid Balance

Set the hybrid cancellation via R_{HB}.

$$R_{HB} = \frac{R_X}{g_{rcv} \times g_{tx}}$$

If a 5 V only codec such as the Agere T7504 is used, dc blocking capacitors must be added as shown in Figure 16. This is because the codec is referenced to 2.5 V and the SLIC to ground—with the ac coupling, a dc bias at T/R is eliminated and power associated with this bias is not consumed.

Typically, values of 0.1 µF to 0.47 µF capacitors are used for dc blocking. The addition of blocking capacitors will cause a shift in the return loss and hybrid balance frequency response toward higher frequencies, degrading the lower-frequency response. The lower the value of the blocking capacitor, the more pronounced the effect is, but the cost of the capacitor is lower. It may be necessary to scale resistor values higher to compensate for the low-frequency response. This effect is best evaluated via simulation. A *PSPICE*® model for the L9214 is available.

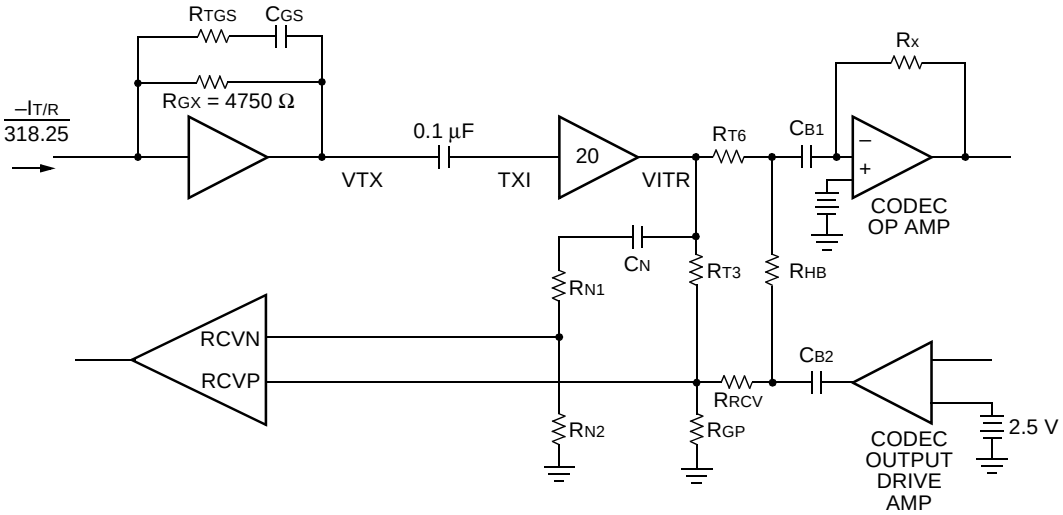
Design equation calculations seldom yield standard component values. Conversion from the calculated value to standard value may have an effect on the ac parameters. This effect should be evaluated and optimized via simulation.

ac Applications (continued)

Design Examples (continued)

ac Interface Using First-Generation Codec (continued)

Blocking Capacitors



5-6401.G (F)

Figure 16. ac Interface Using First-Generation Codec (Including Blocking Capacitors) for Complex Termination Impedance

ac Applications (continued)

Design Examples (continued)

ac Interface Using First-Generation Codec (continued)

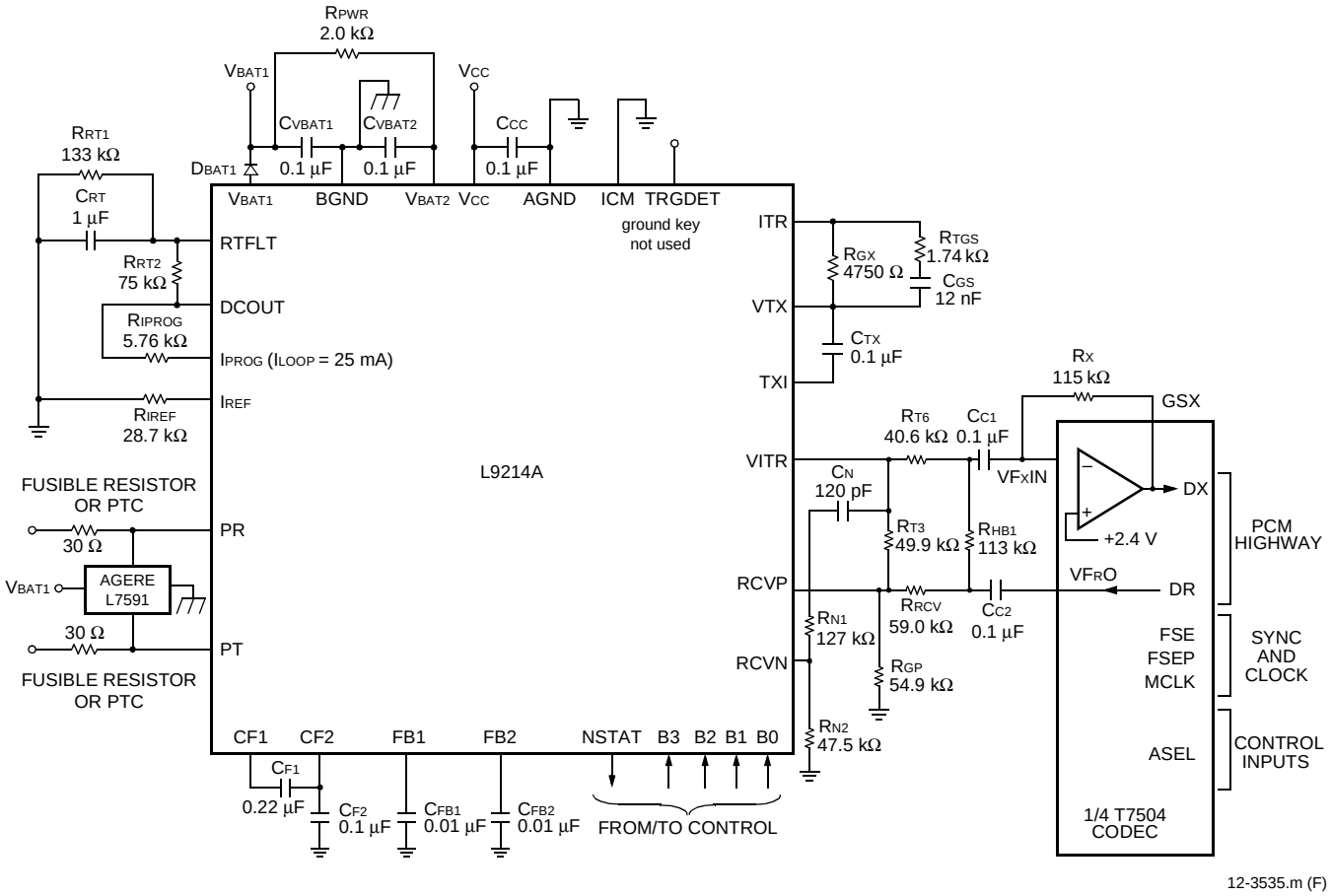


Figure 17. Agere T7504 First-Generation Codec; Complex Termination with Power Control Resistor (3 REN Configuration)

Table 21. L9214 Parts List for Agere T7504 First-Generation Codec; Complex Termination with Power Control Resistor

Name	Value	Tolerance	Rating	Function
Fault Protection				
RPT	30 Ω	1%	Fusible or PTC	Protection resistor.
RPR	30 Ω	1%	Fusible or PTC	Protection resistor.
Protector	Agere L7591	—	—	Secondary protection.

Applications (continued)

Design Examples (continued)

ac Interface Using First-Generation Codec (continued)

Table 21. L9214 Parts List for Agere T7504 First-Generation Codec; Complex Termination with Power Control Resistor (continued)

Name	Value	Tolerance	Rating	Function
Power Supply				
C_{VBAT1}	0.1 µF	20%	100 V	V_{BAT} filter capacitor.
C_{VBAT2}	0.1 µF	20%	50 V	V_{BAT} filter capacitor. $\|V_{BAT2}\| < \|V_{BAT1}\|$.
D_{BAT1}	1N4004	—	—	Reverse current.
C_{CC}	0.1 µF	20%	10 V	V_{CC} filter capacitor.
C_{F1}	0.22 µF	20%	100 V	Filter capacitor.
C_{F2}	0.1 µF	20%	100 V	Filter capacitor.
R_{PWR}	2.0 kΩ	5%	2 W	Power control resistor, provides single battery supply operation.
dc Profile				
R_{IPROG}	5.76 kΩ	1%	1/16 W	With R_{IREF}, fixes dc current limit.
R_{IREF}	28.7 kΩ	1%	1/16 W	With R_{IPROG}, fixes dc current limit.
Ringing/Ring Trip				
C_{RING}	1.0 µF	20%	10 V	Ring trip filter capacitor.
R_{RT1}	133 kΩ	1%	1/16 W	Ring trip filter resistor.
R_{RT2}	75 kΩ	1%	1/16 W	Ring trip filter resistor.
C_{FB1}	0.01 µF	20%	100 V	With C_{FB2}, slows rate of battery reversal. Sets crest factor of balanced power ring signal.
C_{FB2}	0.01 µF	20%	100 V	With C_{FB1}, slows rate of battery reversal. Sets crest factor of balanced power ring signal.
ac Interface				
R_{GX}	4750 Ω	1%	1/16 W	Sets T/R to VITR transconductance.
R_{TGS}	1.74 kΩ	1%	1/16 W	Gain shaping for complex termination.
C_{GS}	12 nF	5%	10 V	Gain shaping for complex termination.
C_{TX}	0.1 µF	20%	10 V	ac/dc separation.
C_{C1}	0.1 µF	20%	10 V	dc blocking capacitor.
C_{C2}	0.1 µF	20%	10 V	dc blocking capacitor.
R_{T3}	49.9 kΩ	1%	1/16 W	With R_{GP} and R_{RCV}, sets termination impedance and receive gain.
R_{T6}	40.2 kΩ	1%	1/16 W	With R_X, sets transmit gain.
R_X	115 kΩ	1%	1/16 W	With R_{T6}, sets transmit gain.
R_{HB1}	113 kΩ	1%	1/16 W	With R_X, sets hybrid balance.
R_{RCV}	59.0 kΩ	1%	1/16 W	With R_{GP} and R_{T3}, sets termination impedance and receive gain.
R_{GP}	54.9 kΩ	1%	1/16 W	With R_{RCV} and R_{T3}, sets termination impedance and receive gain.
C_N	120 pF	20%	10 V	High frequency compensation.
R_{N1}	127 kΩ	1%	1/16 W	High frequency compensation.
R_{N2}	47.5 kΩ	1%	1/16 W	High frequency compensation, compensate for dc offset at RCVP/RCVN.

Note: T_X = 0 dBm, R_X = 0 dBm, termination impedance = 220 Ω + (820 Ω || 115 nF), hybrid balance = 220 Ω + (820 Ω || 115 nF).

ac Applications (continued)

Design Examples (continued)

Third-Generation Codec ac Interface Network—Complex Termination

The following reference circuit shows the complete SLIC schematic for interface to the Agere T8536 third-generation codec. All ac parameters are programmed by the T8536. Note this codec differentiates itself in that no external components are required in the ac interface to provide a dc termination impedance or for stability. Please see the T8535/6 data sheet for information on coefficient programming.

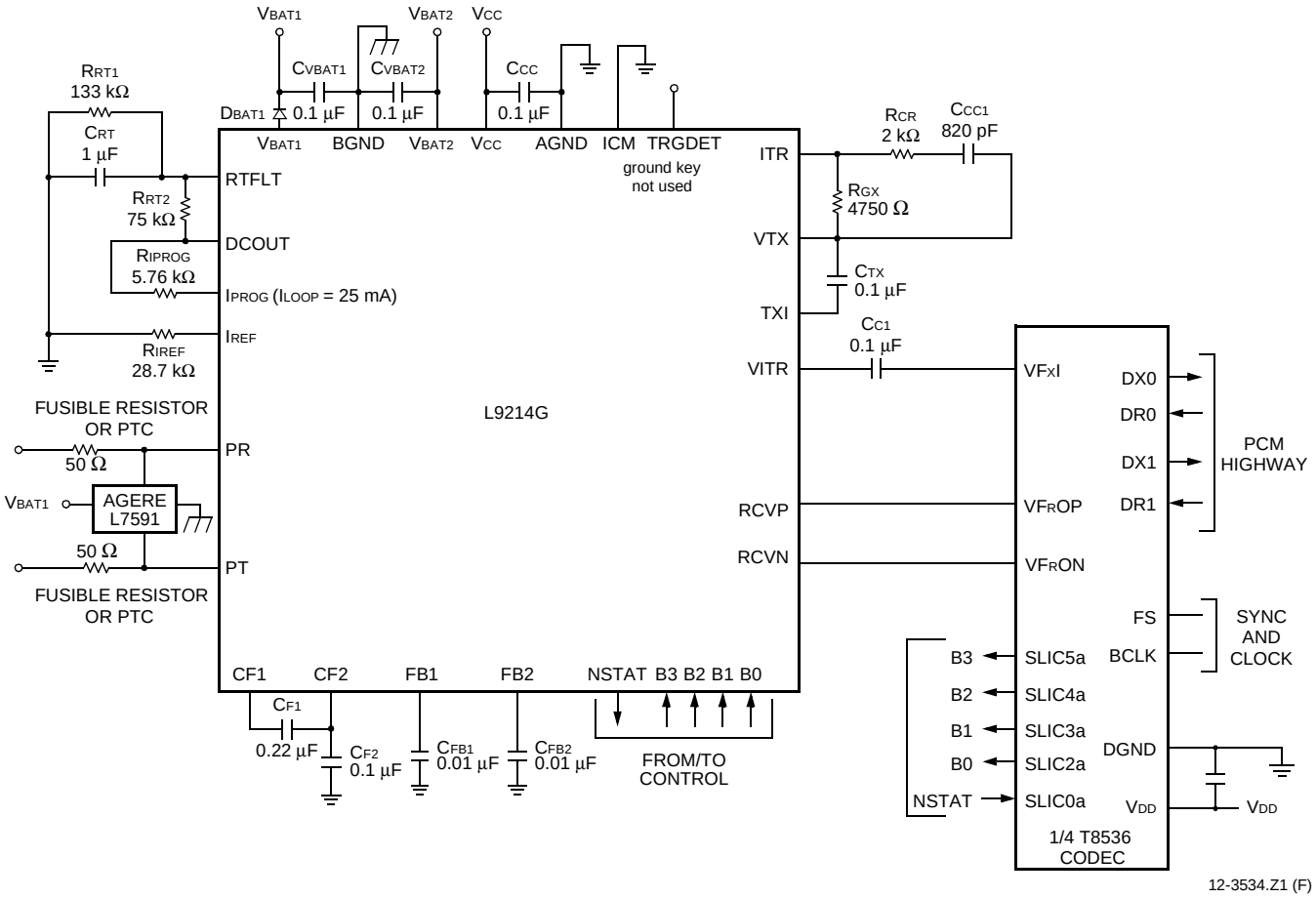


Figure 18. Third-Generation Codec ac Interface Network; Complex Termination (3 REN Configuration)

ac Applications (continued)

Design Examples (continued)

Third-Generation Codec ac Interface Network—Complex Termination (continued)

Table 22. L9214 Parts List for Agere T8536 Third-Generation Codec Meter Pulse Application ac and dc Parameters; Fully Programmable

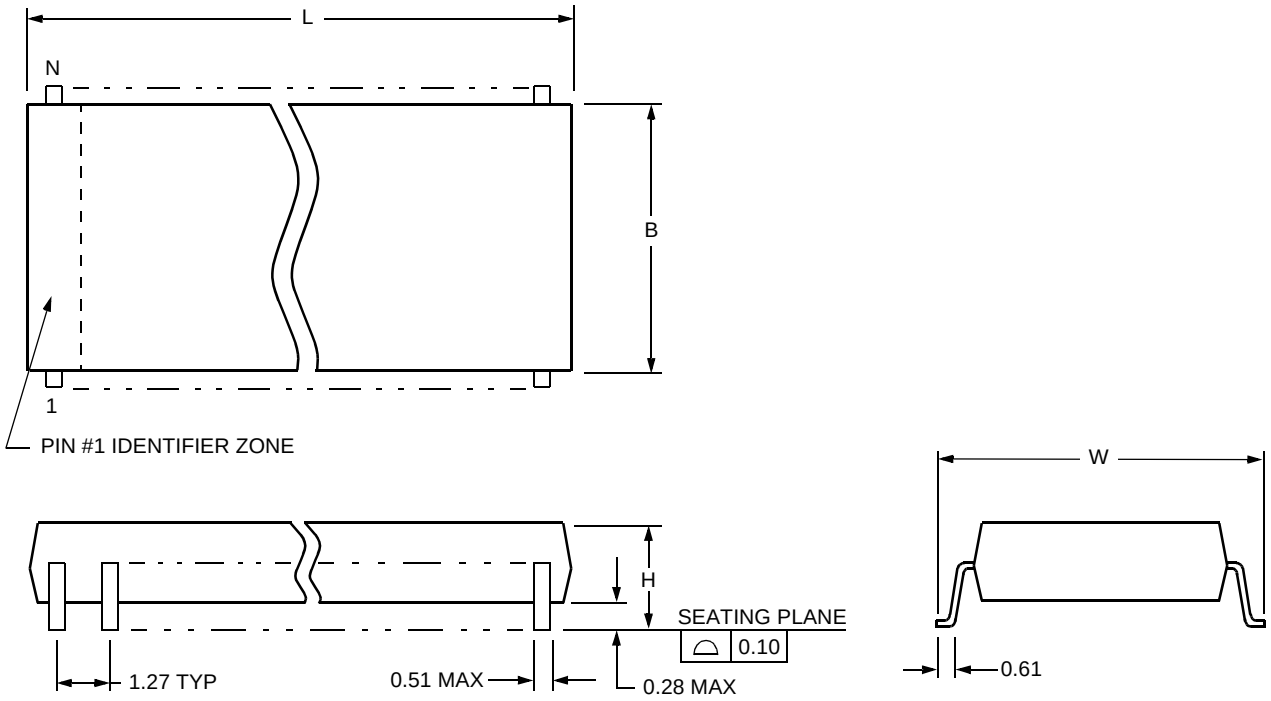
Name	Value	Tolerance	Rating	Function
Fault Protection				
R_{PT}	30 Ω	1%	Fusible or PTC	Protection resistor*****.
R_{PR}	30 Ω	1%	Fusible or PTC	Protection resistor*****.
Protector	Agere L7591	—	—	Secondary protection.
Power Supply				
C_{VBAT1}	0.1 µF	20%	100 V	V_{BAT} filter capacitor.
C_{VBAT2}	0.1 µF	20%	50 V	V_{BAT} filter capacitor. $\|V_{BAT2}\| < \|V_{BAT1}\|$.
D_{BAT1}	1N4004	—	—	Reverse current.
C_{CC}	0.1 µF	20%	10 V	V_{CC} filter capacitor.
C_{F1}	0.22 µF	20%	100 V	Filter capacitor.
C_{F2}	0.1 µF	20%	100 V	Filter capacitor.
dc Profile				
R_{IPROG}	5.76 kΩ	1%	1/16 W	With R_{IREF}, fixes dc current limit.
R_{IREF}	28.7 kΩ	1%	1/16 W	With R_{IPROG}, fixes dc current limit.
Ringing/Ring Trip				
C_{RT}	1.0 µF	20%	10 V	Ring trip filter capacitor.
R_{RT1}	133 kΩ	1%	1/16 W	Ring trip filter resistor.
R_{RT2}	75 kΩ	1%	1/16 W	Ring trip filter resistor.
C_{FB1}	0.01 µF	20%	100 V	With C_{FB2}, slows rate of battery reversal. Sets crest factor of balanced power ring signal.
C_{FB2}	0.01 µF	20%	100 V	With C_{FB1}, slows rate of battery reversal. Sets crest factor of balanced power ring signal.
ac Interface				
R_{GX}	4750 Ω	1%	1/16 W	Sets T/R to VITR transconductance.
R_{CR}	10 kΩ	5%	1/16 W	Compensation resistor.
C_{CC1}	270 pF	20%	10 V	Compensation capacitor.
C_{TX}	0.1 µF	20%	10 V	ac/dc separation.
C_{C1}	0.1 µF	20%	10 V	dc blocking capacitor.

***** For loop stability, increase to 50 Ω minimum if synthesizing 900 Ω or 900 Ω + 2.16 µF termination impedance.

Outline Diagrams

28-Pin SOG

Note: The dimensions in these outline diagrams are intended for informational purposes only. For detailed drawings to assist your design efforts, please contact your Agere Sales Representative.



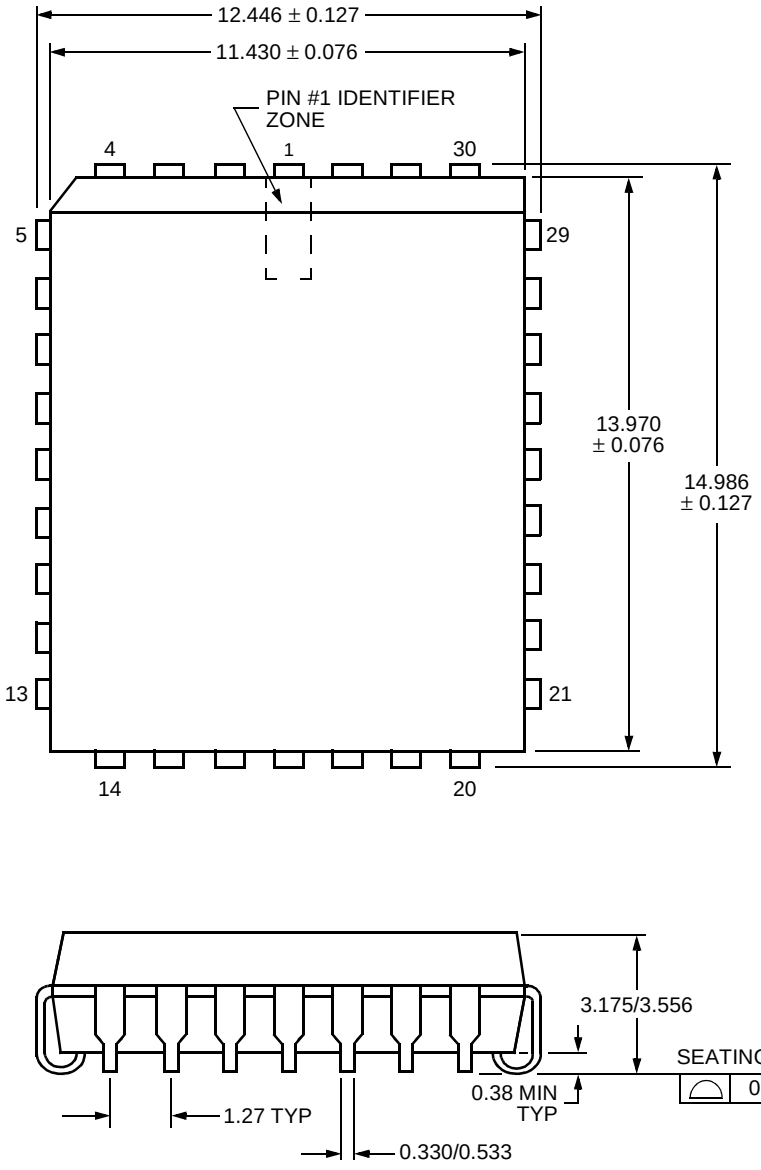
Package Description	Number of Pins N	Package Dimensions			
		Maximum Length L	Maximum Width Without Leads B	Maximum Width Including Leads W	Maximum Height Above Board H
SOG (small outline gull-wing)	28	18.11	7.62	10.64	2.67

5-4414

Outline Diagrams (continued)

32-Pin PLCC

Note: The dimensions in this outline diagram are intended for informational purposes only. For detailed schematics to assist your design efforts, please contact your Agere Sales Representative.



5-3813r2 (F)

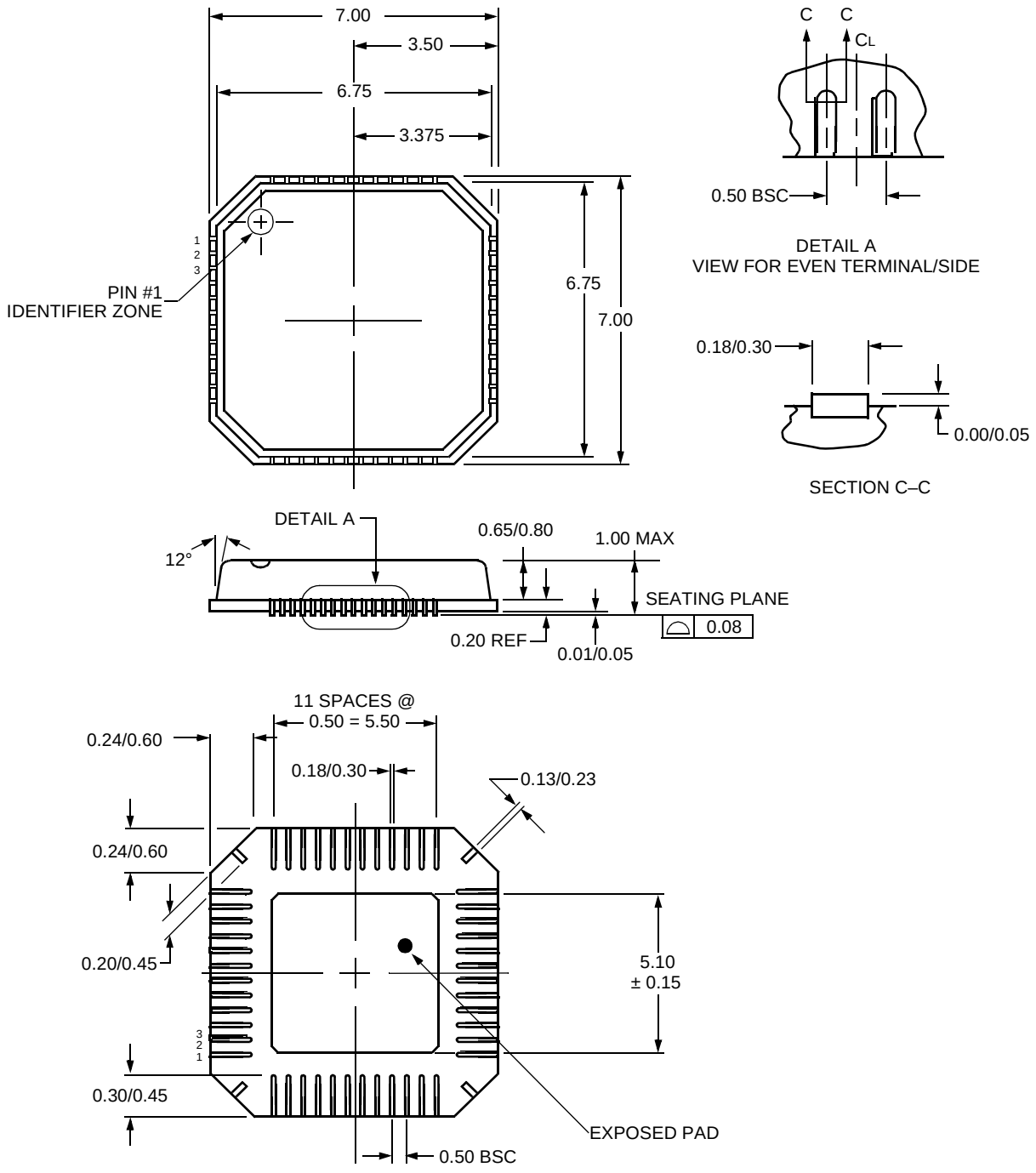
Outline Diagrams (continued)

48-Pin MLCC

Dimensions are in millimeters.

Notes: The dimensions in this outline diagram are intended for informational purposes only. For detailed schematics to assist your design efforts, please contact your Agere Sales Representative.

The exposed pad on the bottom of the package will be at V_{BAT1} potential.



0195

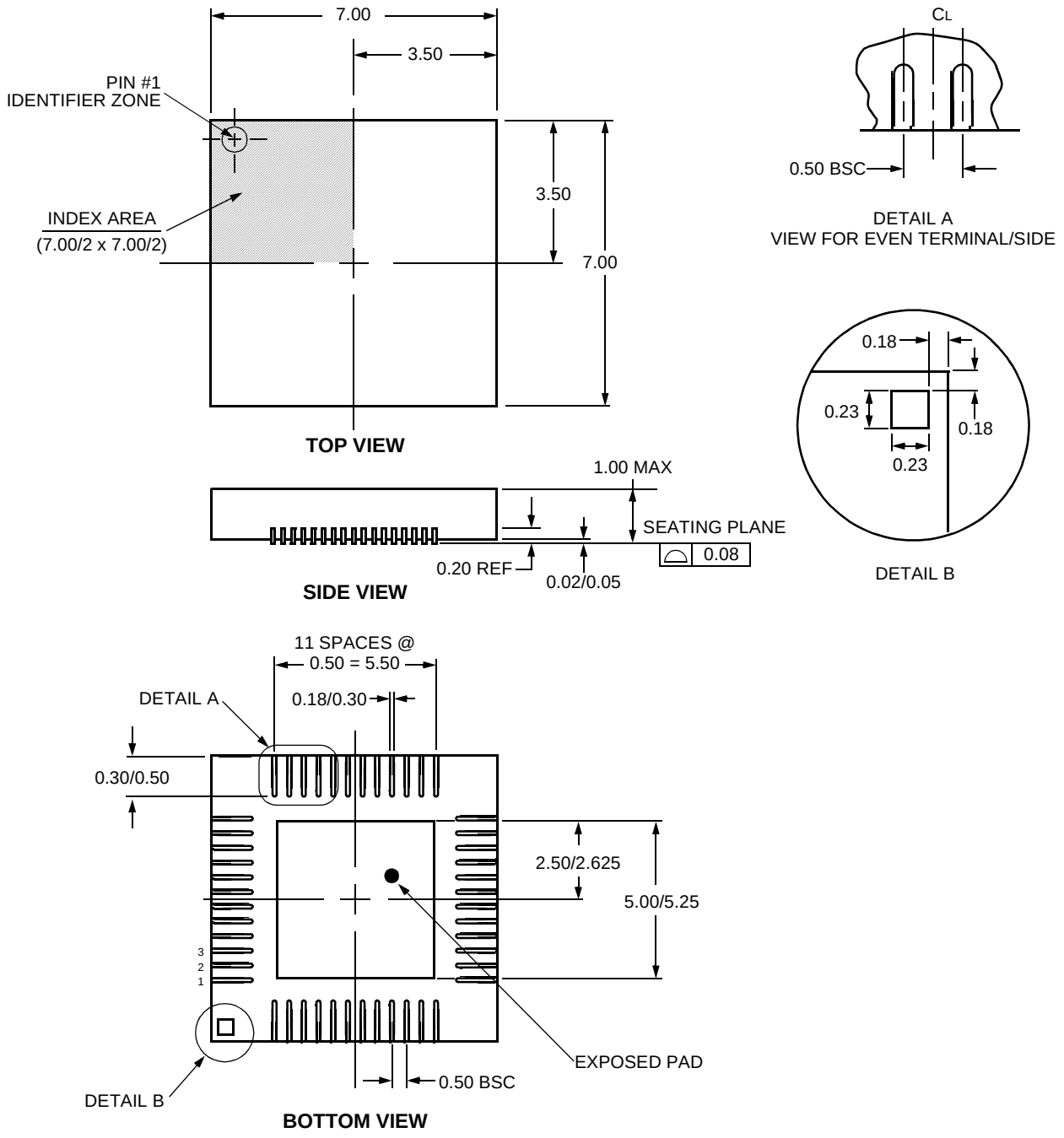
Outline Diagrams (continued)

48-Pin MLCC, JEDEC MO-220 VKKD-2

Dimensions are in millimeters.

Notes: The dimensions in this outline diagram are intended for informational purposes only. For detailed schematics to assist your design efforts, please contact your Agere Sales Representative.

The exposed pad on the bottom of the package will be at V_{BAT1} potential.



0195

Ordering Information

Device Part No.	Description	Package	Comcode
LUCL9214AAJ-D	SLIC Gain = 8	28-Pin SOG*, Dry-bagged	108553892
LUCL9214AAJ-DT	SLIC Gain = 8	28-Pin SOG*, Dry-bagged, Tape and Reel	108553900
LUCL9214AAU-D	SLIC Gain = 8	32-Pin PLCC, Dry-bagged	108697905
LUCL9214AAU-DT	SLIC Gain = 8	32-Pin PLCC, Dry-bagged, Tape and Reel	108697913
LUCL9214ARG-D	SLIC Gain = 8	48-Pin MLCC, Dry-bagged	109058636
LUCL9214ARG-DT	SLIC Gain = 8	48-Pin MLCC, Dry-bagged, Tape and Reel	109058644
LUCL9214GAJ-D	SLIC Gain = 2	28-Pin SOG*, Dry-bagged	108560723
LUCL9214GAJ-DT	SLIC Gain = 2	28-Pin SOG*, Dry-bagged, Tape and Reel	108560731
LUCL9214GAU-D	SLIC Gain = 2	32-Pin PLCC, Dry-bagged	108698309
LUCL9214GAU-DT	SLIC Gain = 2	32-Pin PLCC, Dry-bagged, Tape and Reel	108698317
LUCL9214GRG-D	SLIC Gain = 2	48-Pin MLCC, Dry-bagged	109058651
LUCL9214GRG-DT	SLIC Gain = 2	48-Pin MLCC, Dry-bagged, Tape and Reel	109058669

* Please contact your Agere Sales Representative for availability.

For additional information, contact your Agere Systems Account Manager or the following:
INTERNET: **http://www.agere.com**
E-MAIL: **docmaster@agere.com**
N. AMERICA: Agere Systems Inc., 555 Union Boulevard, Room 30L-15P-BA, Allentown, PA 18109-3286
1-800-372-2447, FAX 610-712-4106 (In CANADA: **1-800-553-2448**, FAX 610-712-4106)
ASIA: Agere Systems Hong Kong Ltd., Suites 3201 & 3210-12, 32/F, Tower 2, The Gateway, Harbour City, Kowloon
Tel. (852) 3129-2000, FAX (852) 3129-2020
CHINA: **(86) 21-5047-1212** (Shanghai), **(86) 10-6522-5566** (Beijing), **(86) 755-695-7224** (Shenzhen)
JAPAN: **(81) 3-5421-1600** (Tokyo), KOREA: **(82) 2-767-1850** (Seoul), SINGAPORE: **(65) 778-8833**, TAIWAN: **(886) 2-2725-5858** (Taipei)
EUROPE: **Tel. (44) 7000 624624**, FAX (44) 1344 488 045

October 2001
DS01-144ALC (Replaces DS00-342ALC)